

SN74LV541A Octal Buffers/Drivers With 3-State Outputs

1 Features

- Operation of 2-V to 5.5-V V_{CC}
- Max t_{pd} of 6 ns at 5 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (output V_{OH} undershoot) > 2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support mixed-mode voltage operation on all ports
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 17

2 Applications

- [Smart grids](#)
- [TVs](#)
- Set-top-boxes
- [Audio](#)
- [Servers](#)
- [Surveillance cameras](#)
- [Network switches](#)
- [Infotainment](#)

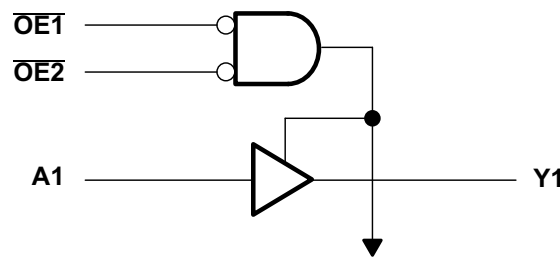
3 Description

The SN74LV541A device is an octal buffer/driver designed for 2-V to 5.5-V V_{CC} operation.

Package Information

PART NUMBER	PACKAGE ¹	PACKAGE SIZE ²
SN74LV244A	DB (SSOP, 20)	7.2 mm × 7.8 mm
	DW (SOIC, 20)	12.80 mm × 10.3 mm
	NS (SO, 20)	12.60 mm × 5.30 mm
	PW (TSSOP, 20)	6.50 mm × 7.8 mm
	RGY (VQFN, 20)	4.5 mm × 3.50 mm
	RKS (VQFN, 20)	4.50 mm × 2.50 mm
	DGS (VSSOP, 20)	5.10 mm × 4.9 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



To Seven Other Channels

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (March 2023) to Revision N (August 2023)	Page
• Deleted <i>DGV</i> from <i>Package Information</i> table and ESD rating from <i>Features</i> section.....	1
• Updated thermal values for PW package from $R\theta_{JA} = 102.8$ to 128.2 , $R\theta_{JC}(\text{top}) = 36.8$ to 70.5 , $R\theta_{JB} = 53.8$ to 79.3 , $\Psi_{JT} = 2.5$ to 23.4 , $\Psi_{JB} = 53.3$ to 78.9 , all values in $^{\circ}\text{C/W}$	5
Changes from Revision L (January 2023) to Revision M (March 2023)	Page
• Updated thermal values for DB package from $R\theta_{JA} = 96.0$ to 118.2 , $R\theta_{JC}(\text{top}) = 56.7$ to 77.2 , $R\theta_{JB} = 51.2$ to 73 , $\Psi_{JT} = 19.4$ to 42.2 , $\Psi_{JB} = 50.8$ to 72.6 , all values in $^{\circ}\text{C/W}$	5
• Updated thermal values for NS package from $R\theta_{JA} = 77.1$ to 108.1 , $R\theta_{JC}(\text{top}) = 43.6$ to 73.9 , $R\theta_{JB} = 44.6$ to 73.1 , $\Psi_{JT} = 17.2$ to 44.1 , $\Psi_{JB} = 44.2$ to 72.8 , all values in $^{\circ}\text{C/W}$	5

5 Pin Configuration and Functions

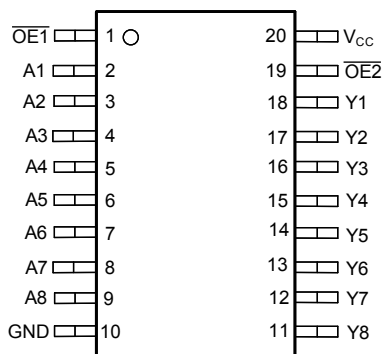


Figure 5-1. DB, DGV, DW, NS, PW or DGS Package, 20-Pin SSOP, TVSOP, SOIC, SO, TSSOP or VSSOP (Top View)

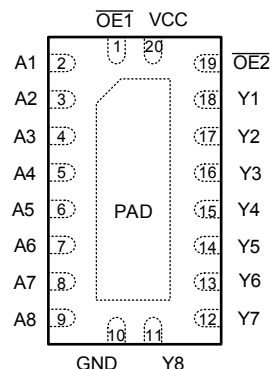


Figure 5-2. RGY and RKS Package, 20-Pin VQFN with (Exposed Thermal Pad Top View)

Table 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
OE1	1	I	Output enable input 1, active low
A1	2	I	Input for channel 1
A2	3	I	Input for channel 2
A3	4	I	Input for channel 3
A4	5	I	Input for channel 4
A5	6	I	Input for channel 5
A6	7	I	Input for channel 6
A7	8	I	Input for channel 7
A8	9	I	Input for channel 8
GND	10	G	Ground
Y8	11	O	Output for channel 8
Y7	12	O	Output for channel 7
Y6	13	O	Output for channel 6
Y5	14	O	Output for channel 5
Y4	15	O	Output for channel 4
Y3	16	O	Output for channel 3
Y2	17	O	Output for channel 2
Y1	18	O	Output for channel 1
OE2	19	I	Output enable input 2, active low
VCC	20	P	Positive supply
Thermal Pad ⁽²⁾		—	The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

(2) RKS package only

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	–0.5	7	V
V_I	Input voltage range ⁽²⁾	–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	–0.5	7	V
V_O	Output voltage range applied in the high or low state ^{(2) (3)}	–0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		–20 mA
I_{OK}	Output clamp current	$V_O < 0$		–50 mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±35 mA
	Continuous current through V_{CC} or GND			±70 mA
T_{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 6.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5-V maximum.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±3000
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins ⁽²⁾	±2000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			SN74LV541A		UNIT
			MIN	MAX	
V _{CC}	Supply voltage		2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7		
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7		
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5	V
		V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3	
V _I	Input voltage		0	5.5	V
V _O	Output voltage	High or low state	0	V _{CC}	V
		3-state	0	5.5	
I _{OH}	High-level output current	V _{CC} = 2 V		–50	μA
		V _{CC} = 2.3 V to 2.7 V		–2	mA
		V _{CC} = 3 V to 3.6 V		–8	
		V _{CC} = 4.5 V to 5.5 V		–16	
I _{OL}	Low-level output current	V _{CC} = 2 V		50	μA
		V _{CC} = 2.3 V to 2.7 V		2	mA
		V _{CC} = 3 V to 3.6 V		8	
		V _{CC} = 4.5 V to 5.5 V		16	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V		200	ns/V
		V _{CC} = 3 V to 3.6 V		100	
		V _{CC} = 4.5 V to 5.5 V		20	
T _A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LV541A								UNIT
		DB	DGV	DW	NS	PW	RGY	RKS	DGS	
		20 PINS								
R _{θJA}	Junction-to-ambient thermal resistance	118.2	116.1	79.8	108.1	128.2	35.1	75.2	125.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	77.2	31.3	45.8	73.9	70.5	43.3	79.4	80.0	
R _{θJB}	Junction-to-board thermal resistance	73	57.6	47.4	73.1	79.3	12.9	47.8	63.8	
Ψ _{JT}	Junction-to-top characterization parameter	42.2	1.0	18.5	44.1	23.4	0.9	14.6	8.4	
Ψ _{JB}	Junction-to-board characterization parameter	72.6	56.9	47.0	72.8	78.9	12.9	47.8	79.9	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	7.9	31.5	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 µA	2 V to 5.5 V	V _{CC} – 0.1			V _{CC} – 0.1		V _{CC} – 0.1		V
	I _{OH} = –2 mA	2.3 V	2			2		2		
	I _{OH} = –8 mA	3 V	2.48			2.48		2.48		
	I _{OH} = –16 mA	4.5 V	3.8			3.8		3.8		
V _{OL}	I _{OL} = 50 µA	2 V to 5.5 V			0.1		0.1		0.1	V
	I _{OL} = 2 mA	2.3 V			0.4		0.4		0.4	
	I _{OL} = 8 mA	3 V			0.44		0.44		0.44	
	I _{OL} = 16 mA	4.5 V			0.55		0.55		0.55	
I _I	V _I = 5.5 V or GND	0 to 5.5 V			±1		±1		±1	µA
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±5		±5		±5	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			20		20		20	µA
I _{off}	V _I or V _O = 0 to 5.5 V	0			5		5		5	µA
C _i	V _I = V _{CC} or GND	3.3 V		2						pF

6.6 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	C _L = 15 pF		6.7	11.3	1	13.5	1	13.5	ns
t _{en}	OE	Y			8.5	16.6	1	19.5	1	19.5	
t _{dis}	OE	Y			8.4	13.1	1	15	1	15	
t _{pd}	A	Y	C _L = 50 pF		8.7	15.9	1	18.5	1	18.5	ns
t _{en}	OE	Y			10.5	20.7	1	24	1	24	
t _{dis}	OE	Y			12.3	17.9	1	20	1	20	
t _{sk(o)}						2		2		2	

6.7 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	C _L = 15 pF		4.8	7	1	8.5	1	8.5	ns
t _{en}	OE	Y			6.1	10.5	1	12.5	1	12.5	
t _{dis}	OE	Y			5.8	11	1	12	1	12	
t _{pd}	A	Y	C _L = 50 pF		6.1	10.5	1	12	1	12	ns
t _{en}	OE	Y			7.4	14	1	16	1	16	
t _{dis}	OE	Y			8.8	15.4	1	17.5	1	17.5	
t _{sk(o)}						1.5		1.5		1.5	

6.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } 85^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	$C_L = 15\text{ pF}$	3.5	5		1	6	1	6	ns
t_{en}	\overline{OE}	Y		4.3	7.2		1	8.5	1	8.5	
t_{dis}	\overline{OE}	Y		3.9	7.5		1	8	1	8	
t_{pd}	A	Y	$C_L = 50\text{ pF}$	4.3	7		1	8	1	8	ns
t_{en}	\overline{OE}	Y		5.3	9.2		1	10.5	1	10.5	
t_{dis}	\overline{OE}	Y		5.6	8.8		1	10	1	10	
$t_{sk(o)}$					1			1		1	

6.9 Noise Characteristics

$V_{CC} = 3.3\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER		SN74LV541A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.4	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

6.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	$C_L = 50\text{ pF}$,	$f = 10\text{ MHz}$	3.3 V	16.3	pF
					5 V	17.8	

6.11 Typical Characteristics

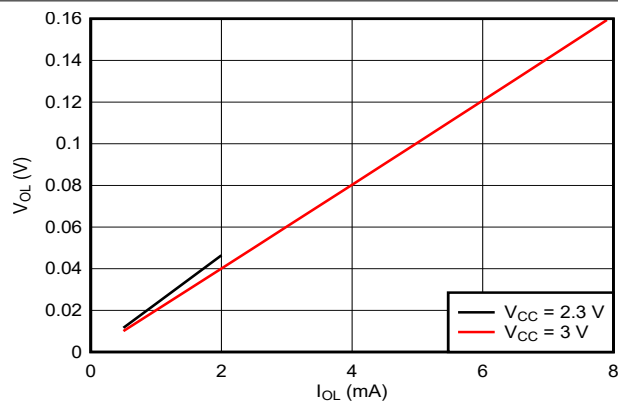


Figure 6-1. Output Voltage in LOW State, 2.3- and 3-V Supply

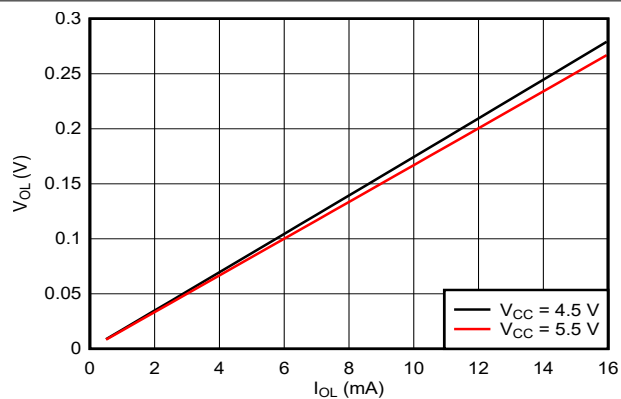


Figure 6-2. Output Voltage in LOW State, 4.5- and 5.5-V Supply

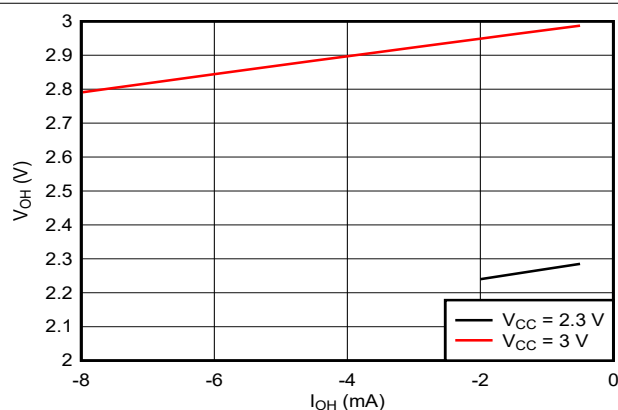


Figure 6-3. Output Voltage in HIGH State, 2.3- and 3-V Supply

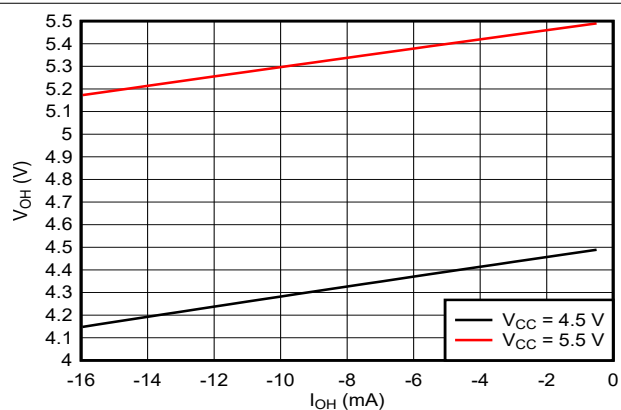


Figure 6-4. Output Voltage in HIGH State, 4.5- and 5.5-V Supply

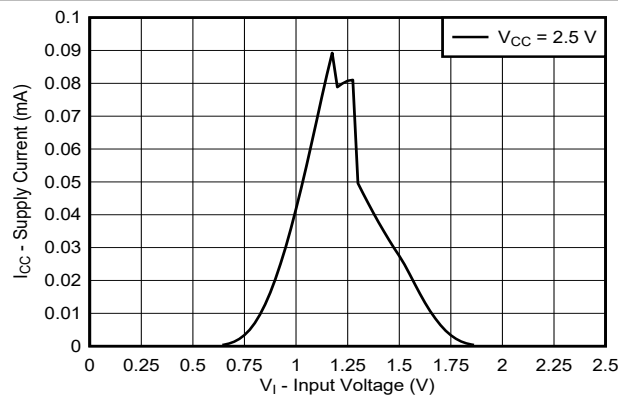


Figure 6-5. Supply Current Across Input Voltage, 2.5-V Supply

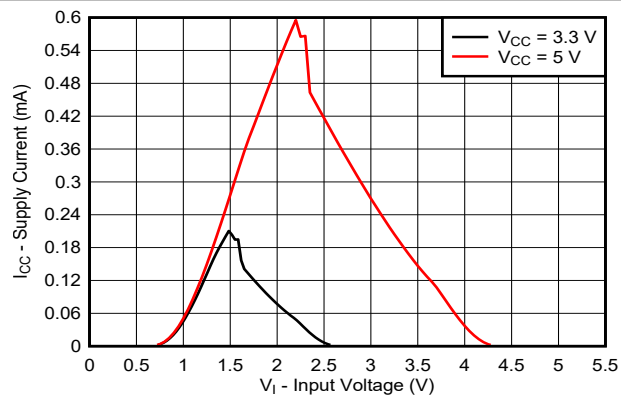


Figure 6-6. Supply Current Across Input Voltage, 3.3- and 5-V Supply

6.11 Typical Characteristics (continued)

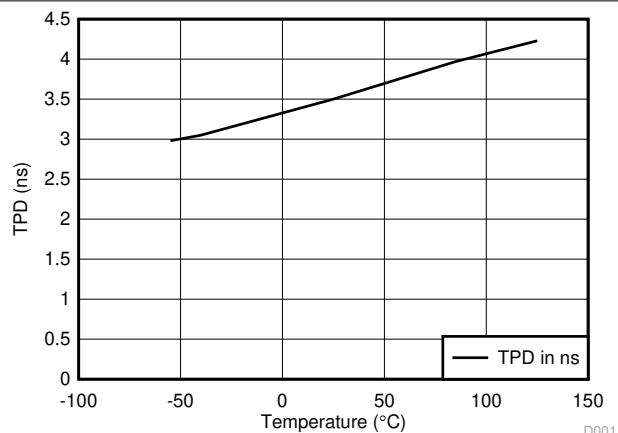


Figure 6-7. TPD vs Temperature

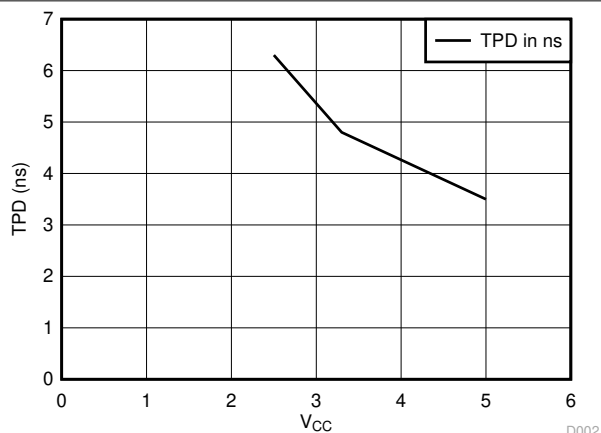
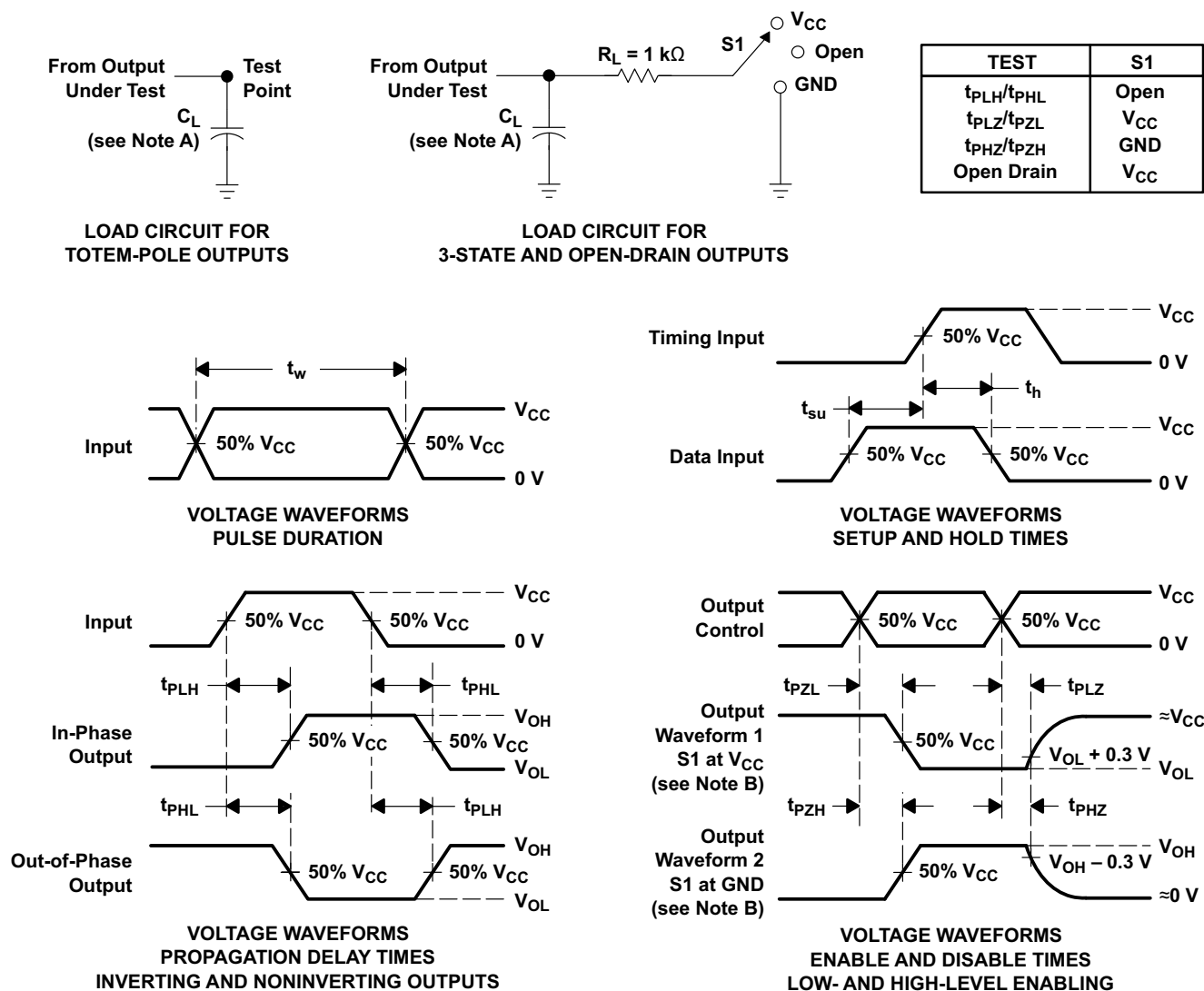


Figure 6-8. TPD vs V_{CC} at 25°C

7 Parameter Measurement Information



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LV541A device is an octal buffers/driver designed for 2-V to 5.5-V V_{CC} operation.

The SN74LV541A device is ideal for driving bus lines or buffer memory address registers. It features inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ($\overline{OE1}$ or $\overline{OE2}$) input is high, all corresponding outputs are in the high-impedance state. The outputs provide non-inverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down, both \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LV541A device are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

8.2 Functional Block Diagram

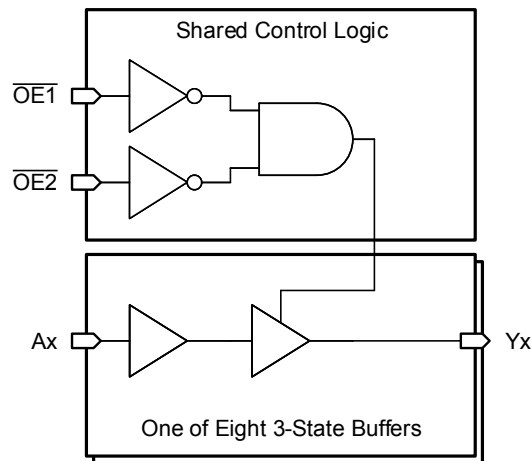


Figure 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance mode, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10-k Ω resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

8.3.2 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0 V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

8.3.3 Clamp Diode Structure

Figure 8-2 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

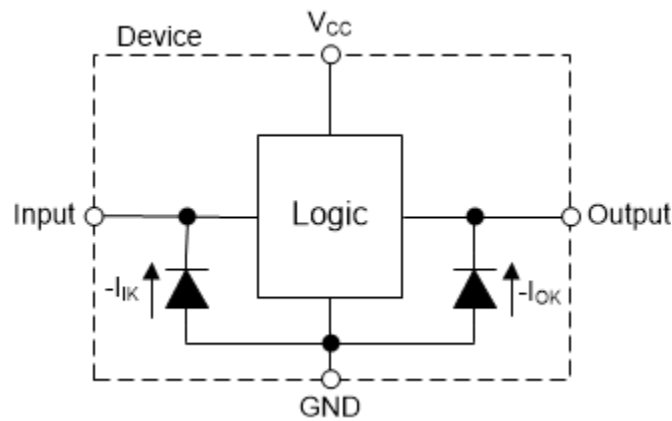


Figure 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

Table 8-1. Function Table
(Each Buffer or Driver)

INPUTS			OUTPUT Y
OE1	OE2	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV541A can be used to drive signals over relatively long traces or transmission lines. In order to reduce ringing caused by impedance mismatches between the driver, transmission line, and receiver, a series damping resistor placed in series with the transmitter's output can be used. The figure in the Application Curve section shows the received signal with three separate resistor values. Just a small amount of resistance can make a significant impact on signal integrity in this type of application.

9.2 Typical Application

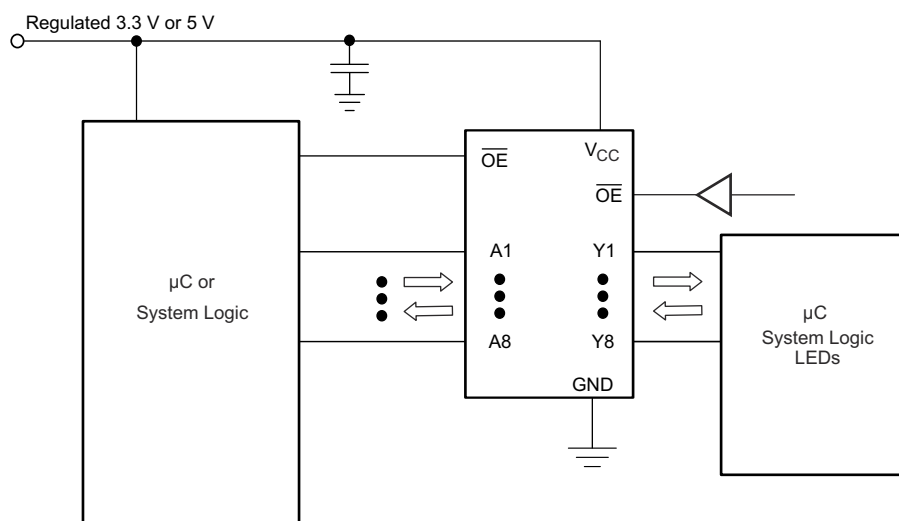


Figure 9-1. Typical Application Schematic

9.2.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV541A plus the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV541A plus the maximum supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV541A can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74LV541A can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV541A (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-k Ω resistor value is often used due to these factors.

The SN74LV541A has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

9.2.4 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV541A to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)}) \Omega$. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in M Ω ; much larger than the minimum calculated previously.

4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

9.2.5 Application Curves

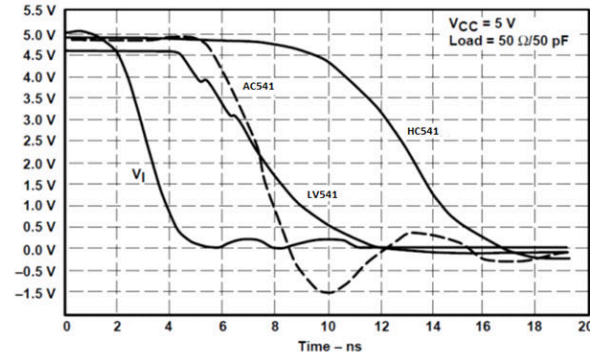


Figure 9-2. Switching Characteristics Comparison

9.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 9-3](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

9.4.2 Layout Example

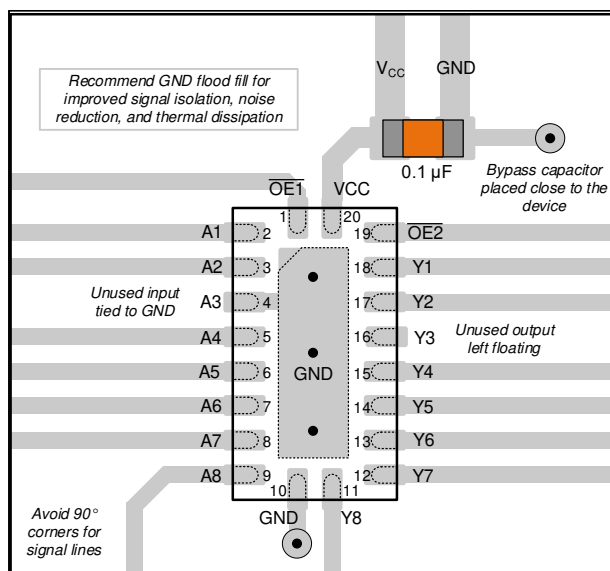


Figure 9-3. Layout Example for the SN74LV541A in the RKS package

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation](#)
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#) application notes
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#)

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LV541ADBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV541A
SN74LV541ADBR.A	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV541A
SN74LV541ADBRE4	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV541A
SN74LV541ADGSR	Active	Production	VSSOP (DGS) 20	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L541A
SN74LV541ADGSR.A	Active	Production	VSSOP (DGS) 20	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L541A
SN74LV541ADW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 125	LV541A
SN74LV541ADWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV541A
SN74LV541ADWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV541A
SN74LV541ANSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV541A
SN74LV541ANSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV541A
SN74LV541APWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV541A
SN74LV541APWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV541A
SN74LV541APWRG4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV541A
SN74LV541APWRG4.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV541A
SN74LV541ARGYR	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV541A
SN74LV541ARGYR.A	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV541A
SN74LV541ARKSR	Active	Production	VQFN (RKS) 20	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV541A
SN74LV541ARKSR.A	Active	Production	VQFN (RKS) 20	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV541A

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV541A :

- Automotive : [SN74LV541A-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



*All dimensions are nominal

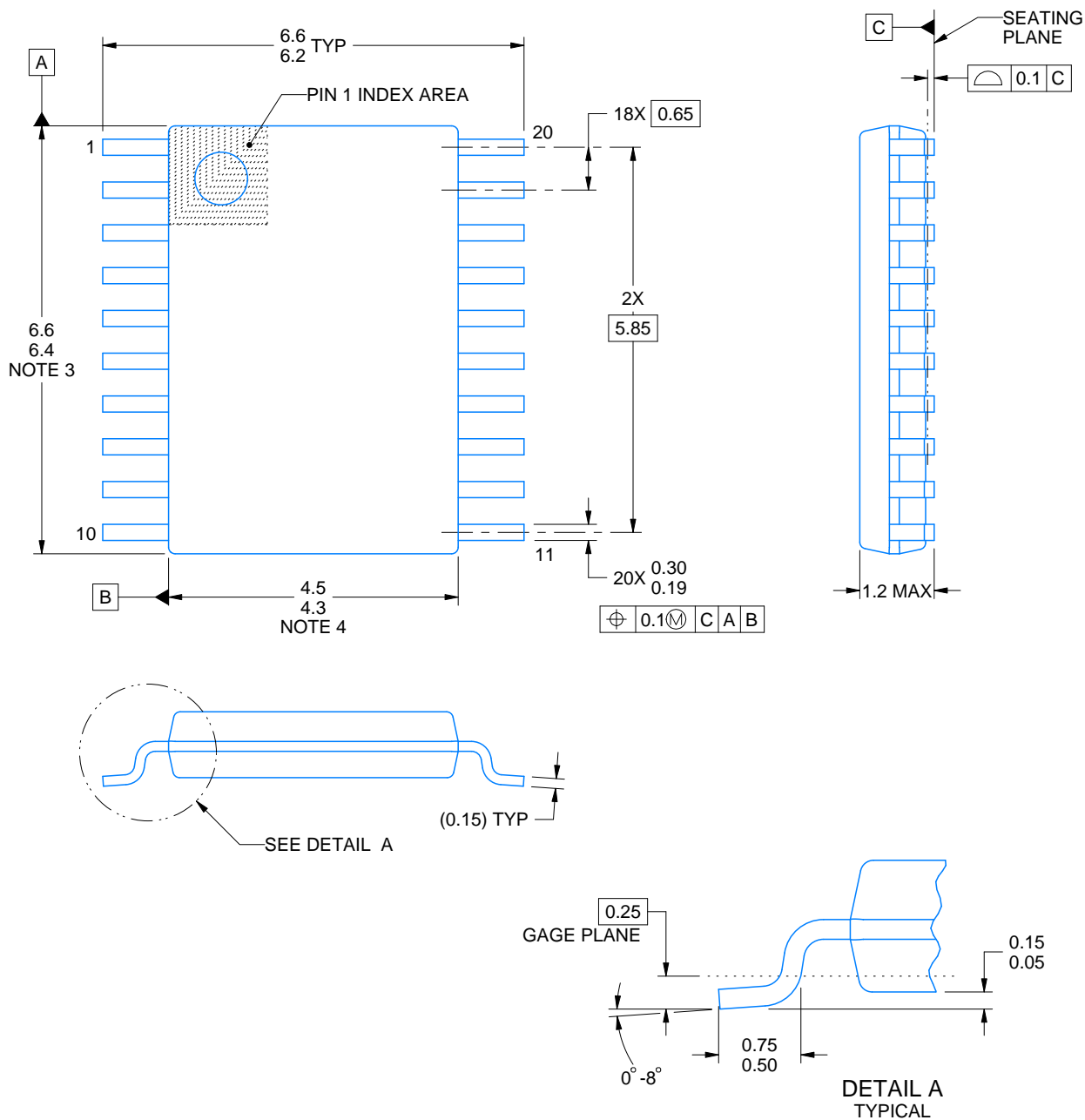
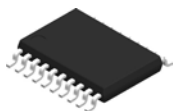
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV541ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LV541ADGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74LV541ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LV541ADWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74LV541ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LV541APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV541APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV541APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LV541ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
SN74LV541ARKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV541ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74LV541ADGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74LV541ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LV541ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LV541ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LV541APWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LV541APWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LV541APWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LV541ARGYR	VQFN	RGY	20	3000	353.0	353.0	32.0
SN74LV541ARKSR	VQFN	RKS	20	3000	210.0	185.0	35.0



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

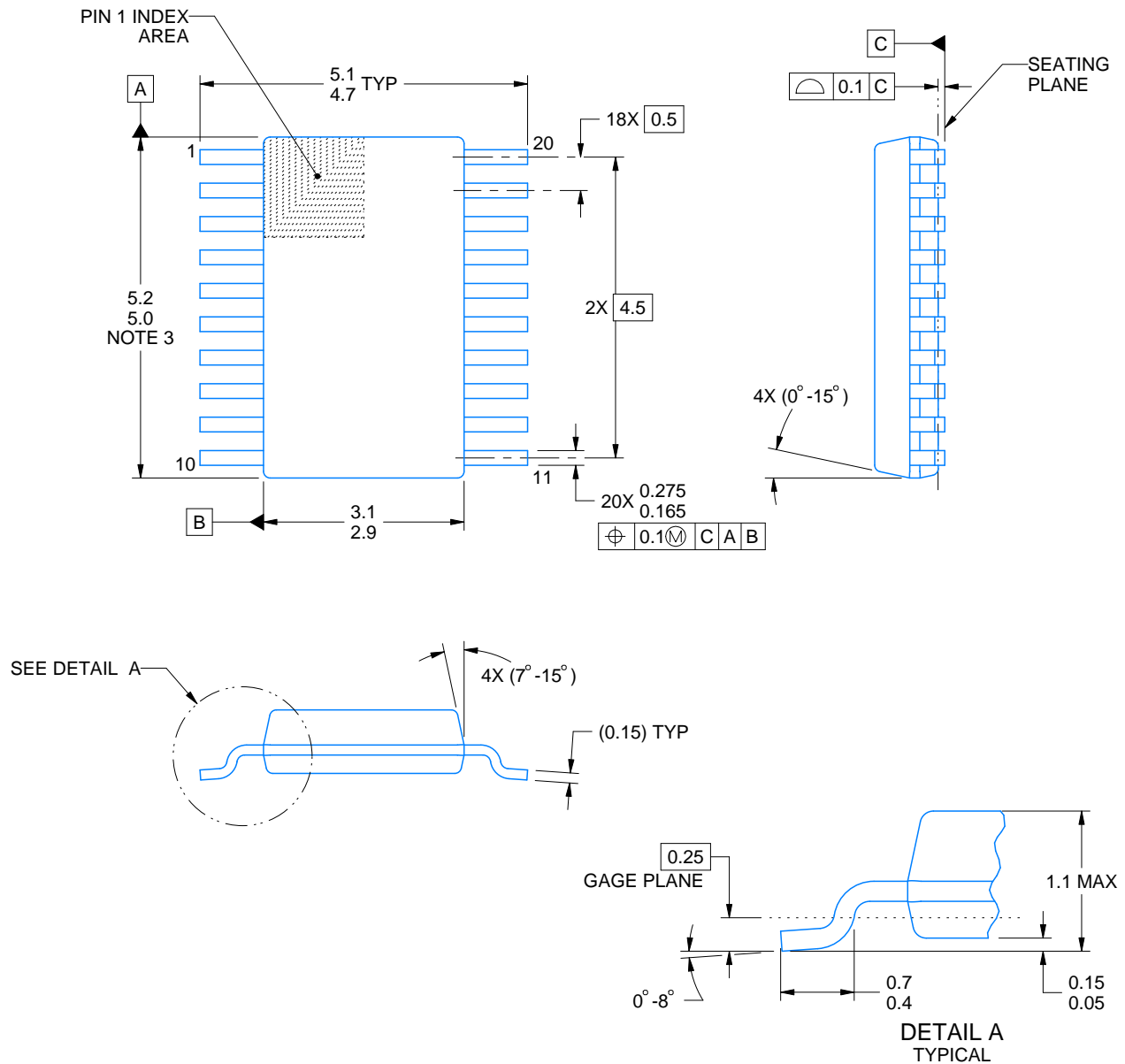


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4226367/A 10/2020

NOTES:

PowerPAD is a trademark of Texas Instruments.

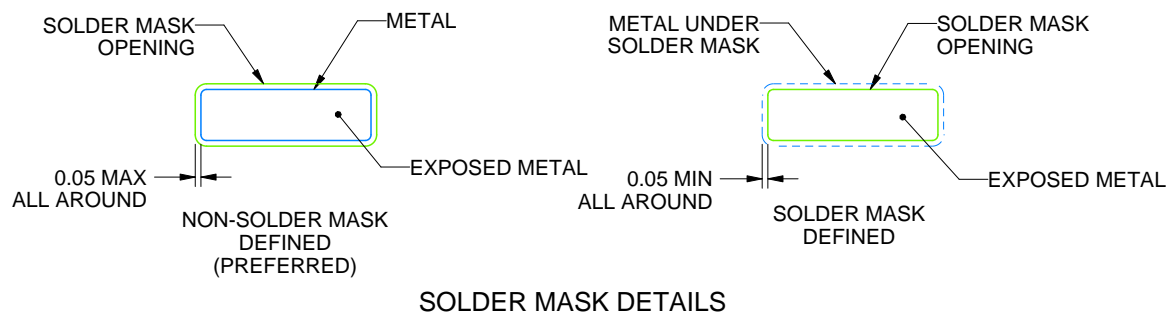
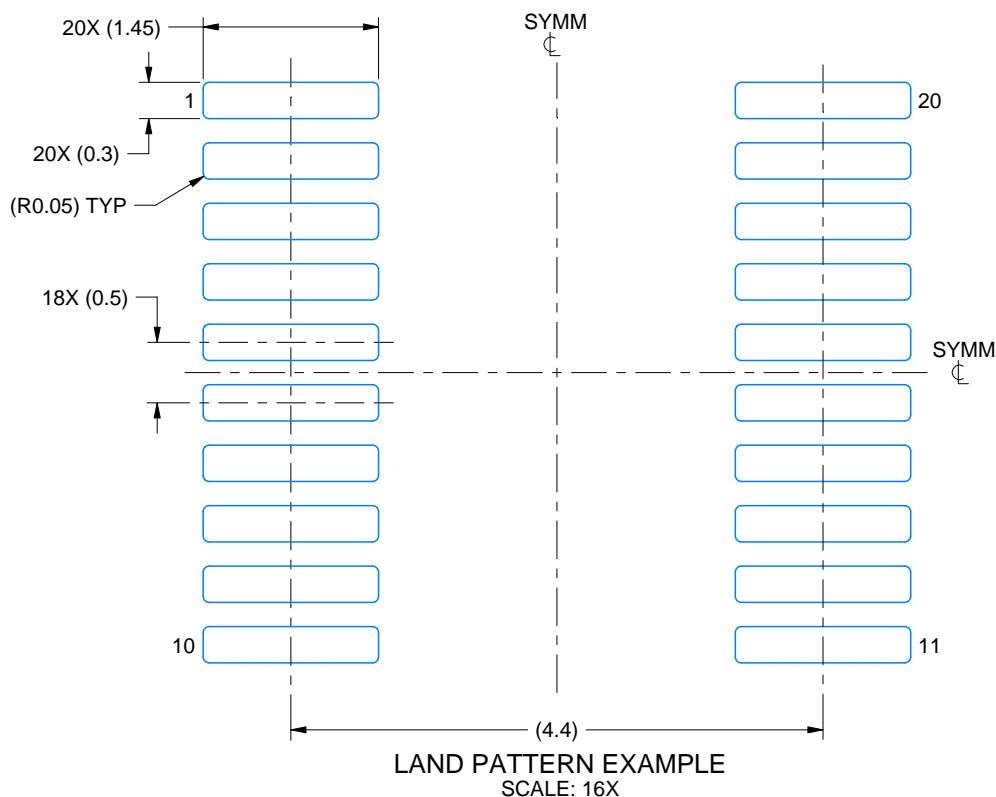
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4226367/A 10/2020

NOTES: (continued)

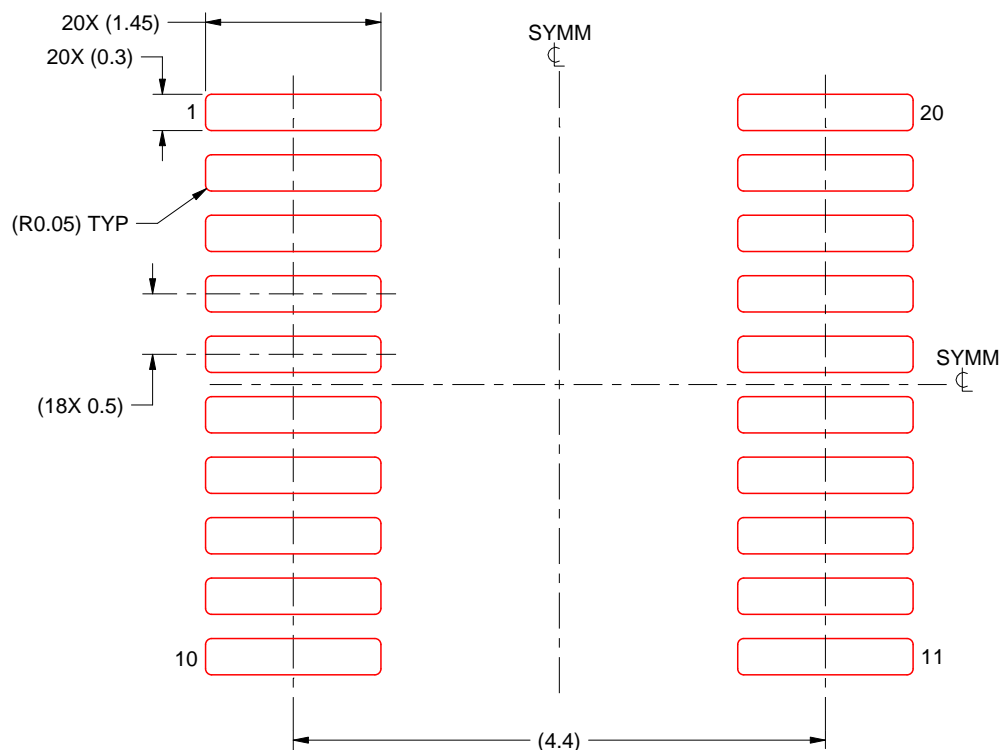
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

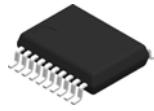


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

RKS 20

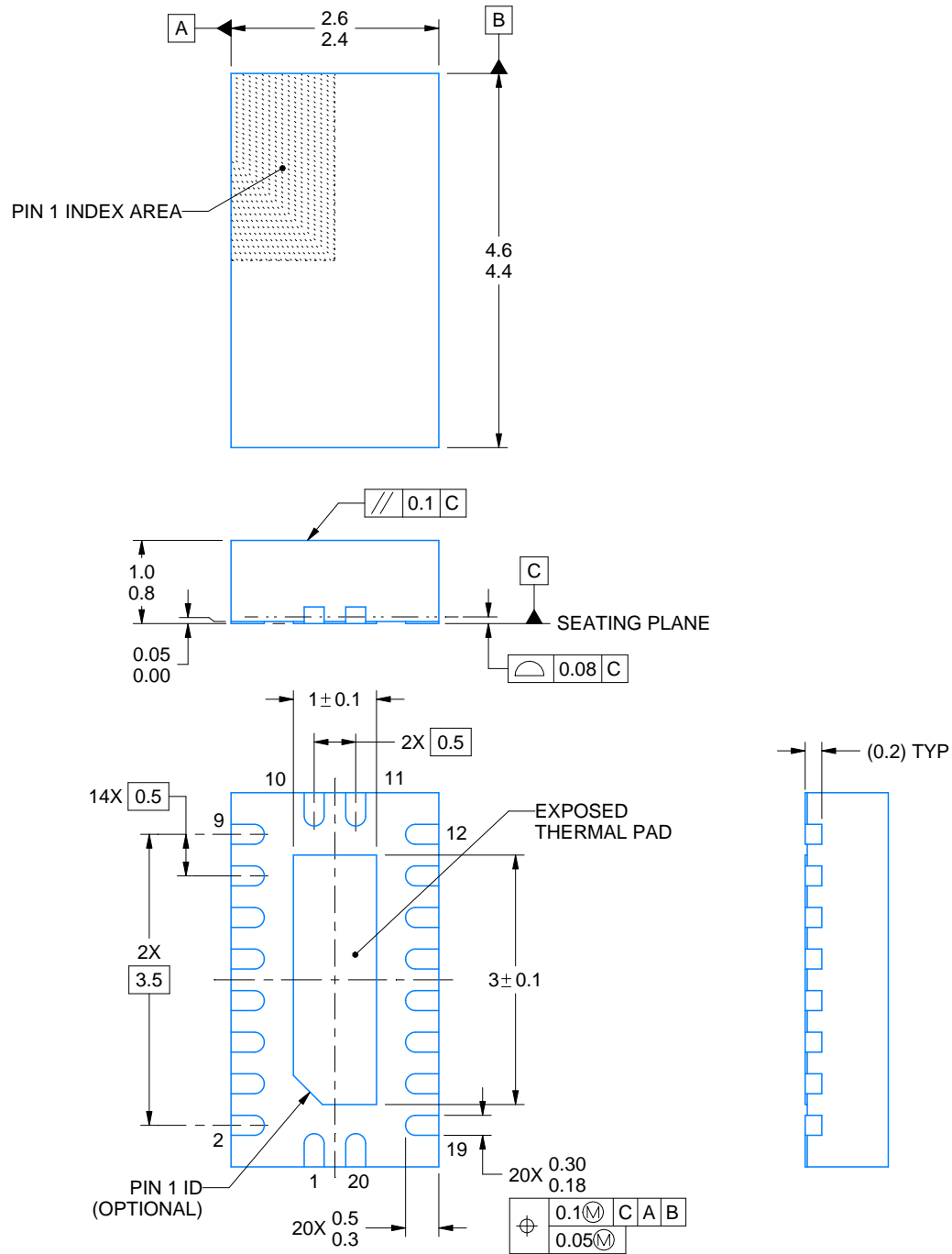
VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





4222490/B 02/2021

NOTES:

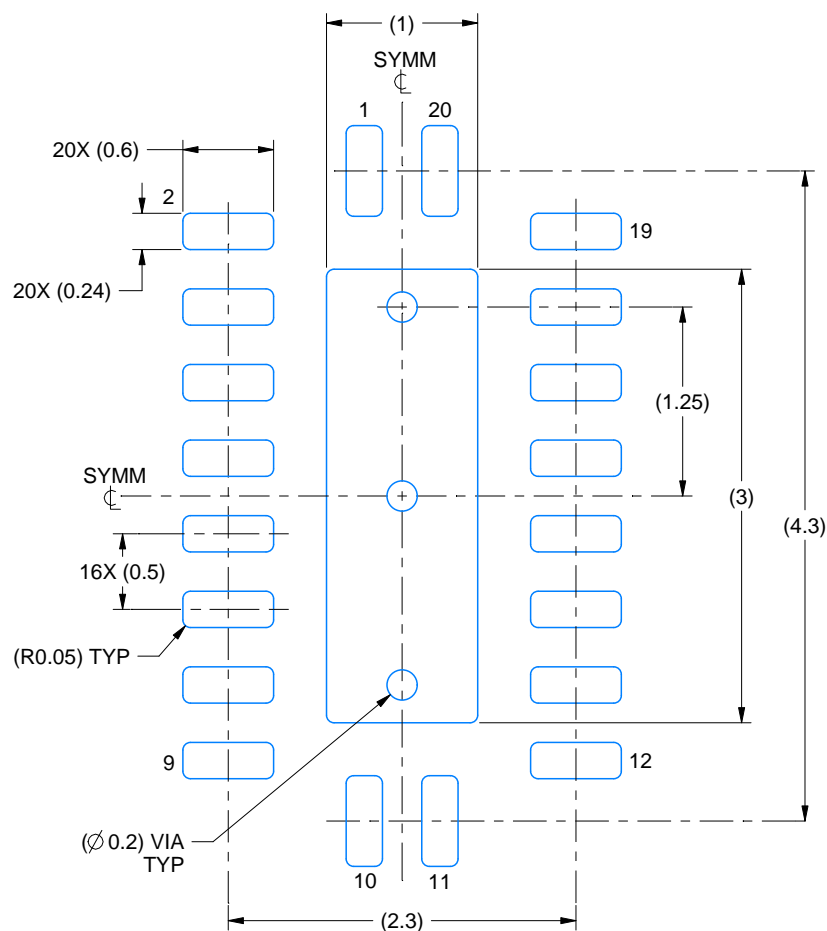
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

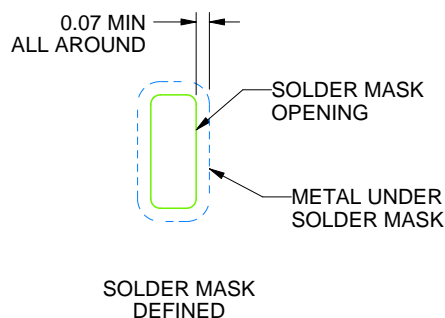
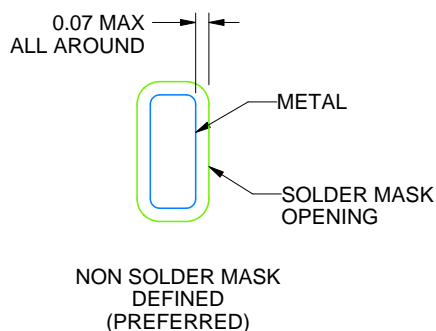
RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

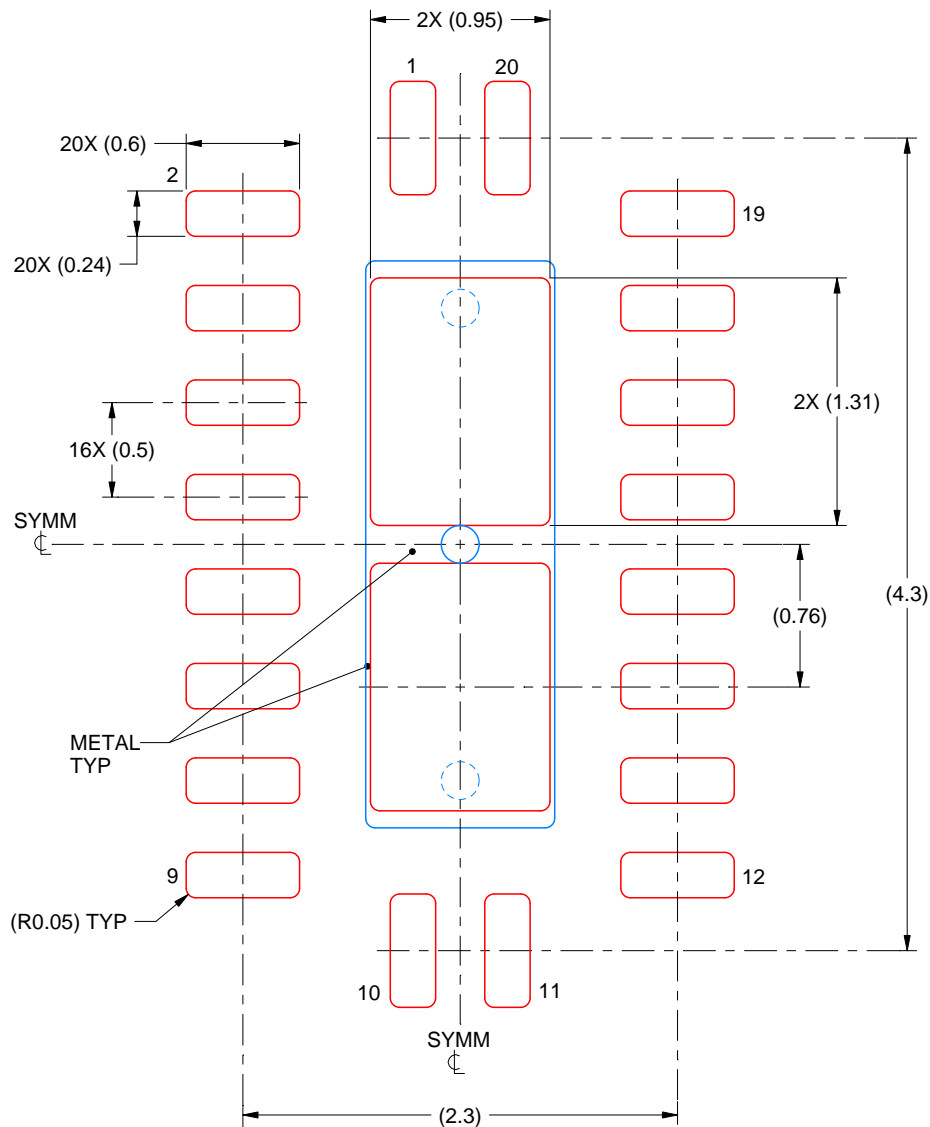
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

RKS0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 83% PRINTED SOLDER COVERAGE BY AREA
 SCALE:25X

4222490/B 02/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

RGY 20

VQFN - 1 mm max height

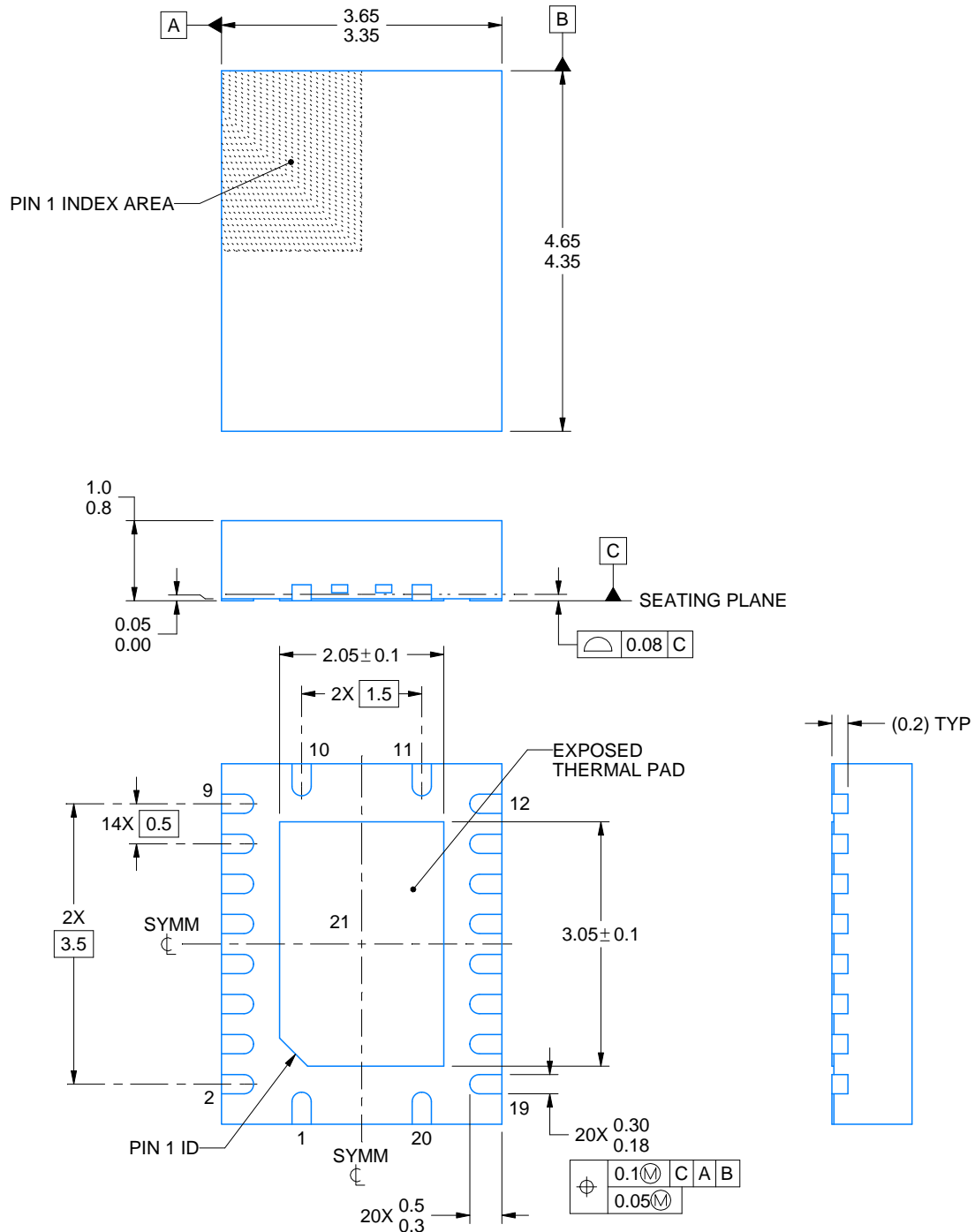
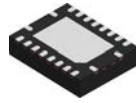
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225264/A



4225320/A 09/2019

NOTES:

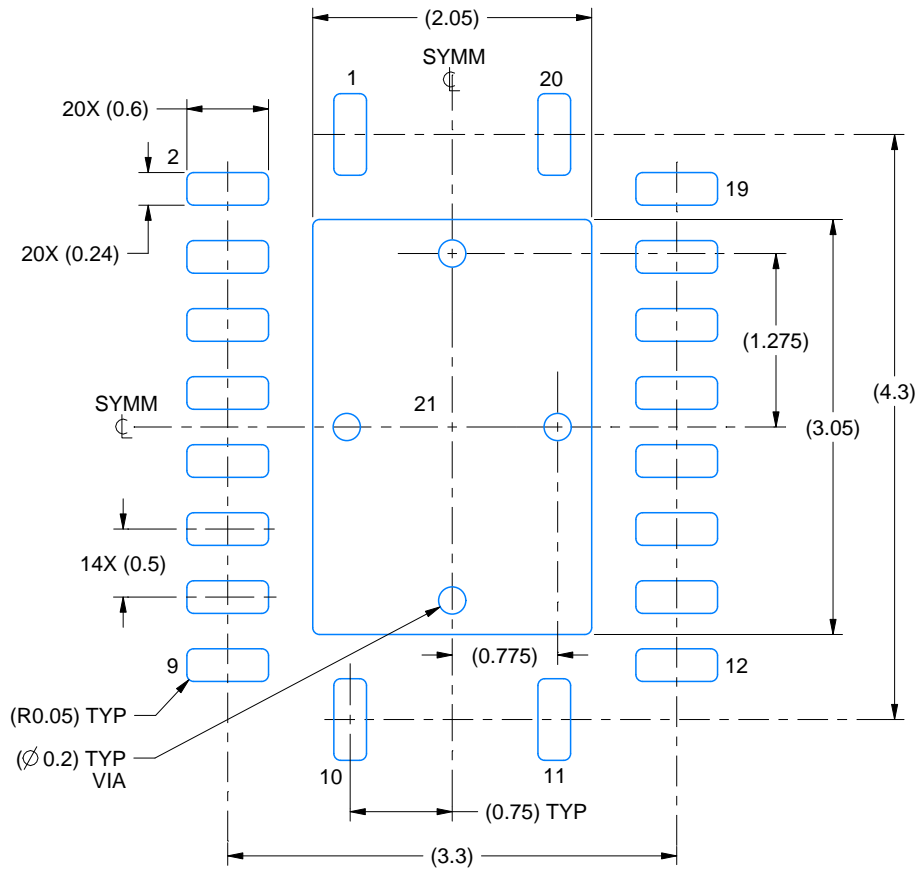
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

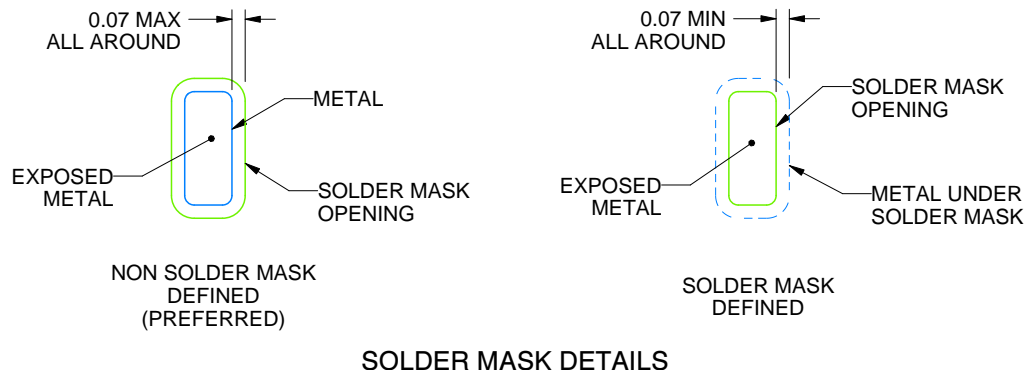
RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



4225320/A 09/2019

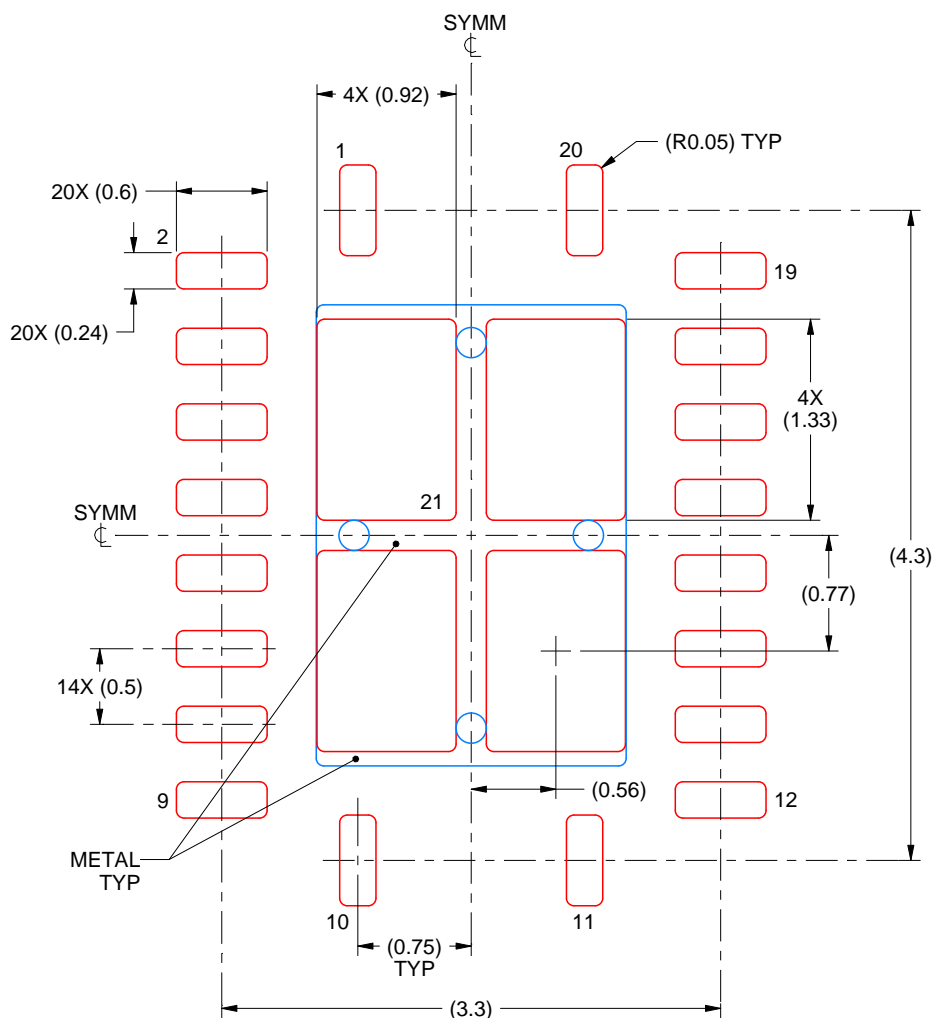
NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

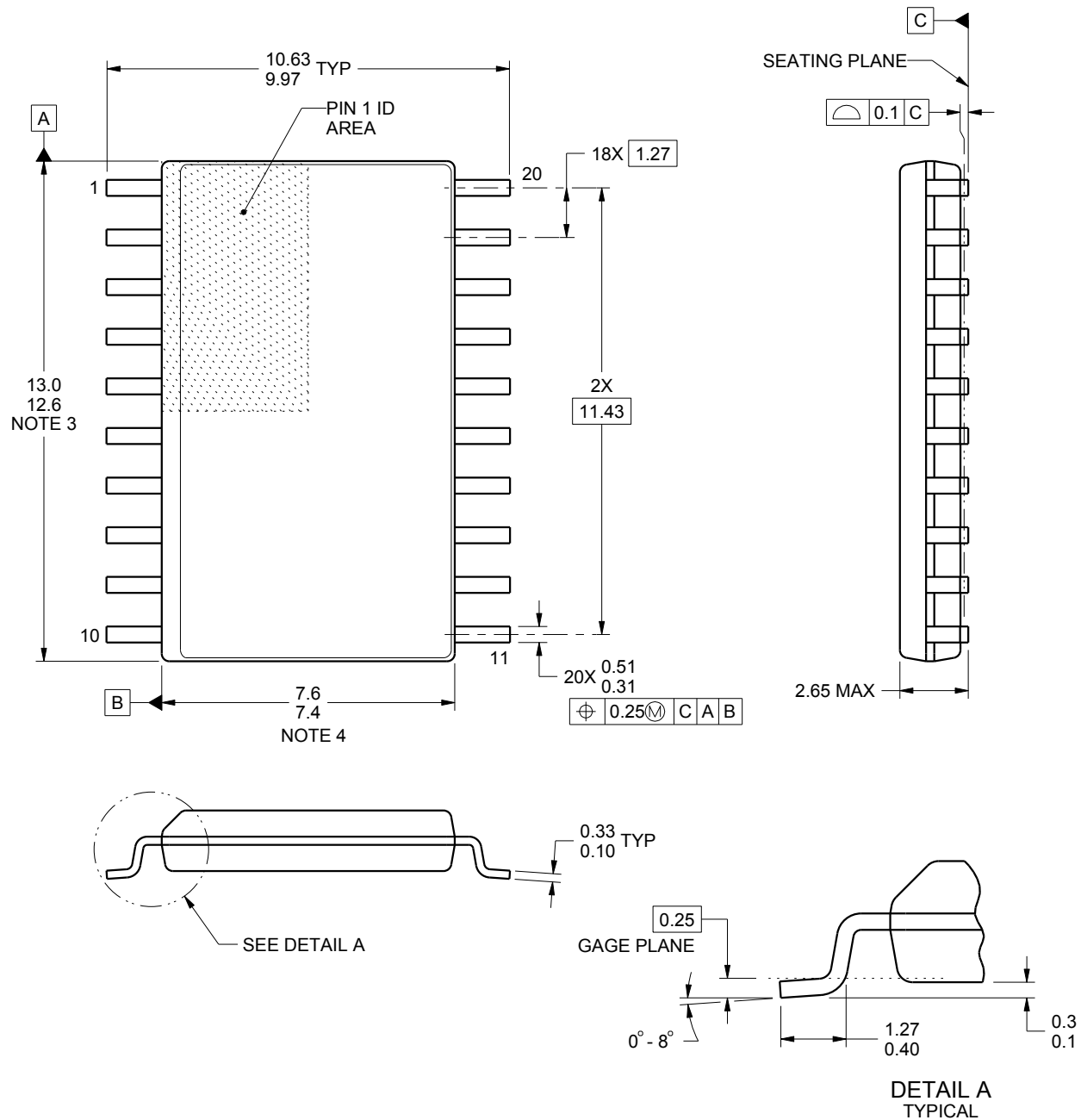
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DW0020A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

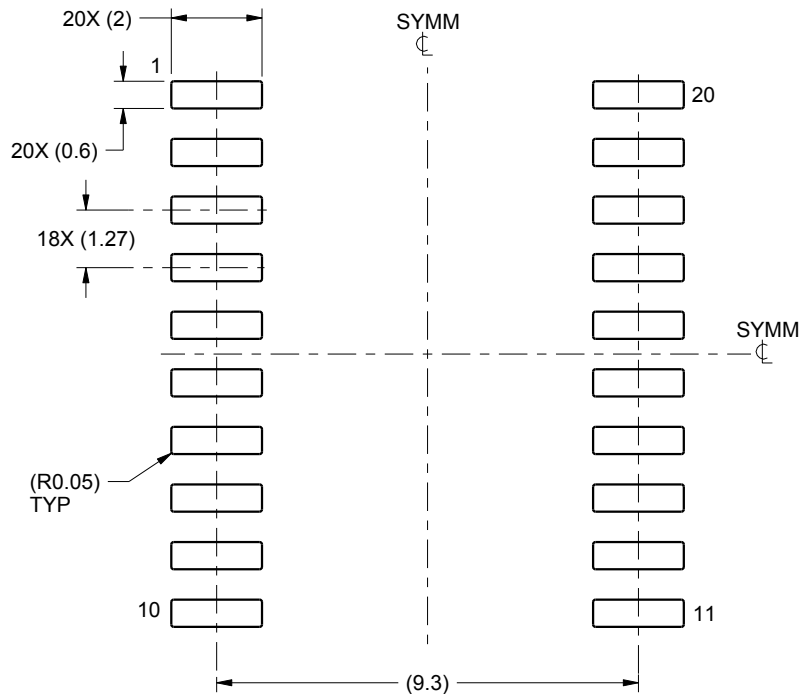
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

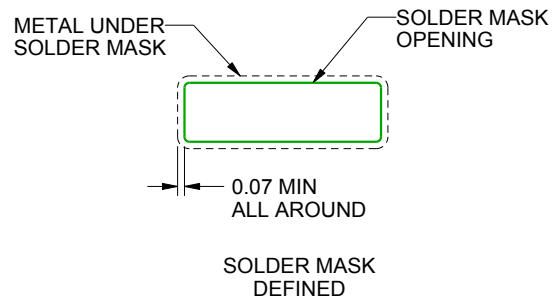
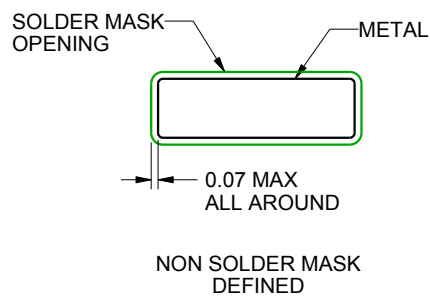
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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