

# SN74LVC02A-Q1 Automotive Quadruple 2-Input Positive-NOR Gate

#### 1 Features

- Qualified for automotive applications
- ESD protection exceeds 2000V per MIL-STD-883, Method 3015
- Inputs accept voltages to 5.5V

### 2 Description

The quadruple 2-input positive-NOR gate is designed for 2.7V to 3.6V V<sub>CC</sub> operation.

The SN74LVC02A-Q1 performs the Boolean function  $Y = \overline{A + B}$  or  $Y = \overline{A} \cdot \overline{B}$  in positive logic.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

#### **Package Information**

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE(2)	BODY SIZE(3)
	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
SN74LVC02A-Q1	D (SOIC, 14)	8.65mm × 6mm	8.65mm × 3.9mm
	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm

- For more information, see Section 10.
- The package size (length × width) is a nominal value and includes pins, where applicable.
- The body size (length × width) is a nominal value and does not include pins.



Logic Diagram, Each Gate (Positive Logic)



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# 3 Pin Configuration and Functions

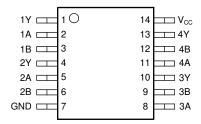


Figure 3-1. SN74LVC02A-Q1 D or PW Package, 14-Pin SOIC or TSSOP (Top View)

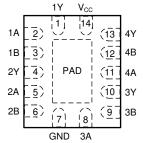


Figure 3-2. SN74LVC02A-Q1 BQA Package, 14-PIN WQFN (Top View)

Table 3-1. Pin Functions

PIN			
NAME	SN74LVC02A -Q1	TYPE <sup>(1)</sup>	DESCRIPTION
	BQA, D, PW		
1Y	1	0	1Y Output
1A	2	I	1A Input
1B	3	I	1B Input
2Y	4	0	2Y Output
2A	5	I	2A Input
2B	6	I	2B Input
GND	7	_	Ground Pin
3A	8	I	3A Input
3B	9	I	3B Input
3Y	10	0	3Y Output
4A	11	I	4A Input
4B	12	I	4B Input
4Y	13	0	4Y Output
V <sub>CC</sub>	14	_	Power Pin
NC	_	_	No Connection

(1) I = input, O = output



## 4 Specifications

## 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	6.5	V
VI	Input voltage range <sup>(1)</sup>		-0.5	6.5	V
Vo	Output voltage range <sup>(1)</sup> (2)		-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through V <sub>CC</sub> or GND			±100	mA
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

## 4.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	V

<sup>(1)</sup> AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 4.3 Recommended Operating Conditions

			MIN	MAX	UNIT
\/	Supply voltage	Operating	2	3.6	V
V <sub>CC</sub>	Supply voltage	Data retention only	1.5		V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2.7V to 3.6V	2		V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2.7V to 3.6V		0.8	V
VI	Input voltage		0	5.5	V
Vo	Output voltage		0	$V_{CC}$	V
1	High-level output current	V <sub>CC</sub> = 2.7V		-12	mA
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 3V		-24	ША
1	Low-level output current	V <sub>CC</sub> = 2.7V		12	mΑ
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 3V		24	ША
T <sub>A</sub>	Operating free-air temperature		-40	125	°C

#### 4.4 Thermal Information

			SN74LVC02A-Q1		
THERMAL METRIC <sup>(1)</sup>		BQA (WQFN)	D (SOIC)	PW (TSSOP)	UNIT
		14 PINS	14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	102.3	127.8	150.8	°C/W

<sup>(1)</sup> For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

Product Folder Links: SN74LVC02A-Q1

<sup>(2)</sup> The value of V<sub>CC</sub> is provided in the recommended operating conditions table.

#### 4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup> MAX	UNIT
	$I_{OH} = -100 \mu A$	2.7V to 3.6V	V <sub>CC</sub> - 0.2		
V <sub>OH</sub>	I <sub>OH</sub> = -12mA	2.7V	2.2		V
VOH	10H = -12111A	3V	2.4		V
	$I_{OH} = -24$ mA	3V	2.2		
	I <sub>OL</sub> = 100μA	2.7V to 3.6V		0.2	
V <sub>OL</sub>	I <sub>OL</sub> = 12mA	2.7V		0.4	V
	I <sub>OL</sub> = 24mA	3V		0.55	
I <sub>I</sub>	V <sub>I</sub> = 5.5V or GND	3.6V		±5	μΑ
I <sub>CC</sub>	$V_1 = V_{CC}$ or GND, $I_0 = 0$	3.6V		10	μΑ
ΔI <sub>CC</sub>	One input at $V_{CC} - 0.6V$ , Other inputs at $V_{CC}$ or GND	2.7V to 3.6V		500	μΑ
C <sub>i</sub>	$V_I = V_{CC}$ or GND	3.3V		5	pF

<sup>(1)</sup> All typical values are at  $V_{CC} = 3.3V$ ,  $T_A = 25$ °C.

# 4.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 2.7V	V <sub>CC</sub> = 3.3V ±0.3V		UNIT
	(INFOT)	(001701)	MIN MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Y	6.5	1	5.5	ns

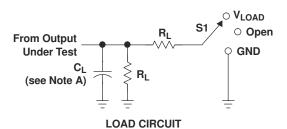
# 4.7 Operating Characteristics

 $T_A = 25^{\circ}C$ 

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 2.5V	V <sub>CC</sub> = 3.3V	UNIT
FARAINETER	TEST CONDITIONS	TYP	TYP	ONIT
C <sub>pd</sub> Power dissipation capacitance per gate	f = 10MHz	8.5	9.5	pF

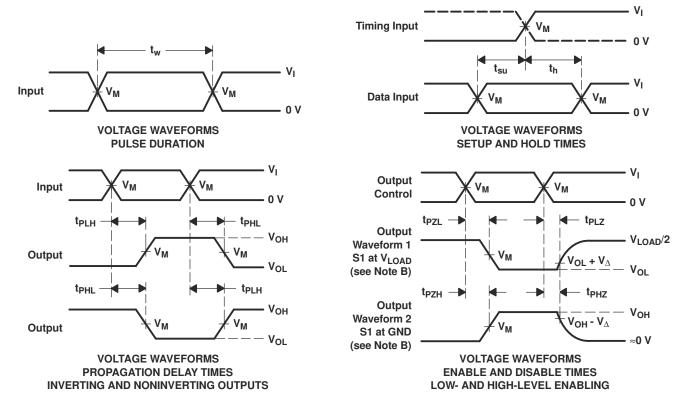


#### **5 Parameter Measurement Information**



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

		INPUTS		V			.,
V <sub>CC</sub>	VI	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	V <sub>LOAD</sub>	CL	RL	$V_{\Delta}$
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V $\pm$ 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	<b>500</b> Ω	0.3 V



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \ \Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.
- H. All parameters and waveforms are not applicable to all devices.

Figure 5-1. Load Circuit and Voltage Waveforms

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# **6 Detailed Description**

# **6.1 Functional Block Diagram**



Figure 6-1. Logic Diagram, Each Gate (Positive Logic)

### **6.2 Device Functional Modes**

# Function Table (Each Gate)

INP	UTS	OUTPUT
Α	В	Υ
Н	Х	L
Х	Н	L
L	L	Н

## 7 Application and Implementation

#### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

## 7.2 Layout

#### 7.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V<sub>CC</sub>, whichever makes more sense for the logic function or is more convenient.

#### 7.2.2 Layout Example

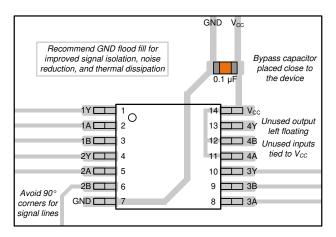


Figure 7-1. Example Layout for the SN74LVC02A-Q1

Product Folder Links: SN74LVC02A-Q1

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## 8 Device and Documentation Support

## 8.1 Documentation Support (Analog)

#### 8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

#### Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY	
SN74LVC02A-Q1	Click here	Click here	Click here	Click here	Click here	

#### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 8.3 Support Resources

TI E2E<sup>™</sup> support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### 8.4 Trademarks

TI E2E<sup>™</sup> is a trademark of Texas Instruments.

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#### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 8.6 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

#### 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Cł	hanges from Revision E (May 2024) to Revision F (December 2024)	Page
•	Updated RθJA values: PW = 86 to 127.8, all values in °C/W	4

# Changes from Revision D (March 2024) to Revision E (May 2024)Page• Updated RθJA values: PW = 113 to 150.8, all values in °C/W4

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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#### PACKAGING INFORMATION

Orderable part number	Status	Material type	Package   Pins	Package qty   Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
SN74LVC02AQDRG4Q1	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC02AQ
SN74LVC02AQDRG4Q1.B	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC02AQ
SN74LVC02AQDRQ1	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC02AQ
SN74LVC02AQDRQ1.A	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC02AQ
SN74LVC02AQDRQ1.B	Active	Production	SOIC (D)   14	2500   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC02AQ
SN74LVC02AQPWRG4Q1	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC02AQ
SN74LVC02AQPWRG4Q1.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC02AQ
SN74LVC02AQPWRQ1	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC02AQ
SN74LVC02AQPWRQ1.A	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC02AQ
SN74LVC02AQPWRQ1.B	Active	Production	TSSOP (PW)   14	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC02AQ
SN74LVC02AWBQARQ1	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC02Q
SN74LVC02AWBQARQ1.A	Active	Production	WQFN (BQA)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC02Q

<sup>(1)</sup> Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

<sup>(2)</sup> Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

<sup>(4)</sup> Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

# PACKAGE OPTION ADDENDUM

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### OTHER QUALIFIED VERSIONS OF SN74LVC02A-Q1:

Catalog: SN74LVC02A

Enhanced Product: SN74LVC02A-EP

Military: SN54LVC02A

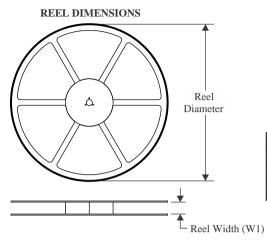
NOTE: Qualified Version Definitions:

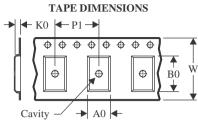
- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications

# **PACKAGE MATERIALS INFORMATION**

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### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

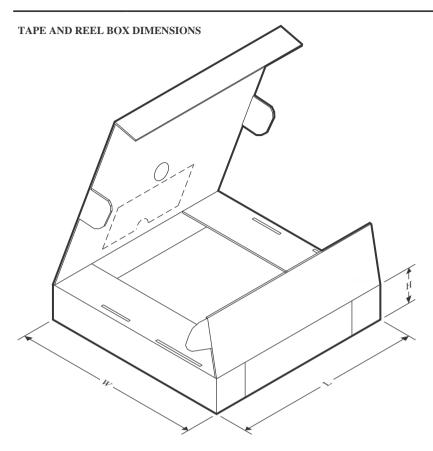


#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC02AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC02AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC02AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC02AWBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1



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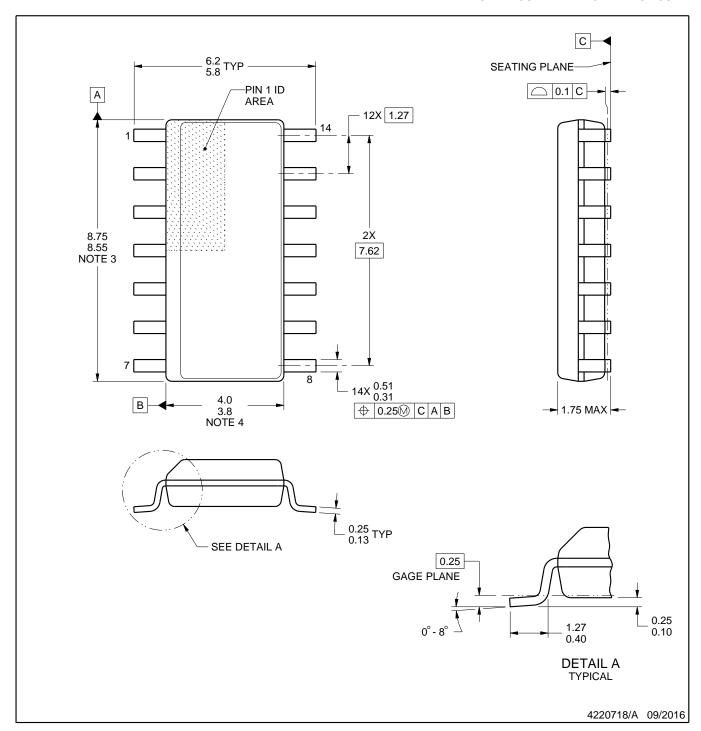


#### \*All dimensions are nominal

7 till dillitoriolorio di o mominar							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC02AQPWRG4Q1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC02AQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC02AQPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC02AWBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0



SMALL OUTLINE INTEGRATED CIRCUIT



#### NOTES:

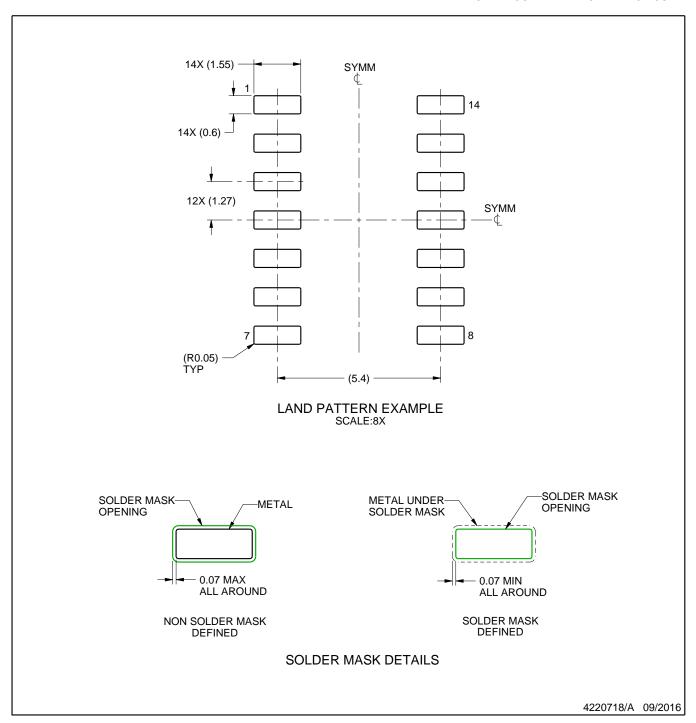
- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
- 5. Reference JEDEC registration MS-012, variation AB.



SMALL OUTLINE INTEGRATED CIRCUIT



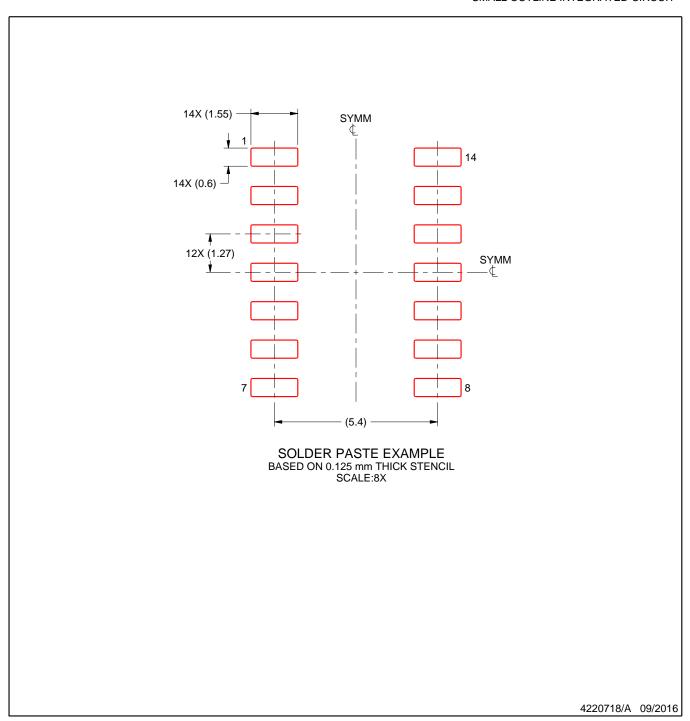
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

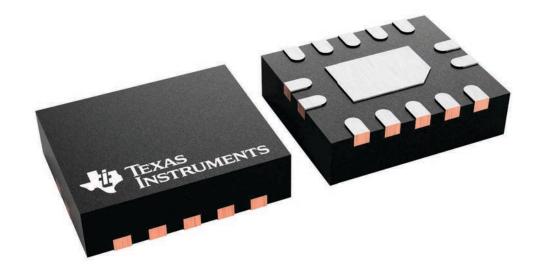
- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

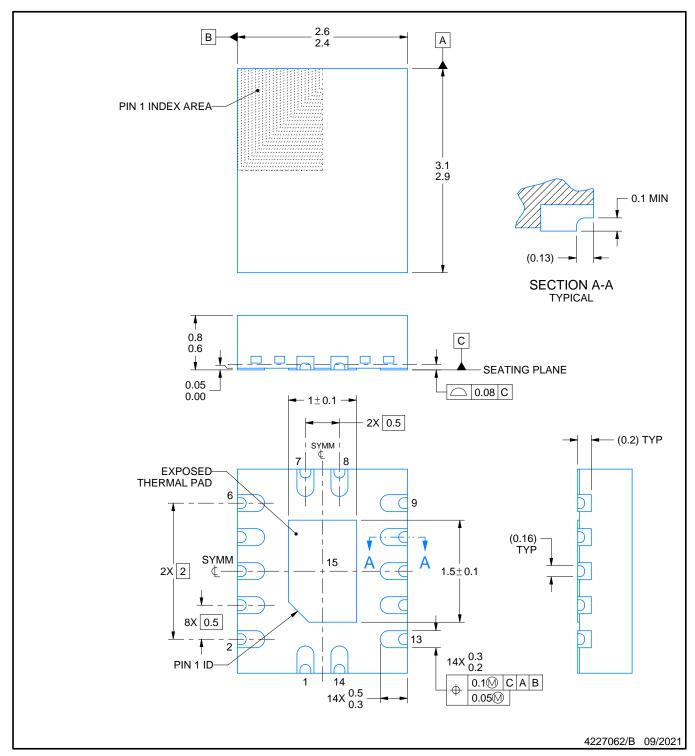
This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



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PLASTIC QUAD FLATPACK - NO LEAD

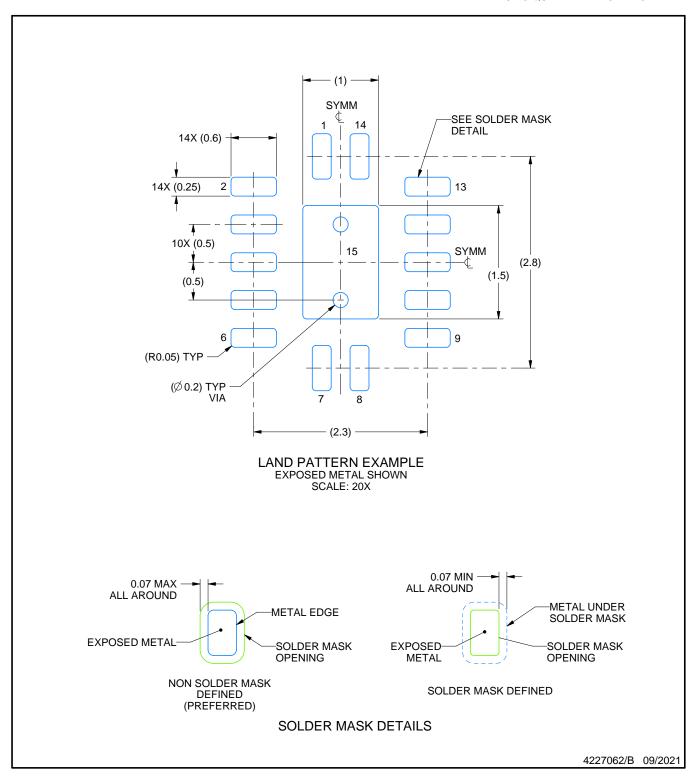


#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD

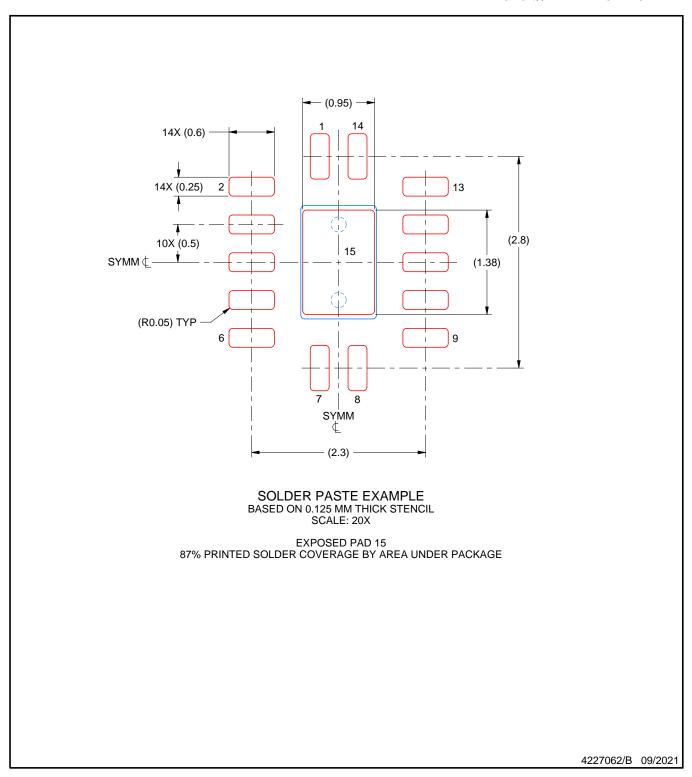


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



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NOTES: (continued)

<sup>6.</sup> Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.





SMALL OUTLINE PACKAGE



#### NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

  2. This drawing is subject to change without notice.

  3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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