



## SNx4LVC04A Hex Inverters

### 1 Features

- Operate From 1.65 V to 3.6 V
- Specified From  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ , and  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Inputs Accept Voltages to 5.5 V
- Maximum  $t_{pd}$  of 4.5 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^{\circ}\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2\text{ V}$  at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^{\circ}\text{C}$
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- Power Sub-Station Controls
- Ethernet Switches
- Flow Meters
- I/O Modules and Digital PLC/DCS Inputs
- Servers
- Tests and Measurement

### 3 Description

The SNx4LVC04A hex inverters contains six independent inverters designed for 2.7-V to 3.6-V  $V_{CC}$  operation, and the SN74LVC04A hex inverter contains six independent inverters designed for 1.65-V to 3.6-V  $V_{CC}$  operation. The SNx4LVC04A devices perform the Boolean function  $Y = \bar{A}$ .

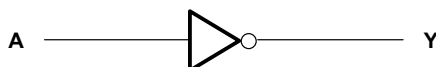
Inputs can be driven from 1.8-V or 3.3-V devices. This feature allows the use of these devices as translators in a mixed 1.8-V or 3.3-V system environment.

**Device Information<sup>(1)</sup>**

| PART NUMBER | PACKAGE    | BODY SIZE (NOM)    |
|-------------|------------|--------------------|
| SN54LVC04A  | CDIP (14)  | 19.56 mm × 6.67 mm |
|             | CFP (14)   | 9.21 mm × 5.97 mm  |
|             | LCCC (20)  | 8.89 mm × 8.89 mm  |
| SN74LVC04A  | SOIC (14)  | 8.65 mm × 3.91 mm  |
|             | SSOP (14)  | 6.20 mm × 5.30 mm  |
|             | TVSOP (14) | 3.60 mm × 4.40 mm  |
|             | SOP (14)   | 6.20 mm × 5.30 mm  |
|             | TSSOP (14) | 5.00 mm × 4.40 mm  |
|             | VQFN (14)  | 3.50 mm × 3.50 mm  |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Logic Diagram, Each Inverter (Positive Logic)



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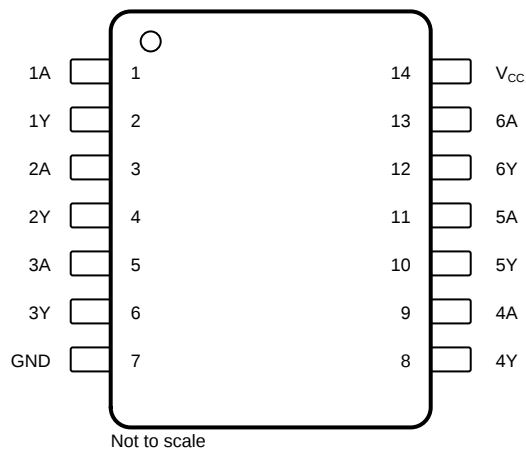
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

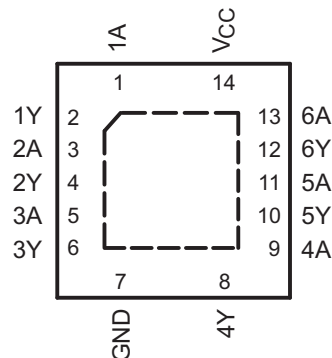
| Changes from Revision S (October 2010) to Revision T                                                                                                                                                                                                                                                                                                                              | Page     |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| • Added <i>Applications</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section ..... | <b>1</b> |
| • Deleted <i>Ordering Information</i> table; see <i>Package Option Addendum</i> at the end of the data sheet .....                                                                                                                                                                                                                                                                | <b>1</b> |
| • Added <i>Thermal Information Table – SN54LVC04A</i> .....                                                                                                                                                                                                                                                                                                                       | <b>6</b> |
| • Changed Package thermal impedance, $R_{\theta JA}$ , values in <i>Thermal Information – SN74LVC04A</i> From: 96 To: 113.1 (DB), From: 127 To: 142.7 (DGV), From: 76 To: 95.4 (NS), From: 113 To: 129.5 (PW), and From: 47 To: 63.2 (RGY) .....                                                                                                                                  | <b>6</b> |

## 5 Pin Configuration and Functions

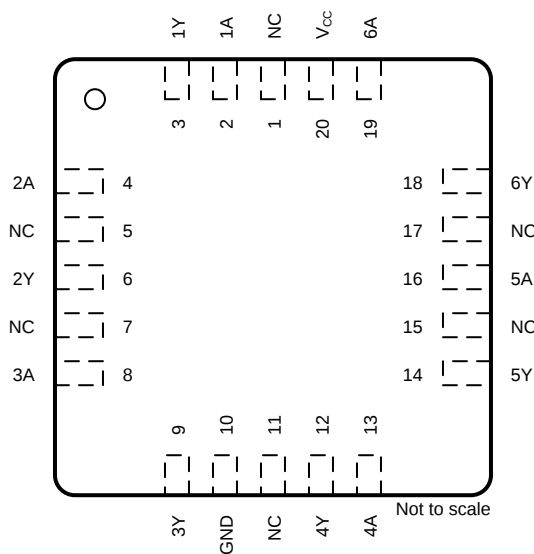
**D, DB, DGV, J, NS, PW, or W Package**  
**14-Pin SOIC, SSOP, TVSOP, CDIP, SOP, TSSOP, or CFP**  
**Top View**



**RGY Package**  
**14-Pin VQFN With Exposed Thermal Pad**  
**Top View**



**FK Package**  
**20-Pin LCCC**  
**Top View**



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**Pin Functions**

| PIN             |                                  |                        | I/O | DESCRIPTION            |
|-----------------|----------------------------------|------------------------|-----|------------------------|
| NAME            | D, DB, DGV, J,<br>NS, PW, RGY, W | FK, LCCC               |     |                        |
| 1A              | 1                                | 2                      | I   | Channel 1 input        |
| 1Y              | 2                                | 3                      | O   | Channel 1 output       |
| 2A              | 3                                | 4                      | I   | Channel 2 input        |
| 2Y              | 4                                | 6                      | O   | Channel 2 output       |
| 3A              | 5                                | 8                      | I   | Channel 3 input        |
| 3Y              | 6                                | 9                      | O   | Channel 3 output       |
| 4A              | 9                                | 13                     | I   | Channel 4 input        |
| 4Y              | 8                                | 12                     | O   | Channel 4 output       |
| 5A              | 11                               | 16                     | I   | Channel 5 input        |
| 5Y              | 10                               | 14                     | O   | Channel 5 output       |
| 6A              | 13                               | 19                     | I   | Channel 6 input        |
| 6Y              | 12                               | 18                     | O   | Channel 6 output       |
| GND             | 7                                | 10                     | —   | Ground                 |
| NC              | —                                | 1, 5, 7,<br>11, 15, 17 | —   | No internal connection |
| V <sub>CC</sub> | 14                               | 20                     | —   | Power supply           |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                                    |                                                                    | MIN  | MAX            | UNIT |
|----------------------------------------------------|--------------------------------------------------------------------|------|----------------|------|
| Supply voltage, $V_{CC}$                           |                                                                    | –0.5 | 6.5            | V    |
| Input voltage, $V_I$ <sup>(2)</sup>                |                                                                    | –0.5 | 6.5            | V    |
| Output voltage, $V_O$ <sup>(2)(3)</sup>            |                                                                    | –0.5 | $V_{CC} + 0.5$ | V    |
| Input clamp current, $I_{IK}$                      | $V_I < 0$                                                          |      | –50            | mA   |
| Output clamp current, $I_{OK}$                     | $V_O < 0$                                                          |      | –50            | mA   |
| Continuous output current, $I_O$                   |                                                                    |      | ±50            | mA   |
| Continuous current through $V_{CC}$ or GND         |                                                                    |      | ±100           | mA   |
| Power dissipation, $P_{tot}$                       | $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ <sup>(4)(5)</sup> |      | 500            | mW   |
| Maximum virtual junction temperature, $T_{J(MAX)}$ |                                                                    |      | 150            | °C   |
| Storage temperature, $T_{stg}$                     |                                                                    | –65  | 150            | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in [Recommended Operating Conditions](#).
- (4) For the D package: above  $70^\circ\text{C}$ , the value of  $P_{tot}$  derates linearly with 8 mW/K.
- (5) For the DB, DGV, NS, and PW packages: above  $60^\circ\text{C}$ , the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

### 6.2 ESD Ratings

|                                     |                                                                                | VALUE | UNIT |
|-------------------------------------|--------------------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|                                     | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1000 |      |
|                                     | Machine Model (MM)                                                             | ±200  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                           |                                                     | MIN        | MAX                    | UNIT            |    |
|-----------------|---------------------------|-----------------------------------------------------|------------|------------------------|-----------------|----|
| V <sub>CC</sub> | Supply voltage            | Operating                                           | SN54LVC04A | 2                      | 3.6             | V  |
|                 |                           |                                                     | SN74LVC04A | 1.65                   | 3.6             |    |
|                 |                           | Data retention only                                 |            | 1.5                    |                 |    |
| V <sub>IH</sub> | High-level input voltage  | V <sub>CC</sub> = 1.65 V to 1.95 V, SN74LVC04A only |            | 0.65 × V <sub>CC</sub> |                 | V  |
|                 |                           | V <sub>CC</sub> = 2.3 V to 2.7 V, SN74LVC04A only   |            | 1.7                    |                 |    |
|                 |                           | V <sub>CC</sub> = 2.7 V to 3.6 V                    |            | 2                      |                 |    |
| V <sub>IL</sub> | Low-level input voltage   | V <sub>CC</sub> = 1.65 V to 1.95 V, SN74LVC04A only |            | 0.35 × V <sub>CC</sub> |                 | V  |
|                 |                           | V <sub>CC</sub> = 2.3 V to 2.7 V, SN74LVC04A only   |            | 0.7                    |                 |    |
|                 |                           | V <sub>CC</sub> = 2.7 V to 3.6 V                    |            | 0.8                    |                 |    |
| V <sub>I</sub>  | Input voltage             |                                                     |            | 0                      | 5.5             | V  |
| V <sub>O</sub>  | Output voltage            |                                                     |            | 0                      | V <sub>CC</sub> | V  |
| I <sub>OH</sub> | High-level output current | V <sub>CC</sub> = 1.65 V, SN74LVC04A only           |            | −4                     |                 | mA |
|                 |                           | V <sub>CC</sub> = 2.3 V, SN74LVC04A only            |            | −8                     |                 |    |
|                 |                           | V <sub>CC</sub> = 2.7 V                             |            | −12                    |                 |    |
|                 |                           | V <sub>CC</sub> = 3 V                               |            | −24                    |                 |    |

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. See TI application report, [Implications of Slow or Floating CMOS Inputs](#) (SCBA004).

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### Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|          |                                            | MIN | MAX | UNIT |
|----------|--------------------------------------------|-----|-----|------|
| $I_{OL}$ | Low-level output current                   |     |     |      |
|          | $V_{CC} = 1.65\text{ V}$ , SN74LVC04A only |     | 4   | mA   |
|          | $V_{CC} = 2.3\text{ V}$ , SN74LVC04A only  |     | 8   |      |
|          | $V_{CC} = 2.7\text{ V}$                    |     | 12  |      |
|          | $V_{CC} = 3\text{ V}$                      |     | 24  |      |

### 6.4 Thermal Information – SN54LVC04A

| THERMAL METRIC <sup>(1)</sup> |                                              | SN54LVC04A |         |           | UNIT |
|-------------------------------|----------------------------------------------|------------|---------|-----------|------|
|                               |                                              | J (CDIP)   | W (CFP) | FK (LCCC) |      |
|                               |                                              | 14 PINS    | 14 PINS | 20 PINS   |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 92         | 158.2   | 85        | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 55.1       | 88.7    | 62.5      | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 80.5       | 156.5   | 61.2      | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 40.2       | 58.5    | 55.8      | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 74.2       | 135.5   | 61.2      | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | 25.3       | 15.3    | 10.4      | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 6.5 Thermal Information – SN74LVC04A

| THERMAL METRIC <sup>(1)</sup> |                                              | SN74LVC04A |           |             |          |            |            | UNIT |
|-------------------------------|----------------------------------------------|------------|-----------|-------------|----------|------------|------------|------|
|                               |                                              | D (SOIC)   | DB (SSOP) | DGV (TVSOP) | NS (SOP) | PW (TSSOP) | RGY (VQFN) |      |
|                               |                                              | 14 PINS    | 14 PINS   | 14 PINS     | 14 PINS  | 14 PINS    | 14 PINS    |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 105.7      | 113.1     | 142.7       | 95.4     | 129.5      | 63.2       | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 50.8       | 65.1      | 61.9        | 53.2     | 57.9       | 61         | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 46.1       | 60.5      | 72.1        | 54.2     | 71.3       | 39.1       | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 8.2        | 29.1      | 10.1        | 21.9     | 9.9        | 5.2        | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 45.6       | 60        | 71.4        | 53.8     | 70.7       | 39.1       | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | —          | —         | —           | —        | —          | 20.3       | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.6 Electrical Characteristics – SN54LVC04A

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                | TEST CONDITIONS                                                                                 | MIN               | TYP | MAX     | UNIT    |
|------------------------------------------|-------------------------------------------------------------------------------------------------|-------------------|-----|---------|---------|
| $V_{OH}$ High-level output voltage       | $I_{OH} = -100\ \mu A$ , $V_{CC} = 2.7\ V$ to $3.6\ V$                                          | $V_{CC} - 0.2$    |     |         | V       |
|                                          | $I_{OH} = -12\ mA$                                                                              | $V_{CC} = 2.7\ V$ | 2.2 |         |         |
|                                          |                                                                                                 | $V_{CC} = 3\ V$   | 2.4 |         |         |
|                                          | $I_{OH} = -24\ mA$ , $V_{CC} = 3\ V$                                                            | 2.2               |     |         |         |
| $V_{OL}$ Low-level output voltage        | $I_{OL} = 100\ \mu A$ , $V_{CC} = 2.7\ V$ to $3.6\ V$                                           |                   |     | 0.2     | V       |
|                                          | $I_{OL} = 12\ mA$ , $V_{CC} = 2.7\ V$                                                           |                   |     | 0.4     |         |
|                                          | $I_{OL} = 24\ mA$ , $V_{CC} = 3\ V$                                                             |                   |     | 0.55    |         |
| $I_I$ Input current                      | $V_I = 5.5\ V$ or GND, $V_{CC} = 3.6\ V$                                                        |                   |     | $\pm 5$ | $\mu A$ |
| $I_{CC}$ Supply current                  | $V_I = V_{CC}$ or GND, $I_O = 0$ , $V_{CC} = 3.6\ V$                                            |                   |     | 10      | $\mu A$ |
| $\Delta I_{CC}$ Change in supply current | One input at $V_{CC} - 0.6\ V$ , Other inputs at $V_{CC}$ or GND, $V_{CC} = 2.7\ V$ to $3.6\ V$ |                   |     | 500     | $\mu A$ |

## 6.7 Electrical Characteristics – SN74LVC04A

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                          | TEST CONDITIONS                                            | MIN                                  | TYP                                  | MAX            | UNIT    |
|------------------------------------|------------------------------------------------------------|--------------------------------------|--------------------------------------|----------------|---------|
| $V_{OH}$ High-level output voltage | $I_{OH} = -100\ \mu A$ ,<br>$V_{CC} = 1.65\ V$ to $3.6\ V$ | $T_A = 25^\circ C$                   |                                      | $V_{CC} - 0.2$ | V       |
|                                    |                                                            | $T_A = -40^\circ C$ to $125^\circ C$ |                                      | $V_{CC} - 0.3$ |         |
|                                    | $I_{OH} = -4\ mA$ , $V_{CC} = 1.65\ V$                     | $T_A = 25^\circ C$                   |                                      | 1.29           |         |
|                                    |                                                            | $T_A = -40^\circ C$ to $85^\circ C$  |                                      | 1.2            |         |
|                                    |                                                            | $T_A = -40^\circ C$ to $125^\circ C$ |                                      | 1.05           |         |
|                                    | $I_{OH} = -8\ mA$ , $V_{CC} = 2.3\ V$                      | $T_A = 25^\circ C$                   |                                      | 1.9            |         |
|                                    |                                                            | $T_A = -40^\circ C$ to $85^\circ C$  |                                      | 1.7            |         |
|                                    |                                                            | $T_A = -40^\circ C$ to $125^\circ C$ |                                      | 1.55           |         |
|                                    | $I_{OH} = -12\ mA$                                         | $V_{CC} = 2.7\ V$                    | $T_A = 25^\circ C$                   | 2.2            |         |
|                                    |                                                            |                                      | $T_A = -40^\circ C$ to $125^\circ C$ | 2.05           |         |
|                                    |                                                            | $V_{CC} = 3\ V$                      | $T_A = 25^\circ C$                   | 2.4            |         |
|                                    |                                                            |                                      | $T_A = -40^\circ C$ to $125^\circ C$ | 2.25           |         |
|                                    | $I_{OH} = -24\ mA$ , $V_{CC} = 3\ V$                       | $T_A = 25^\circ C$                   |                                      | 2.3            |         |
|                                    |                                                            | $T_A = -40^\circ C$ to $85^\circ C$  |                                      | 2.2            |         |
|                                    |                                                            | $T_A = -40^\circ C$ to $125^\circ C$ |                                      | 2              |         |
| $V_{OL}$ Low-level output voltage  | $I_{OL} = 100\ \mu A$ ,<br>$V_{CC} = 1.65\ V$ to $3.6\ V$  | $T_A = 25^\circ C$                   |                                      | 0.1            | V       |
|                                    |                                                            | $T_A = -40^\circ C$ to $85^\circ C$  |                                      | 0.2            |         |
|                                    |                                                            | $T_A = -40^\circ C$ to $125^\circ C$ |                                      | 0.3            |         |
|                                    | $I_{OL} = 4\ mA$ , $V_{CC} = 1.65\ V$                      | $T_A = 25^\circ C$                   |                                      | 0.24           |         |
|                                    |                                                            | $T_A = -40^\circ C$ to $85^\circ C$  |                                      | 0.45           |         |
|                                    |                                                            | $T_A = -40^\circ C$ to $125^\circ C$ |                                      | 0.6            |         |
|                                    | $I_{OL} = 8\ mA$ , $V_{CC} = 2.3\ V$                       | $T_A = 25^\circ C$                   |                                      | 0.3            |         |
|                                    |                                                            | $T_A = -40^\circ C$ to $85^\circ C$  |                                      | 0.7            |         |
|                                    |                                                            | $T_A = -40^\circ C$ to $125^\circ C$ |                                      | 0.85           |         |
|                                    | $I_{OL} = 12\ mA$ , $V_{CC} = 2.7\ V$                      | $T_A = 25^\circ C$                   |                                      | 0.4            |         |
|                                    |                                                            | $T_A = -40^\circ C$ to $125^\circ C$ |                                      | 0.6            |         |
|                                    | $I_{OL} = 24\ mA$ , $V_{CC} = 3\ V$                        | $T_A = 25^\circ C$                   |                                      | 0.55           |         |
|                                    |                                                            | $T_A = -40^\circ C$ to $125^\circ C$ |                                      | 0.8            |         |
| $I_I$ Input current                | $V_I = 5.5\ V$ or GND, $V_{CC} = 3.6\ V$                   | $T_A = 25^\circ C$                   |                                      | $\pm 1$        | $\mu A$ |
|                                    |                                                            | $T_A = -40^\circ C$ to $85^\circ C$  |                                      | $\pm 5$        |         |
|                                    |                                                            | $T_A = -40^\circ C$ to $125^\circ C$ |                                      | $\pm 20$       |         |

**SN54LVC04A, SN74LVC04A**

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**Electrical Characteristics – SN74LVC04A (continued)**

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                                | TEST CONDITIONS                                                                                   | MIN                                              | TYP | MAX  | UNIT          |
|------------------------------------------|---------------------------------------------------------------------------------------------------|--------------------------------------------------|-----|------|---------------|
| $I_{CC}$ Supply current                  | $V_I = V_{CC}$ or GND, $I_O = 0$ ,<br>$V_{CC} = 3.6$ V                                            | $T_A = 25^\circ\text{C}$                         |     | 1    | $\mu\text{A}$ |
|                                          |                                                                                                   | $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$  |     | 10   |               |
|                                          |                                                                                                   | $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ |     | 40   |               |
| $\Delta I_{CC}$ Change in supply current | One input at $V_{CC} - 0.6$ V,<br>other inputs at $V_{CC}$ or GND,<br>$V_{CC} = 2.7$ V to $3.6$ V | $T_A = 25^\circ\text{C}$                         |     | 500  | $\mu\text{A}$ |
|                                          |                                                                                                   | $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ |     | 5000 |               |
| $C_i$ Input capacitance                  | $V_I = V_{CC}$ or GND, $V_{CC} = 3.3$ V                                                           |                                                  |     | 5    | pF            |

**6.8 Switching Characteristics**

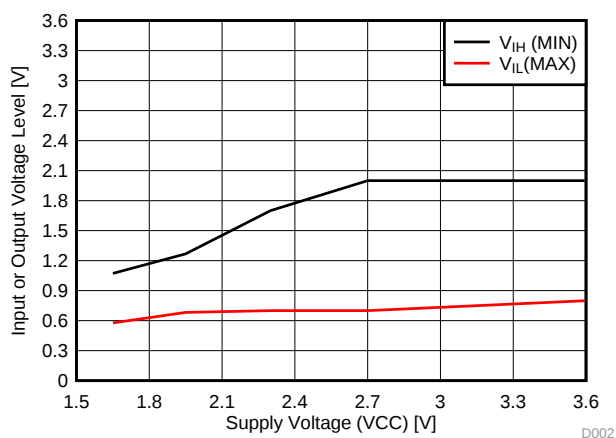
over recommended operating free-air temperature range (unless otherwise noted; see [Figure 2](#))

| PARAMETER                                   |                          | TEST CONDITIONS                                 |                                                  |                                             | MIN | TYP | MAX | UNIT |
|---------------------------------------------|--------------------------|-------------------------------------------------|--------------------------------------------------|---------------------------------------------|-----|-----|-----|------|
| t <sub>pd</sub>                             | Propagation (delay) time | From A (input) to Y (output)                    | V <sub>CC</sub> = 1.8 V ±0.15 V, SN74LVC04A only | T <sub>A</sub> = 25°C                       | 1   | 4.1 | 7.5 | ns   |
|                                             |                          |                                                 |                                                  | T <sub>A</sub> = −40°C to 85°C              | 1   |     | 8   |      |
|                                             |                          |                                                 |                                                  | T <sub>A</sub> = −40°C to 125°C             | 1   |     | 9.5 |      |
|                                             |                          |                                                 | V <sub>CC</sub> = 2.5 V ±0.2 V, SN74LVC04A only  | T <sub>A</sub> = 25°C                       | 1   | 3.6 | 7   |      |
|                                             |                          |                                                 |                                                  | T <sub>A</sub> = −40°C to 85°C              | 1   |     | 7.5 |      |
|                                             |                          |                                                 |                                                  | T <sub>A</sub> = −40°C to 125°C             | 1   |     | 9   |      |
|                                             |                          |                                                 | V <sub>CC</sub> = 2.7 V                          | T <sub>A</sub> = −55°C to 125°C, SN54LVC04A |     |     | 5.5 |      |
|                                             |                          |                                                 |                                                  | T <sub>A</sub> = 25°C, SN74LVC04A           | 1   | 3   | 5.3 |      |
|                                             |                          |                                                 |                                                  | T <sub>A</sub> = −40°C to 85°C, SN74LVC04A  | 1   |     | 5.5 |      |
|                                             |                          |                                                 |                                                  | T <sub>A</sub> = −40°C to 125°C, SN74LVC04A | 1   |     | 7   |      |
|                                             |                          |                                                 | V <sub>CC</sub> = 3.3 V ±0.3 V                   | T <sub>A</sub> = −55°C to 125°C, SN54LVC04A | 0.5 |     | 4.5 |      |
|                                             |                          |                                                 |                                                  | T <sub>A</sub> = 25°C, SN74LVC04A           | 1   | 2.5 | 4.3 |      |
| T <sub>A</sub> = −40°C to 85°C, SN74LVC04A  | 1                        |                                                 |                                                  | 4.5                                         |     |     |     |      |
| T <sub>A</sub> = −40°C to 125°C, SN74LVC04A | 1                        |                                                 |                                                  | 6                                           |     |     |     |      |
| t <sub>sk(o)</sub>                          | Skew (time), output      | V <sub>CC</sub> = 3.3 V ±0.3 V, SN74LVC04A only | T <sub>A</sub> = −40°C to 85°C                   |                                             |     | 1   | ns  |      |
|                                             |                          |                                                 | T <sub>A</sub> = −40°C to 125°C                  |                                             |     | 1.5 |     |      |

**6.9 Operating Characteristics**
 $T_A = 25^\circ\text{C}$  (unless otherwise noted)

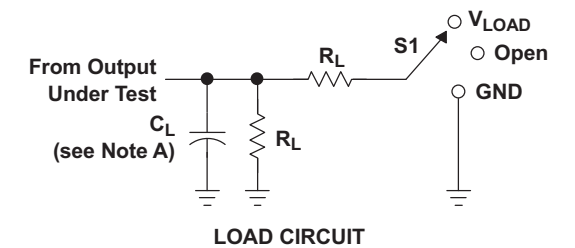
| PARAMETER                                       | TEST CONDITIONS                        | MIN              | TYP | MAX | UNIT |
|-------------------------------------------------|----------------------------------------|------------------|-----|-----|------|
| $C_{pd}$ Power dissipation capacitance per gate | $f = 10$ MHz, $T_A = 25^\circ\text{C}$ | $V_{CC} = 1.8$ V |     | 6   | pF   |
|                                                 |                                        | $V_{CC} = 2.5$ V |     | 7   |      |
|                                                 |                                        | $V_{CC} = 3.3$ V |     | 8   |      |

## 6.10 Typical Characteristics



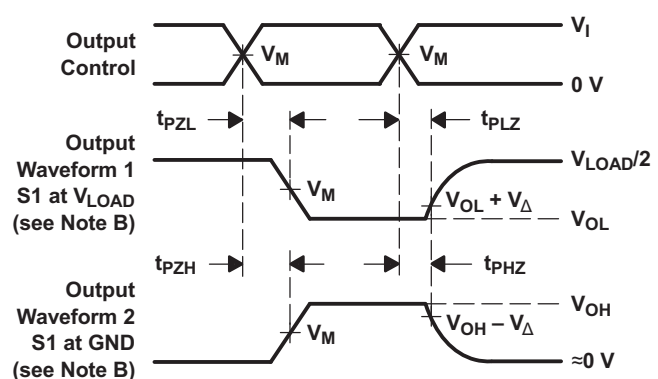
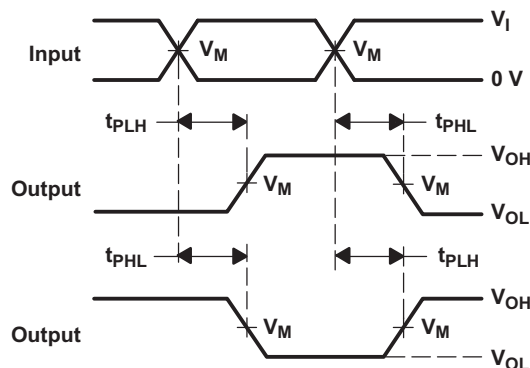
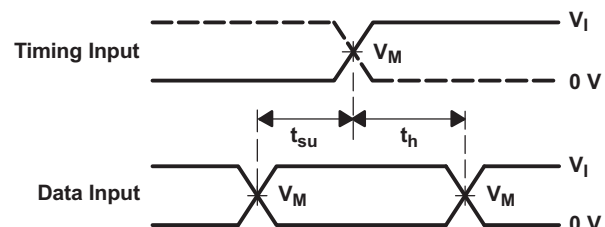
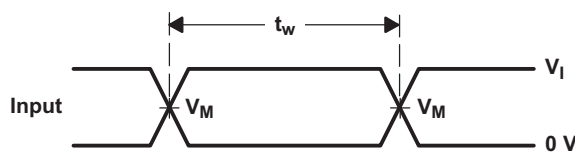
**Figure 1.  $V_{IH}$  Minimum and  $V_{IL}$  Maximum vs Supply Voltage**

## 7 Parameter Measurement Information



| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_r/t_f$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| 2.7 V                            | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |



- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
- The outputs are measured one at a time, with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- All parameters and waveforms are not applicable to all devices.

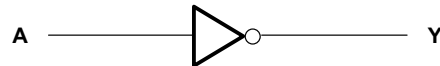
**Figure 2. Load Circuit and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

These hex inverters are designed for 1.65-V to 3.6-V  $V_{CC}$  operation. The SN74LVC04A devices contain six independent inverters. These devices perform the Boolean function  $Y = \overline{A}$ . These devices are fully specified for partial-power-down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The inputs are high impedance when  $V_{CC} = 0V$ .

### 8.2 Functional Block Diagram



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### 8.3 Feature Description

Wide operating voltage range from 1.65 V to 3.6 V. Allows down-voltage translation with inputs accept voltages to 3.6 V.  $I_{OFF}$  feature supports live insertion, partial power down mode, and back drive protection.

### 8.4 Device Functional Modes

[Table 1](#) lists the functional modes of the SNx4LVC04A.

**Table 1. Function Table  
(Each Inverter)**

| INPUT<br>A | OUTPUT<br>Y |
|------------|-------------|
| H          | L           |
| L          | H           |

## 9 Application and Implementation

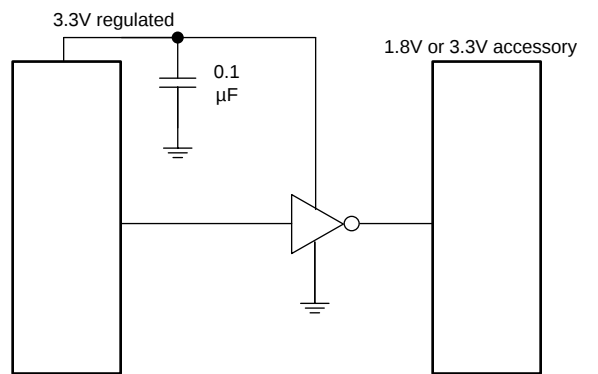
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

SN74LVC04A is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 3.6 V at any valid  $V_{CC}$  making it ideal for down translation.

### 9.2 Typical Application



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**Figure 3. Typical Application Schematic**

#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention, because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

Recommended Input Conditions:

- For rise time and fall time specifications, see  $\Delta t/\Delta V$  in [Recommended Operating Conditions](#).
- For specified high and low levels, see  $V_{IH}$  and  $V_{IL}$  in [Recommended Operating Conditions](#).
- Inputs are overvoltage tolerant allowing them to go as high as 3.6 V at any valid  $V_{CC}$ .

Recommend Output Conditions:

- Load currents must not exceed 25 mA per output and 50 mA total for the part.
- Outputs must not be pulled above  $V_{CC}$ .

## Typical Application (continued)

### 9.2.3 Application Curves

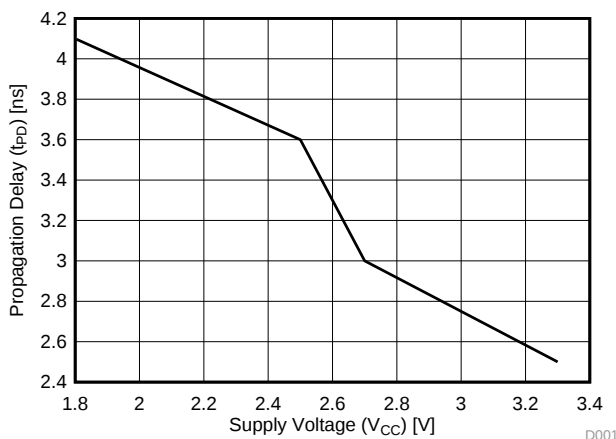


Figure 4. Typical Application Curve

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#).

Each  $V_{CC}$  pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu$ F is recommended. If there are multiple  $V_{CC}$  pins, 0.01  $\mu$ F or 0.022  $\mu$ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu$ F and 1  $\mu$ F are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices, inputs must not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 5](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it disables the outputs section of the part when asserted. This does not disable the input section of the I/Os so they also cannot float when disabled.

### 11.2 Layout Example

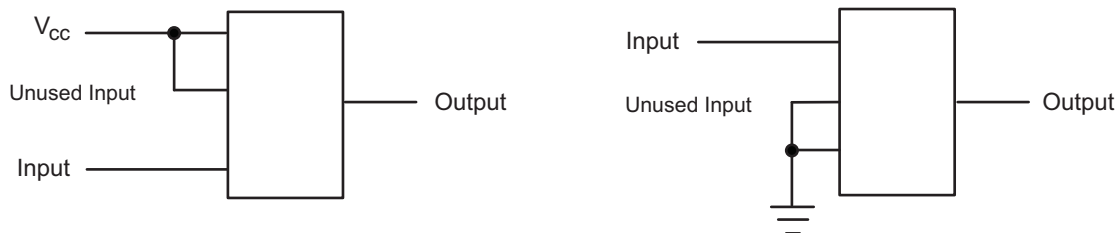


Figure 5. Layout Diagram

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#) (SCBA004)

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

| PARTS      | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54LVC04A | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| SN74LVC04A | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.5 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins   | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)                      |
|---------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|------------------------------------------|
| <a href="#">5962-9760501Q2A</a> | Active        | Production           | LCCC (FK)   20   | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-<br>9760501Q2A<br>SNJ54LVC<br>04AFK |
| <a href="#">5962-9760501QCA</a> | Active        | Production           | CDIP (J)   14    | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9760501QC<br>A<br>SNJ54LVC04AJ      |
| <a href="#">5962-9760501QDA</a> | Active        | Production           | CFP (W)   14     | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9760501QD<br>A<br>SNJ54LVC04AW      |
| <a href="#">SN74LVC04AD</a>     | Active        | Production           | SOIC (D)   14    | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC04A                                   |
| SN74LVC04AD.B                   | Active        | Production           | SOIC (D)   14    | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC04A                                   |
| <a href="#">SN74LVC04ADBR</a>   | Active        | Production           | SSOP (DB)   14   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC04A                                    |
| SN74LVC04ADBR.B                 | Active        | Production           | SSOP (DB)   14   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC04A                                    |
| SN74LVC04ADBRG4                 | Active        | Production           | SSOP (DB)   14   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC04A                                    |
| <a href="#">SN74LVC04ADGVR</a>  | Active        | Production           | TVSOP (DGV)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC04A                                    |
| SN74LVC04ADGVR.B                | Active        | Production           | TVSOP (DGV)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC04A                                    |
| SN74LVC04ADGVRE4                | Active        | Production           | TVSOP (DGV)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC04A                                    |
| <a href="#">SN74LVC04ADR</a>    | Active        | Production           | SOIC (D)   14    | 2500   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 125   | LVC04A                                   |
| SN74LVC04ADR.B                  | Active        | Production           | SOIC (D)   14    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC04A                                   |
| <a href="#">SN74LVC04ADRG3</a>  | Active        | Production           | SOIC (D)   14    | 2500   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | LVC04A                                   |
| SN74LVC04ADRG3.B                | Active        | Production           | SOIC (D)   14    | 2500   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | LVC04A                                   |
| <a href="#">SN74LVC04ADRG4</a>  | Active        | Production           | SOIC (D)   14    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC04A                                   |
| SN74LVC04ADRG4.B                | Active        | Production           | SOIC (D)   14    | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC04A                                   |
| <a href="#">SN74LVC04ADT</a>    | Active        | Production           | SOIC (D)   14    | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC04A                                   |
| SN74LVC04ADT.B                  | Active        | Production           | SOIC (D)   14    | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC04A                                   |
| SN74LVC04ANS.B                  | Active        | Production           | SOP (NS)   14    | 50   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC04A                                   |
| <a href="#">SN74LVC04ANSR</a>   | Active        | Production           | SOP (NS)   14    | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC04A                                   |
| SN74LVC04ANSR.B                 | Active        | Production           | SOP (NS)   14    | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC04A                                   |
| SN74LVC04ANSR1G4                | Active        | Production           | SOP (NS)   14    | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC04A                                   |
| SN74LVC04ANSR1G4.B              | Active        | Production           | SOP (NS)   14    | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LVC04A                                   |

| Orderable part number           | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6)              |
|---------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|----------------------------------|
| <a href="#">SN74LVC04APW</a>    | Active        | Production           | TSSOP (PW)   14 | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC04A                            |
| SN74LVC04APW.B                  | Active        | Production           | TSSOP (PW)   14 | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC04A                            |
| SN74LVC04APWE4                  | Active        | Production           | TSSOP (PW)   14 | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC04A                            |
| SN74LVC04APWG4                  | Active        | Production           | TSSOP (PW)   14 | 90   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC04A                            |
| <a href="#">SN74LVC04APWR</a>   | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -40 to 125   | LC04A                            |
| SN74LVC04APWR.B                 | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC04A                            |
| SN74LVC04APWRE4                 | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC04A                            |
| <a href="#">SN74LVC04APWRG3</a> | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | LC04A                            |
| SN74LVC04APWRG3.B               | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | SN                                   | Level-1-260C-UNLIM                | -40 to 125   | LC04A                            |
| <a href="#">SN74LVC04APWRG4</a> | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC04A                            |
| SN74LVC04APWRG4.B               | Active        | Production           | TSSOP (PW)   14 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC04A                            |
| <a href="#">SN74LVC04APWT</a>   | Active        | Production           | TSSOP (PW)   14 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC04A                            |
| SN74LVC04APWT.B                 | Active        | Production           | TSSOP (PW)   14 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC04A                            |
| SN74LVC04APWTG4                 | Active        | Production           | TSSOP (PW)   14 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 125   | LC04A                            |
| <a href="#">SN74LVC04ARGYR</a>  | Active        | Production           | VQFN (RGY)   14 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | LC04A                            |
| SN74LVC04ARGYR.B                | Active        | Production           | VQFN (RGY)   14 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | LC04A                            |
| SN74LVC04ARGYRG4                | Active        | Production           | VQFN (RGY)   14 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | LC04A                            |
| <a href="#">SNJ54LVC04AFK</a>   | Active        | Production           | LCCC (FK)   20  | 55   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9760501Q2A<br>SNJ54LVC04AFK |
| <a href="#">SNJ54LVC04AJ</a>    | Active        | Production           | CDIP (J)   14   | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9760501QCA<br>SNJ54LVC04AJ  |
| <a href="#">SNJ54LVC04AW</a>    | Active        | Production           | CFP (W)   14    | 25   TUBE             | No          | SNPB                                 | N/A for Pkg Type                  | -55 to 125   | 5962-9760501QDA<br>SNJ54LVC04AW  |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LVC04A, SN74LVC04A :**

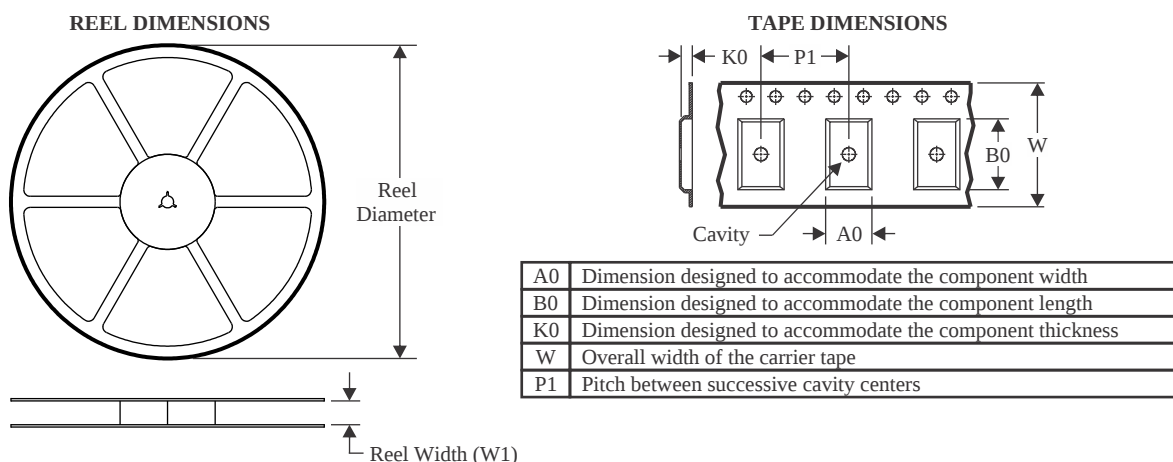
- Catalog : [SN74LVC04A](#)
- Automotive : [SN74LVC04A-Q1](#), [SN74LVC04A-Q1](#)
- Enhanced Product : [SN74LVC04A-EP](#), [SN74LVC04A-EP](#)
- Military : [SN54LVC04A](#)

**NOTE: Qualified Version Definitions:**

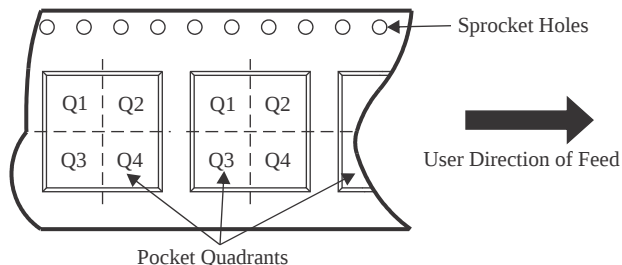
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



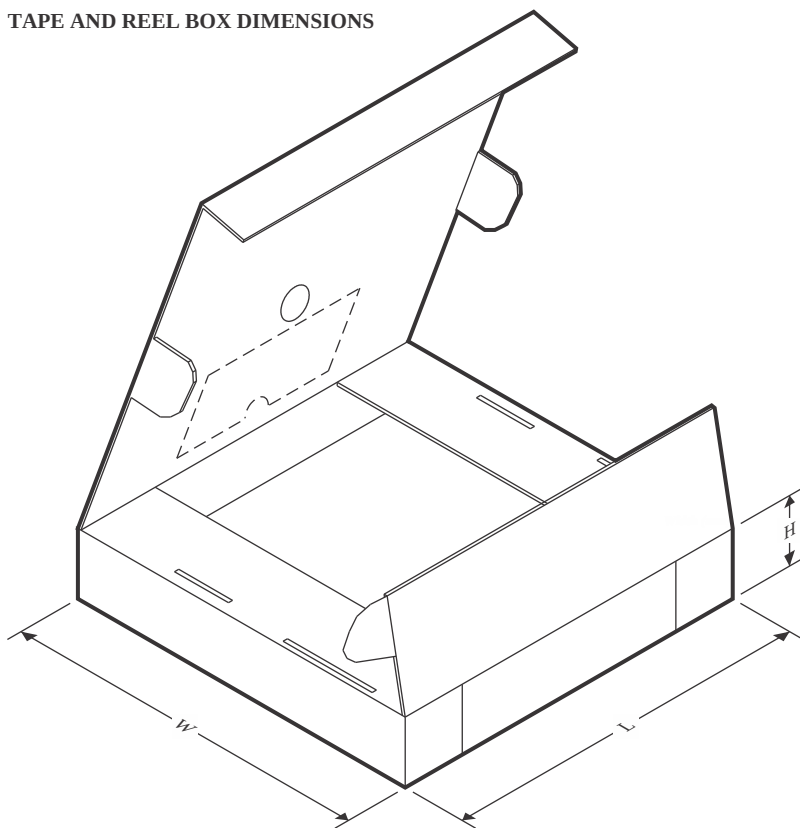
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC04ADBR    | SSOP         | DB              | 14   | 2000 | 330.0              | 16.4               | 8.35    | 6.6     | 2.4     | 12.0    | 16.0   | Q1            |
| SN74LVC04ADGVR   | TVSOP        | DGV             | 14   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC04ADR     | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC04ADRG3   | SOIC         | D               | 14   | 2500 | 330.0              | 16.8               | 6.5     | 9.5     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC04ADRG4   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC04ADRG4   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC04ADT     | SOIC         | D               | 14   | 250  | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74LVC04ANSR    | SOP          | NS              | 14   | 2000 | 330.0              | 16.4               | 8.1     | 10.4    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LVC04ANSR1G4 | SOP          | NS              | 14   | 2000 | 330.0              | 16.4               | 8.1     | 10.4    | 2.5     | 12.0    | 16.0   | Q1            |
| SN74LVC04APWR    | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC04APWRG3  | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC04APWRG4  | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC04APWT    | TSSOP        | PW              | 14   | 250  | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74LVC04ARGYR   | VQFN         | RGY             | 14   | 3000 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |

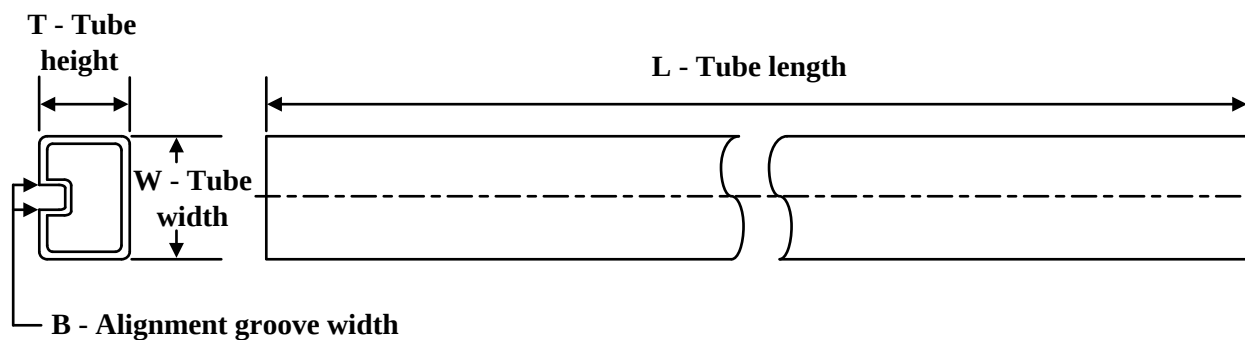
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC04ADBR    | SSOP         | DB              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LVC04ADGVR   | TVSOP        | DGV             | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LVC04ADR     | SOIC         | D               | 14   | 2500 | 353.0       | 353.0      | 32.0        |
| SN74LVC04ADRG3   | SOIC         | D               | 14   | 2500 | 364.0       | 364.0      | 27.0        |
| SN74LVC04ADRG4   | SOIC         | D               | 14   | 2500 | 353.0       | 353.0      | 32.0        |
| SN74LVC04ADRG4   | SOIC         | D               | 14   | 2500 | 340.5       | 336.1      | 32.0        |
| SN74LVC04ADT     | SOIC         | D               | 14   | 250  | 213.0       | 191.0      | 35.0        |
| SN74LVC04ANSR    | SOP          | NS              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LVC04ANSR1G4 | SOP          | NS              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LVC04APWR    | TSSOP        | PW              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LVC04APWRG3  | TSSOP        | PW              | 14   | 2000 | 364.0       | 364.0      | 27.0        |
| SN74LVC04APWRG4  | TSSOP        | PW              | 14   | 2000 | 353.0       | 353.0      | 32.0        |
| SN74LVC04APWT    | TSSOP        | PW              | 14   | 250  | 353.0       | 353.0      | 32.0        |
| SN74LVC04ARGYR   | VQFN         | RGY             | 14   | 3000 | 353.0       | 353.0      | 32.0        |

## TUBE

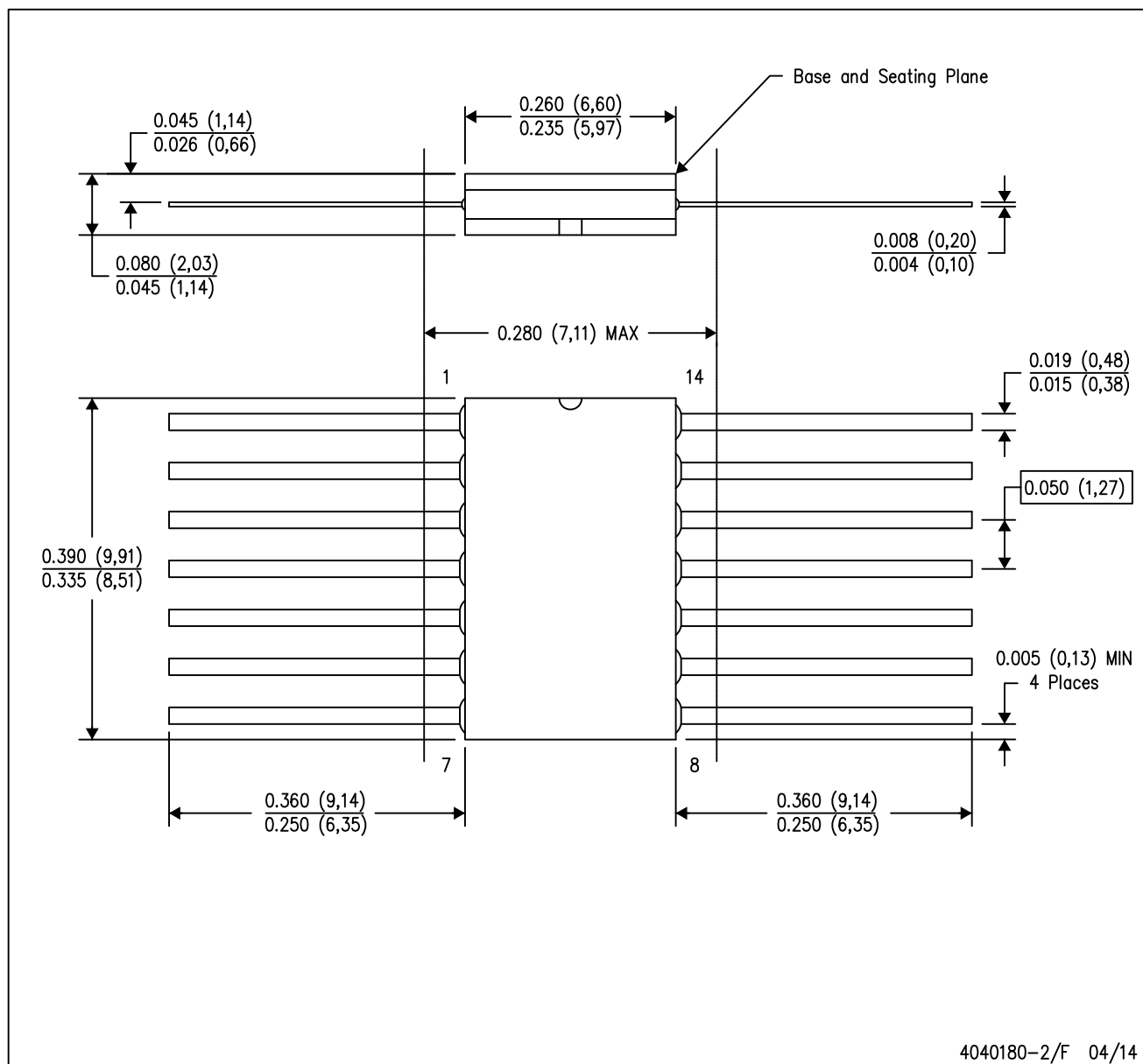


\*All dimensions are nominal

| Device          | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9760501Q2A | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| 5962-9760501QDA | W            | CFP          | 14   | 25  | 506.98 | 26.16  | 6220   | NA     |
| SN74LVC04AD     | D            | SOIC         | 14   | 50  | 507    | 8      | 3940   | 4.32   |
| SN74LVC04AD     | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| SN74LVC04AD.B   | D            | SOIC         | 14   | 50  | 507    | 8      | 3940   | 4.32   |
| SN74LVC04AD.B   | D            | SOIC         | 14   | 50  | 506.6  | 8      | 3940   | 4.32   |
| SN74LVC04ANS.B  | NS           | SOP          | 14   | 50  | 530    | 10.5   | 4000   | 4.1    |
| SN74LVC04APW    | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |
| SN74LVC04APW.B  | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |
| SN74LVC04APWE4  | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |
| SN74LVC04APWG4  | PW           | TSSOP        | 14   | 90  | 530    | 10.2   | 3600   | 3.5    |
| SNJ54LVC04AFK   | FK           | LCCC         | 20   | 55  | 506.98 | 12.06  | 2030   | NA     |
| SNJ54LVC04AW    | W            | CFP          | 14   | 25  | 506.98 | 26.16  | 6220   | NA     |

W (R-GDFP-F14)

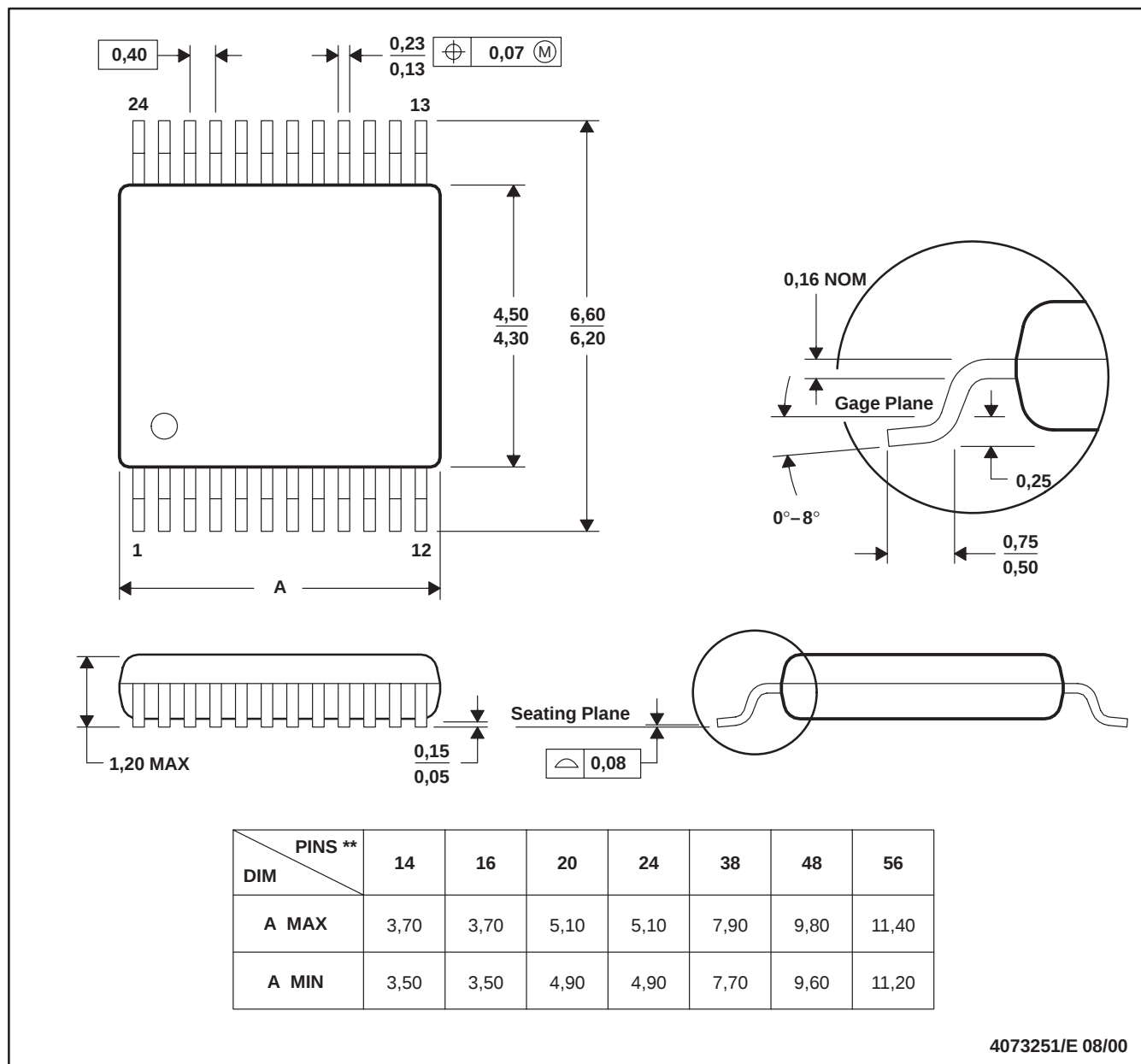
CERAMIC DUAL FLATPACK



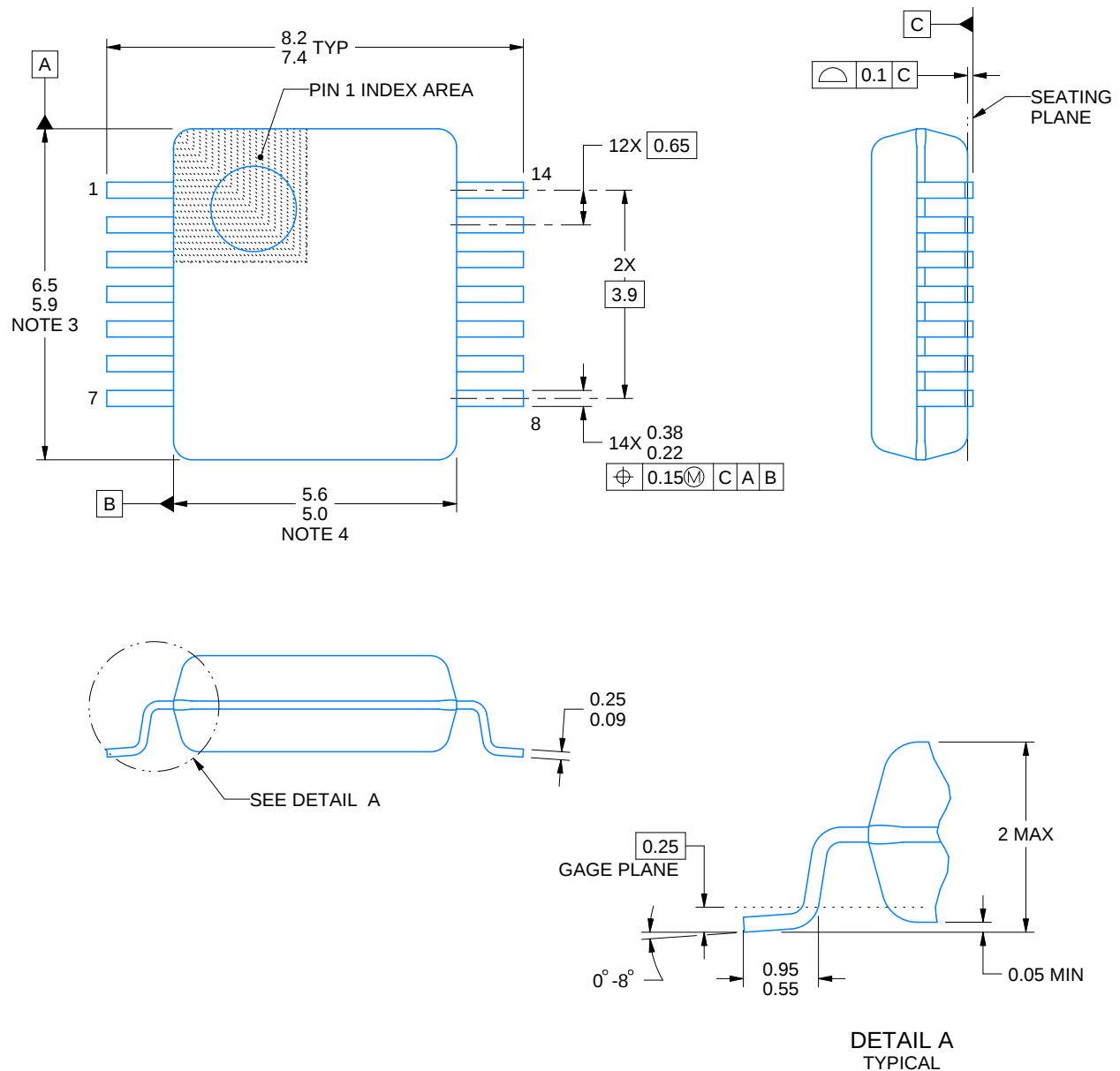
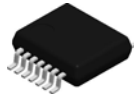
## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



4220762/A 05/2024

## NOTES:

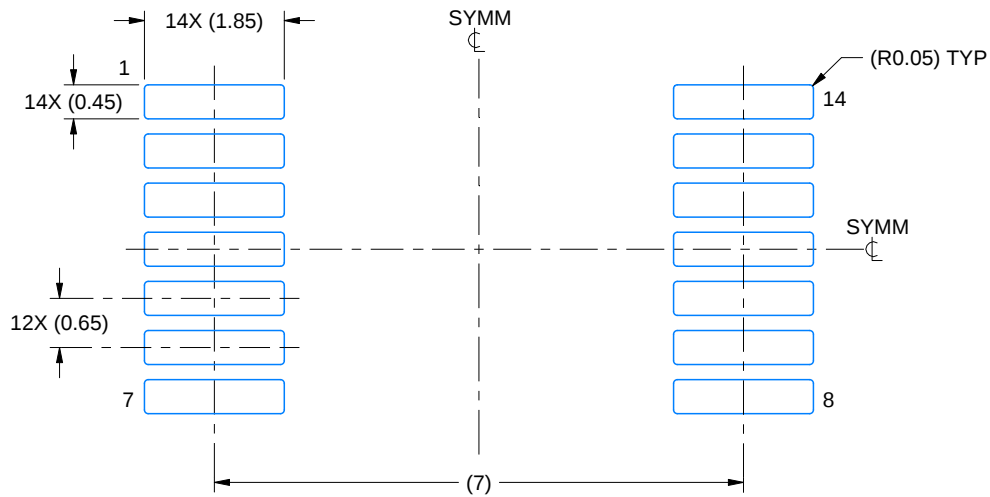
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

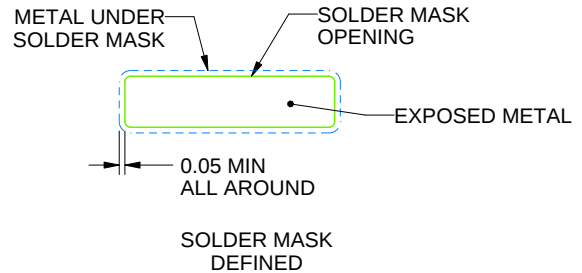
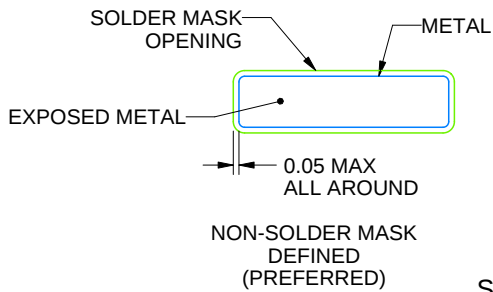
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

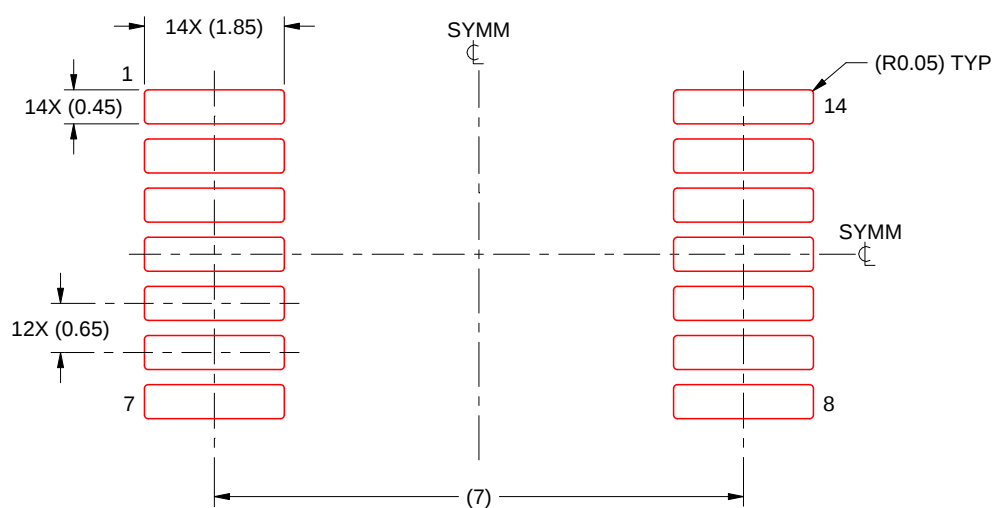
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

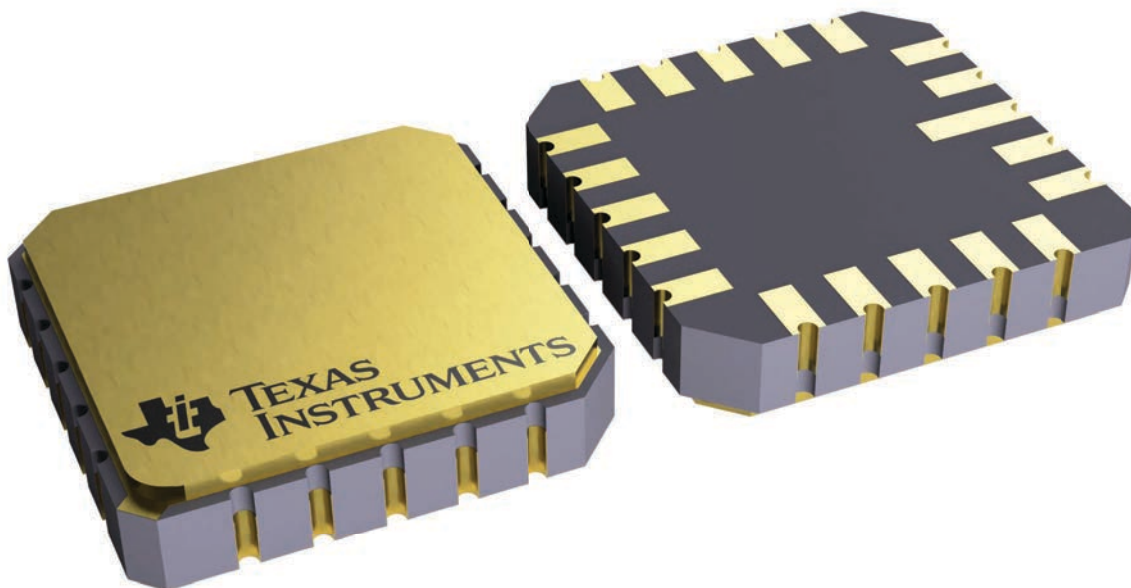
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



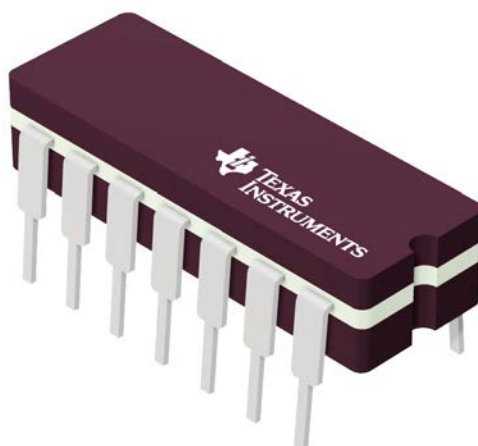
4229370VA\

**J 14**

## GENERIC PACKAGE VIEW

**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

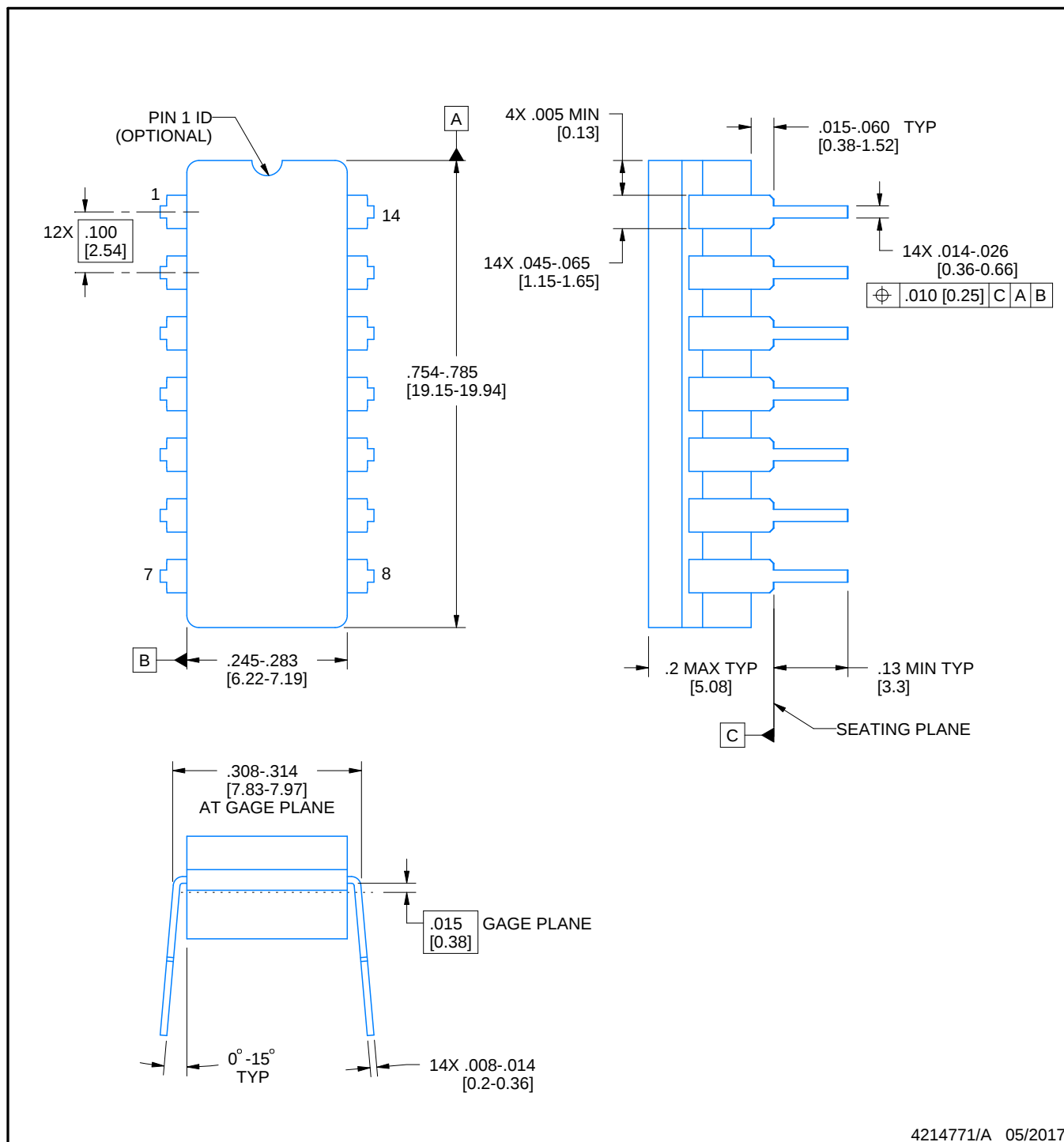


**J0014A**

## PACKAGE OUTLINE

**CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE

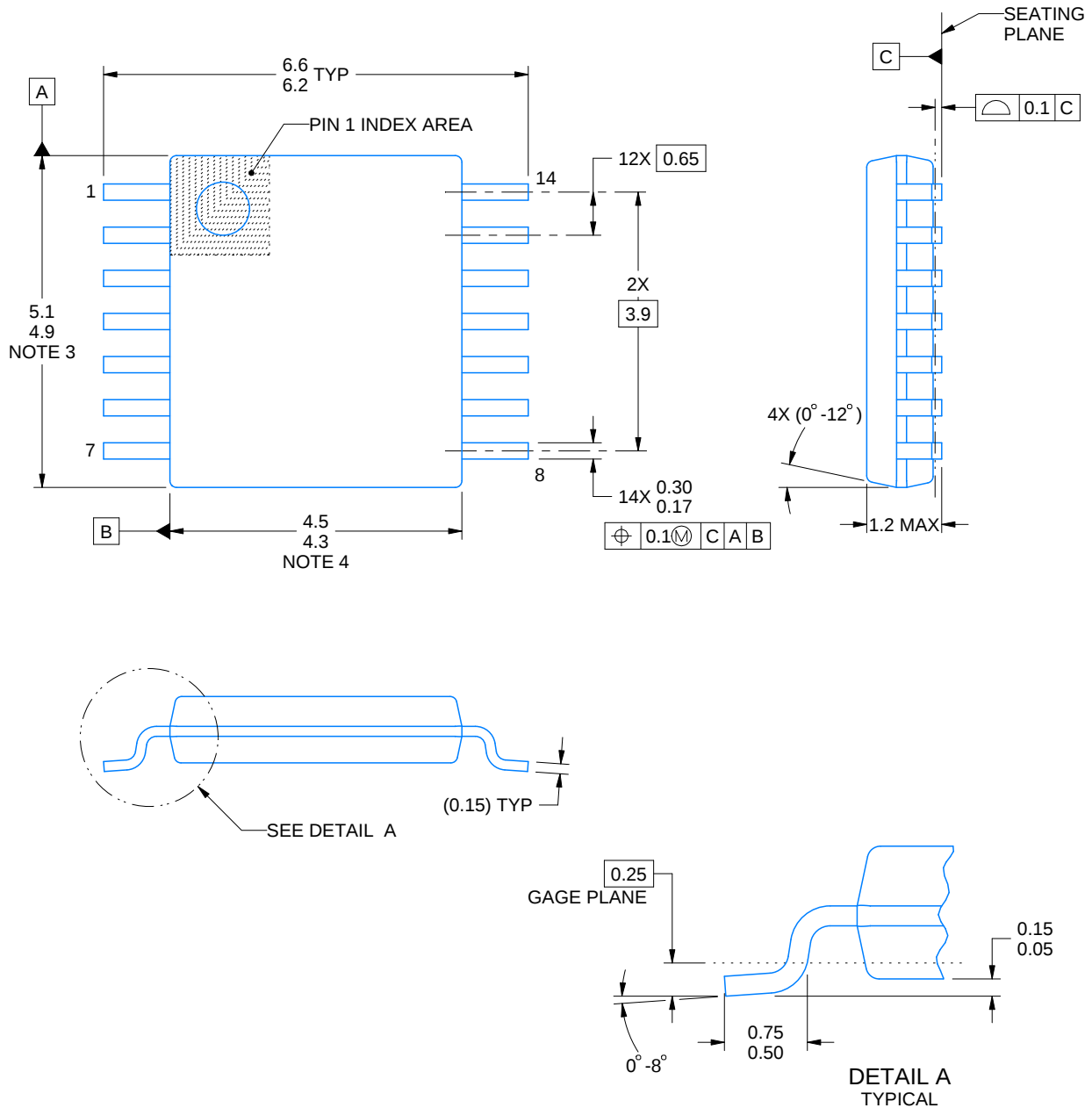
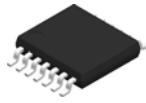


4214771/A 05/2017

### NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.





4220202/B 12/2023

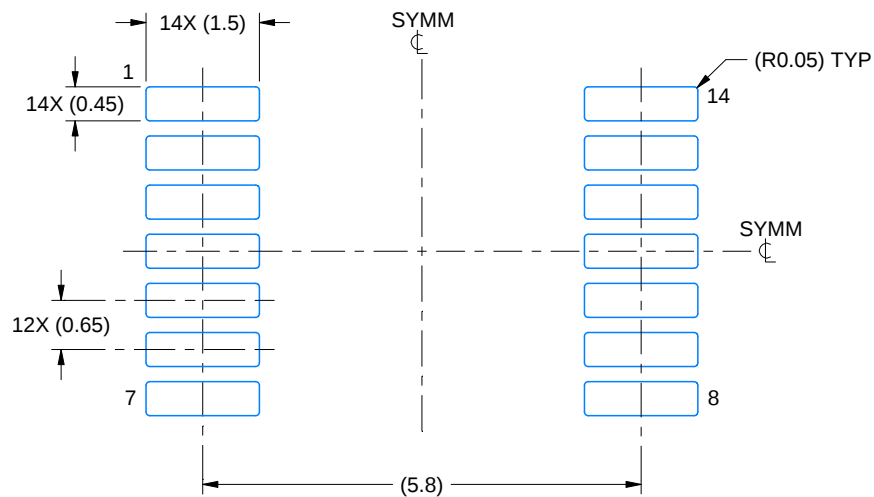
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

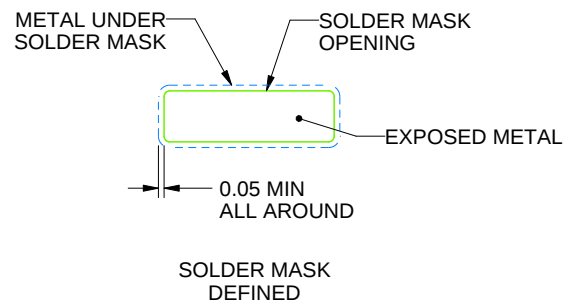
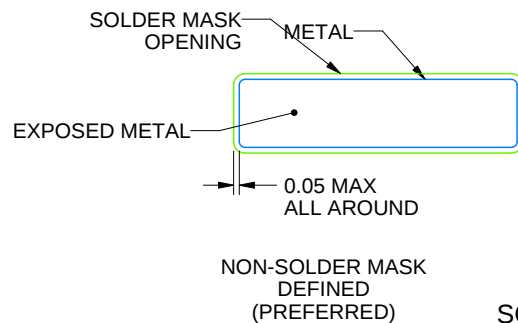
**PW0014A**

**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



## SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

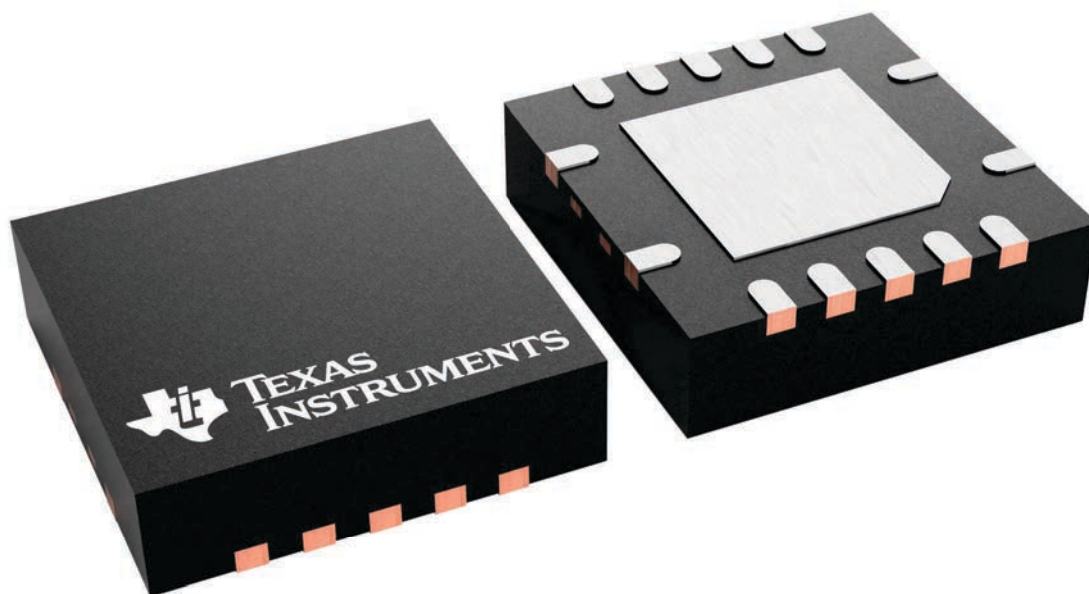
**RGY 14**

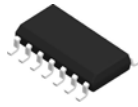
**VQFN - 1 mm max height**

3.5 x 3.5, 0.5 mm pitch

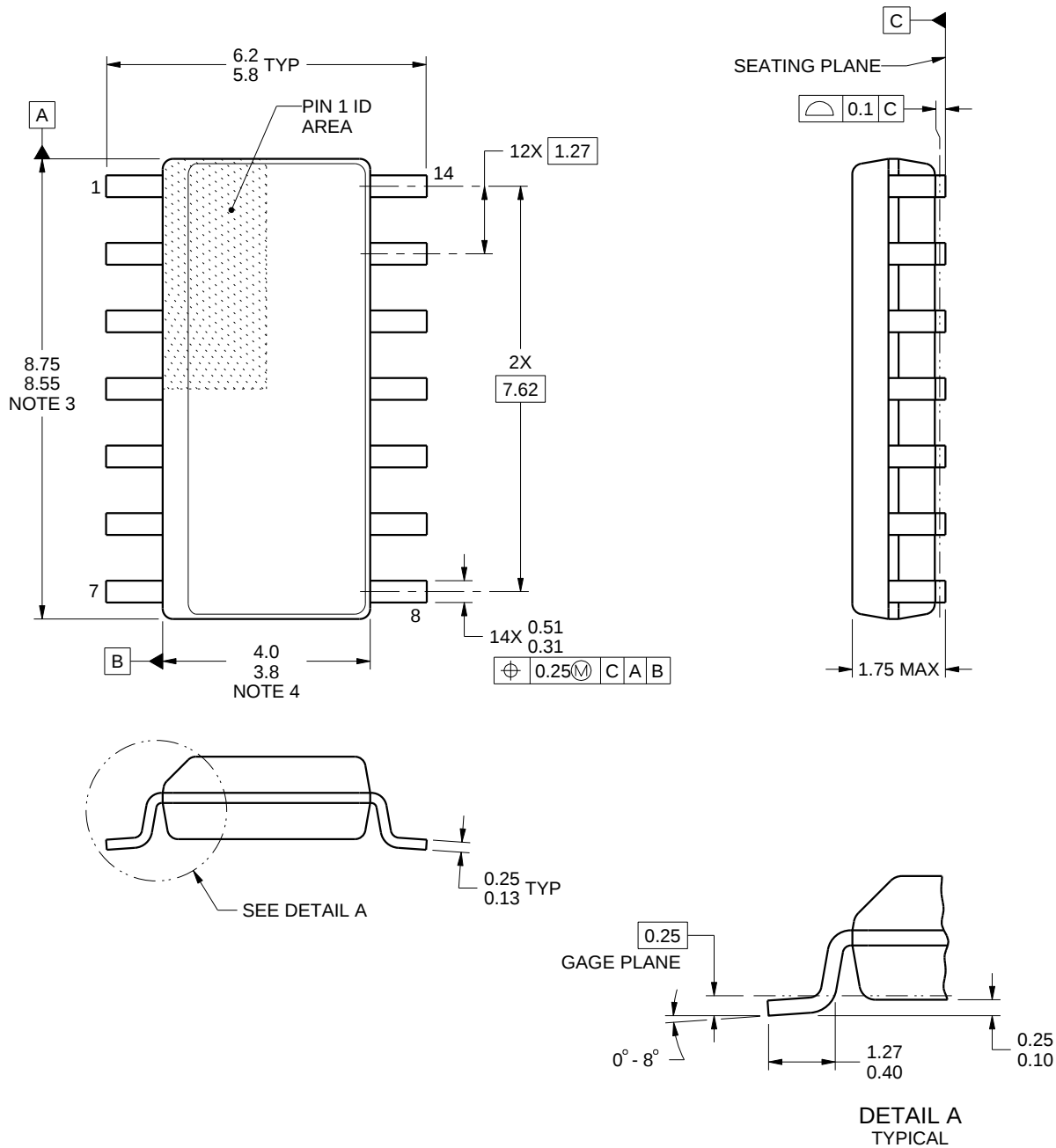
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



**D0014A****PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

**NOTES:**

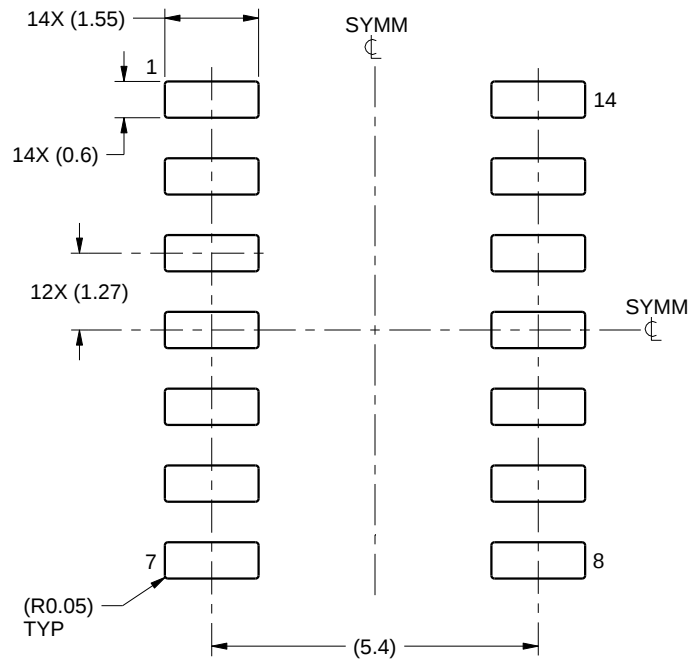
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

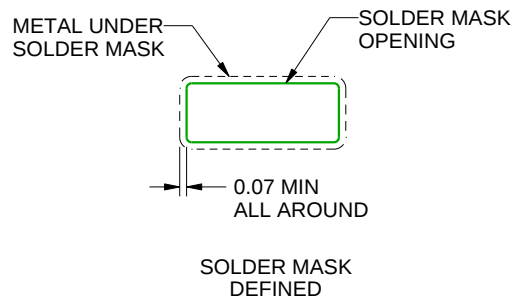
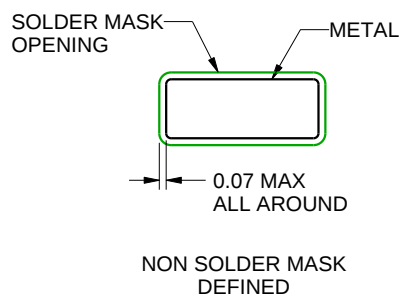
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

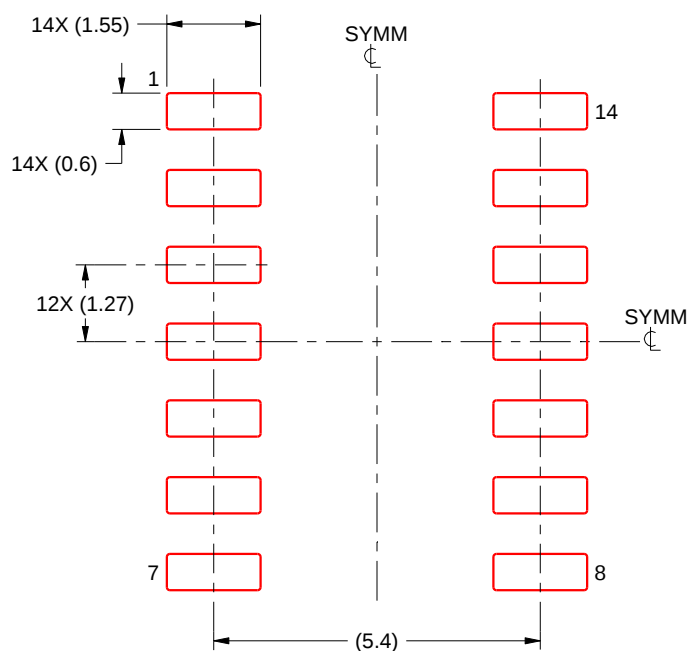
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

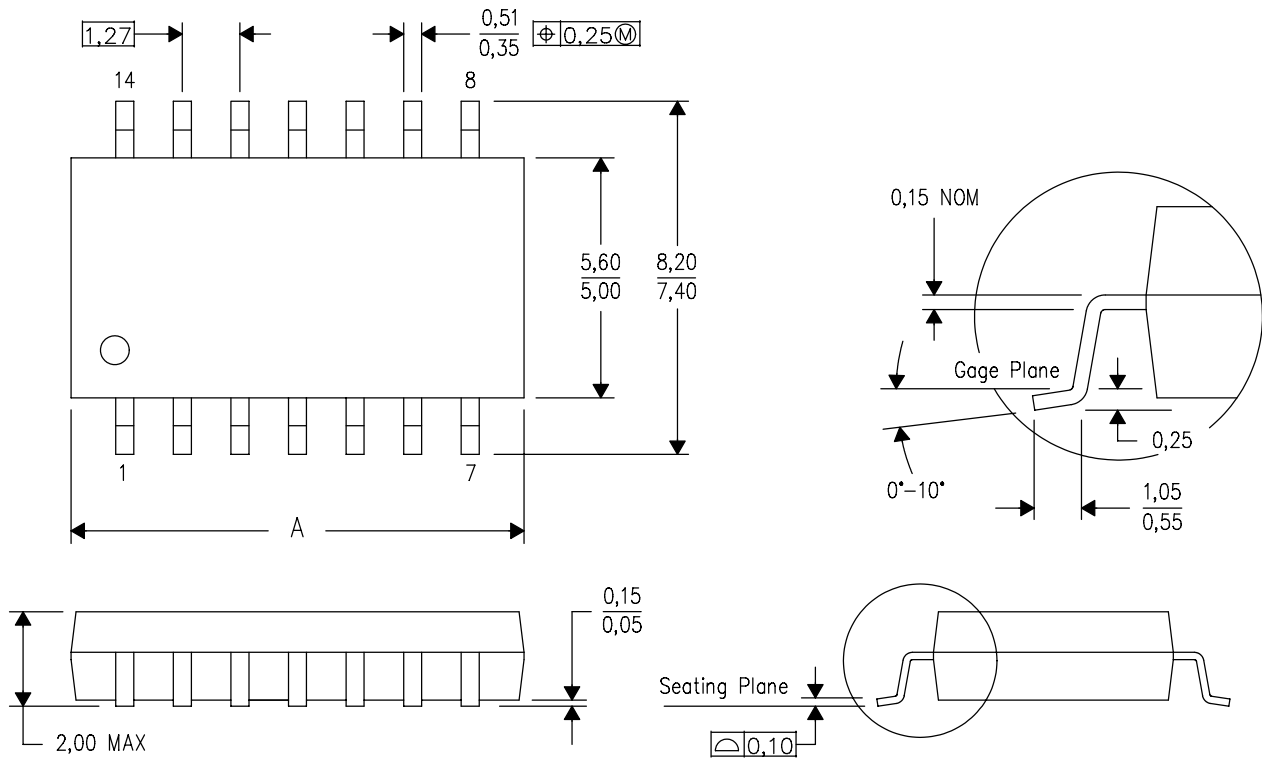
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



| DIM \ PINS ** | 14    | 16    | 20    | 24    |
|---------------|-------|-------|-------|-------|
| A MAX         | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN         | 9,90  | 9,90  | 12,30 | 14,70 |

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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Last updated 10/2025