

SN74LVC11A-Q1 Automotive Triple 3-Input AND Gates

1 Features

- AEC-Q100 qualified for automotive applications:
 - Device temperature grade 1: -40°C to +125°C
 - Device HBM ESD classification level 2
 - Device CDM ESD classification level C4B
- Available in [wettable flanks](#) QFN (WBQA) package
- Operating range from 1.1V to 3.6V
- 5.5V tolerant input pins
- Supports standard pinouts
- Latch-up performance exceeds 250mA per JESD 17
- ESD protection exceeds JESD 22
 - 2000V Human-Body Model (A114-A)
 - 1000V Charged-Device Model (C101)

2 Applications

- [Combining power good signals](#)
- [Enable digital signals](#)

3 Description

This device contains three independent 3-input AND gates. Each gate performs the Boolean function $Y = A \times B \times C$ in positive logic.

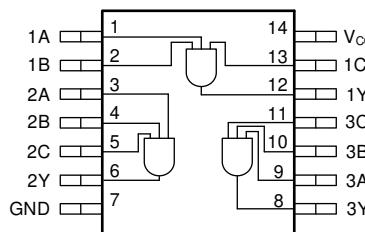
Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SN74LVC11A-Q1	D (SOIC, 14)	8.65mm x 6mm	8.65mm x 3.9mm
	BQA (WQFN, 14)	3mm x 2.5mm	3mm x 2.5mm
	PW (TSSOP,14)	5mm x 6.4mm	5mm x 4.4mm

(1) For more information, see [Section 11](#).

(2) The package size (length x width) is a nominal value and includes pins, where applicable.

(3) The body size (length x width) is a nominal value and does not include pins.



Functional Pinout



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

Table of Contents

1 Features	1	7.3 Feature Description.....	10
2 Applications	1	7.4 Device Functional Modes.....	11
3 Description	1	8 Application and Implementation	12
4 Pin Configuration and Functions	3	8.1 Application Information.....	12
5 Specifications	4	8.2 Typical Application.....	12
5.1 Absolute Maximum Ratings.....	4	8.3 Power Supply Recommendations.....	14
5.2 ESD Ratings.....	4	8.4 Layout.....	14
5.3 Recommended Operating Conditions.....	4	9 Device and Documentation Support	15
5.4 Thermal Information.....	5	9.1 Documentation Support.....	15
5.5 Electrical Characteristics.....	5	9.2 Receiving Notification of Documentation Updates.....	15
5.6 Switching Characteristics.....	6	9.3 Support Resources.....	15
5.7 Noise Characteristics.....	6	9.4 Trademarks.....	15
5.8 Typical Characteristics.....	6	9.5 Electrostatic Discharge Caution.....	15
5.9 Electrical Characteristics.....	6	9.6 Glossary.....	15
6 Parameter Measurement Information	9	10 Revision History	15
7 Detailed Description	10	11 Mechanical, Packaging, and Orderable Information	16
7.1 Overview.....	10		
7.2 Functional Block Diagram.....	10		

4 Pin Configuration and Functions

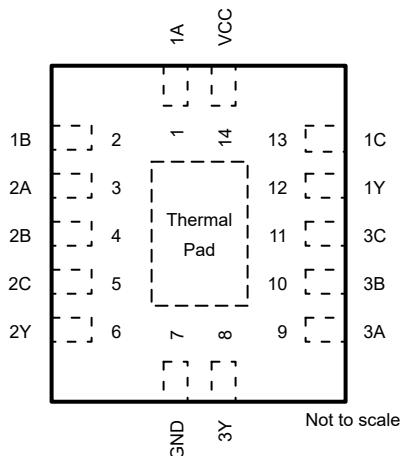


Figure 4-1. SN74LVC11A-Q1 BQA Package, 14-Pin WQFN (Top View)

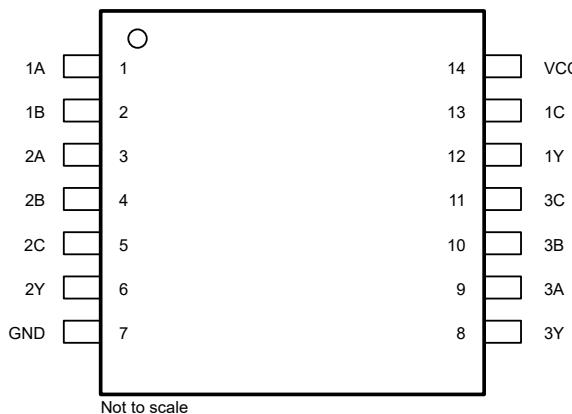


Figure 4-2. SN74LVC11A-Q1 D or PW Packages, 14-Pin SOIC or TSSOP (Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1A	1	I	Channel 1, Input A
1B	2	I	Channel 1, Input B
2A	3	I	Channel 2, Input A
2B	4	I	Channel 2, Input B
2C	5	I	Channel 2, Input C
2Y	6	O	Channel 2, Output Y
GND	7	—	Ground
3Y	8	O	Channel 3, Output Y
3A	9	I	Channel 3, Input A
3B	10	I	Channel 3, Input B
3C	11	I	Channel 3, Input C
1Y	12	O	Channel 1, Output Y
1C	13	I	Channel 1, Input C
VCC	14	—	Positive Supply
Thermal Pad ⁽²⁾	—	—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

(2) BQA package only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range ⁽²⁾		-0.5	6.5	V
V_O	Output voltage range ⁽²⁾		-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0 \text{ V}$		-50	mA
I_{OK}	Output clamp current	$V_O < 0 \text{ V}$		-50	mA
I_O	Continuous output current			± 50	mA
I_O	Continuous output current through V_{CC} or GND			± 100	mA
T_J	Junction temperature		-65	150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 ⁽¹⁾	± 2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	± 1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		1.1	3.6	V
V_I	Input voltage			5.5	V
V_O	Output voltage	(High or low state)		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 1.8 \text{ V}$		-4	mA
		$V_{CC} = 2.3 \text{ V}$		-8	
		$V_{CC} = 2.7 \text{ V}$		-12	
		$V_{CC} = 3 \text{ V}$		-24	
I_{OL}	Low-level output current	$V_{CC} = 1.8 \text{ V}$		4	mA
		$V_{CC} = 2.3 \text{ V}$		8	
		$V_{CC} = 2.7 \text{ V}$		12	
		$V_{CC} = 3 \text{ V}$		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		-40	125	°C
V_{IH}	High-level input voltage	$V_{CC} = 1.1 \text{ V}$	0.75		V
V_{IH}	High-level input voltage	$V_{CC} = 1.2 \text{ V}$	0.78		V
V_{IH}	High-level input voltage	$V_{CC} = 1.5 \text{ V}$	0.975		V
V_{IH}	High-level input voltage	$V_{CC} = 1.65 \text{ V}$	1.075		V
V_{IH}	High-level input voltage	$V_{CC} = 1.95 \text{ V}$	1.2675		V

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V_{IH}	High-level input voltage	$V_{CC} = 2.3\text{ V}$	1.7		V
V_{IH}	High-level input voltage	$V_{CC} = 2.7\text{ V}$	1.7		V
V_{IH}	High-level input voltage	$V_{CC} = 3.6\text{ V}$	2		V
V_{IL}	Low-Level input voltage	$V_{CC} = 1.1\text{ V}$		0.40	V
V_{IL}	Low-Level input voltage	$V_{CC} = 1.2\text{ V}$		0.42	V
V_{IL}	Low-Level input voltage	$V_{CC} = 1.5\text{ V}$		0.525	V
V_{IL}	Low-Level input voltage	$V_{CC} = 1.65\text{ V}$		0.5775	V
V_{IL}	Low-Level input voltage	$V_{CC} = 1.95\text{ V}$		0.6825	V
V_{IL}	Low-Level input voltage	$V_{CC} = 2.3\text{ V}$		0.7	V
V_{IL}	Low-Level input voltage	$V_{CC} = 2.7\text{ V}$		0.7	V
V_{IL}	Low-Level input voltage	$V_{CC} = 3.6\text{ V}$		0.8	V

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		Package Options			UNIT
		BQA (WQFN)	PW (TSSOP)	D (SOIC)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.3	150.8	127.8	°C/W
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	96.8	78.3	81.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.9	93.8	84.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	16.6	24.7	39.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	70.9	93.2	83.9	°C/W
$R_{\theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	50.1	-	-	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
V_{OH}	$I_{OH} = -100\text{ }\mu\text{A}$	1.1 V to 3.6 V		$V_{CC} - 0.2$		V
V_{OH}	$I_{OH} = -4\text{ mA}$	1.65 V		1.2		V
V_{OH}	$I_{OH} = -8\text{ mA}$	2.3 V		1.75		V
V_{OH}	$I_{OH} = -12\text{ mA}$	2.7 V		2.2		V
V_{OH}	$I_{OH} = -24\text{ mA}$	3 V		2.4		V
V_{OL}	$I_{OH} = 100\text{ }\mu\text{A}$	1.1 V to 3.6 V			0.15	V
V_{OL}	$I_{OH} = 4\text{ mA}$	1.65 V			0.45	V
V_{OL}	$I_{OH} = 8\text{ mA}$	2.3 V			0.7	V
V_{OL}	$I_{OH} = 12\text{ mA}$	2.7 V			0.4	V
V_{OL}	$I_{OH} = 24\text{ mA}$	3 V			0.55	V
I_I	$V_I = V_{CC}$ or GND	3.6 V			±5	μA
I_{off}	V_I or $V_O = V_{CC}$	0 V			±10	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μA
ΔI_{CC}	One input at $V_{CC} - 0.6\text{ V}$, other inputs at V_{CC} or GND	2.7 V to 3.6 V			500	μA

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
C _I	V _I = V _{CC} or GND	3.3 V		4.9		pF
C _O	V _O = V _{CC} or GND	3.3 V		6.3		pF
C _{PD}	f = 10 MHz	1.8 V		31		pF
C _{PD}	f = 10 MHz	2.5 V		31		pF
C _{PD}	f = 10 MHz	3.3 V		32		pF

5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t _{pd}	A, B or C	Y	C _L = 15 pF	1.2 V ± 0.1 V		12	23	ns
			C _L = 15 pF	1.5 V ± 0.12 V		9	12	
t _{pd}	A, B or C	Y	C _L = 30 pF	1.8 V ± 0.15 V			10.2	ns
			C _L = 30 pF	2.5 V ± 0.2 V			6.9	
			C _L = 50 pF	2.7 V			4.8	
			C _L = 50 pF	3.3 V ± 0.3 V			4.1	
				3.3 V ± 0.3 V			1.5	ns
t _{sk(o)}								

5.7 Noise Characteristics

V_{CC} = 3.3 V, CL = 50 pF, TA = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}			0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}	-0.8	-0.3		V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}	2.2	3.3		V
V _{IH(D)}	High-level dynamic input voltage	2.0			V
V _{IL(D)}	Low-level dynamic input voltage			0.8	V

5.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

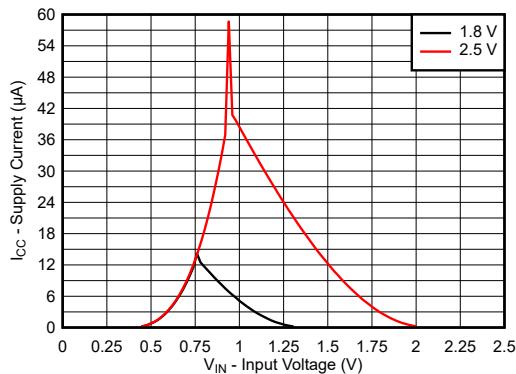


Figure 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply

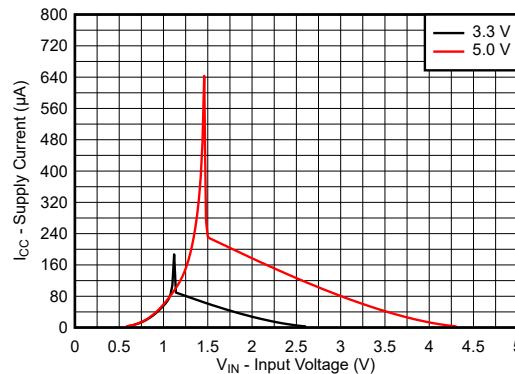


Figure 5-2. Supply Current Across Input Voltage 3.3V and 5.0V Supply

5.8 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

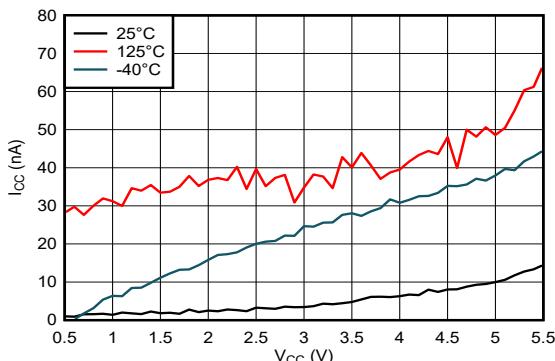


Figure 5-3. Supply Current Across Supply Voltage

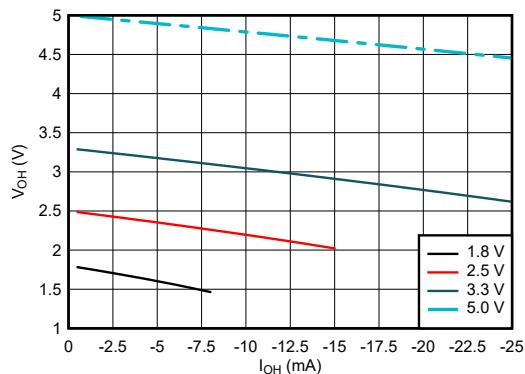


Figure 5-4. Output Voltage vs Current in HIGH State

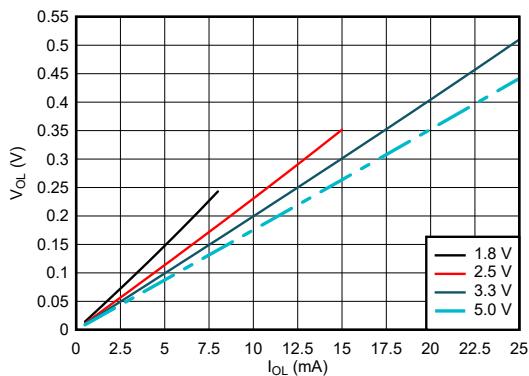


Figure 5-5. Output Voltage vs Current in LOW State

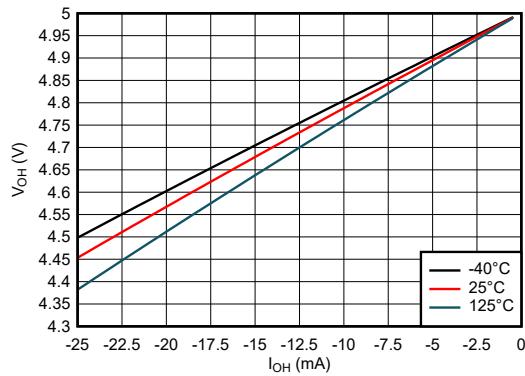


Figure 5-6. Output Voltage vs Current in HIGH State; 5V Supply

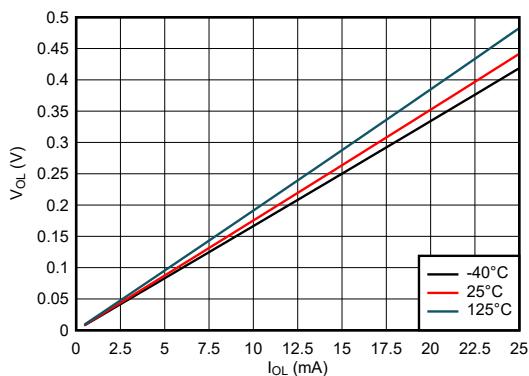


Figure 5-7. Output Voltage vs Current in LOW State; 5V Supply

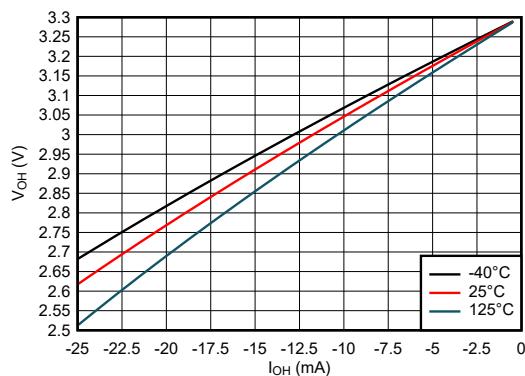


Figure 5-8. Output Voltage vs Current in HIGH State; 3.3V Supply

5.8 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

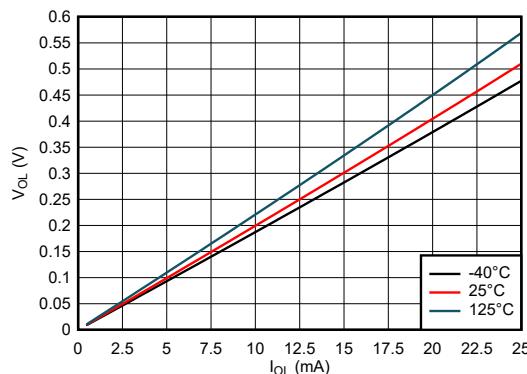


Figure 5-9. Output Voltage vs Current in LOW State; 3.3V Supply

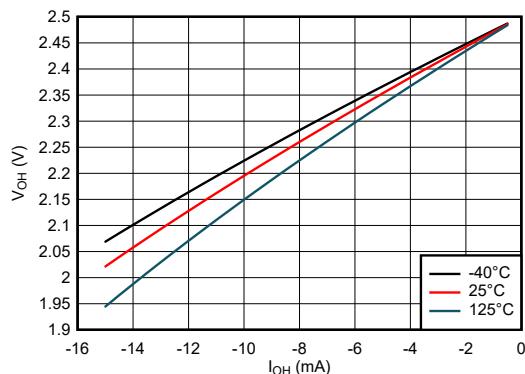


Figure 5-10. Output Voltage vs Current in HIGH State; 2.5V Supply

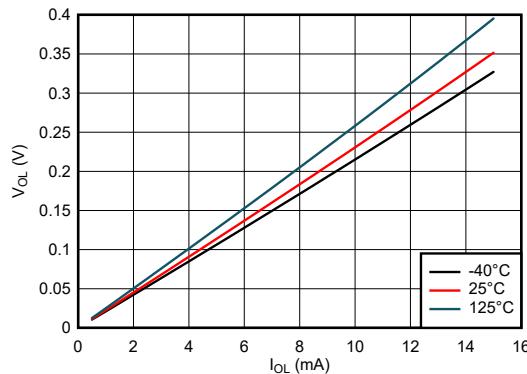


Figure 5-11. Output Voltage vs Current in LOW State; 2.5V Supply

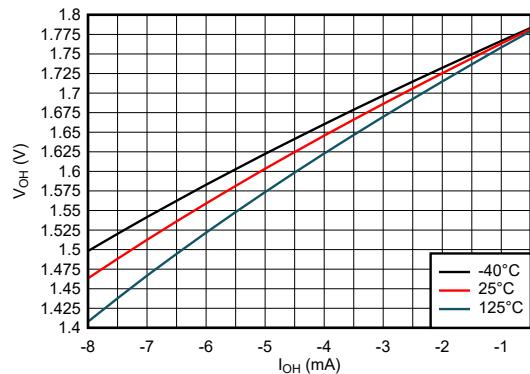


Figure 5-12. Output Voltage vs Current in HIGH State; 1.8V Supply

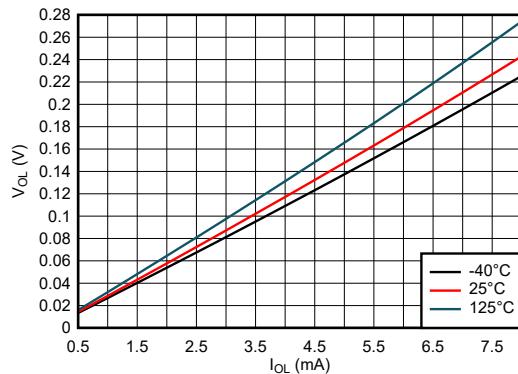


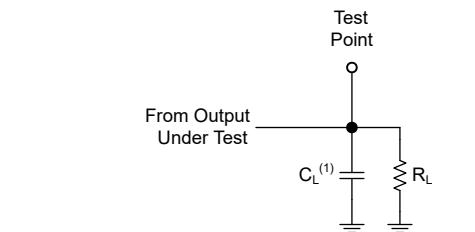
Figure 5-13. Output Voltage vs Current in LOW State; 1.8V Supply

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR \leq 1MHz, $Z_0 = 50\Omega$, $t_t \leq 2.5\text{ns}$.

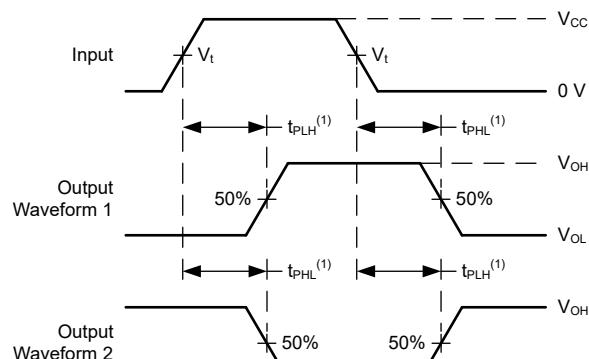
The outputs are measured individually with one input transition per measurement.

V_{CC}	V_t	R_L	C_L	ΔV
$1.2V \pm 0.1V$	$V_{CC}/2$	$2k\Omega$	15pF	$0.1V$
$1.5V \pm 0.12V$	$V_{CC}/2$	$2k\Omega$	15pF	$0.1V$
$1.8V \pm 0.15V$	$V_{CC}/2$	$1k\Omega$	30pF	$0.15V$
$2.5V \pm 0.2V$	$V_{CC}/2$	500Ω	30pF	$0.15V$
$2.7V$	$1.5V$	500Ω	50pF	$0.3V$
$3.3V \pm 0.3V$	$1.5V$	500Ω	50pF	$0.3V$



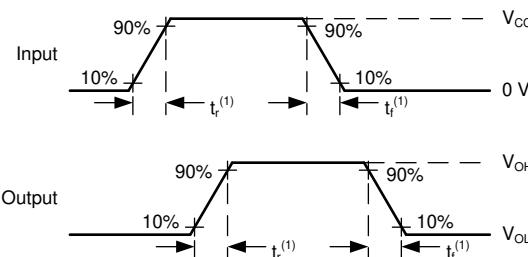
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

Figure 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t .

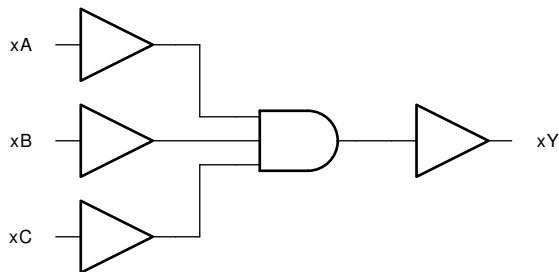
Figure 6-3. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

This device contains three independent 3-input AND gates. Each gate performs the Boolean function $Y = A \times B \times C$ in positive logic.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the *Electrical Characteristics - 74*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics - 74*, using ohm's law ($R = V \div I$).

Signals applied to the inputs need to have fast edge rates, as defined by the input transition time in the *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

7.3.2 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

The SN74LVC11A-Q1 can drive a load with a total capacitance less than or equal to the maximum load listed in the *Switching Characteristics -74* connected to a high-impedance CMOS input while still meeting all of the data sheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the *Absolute Maximum Ratings*.

7.3.3 Clamp Diode Structure

Figure 7-1 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

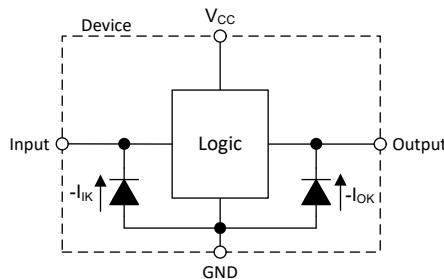


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

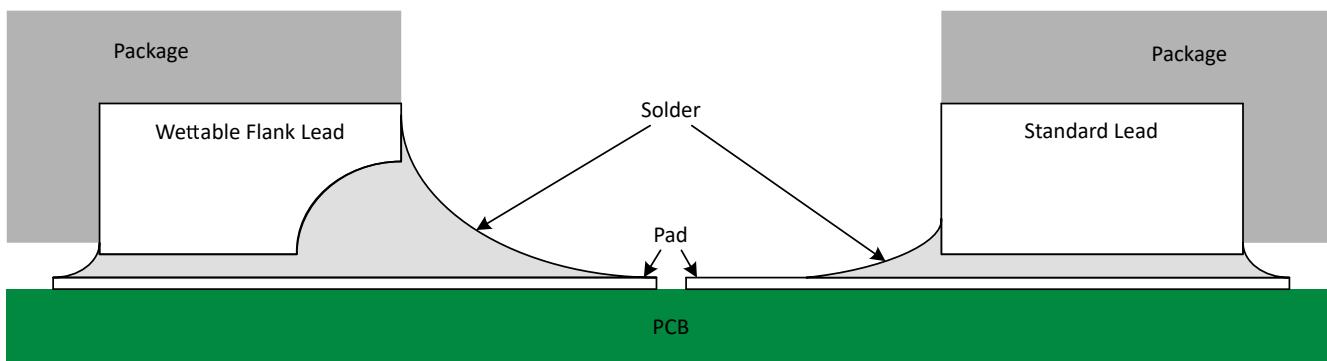


Figure 7-2. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in Figure 7-2, a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

7.4 Device Functional Modes

Table 7-1. Function Table⁽¹⁾

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

(1) H = high voltage level, L = low voltage level, X = do not care

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, this device is used to directly control the RESET pin of a motor controller. The controller requires three input signals to all be HIGH before being enabled, and should be disabled in the event that any one signal goes LOW. The 3-input AND gate function combines the three individual reset signals into a single active-low reset signal.

8.2 Typical Application

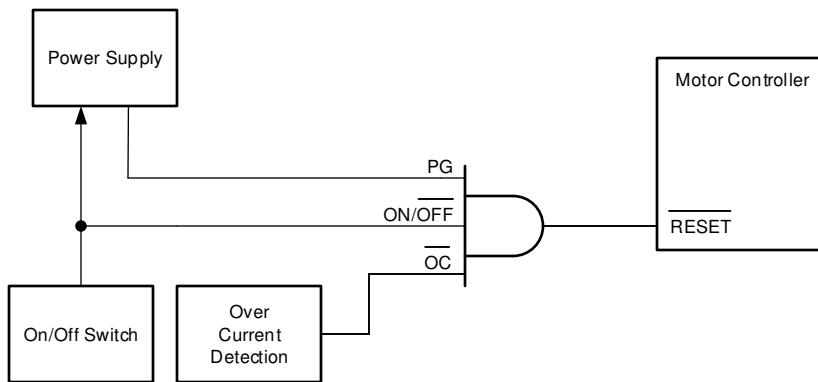


Figure 8-1. Typical Application Schematic

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LVC11A-Q1 plus the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LVC11A-Q1 plus the maximum supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LVC11A-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74LVC11A-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the HIGH state,

the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the [CMOS Power Consumption and Cpd Calculation](#) application note.

Thermal increase can be calculated using the information provided in the [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#) application note.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LVC11A-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10k Ω resistor value is often used due to these factors.

The SN74LVC11A-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in *Layout Examples*.
2. Ensure the capacitive load at the output is $\leq 70\text{pF}$. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LVC11A-Q1 to the receiving device.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_O(\text{max})) \Omega$, so that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in mega ohms; much larger than the minimum calculated previously.

4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#)

8.2.3 Application Curves

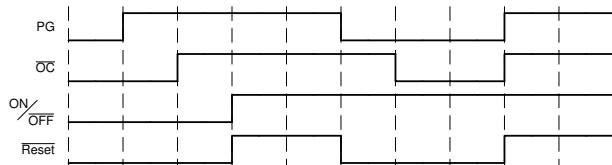


Figure 8-2. Typical Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A $0.1\mu F$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1\mu F$ and $1\mu F$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in [Layout Example](#).

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example

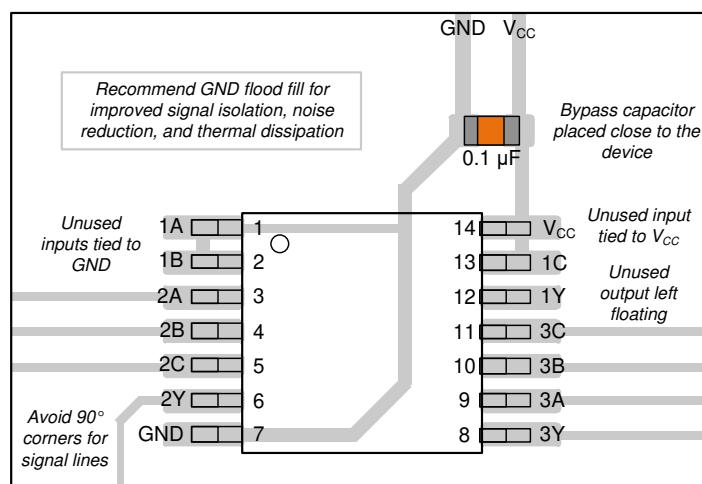


Figure 8-3. Example Layout for the SN74LVC11A-Q1

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and Cpd Calculation](#) application note
- Texas Instruments, [Designing With Logic](#) application note
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#) application note
- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#) application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2024) to Revision B (May 2024)	Page
• Added D package to <i>Package Information</i> table, <i>Pin Configuration and Functions</i> section, and <i>Thermal Information</i> table.....	1
• Updated operating range in <i>Features</i> section from 1.2V to 1.1V and deleted note from <i>Description</i> section....	1

Changes from Revision * (August 2023) to Revision A (February 2024)	Page
• Changed the status from: <i>Advanced Information</i> to: <i>Production Data</i>	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC11ADRQ1	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC11AQ
SN74LVC11ADRQ1.A	Active	Production	SOIC (D) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC11AQ
SN74LVC11APWRQ1	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC11AQ
SN74LVC11APWRQ1.A	Active	Production	TSSOP (PW) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC11AQ
SN74LVC11AWBQARQ1	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC11Q
SN74LVC11AWBQARQ1.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC11Q

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

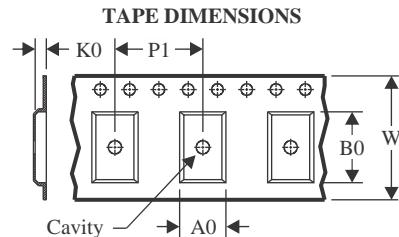
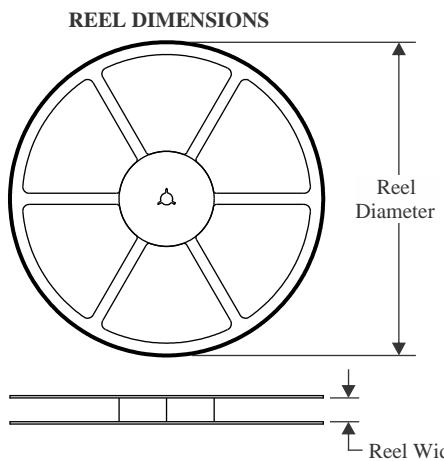
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC11A-Q1 :

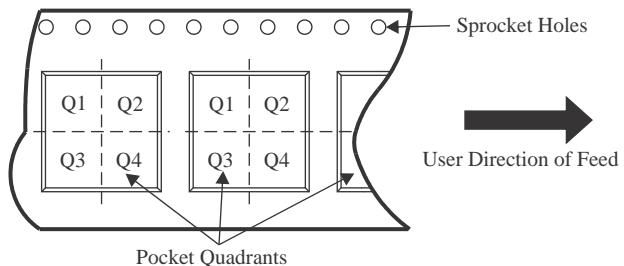
- Catalog : [SN74LVC11A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

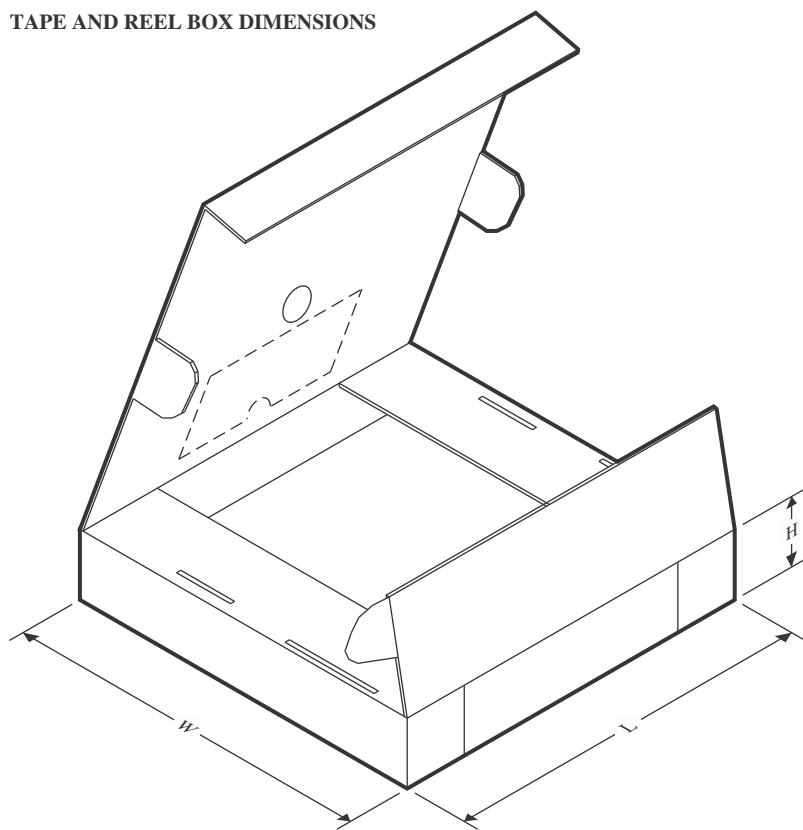
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC11ADRQ1	SOIC	D	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74LVC11APWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC11AWBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC11ADRQ1	SOIC	D	14	3000	340.5	336.1	32.0
SN74LVC11APWRQ1	TSSOP	PW	14	3000	353.0	353.0	32.0
SN74LVC11AWBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0

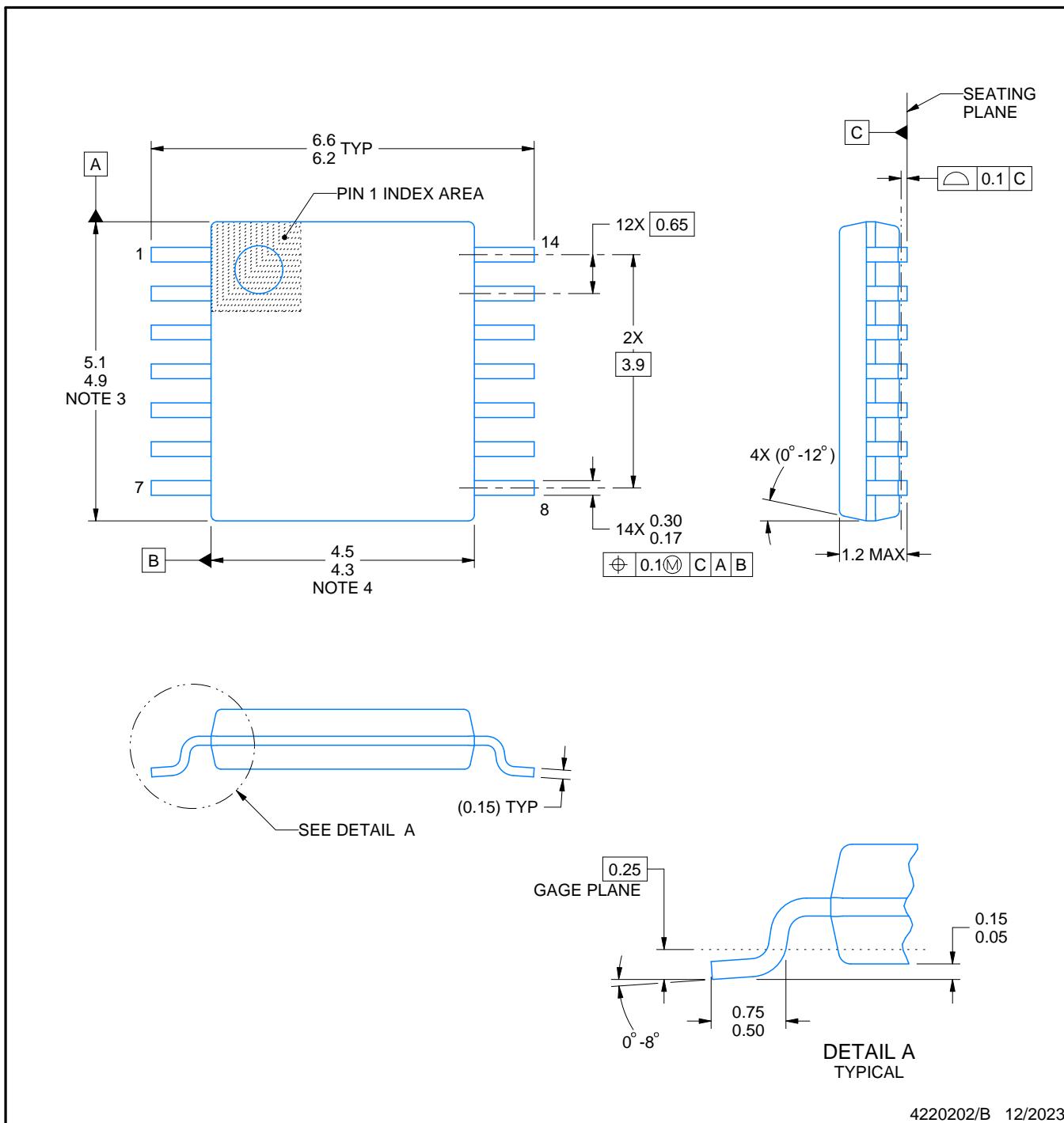
PACKAGE OUTLINE

PW0014A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

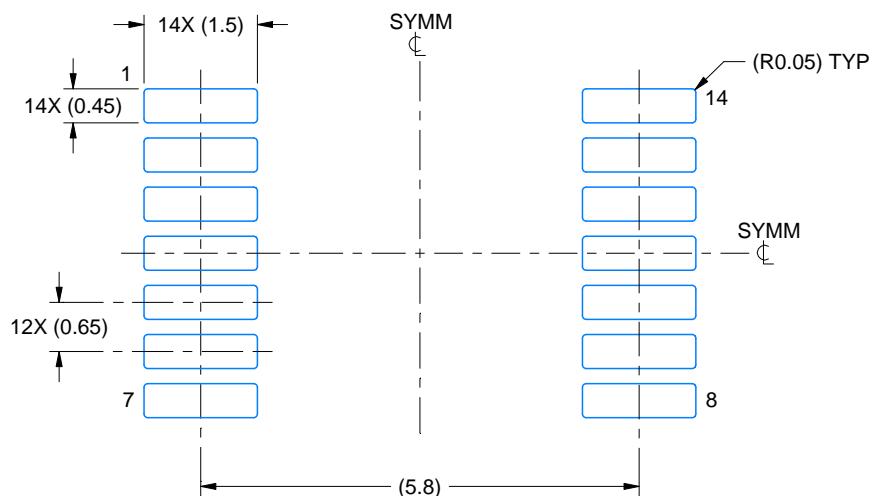
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

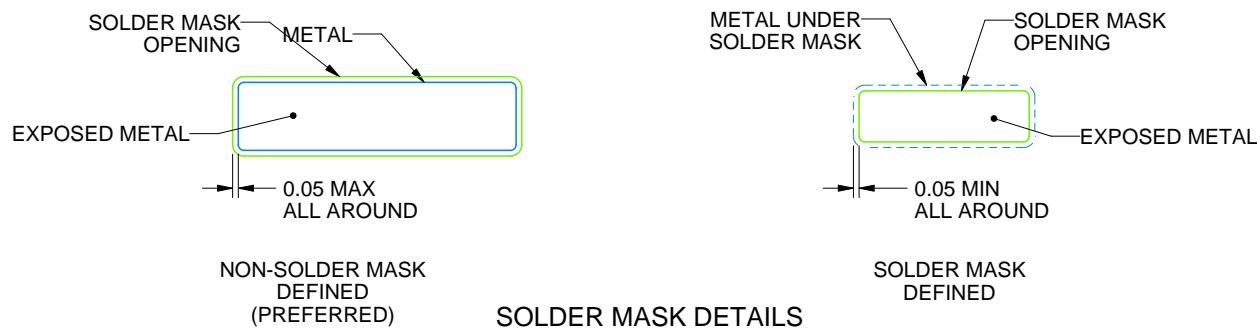
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

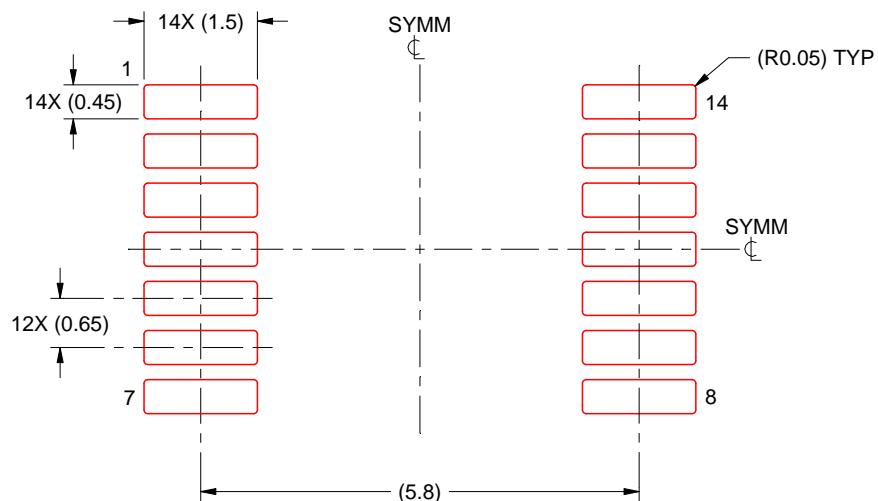
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X**

4220202/B 12/2023

NOTES: (continued)

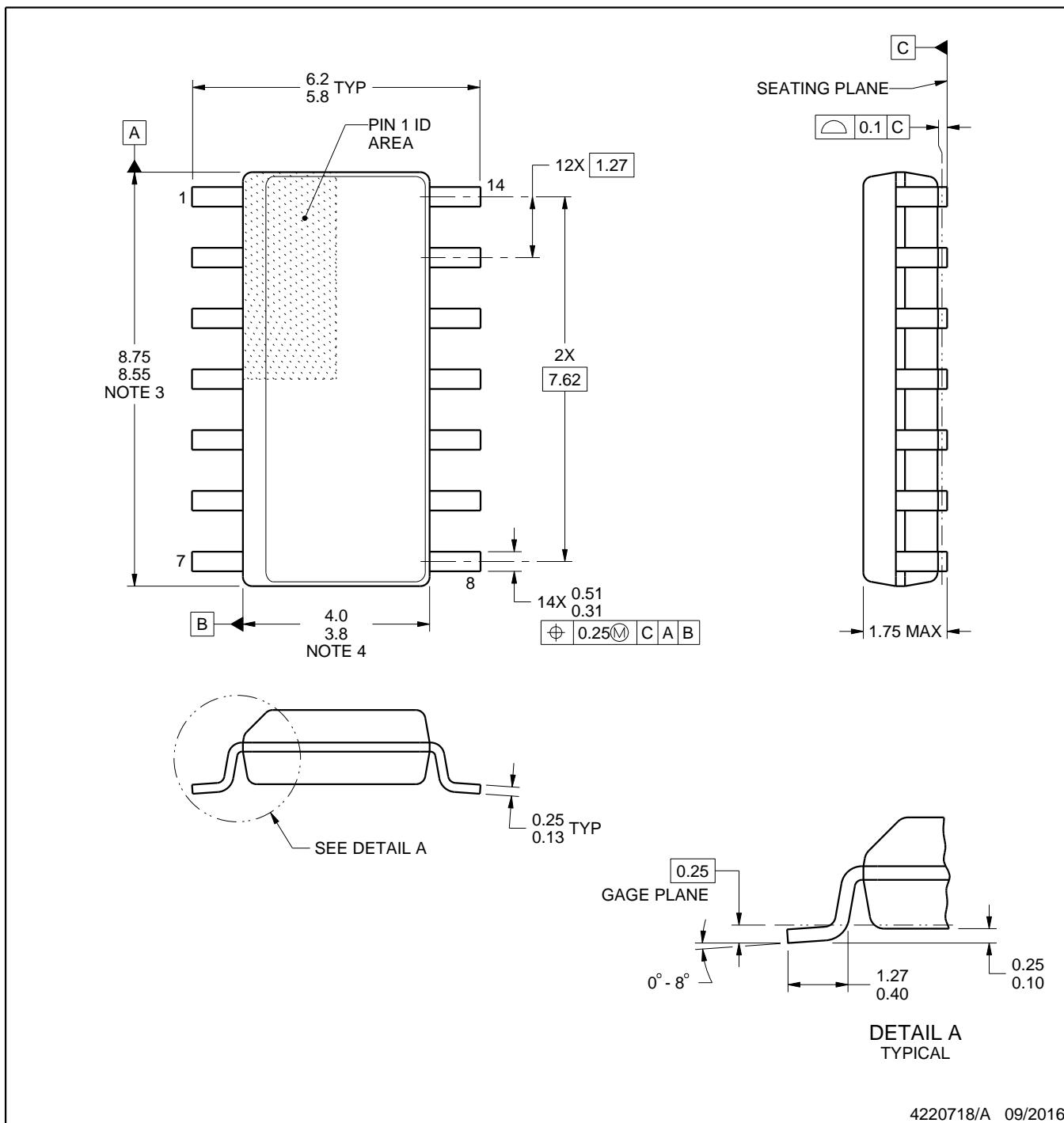
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

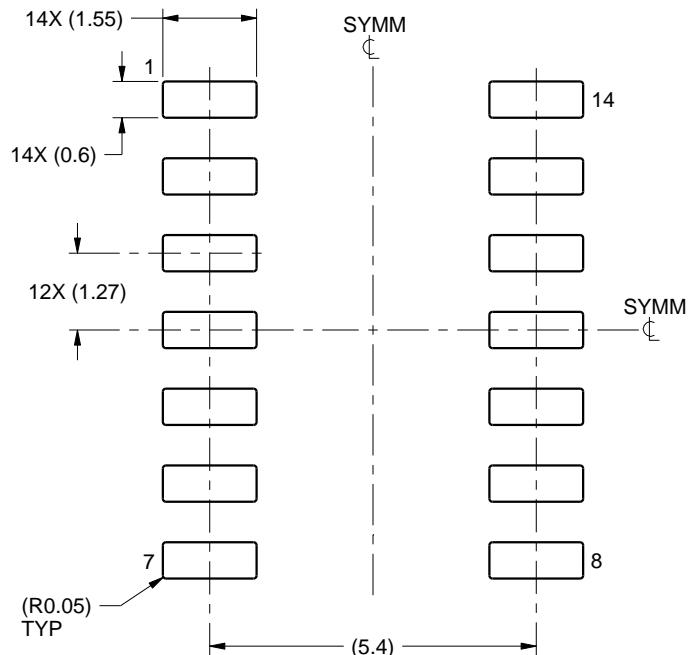
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

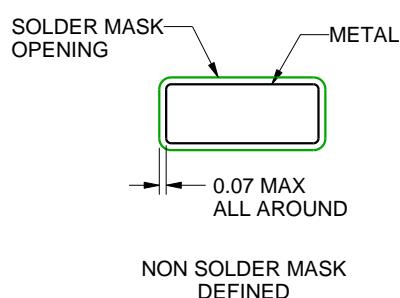
D0014A

SOIC - 1.75 mm max height

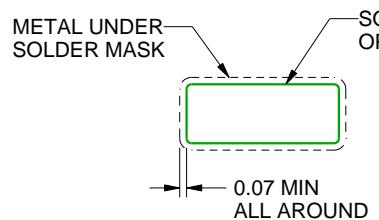
SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

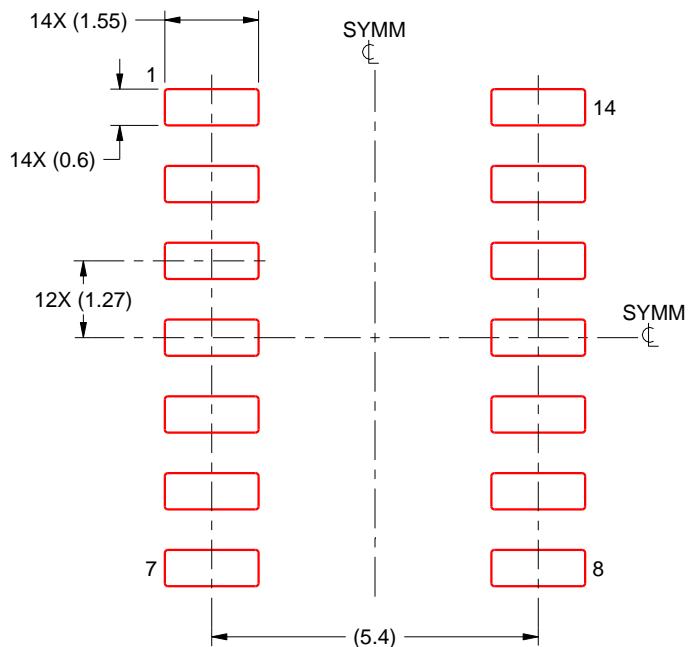
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



**SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X**

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

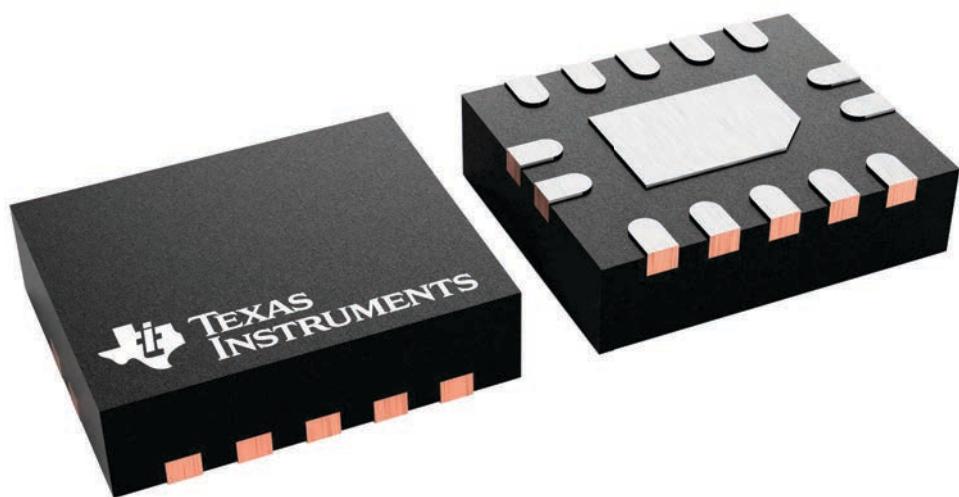
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227145/A

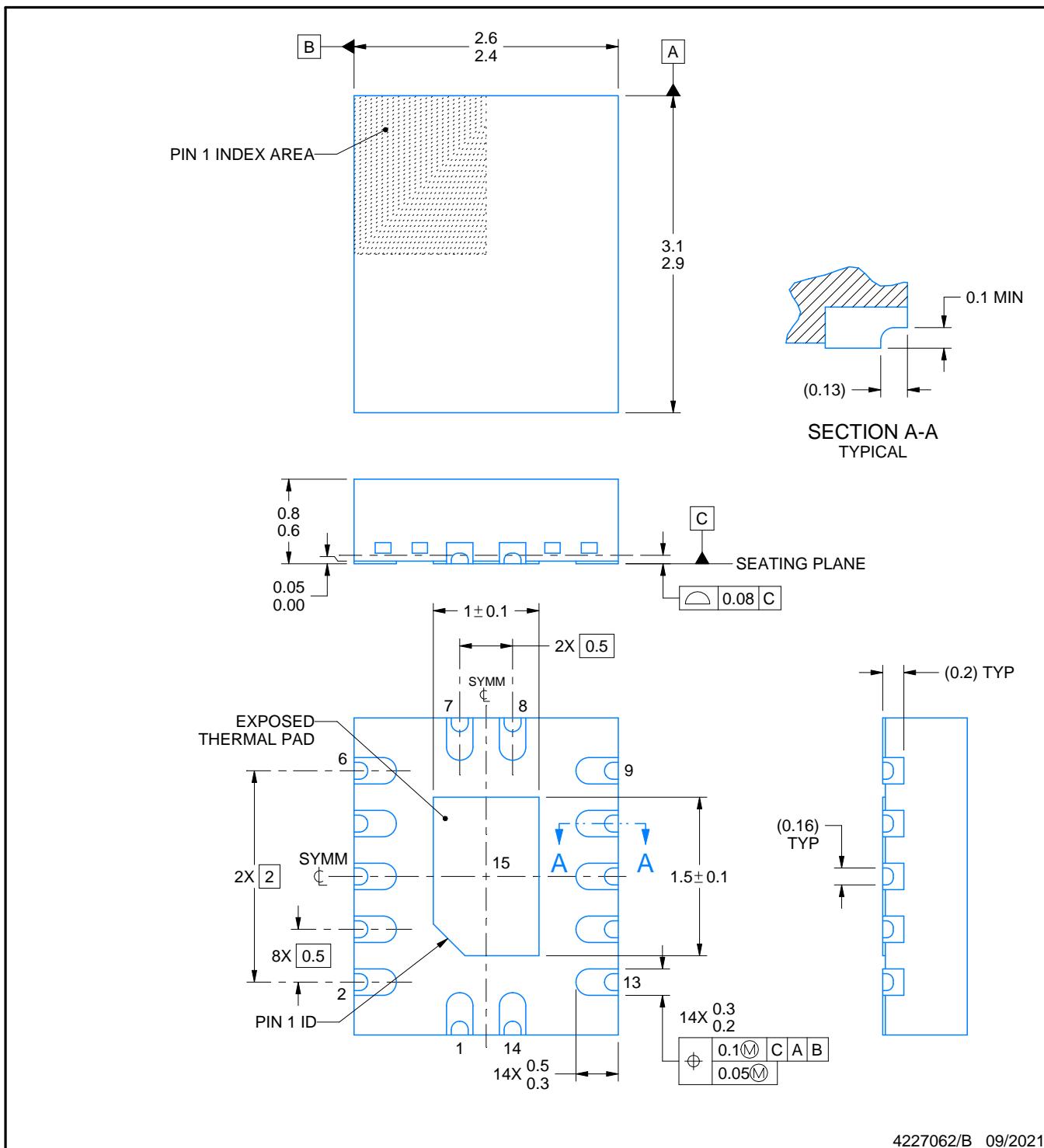
PACKAGE OUTLINE

BQA0014B



WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4227062/B 09/2021

NOTES:

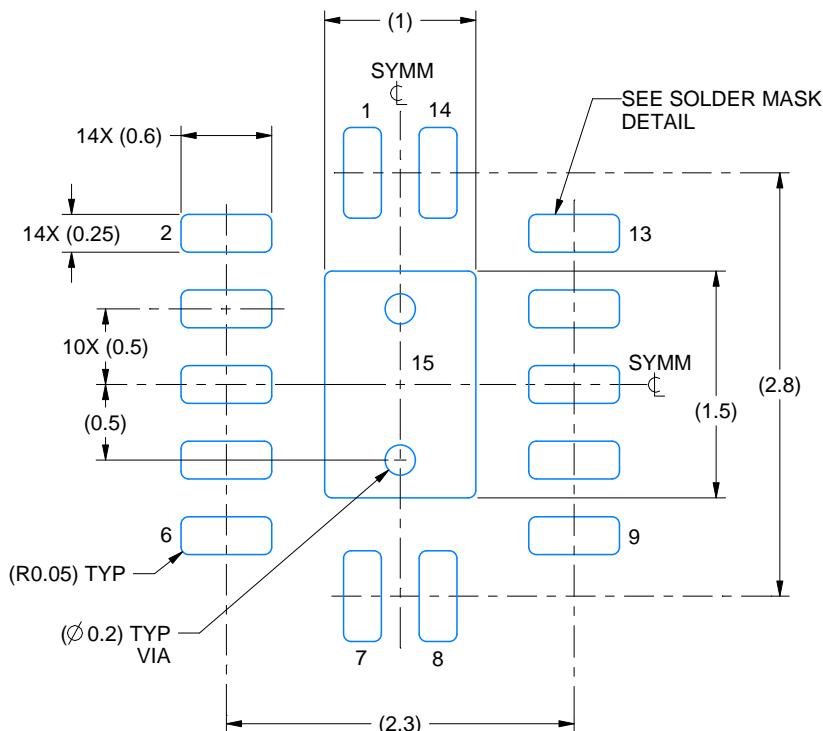
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

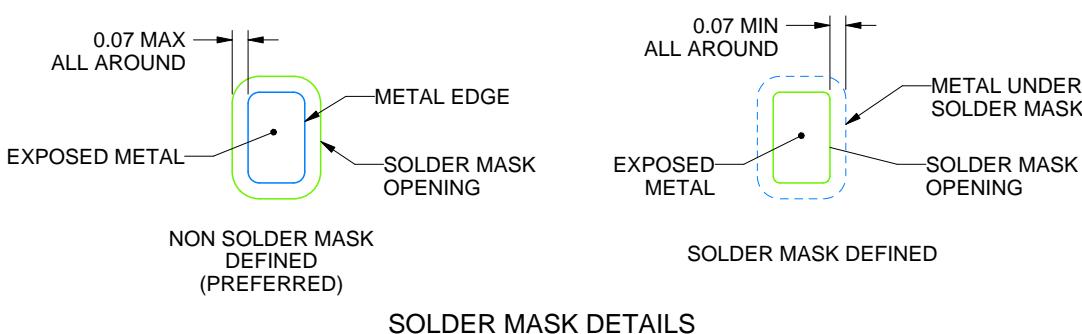
BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4227062/B 09/2021

NOTES: (continued)

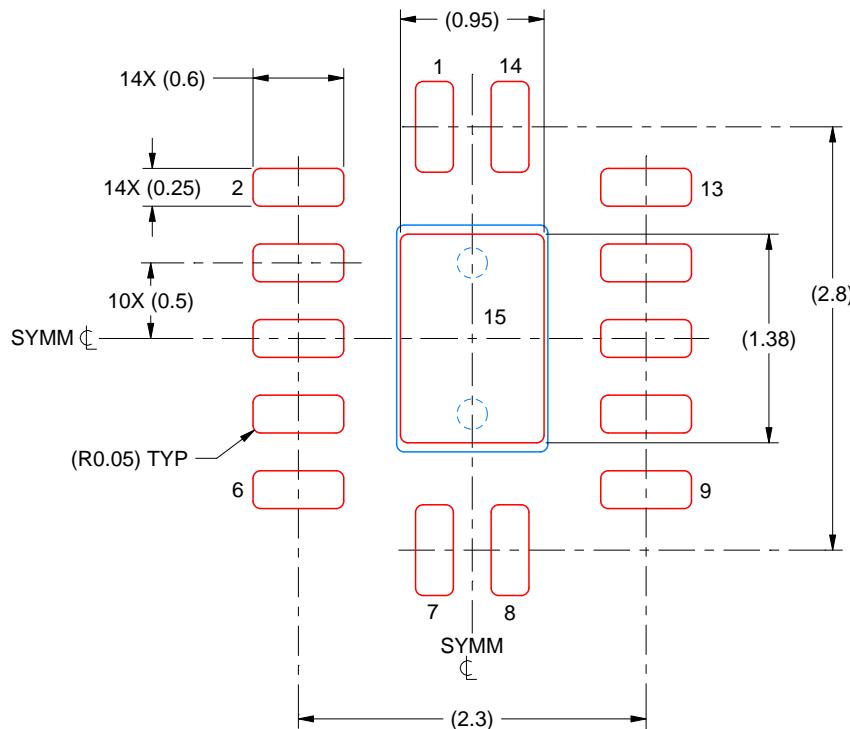
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4227062/B 09/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025