

SN74LVC1G34 Single Buffer Gate

1 Features

- Available in the ultra small 0.64mm² package (DPW) with 0.5mm pitch
- Supports 5V V_{CC} operation
- Inputs accept voltages to 5.5V
- Provides down translation to V_{CC}
- Maximum t_{pd} of 3.5ns at 3.3V
- Low power consumption, 1µA maximum I_{CC}
- ±24mA output drive at 3.3V
- I_{off} supports live insertion, partial power down mode, and back drive protection
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD protection exceeds JESD 22
 - 2000V human-body model (A114A)
 - 200V machine model (A115A)
 - 1000V charged-device model (C101)

2 Applications

- AV receiver
- Audio dock: portable
- Blu-ray player and home theater
- DVD recorder and player
- Embedded PC
- MP3 player/recorder (portable audio)
- Personal Digital Assistant (PDA)
- Power: telecom/server AC/DC supply: single controller: analog and digital
- Solid State Drive (SSD): client and enterprise
- TV: LCD/digital and high-definition (HDTV)
- Tablet: enterprise
- Video analytics: server
- Wireless headset, keyboard, and mouse

3 Description

This single buffer gate is designed for 1.65V to 5.5V V_{CC} operation.

The SN74LVC1G34 device performs the Boolean function $Y = A$ in positive logic.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} Operating range.

The SN74LVC1G34 is available in a variety of packages, including the ultra-small DPW package with a body size of 0.8mm × 0.8mm.

Package Information

| DEVICE NAME | PACKAGE (1) | PACKAGE SIZE(2) | BODY SIZE (NOM)(3) |
|-------------|-----------------|-----------------|--------------------|
| SN74LVC1G34 | YFP (DSBGA, 4) | 1.00mm × 1.00mm | 0.76mm × 0.76mm |
| | YZP (DSBGA, 5) | 1.75mm × 1.25mm | 1.38mm × 0.88mm |
| | YZV (DSBGA, 4) | 1.25mm × 1.25mm | 0.88mm × 0.88mm |
| | DPW (X2SON, 5) | 0.80mm × 0.80mm | 0.80mm × 0.80mm |
| | DBV (SOT-23, 5) | 2.90mm × 2.80mm | 2.90mm × 2.80mm |
| | DCK (SC70, 5) | 2.00mm × 2.10mm | 2.00mm × 2.10mm |
| | DRL (SOT, 5) | 1.60mm × 1.60mm | 1.60mm × 1.60mm |
| | DRY (USON (6) | 1.45mm × 1.00mm | 1.45mm × 1.00mm |
| | DSF (X2SON, 6) | 1.00mm × 1.00mm | 1.00mm × 1.00mm |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



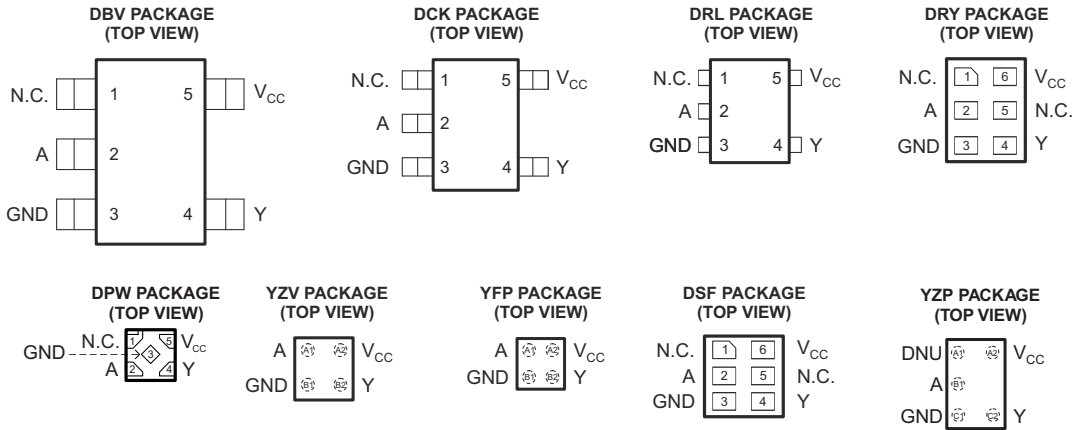
Simplified Schematic



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4 Pin Configuration and Functions



See mechanical drawings for dimensions.
N.C. – No internal connection
DNU – Do not use

Table 4-1. Pin Functions

| NAME | PIN | | | | | DESCRIPTION |
|-----------------|---------------|-----|----------|-----|----------|---------------|
| | DRL, DCK, DBV | DPW | DRY, DSF | YZP | YFP, YZV | |
| NC | 1 | 1 | 1, 5 | A1 | – | Not connected |
| A | 2 | 2 | 2 | B1 | A1 | Input |
| GND | 3 | 3 | 3 | C1 | B1 | Ground |
| Y | 4 | 4 | 4 | C2 | B2 | Output |
| V _{CC} | 5 | 5 | 6 | A2 | A2 | Power pin |

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

| (1) | | MIN | MAX | UNIT |
|-----------|---|-----------|----------------|------|
| V_{CC} | Supply voltage range | -0.5 | 6.5 | V |
| V_I | Input voltage range | -0.5 | 6.5 | V |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 6.5 | V |
| V_O | Voltage range applied to any output in the high or low state ^{(2) (3)} | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current | $V_I < 0$ | -50 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ | -50 | mA |
| I_O | Continuous output current | | ±50 | mA |
| | Continuous current through V_{CC} or GND | | ±100 | mA |
| T_{stg} | Storage temperature range | -65 | 150 | °C |
| T_J | Max Junction temperature | | 150 | °C |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

5.2 ESD Ratings

| | | | MIN | MAX | UNIT |
|-------------|-------------------------|--|-----|-----|------|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | | ±2 | kV |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | | ±1 | |

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

| (1) | | MIN | MAX | UNIT | |
|-----------------|------------------------------------|---|------------------------|------|------|
| V _{CC} | Supply voltage | Operating | 1.65 | 5.5 | V |
| | | Data retention only | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65V to 1.95V | 0.65 × V _{CC} | | V |
| | | V _{CC} = 2.3V to 2.7V | 1.7 | | |
| | | V _{CC} = 3V to 3.6V | 2 | | |
| | | V _{CC} = 4.5V to 5.5V | 0.7 × V _{CC} | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65V to 1.95V | 0.35 × V _{CC} | | V |
| | | V _{CC} = 2.3V to 2.7V | 0.7 | | |
| | | V _{CC} = 3V to 3.6V | 0.8 | | |
| | | V _{CC} = 4.5V to 5.5V | 0.3 × V _{CC} | | |
| V _I | Input voltage | 0 | 5.5 | V | |
| V _O | Output voltage | 0 | V _{CC} | V | |
| I _{OH} | High-level output current | V _{CC} = 1.65V | -4 | | mA |
| | | V _{CC} = 2.3V | -8 | | |
| | | V _{CC} = 3V | -16 | | |
| | | V _{CC} = 4.5V | -24 | | |
| I _{OL} | Low-level output current | V _{CC} = 1.65V | 4 | | mA |
| | | V _{CC} = 2.3V | 8 | | |
| | | V _{CC} = 3V | 16 | | |
| | | V _{CC} = 4.5V | 24 | | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 1.8V ± 0.15V, 2.5V ± 0.2V | 20 | | ns/V |
| | | V _{CC} = 3.3V ± 0.3V | 10 | | |
| | | V _{CC} = 5V ± 0.5V | 10 | | |
| T _A | Operating free-air temperature | DSBGA package | -40 | 85 | °C |
| | | All other packages | -40 | 125 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

5.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | SN74LVC1G34 | | | | | | UNIT | |
|-------------------------------|--|--------|--------|--------|--------|--------|------|------|
| | DBV | DCK | DRL | DRY | YZP | DPW | | |
| | 5 PINS | 5 PINS | 5 PINS | 6 PINS | 5 PINS | 4 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 357.1 | 371.0 | 243 | 439 | 130 | 340 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 263.7 | 297.5 | 78 | 277 | 54 | 215 | |
| R _{θJB} | Junction-to-board thermal resistance | 264.4 | 258.6 | 78 | 271 | 51 | 294 | |
| ψ _{JT} | Junction-to-top characterization parameter | 195.6 | 195.6 | 10 | 84 | 1 | 41 | |
| ψ _{JB} | Junction-to-board characterization parameter | 262.2 | 256.2 | 77 | 271 | 50 | 294 | |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | – | – | – | – | – | 250 | |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | –40°C to 85°C | | | –40°C to 125°C | | | UNIT |
|------------------|--|-----------------|-----------------------|--------------------|-----|-----------------------|--------------------|-----|------|
| | | | MIN | TYP ⁽¹⁾ | MAX | MIN | TYP ⁽¹⁾ | MAX | |
| V _{OH} | I _{OH} = –100μA | 1.65V to 5.5V | V _{CC} – 0.1 | | | V _{CC} – 0.1 | | | V |
| | I _{OH} = –4mA | 1.65V | 1.2 | | | 1.2 | | | |
| | I _{OH} = –8mA | 2.3V | 1.9 | | | 1.9 | | | |
| | I _{OH} = –16mA | 3V | 2.4 | | | 2.4 | | | |
| | I _{OH} = –24mA | | 2.3 | | | 2.3 | | | |
| | I _{OH} = –32mA | 4.5V | 3.8 | | | 3.8 | | | |
| V _{OL} | I _{OL} = 100μA | 1.65V to 5.5V | 0.1 | | | 0.1 | | | V |
| | I _{OL} = 4mA | 1.65V | 0.45 | | | 0.45 | | | |
| | I _{OL} = 8mA | 2.3V | 0.3 | | | 0.3 | | | |
| | I _{OL} = 16mA | 3V | 0.4 | | | 0.4 | | | |
| | I _{OL} = 24mA | | 0.55 | | | 0.55 | | | |
| | I _{OL} = 32mA | 4.5V | 0.55 | | | 0.55 | | | |
| I _I | V _I = 5.5V or GND | 0 to 5.5V | ±1 | | | ±2 | | | μA |
| I _{off} | V _I or V _O = 5.5V | 0 | ±10 | | | ±10 | | | μA |
| I _{CC} | V _I = 5.5V or GND, I _O = 0 | 1.65V to 5.5V | 1 | | | 10 | | | μA |
| ΔI _{CC} | One input at V _{CC} – 0.6V, Other inputs at V _{CC} or GND | 3V to 5.5V | 500 | | | 500 | | | μA |
| C _i | V _I = V _{CC} or GND | 3.3V | 3.5 | | | | | | pF |

(1) All typical values are at V_{CC} = 3.3V, T_A = 25°C.

5.6 Switching Characteristics, $C_L = 15\text{pF}$

over recommended operating free-air temperature range, $C_L = 15\text{pF}$ (unless otherwise noted) (see [Figure 6-1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -40°C to 85°C | | | | | | | | UNIT |
|-----------|--------------|-------------|---|-----|--|-----|--|-----|--------------------------------------|-----|------|
| | | | $V_{CC} = 1.8\text{V} \pm 0.15\text{V}$ | | $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$ | | $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ | | $V_{CC} = 5\text{V} \pm 0.5\text{V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A | Y | 2 | 9.9 | 1.5 | 6 | 1 | 3.5 | 1 | 2.9 | ns |

5.7 Switching Characteristics, -40°C to 85°C

over recommended operating free-air temperature range, $C_L = 30\text{pF}$ or 50pF (unless otherwise noted) (see [Figure 6-2](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -40°C to 85°C | | | | | | | | UNIT |
|-----------|--------------|-------------|---|-----|--|-----|--|-----|--------------------------------------|-----|------|
| | | | $V_{CC} = 1.8\text{V} \pm 0.15\text{V}$ | | $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$ | | $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ | | $V_{CC} = 5\text{V} \pm 0.5\text{V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A | Y | 3.2 | 8.6 | 1.5 | 4.4 | 1.5 | 4.1 | 1 | 3.2 | ns |

5.8 Switching Characteristics, -40°C to 125°C

over recommended operating free-air temperature range, $C_L = 30\text{pF}$ or 50pF (unless otherwise noted) (see [Figure 6-2](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -40°C to 125°C | | | | | | | | UNIT |
|-----------|--------------|-------------|---|-----|--|-----|--|-----|--------------------------------------|-----|------|
| | | | $V_{CC} = 1.8\text{V} \pm 0.15\text{V}$ | | $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$ | | $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ | | $V_{CC} = 5\text{V} \pm 0.5\text{V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A | Y | 3.2 | 9.5 | 1.5 | 5.1 | 1.5 | 4.7 | 1 | 3.9 | ns |

5.9 Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | $V_{CC} = 1.8\text{V}$ | $V_{CC} = 2.5\text{V}$ | $V_{CC} = 3.3\text{V}$ | $V_{CC} = 5\text{V}$ | UNIT |
|-----------|---|------------------------|------------------------|------------------------|----------------------|------|
| | | TYP | TYP | TYP | TYP | |
| C_{pd} | Power dissipation capacitance $f = 10\text{MHz}$ | 16 | 16 | 16 | 18 | pF |

5.10 Typical Characteristics

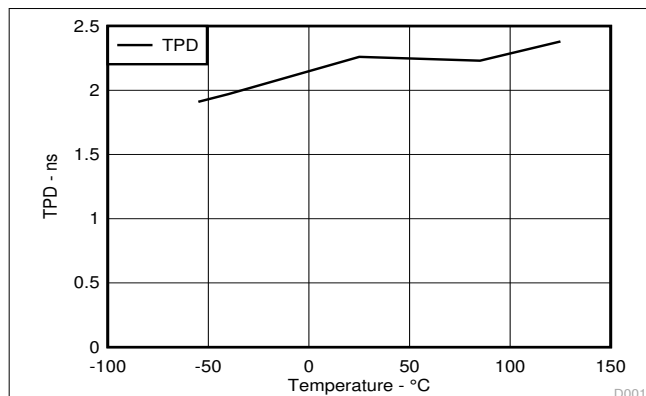


Figure 5-1. TPD Across Temperature at 3.3V Vcc

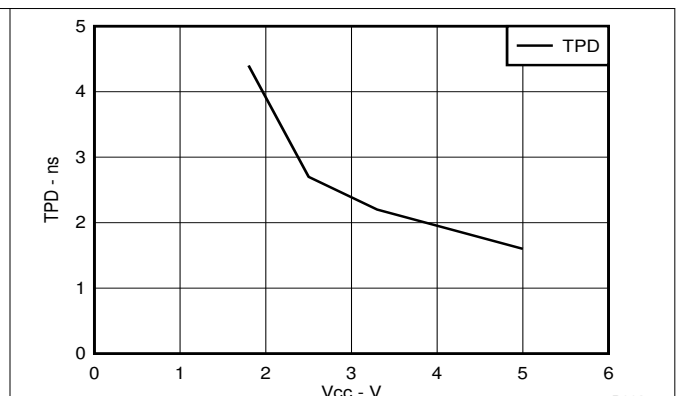
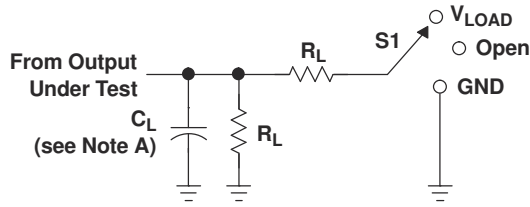


Figure 5-2. TPD Across Vcc at 25°C

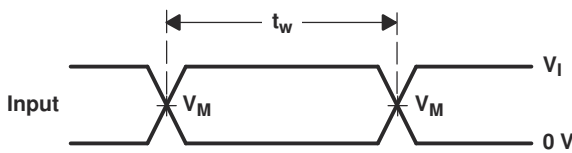
6 Parameter Measurement Information



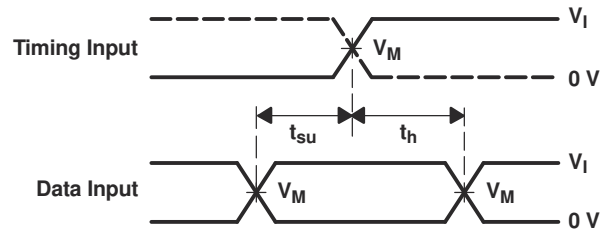
LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

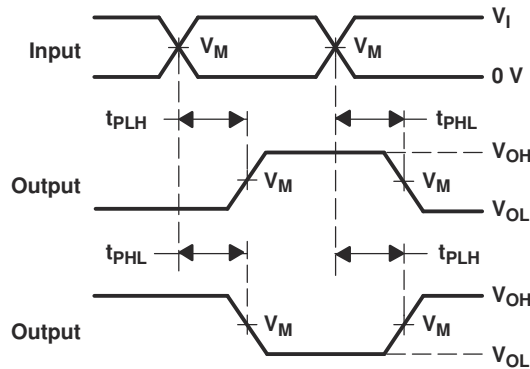
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 3 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 15 pF | 1 M Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M Ω | 0.3 V |



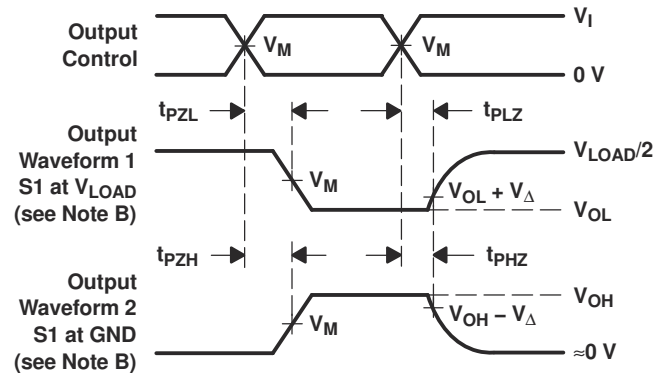
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



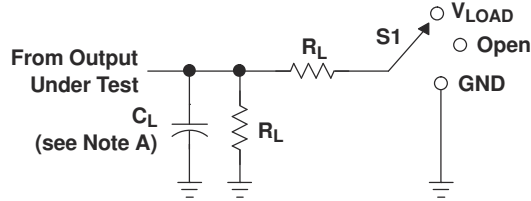
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

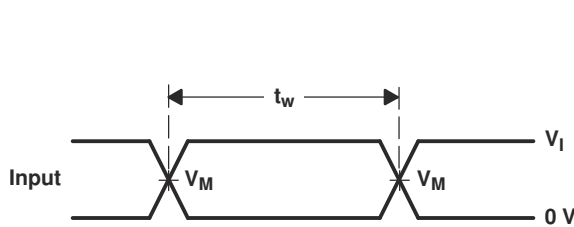
Figure 6-1. Load Circuit and Voltage Waveforms



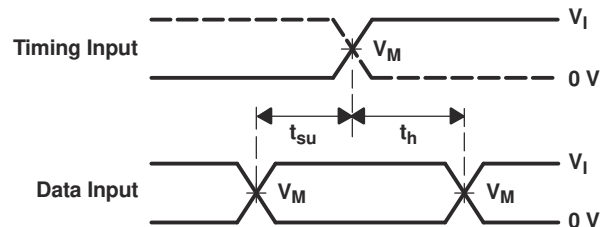
LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

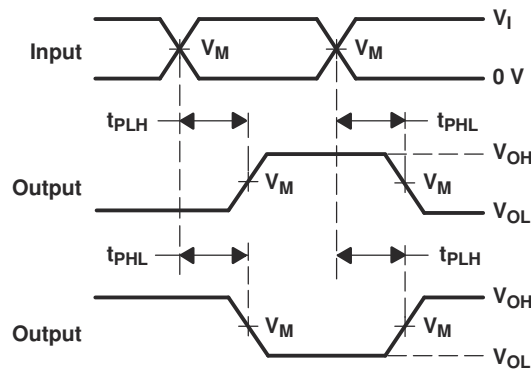
| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 3 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | V_{CC} | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



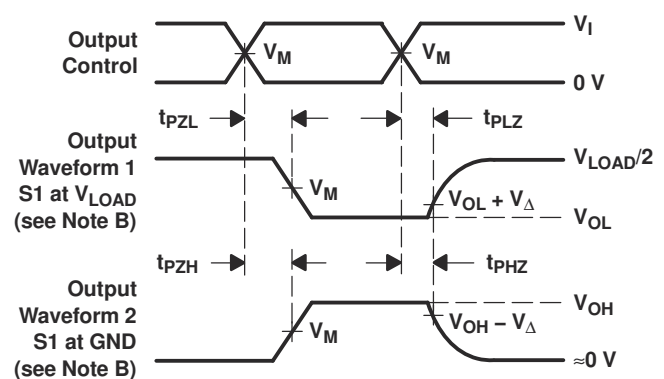
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
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VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 6-2. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74LVC1G34 device contains one buffer gate device and performs the Boolean function $Y = A$. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

7.2 Functional Block Diagram



7.3 Feature Description

7.4 Device Functional Modes

Function Table

| INPUT A | OUTPUT Y |
|------------|-------------|
| H | H |
| L | L |

8 Application and Implementation

Note

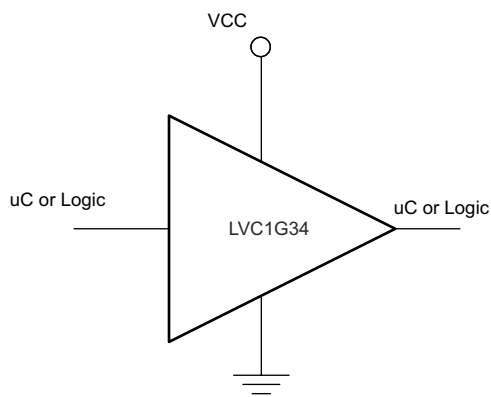
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

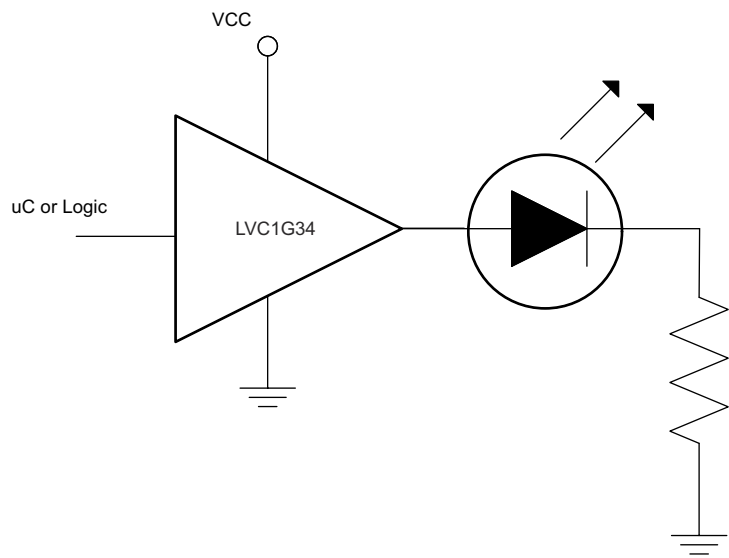
The SN74LVC1G34 is a high drive CMOS device that can be used as a buffer to drive an LED. It can produce 24mA of drive current at 3.3V making it ideal for driving multiple outputs and good for high speed applications up to 100MHz.

8.2 Typical Application

Buffer Function



Basic LED Driver



8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure that the desired supply voltage is within the range specified in the *Electrical Characteristics*. The supply voltage sets the device electrical characteristics of the device, as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LVC1G34 plus the maximum supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74LVC1G34 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74LVC1G34 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the [CMOS Power Consumption and Cpd Calculation application note](#).

Thermal increase can be calculated using the information provided in the [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#).

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross to be considered a logic LOW, and to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LVC1G34 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10k Ω resistor value is often used due to these factors.

Refer to the *Feature Description* for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

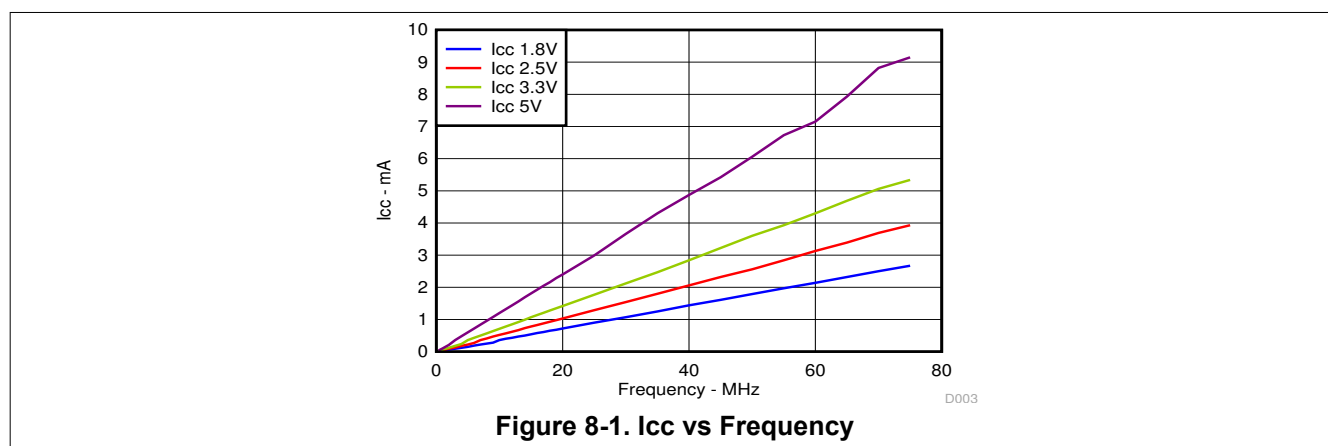
Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.1.4 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Verify that the capacitive load at the output is $\leq 50\text{pF}$. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LVC1G34 to one or more of the receiving devices.
3. Verify that the resistive load at the output is larger than $(V_{CC} / I_{O(max)})\Omega$. Doing this prevents the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in $M\Omega$; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the [CMOS Power Consumption and Cpd Calculation application note](#).

8.2.2 Application Curves



8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance.

A $0.1\mu\text{F}$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1\mu\text{F}$ and $1\mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

- Bypass capacitor placement
 - Place near the positive supply terminal of the device
 - Provide an electrically short ground return path
 - Use wide traces to minimize impedance
 - Keep the device, capacitors, and traces on the same side of the board whenever possible
- Signal trace geometry
 - 8mil to 12mil trace width
 - Lengths less than 12cm to minimize transmission line effects
 - Avoid 90° corners for signal traces
 - Use an unbroken ground plane below signal traces
 - Flood fill areas around signal traces with ground
 - Parallel traces must be separated by at least 3x dielectric thickness
 - For traces longer than 12cm
 - Use impedance controlled traces
 - Source-terminate using a series damping resistor near the output
 - Avoid branches; buffer each signal that must branch separately

8.4.2 Layout Example

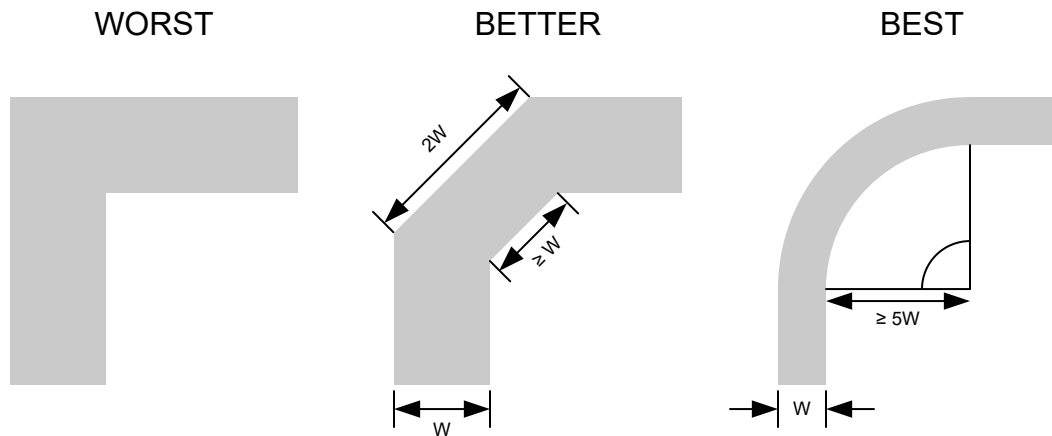


Figure 8-2. Example Trace Corners for Improved Signal Integrity

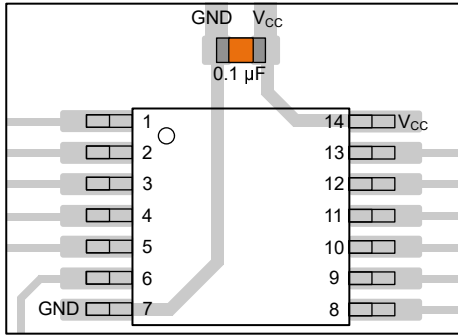


Figure 8-3. Example Bypass Capacitor Placement for TSSOP and Similar Packages



Figure 8-4. Example Bypass Capacitor Placement for WQFN and Similar Packages

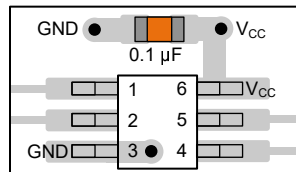


Figure 8-5. Example Bypass Capacitor Placement for SOT, SC70 and Similar Packages

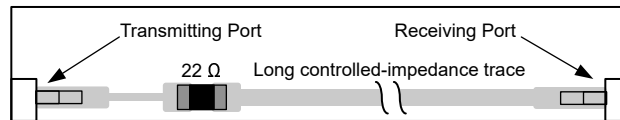


Figure 8-6. Example Damping Resistor Placement for Improved Signal Integrity

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CMOS Power Consumption and \$C_{pd}\$ Calculation application note](#)
- Texas Instruments, [Designing With Logic application note](#)
- Texas Instruments, [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices application note](#)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision N (June 2025) to Revision O (October 2025) | Page |
|---|-------------|
| • Changed Junction-to-ambient thermal resistance value for DCK package from: 278°C/W to: 371.0°C/W | 5 |
| • Changed Junction-to-case (top) thermal resistance value for DCK package from: 93°C/W to: 297.5°C/W..... | 5 |
| • Changed Junction-to-board thermal resistance value for DCK package from: 65°C/W to: 258.6°C/W..... | 5 |
| • Changed Junction-to-top characterization value for DCK package from: 2°C/W to: 195.6°C/W..... | 5 |
| • Changed Junction-to-board characterization value for DCK package from: 64°C/W to: 256.2°C/W..... | 5 |

| Changes from Revision M (April 2016) to Revision N (June 2025) | Page |
|---|-------------|
| • Updated the numbering format for tables, figures, and cross-references throughout the document..... | 1 |
| • Changed <i>Device Information</i> table to <i>Package Information</i> | 1 |
| • Changed Junction-to-ambient thermal resistance value for DBV package from: 229°C/W to: 357.1°C/W | 5 |
| • Changed Junction-to-case (top) thermal resistance value for DBV package from: 164°C/W to: 263.7°C/W | 5 |
| • Changed Junction-to-board thermal resistance value for DBV package from: 62°C/W to: 264.4°C/W | 5 |
| • Changed Junction-to-top characterization value for DBV package from: 44°C/W to: 195.6°C/W | 5 |
| • Changed Junction-to-board characterization value for DBV package from: 62°C/W to: 262.2°C/W | 5 |

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---|
| SN74LVC1G34DBVR | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | (3O3H, C345, C34F, C34J, C34K, C 34R) (C34H, C34P, C34S) |
| SN74LVC1G34DBVR.A | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (3O3H, C345, C34F, C34J, C34K, C 34R) (C34H, C34P, C34S) |
| SN74LVC1G34DBVR.B | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (3O3H, C345, C34F, C34J, C34K, C 34R) (C34H, C34P, C34S) |
| SN74LVC1G34DBVRE4 | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C345 C34S |
| SN74LVC1G34DBVRG4 | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C345 C34S |
| SN74LVC1G34DBVRG4.B | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C345 C34S |
| SN74LVC1G34DBVT | Active | Production | SOT-23 (DBV) 5 | 250 SMALL T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | (C345, C34J, C34K, C34R) (C34H, C34S) |
| SN74LVC1G34DBVT.B | Active | Production | SOT-23 (DBV) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C345, C34J, C34K, C34R) (C34H, C34S) |
| SN74LVC1G34DBVTE4 | Active | Production | SOT-23 (DBV) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C345 C34S |
| SN74LVC1G34DBVTG4 | Active | Production | SOT-23 (DBV) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C345 C34S |
| SN74LVC1G34DBVTG4.B | Active | Production | SOT-23 (DBV) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C345 C34S |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------------|---------------|----------------------|-------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---|
| SN74LVC1G34DCKR | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | (C95, C9F, C9J, C9R) (C9H, C9P, C9S) |
| SN74LVC1G34DCKR.A | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (C95, C9F, C9J, C9R) (C9H, C9P, C9S) |
| SN74LVC1G34DCKR.B | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | SN | Level-1-260C-UNLIM | -40 to 125 | (C95, C9F, C9J, C9R) (C9H, C9P, C9S) |
| SN74LVC1G34DCKRE4 | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C95 C9S |
| SN74LVC1G34DCKRG4 | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C95 C9S |
| SN74LVC1G34DCKRG4.A | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C95 C9S |
| SN74LVC1G34DCKRG4.B | Active | Production | SC70 (DCK) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C95 C9S |
| SN74LVC1G34DCKT | Active | Production | SC70 (DCK) 5 | 250 SMALL T&R | Yes | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | (C95, C9J, C9R) (C9H, C9S) |
| SN74LVC1G34DCKT.B | Active | Production | SC70 (DCK) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (C95, C9J, C9R) (C9H, C9S) |
| SN74LVC1G34DCKTG4 | Active | Production | SC70 (DCK) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C95 C9S |
| SN74LVC1G34DCKTG4.B | Active | Production | SC70 (DCK) 5 | 250 SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C95 C9S |
| SN74LVC1G34DPWR | Active | Production | X2SON (DPW) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | P4 |
| SN74LVC1G34DPWR.B | Active | Production | X2SON (DPW) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | P4 |
| SN74LVC1G34DRLR | Active | Production | SOT-5X3 (DRL) 5 | 4000 LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | (C97, C9R) |
| SN74LVC1G34DRLR.B | Active | Production | SOT-5X3 (DRL) 5 | 4000 LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | (C97, C9R) |
| SN74LVC1G34DRYR | Active | Production | SON (DRY) 6 | 5000 LARGE T&R | Yes | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | C9 |
| SN74LVC1G34DRYR.B | Active | Production | SON (DRY) 6 | 5000 LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | C9 |
| SN74LVC1G34DRYRG4 | Active | Production | SON (DRY) 6 | 5000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C9 |
| SN74LVC1G34DRYRG4.B | Active | Production | SON (DRY) 6 | 5000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C9 |
| SN74LVC1G34DSFR | Active | Production | SON (DSF) 6 | 5000 LARGE T&R | Yes | NIPDAU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | C9 |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| SN74LVC1G34DSFR.B | Active | Production | SON (DSF) 6 | 5000 LARGE T&R | Yes | NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | C9 |
| SN74LVC1G34DSFRG4 | Active | Production | SON (DSF) 6 | 5000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C9 |
| SN74LVC1G34DSFRG4.B | Active | Production | SON (DSF) 6 | 5000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | C9 |
| SN74LVC1G34YFPR | Active | Production | DSBGA (YFP) 4 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | C9 N |
| SN74LVC1G34YFPR.B | Active | Production | DSBGA (YFP) 4 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | C9 N |
| SN74LVC1G34YZPR | Active | Production | DSBGA (YZP) 5 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | C9N |
| SN74LVC1G34YZPR.B | Active | Production | DSBGA (YZP) 5 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | C9N |
| SN74LVC1G34YZVR | Active | Production | DSBGA (YZV) 4 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | C9 N |
| SN74LVC1G34YZVR.B | Active | Production | DSBGA (YZV) 4 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | C9 N |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G34 :

- Automotive : [SN74LVC1G34-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC1G34DBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DBVRG4 | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.2 | 3.3 | 3.23 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.3 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DBVTG4 | SOT-23 | DBV | 5 | 250 | 178.0 | 9.2 | 3.3 | 3.23 | 1.55 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 8.4 | 2.25 | 2.45 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DCKRG4 | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DCKT | SC70 | DCK | 5 | 250 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DCKTG4 | SC70 | DCK | 5 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DPWR | X2SON | DPW | 5 | 3000 | 178.0 | 8.4 | 0.91 | 0.91 | 0.5 | 2.0 | 8.0 | Q3 |
| SN74LVC1G34DRLR | SOT-5X3 | DRL | 5 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74LVC1G34DRYR | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| SN74LVC1G34DRYRG4 | SON | DRY | 6 | 5000 | 180.0 | 9.5 | 1.15 | 1.6 | 0.75 | 4.0 | 8.0 | Q1 |
| SN74LVC1G34DSFR | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC1G34DSFRG4 | SON | DSF | 6 | 5000 | 180.0 | 9.5 | 1.16 | 1.16 | 0.5 | 4.0 | 8.0 | Q2 |
| SN74LVC1G34YFPR | DSBGA | YFP | 4 | 3000 | 178.0 | 9.2 | 0.89 | 0.89 | 0.58 | 4.0 | 8.0 | Q1 |
| SN74LVC1G34YZPR | DSBGA | YZP | 5 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |
| SN74LVC1G34YZVR | DSBGA | YZV | 4 | 3000 | 178.0 | 9.2 | 1.0 | 1.0 | 0.63 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC1G34DBVR | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| SN74LVC1G34DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| SN74LVC1G34DBVRG4 | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G34DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G34DBVTG4 | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G34DCKR | SC70 | DCK | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| SN74LVC1G34DCKRG4 | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G34DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G34DCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G34DCKT | SC70 | DCK | 5 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G34DCKTG4 | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1G34DPWR | X2SON | DPW | 5 | 3000 | 205.0 | 200.0 | 33.0 |
| SN74LVC1G34DRLR | SOT-5X3 | DRL | 5 | 4000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1G34DRYR | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G34DRYRG4 | SON | DRY | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G34DSFR | SON | DSF | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G34DSFRG4 | SON | DSF | 6 | 5000 | 184.0 | 184.0 | 19.0 |
| SN74LVC1G34YFPR | DSBGA | YFP | 4 | 3000 | 220.0 | 220.0 | 35.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC1G34YZPR | DSBGA | YZP | 5 | 3000 | 220.0 | 220.0 | 35.0 |
| SN74LVC1G34YZVR | DSBGA | YZV | 4 | 3000 | 220.0 | 220.0 | 35.0 |

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRY 6

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G

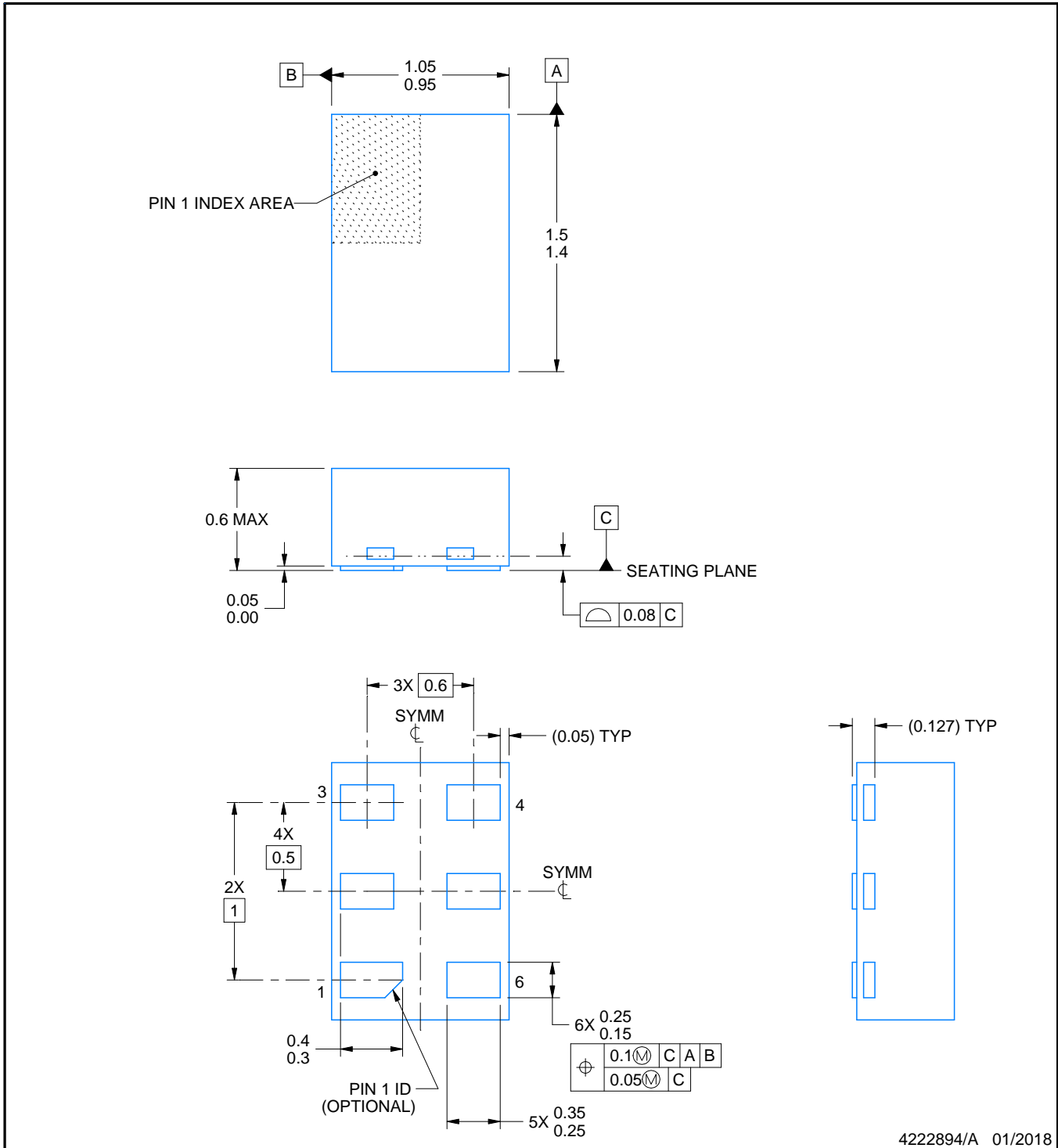
DRY0006A



PACKAGE OUTLINE

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/sluea271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

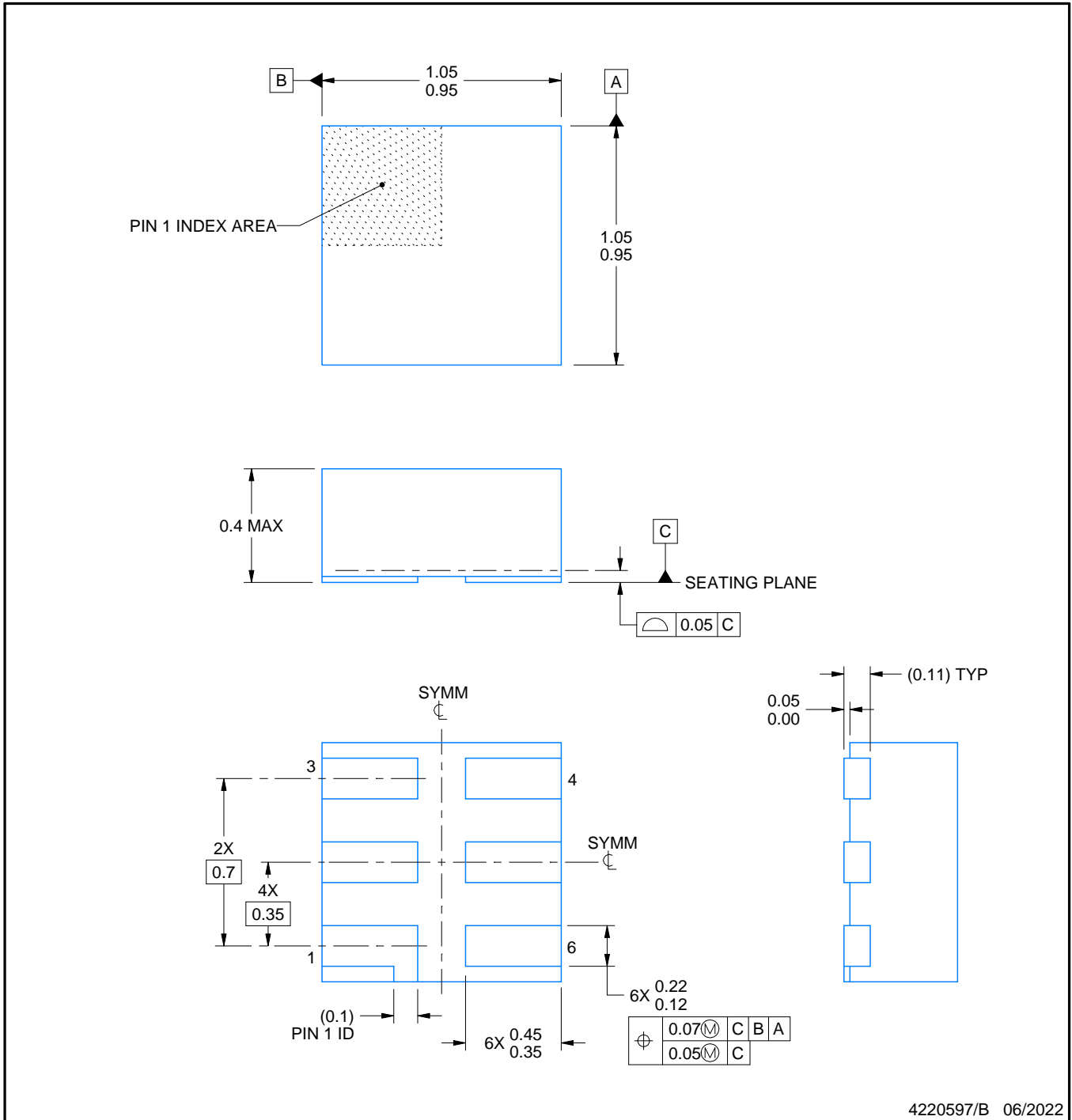


DSF0006A

PACKAGE OUTLINE

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220597/B 06/2022

NOTES:

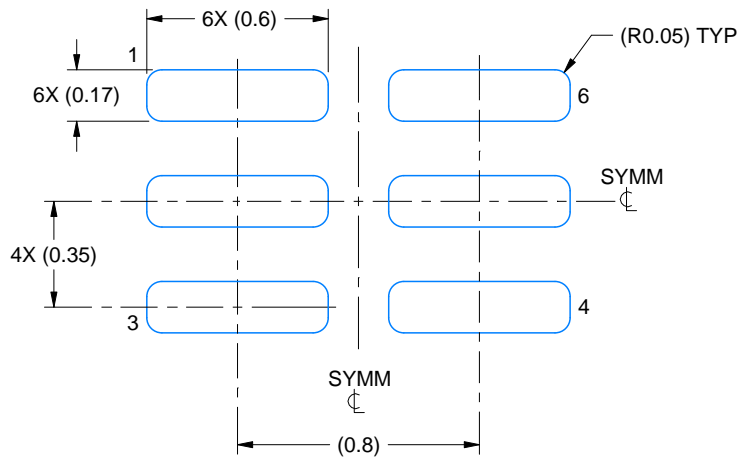
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

EXAMPLE BOARD LAYOUT

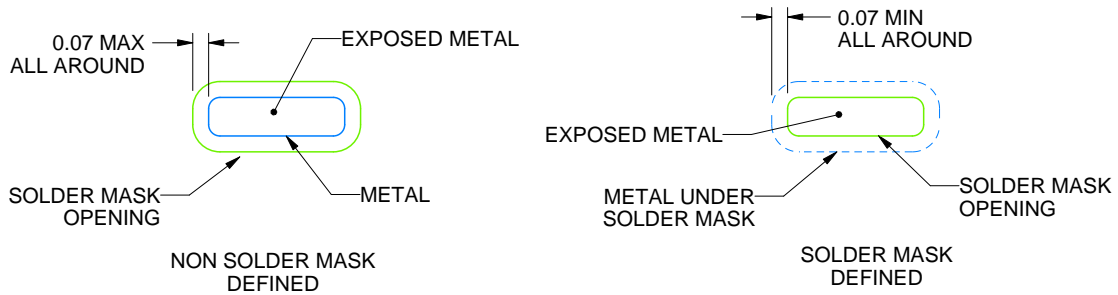
DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

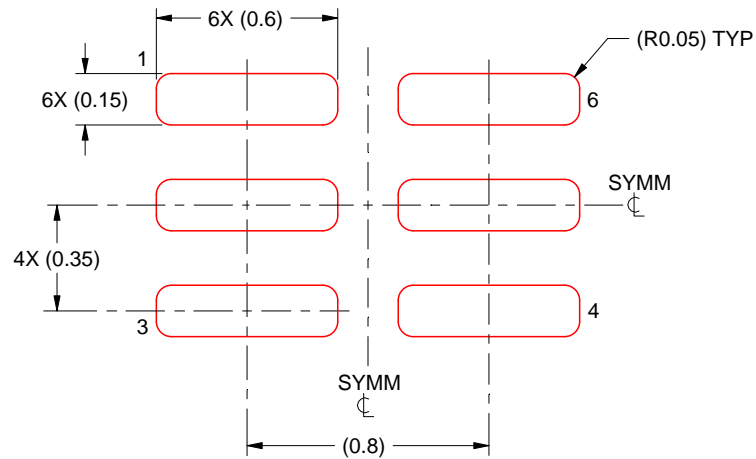
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

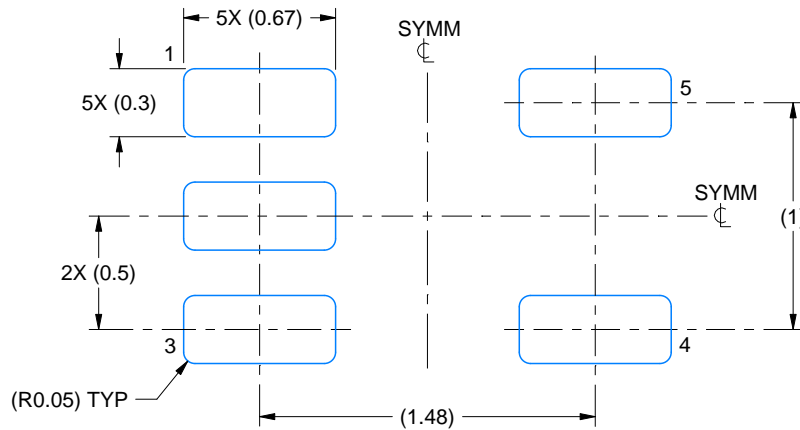
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

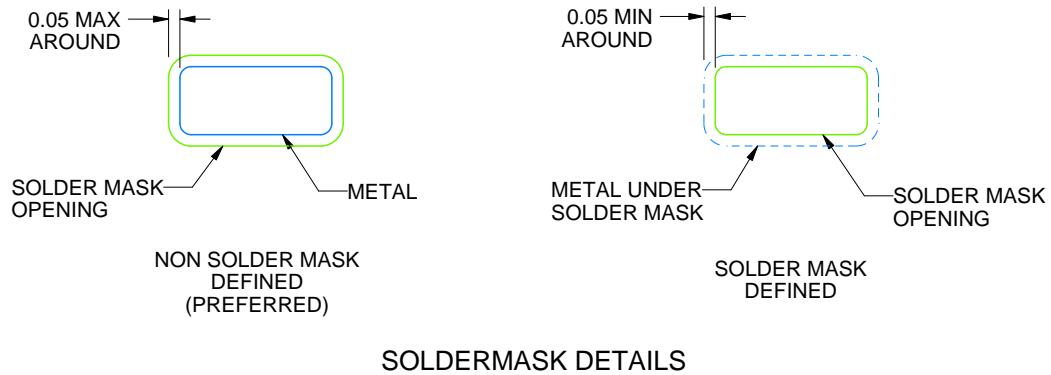
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

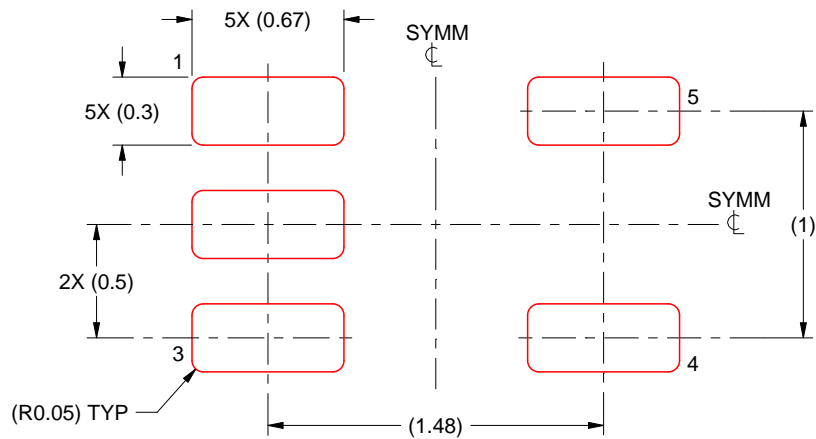
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5

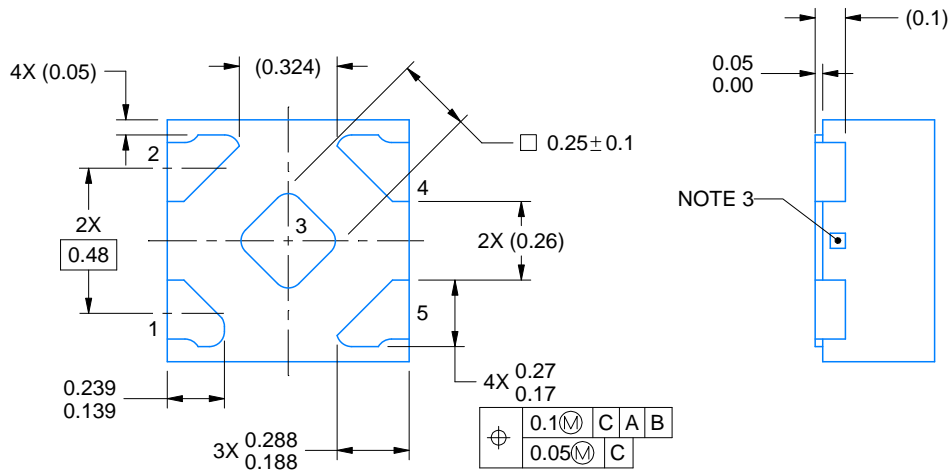
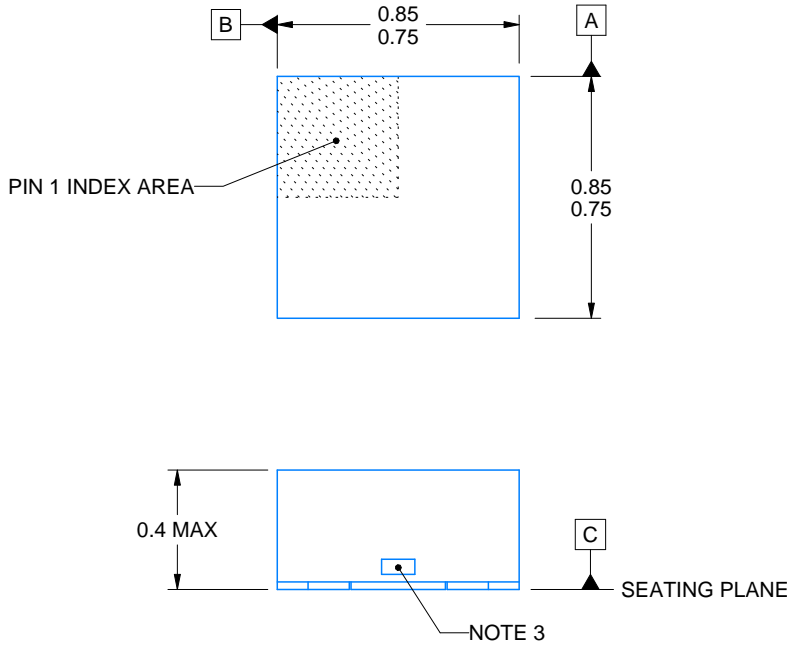
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4211218-3/D



4223102/D 03/2022

NOTES:

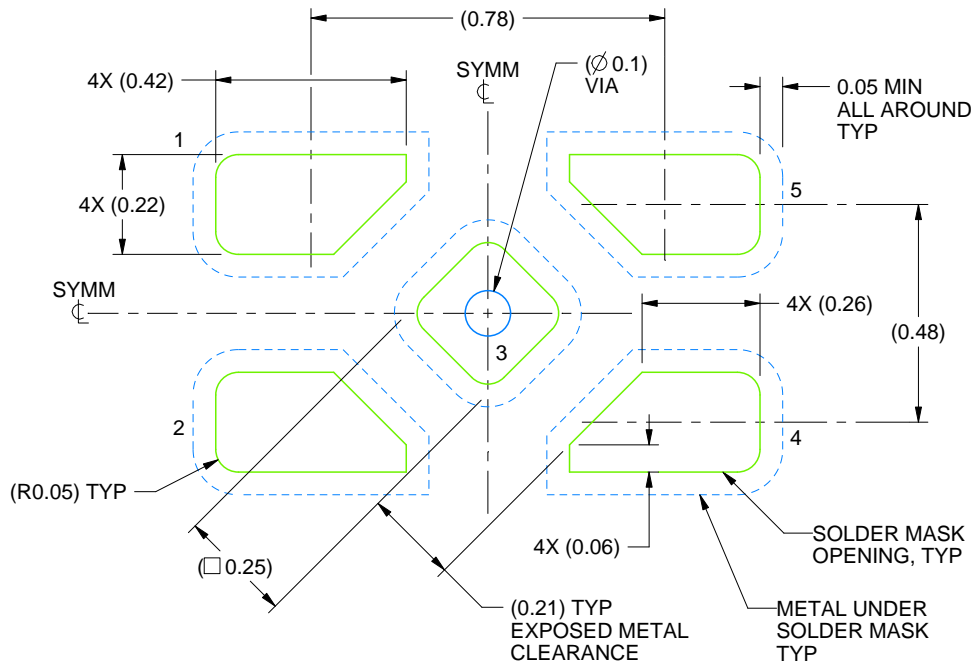
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

EXAMPLE BOARD LAYOUT

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

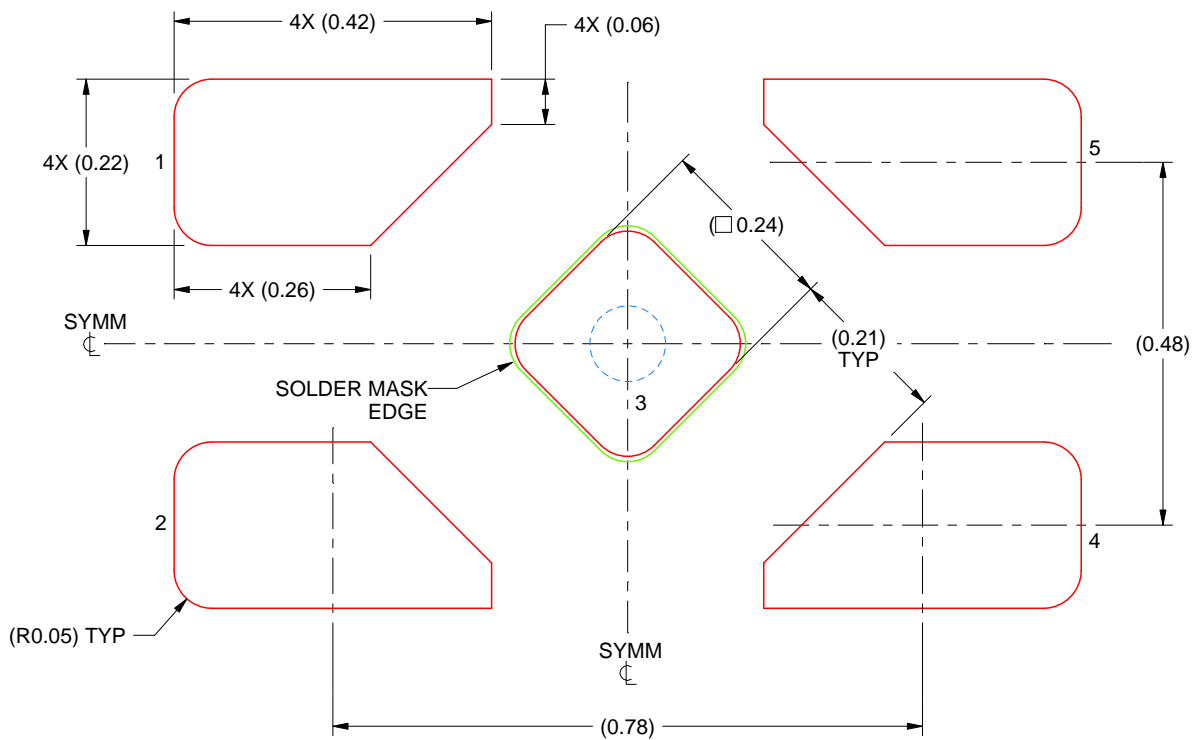
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/sl原因271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

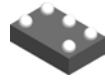
EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

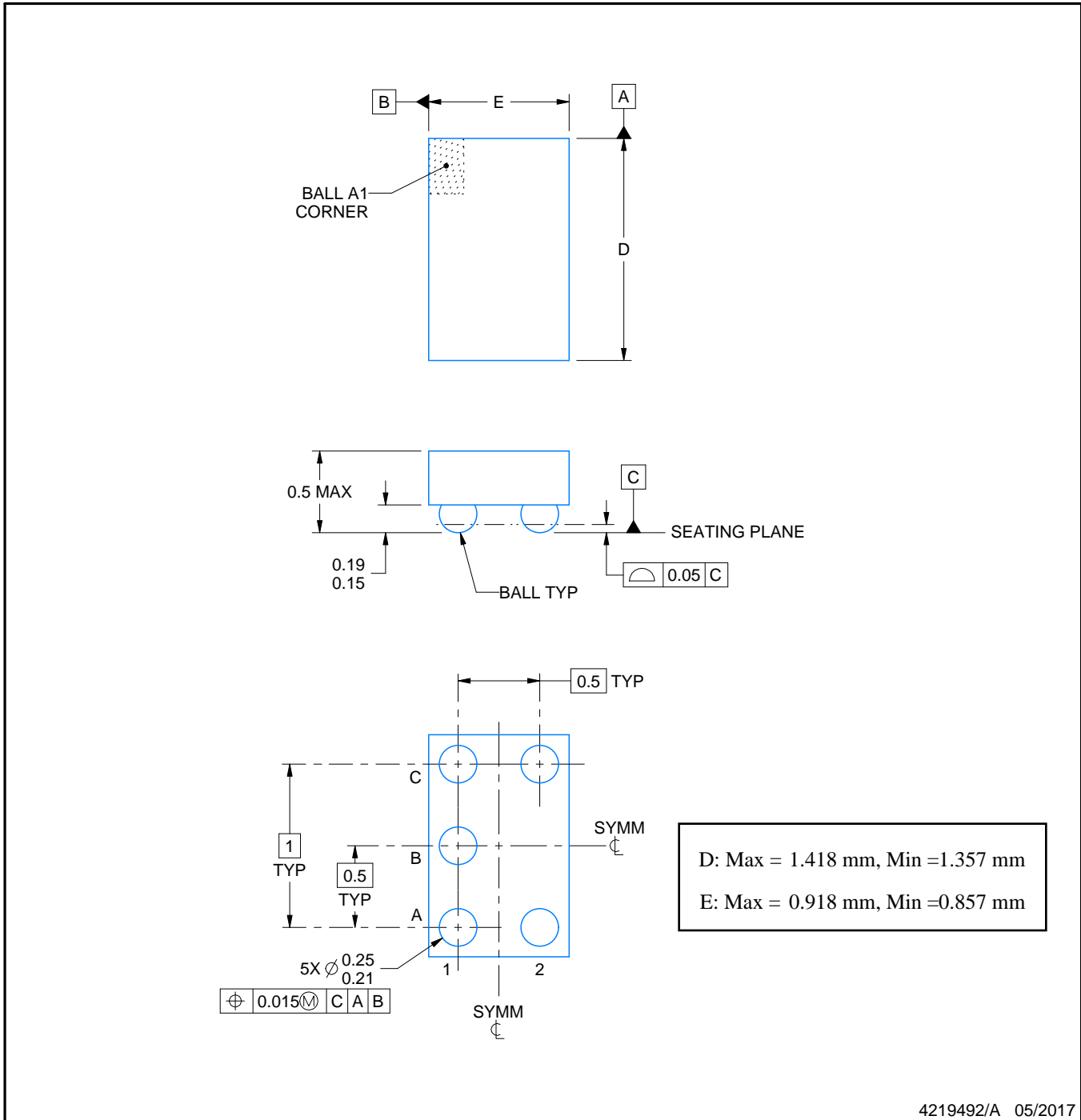
YZP0005



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

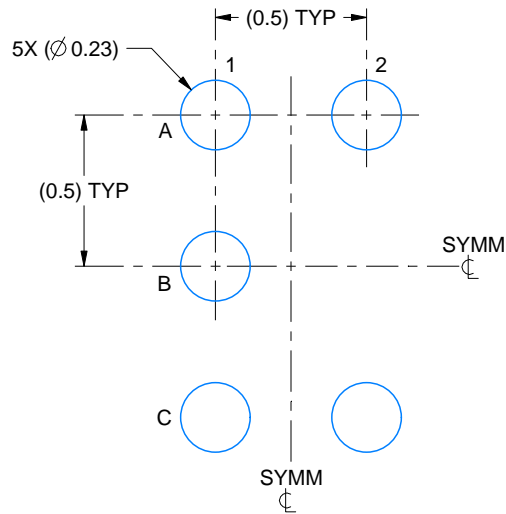
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

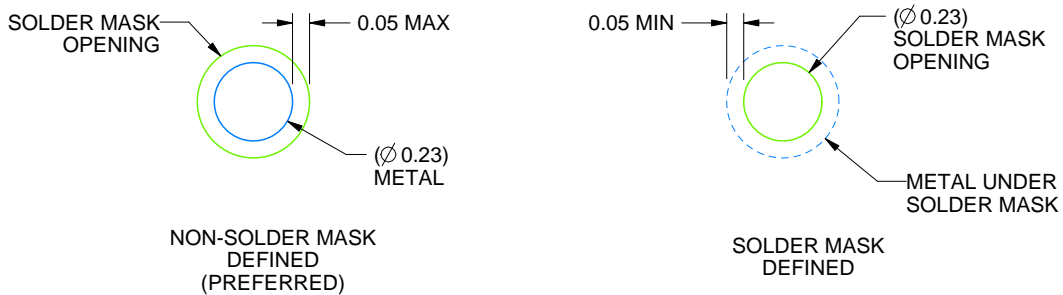
YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

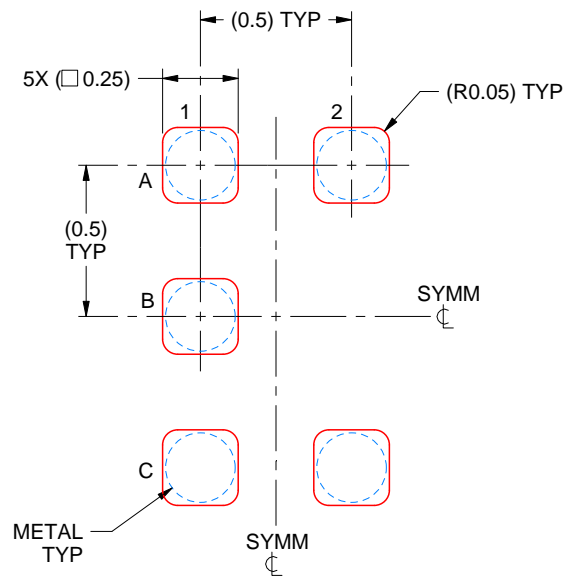
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

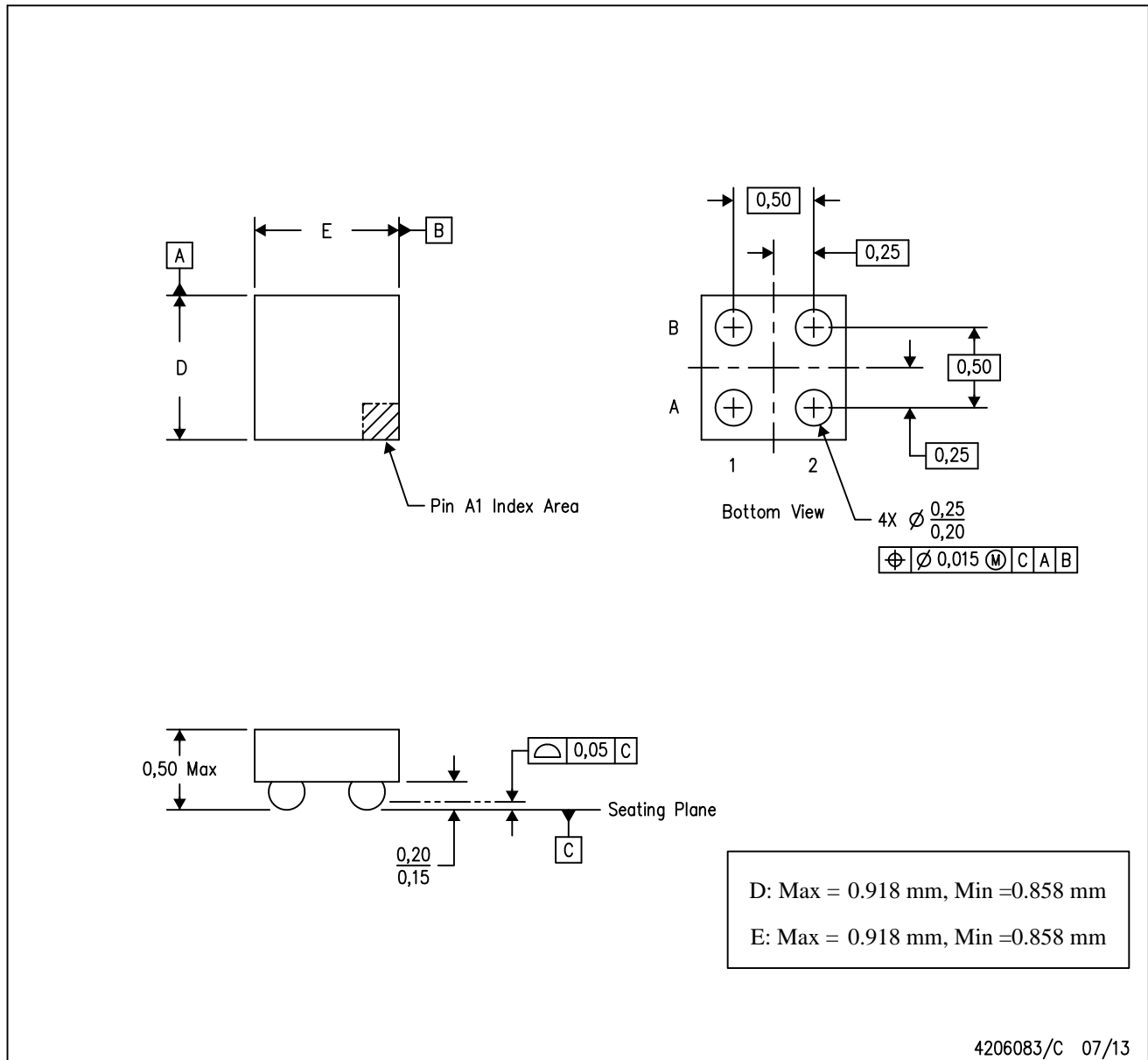
4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

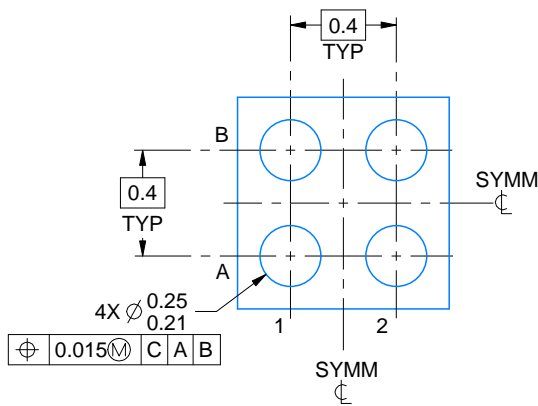
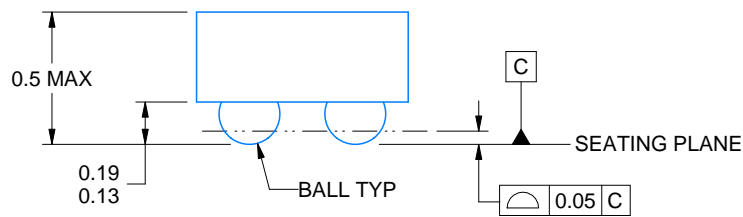
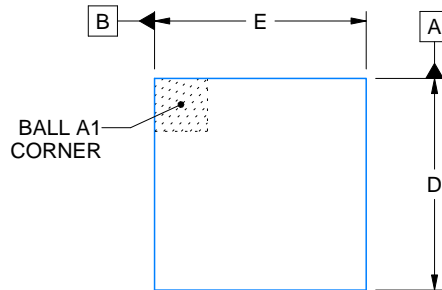
YZV (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.



D: Max = 0.79 mm, Min = 0.73 mm
 E: Max = 0.79 mm, Min = 0.73 mm

4223507/A 01/2017

NOTES:

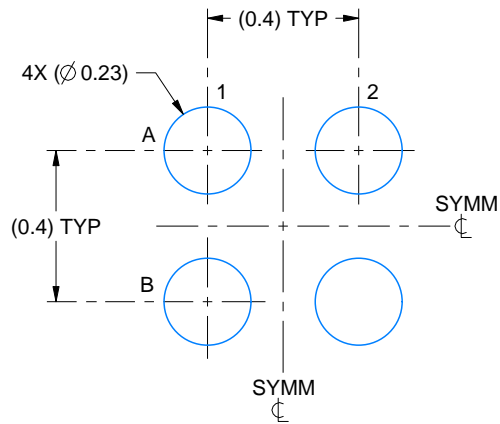
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

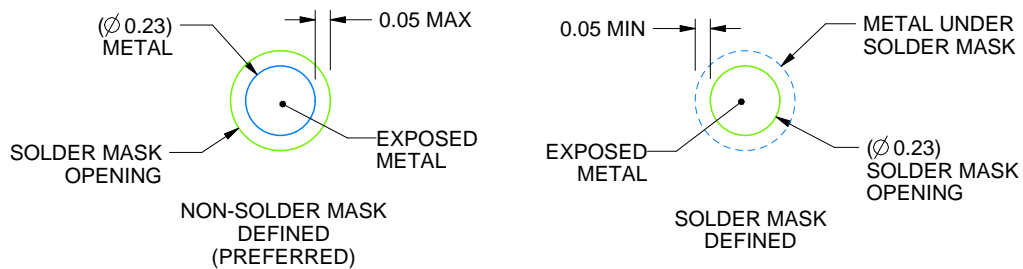
YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

4223507/A 01/2017

NOTES: (continued)

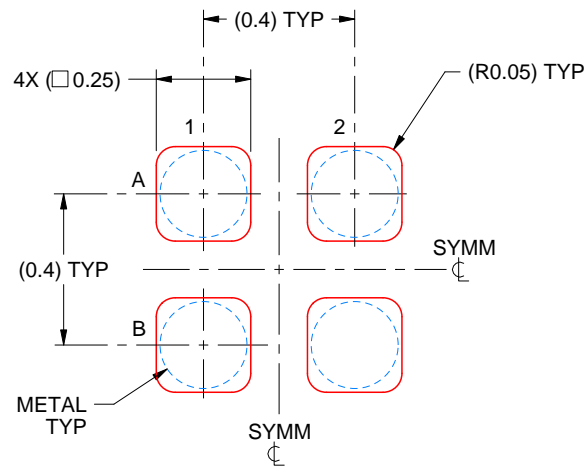
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFP0004

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223507/A 01/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

- Publication IPC-7351 may have alternate designs.
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE: 18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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