SN74LVC1G80 Single Positive-Edge-Triggered D-Type Flip-Flop

1 Features

- Available in the Texas Instruments NanoFree™ package
- Latch-up performance exceeds 100mA per JESD 78, Class II
- Supports 5V V_{CC} operation
- Inputs accept voltages to 5.5V
- Supports down translation to V_{CC}
- Maximum t_{pd} of 4.2ns at 3.3V
- Low power consumption, 10µA maximum I_{CC}
- ±24mA output drive at 3.3V
- I_{off} supports partial-power-down mode and back-drive protection
- Latch-up performance exceeds 100mA per JESD 78, Class II

2 Applications

- Test and measurement
- Enterprise switching
- Telecom infrastructure
- Personal electronics
- White goods

3 Description

The SN74LVC1G80 device is a single positive-edge-triggered D-type flip-flop that is designed for 1.65V to 5.5V V_{CC} operation.

When data at the data (D) input meets the setup time requirement, the data is transferred to the $\overline{Q}$ output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the level at the output.

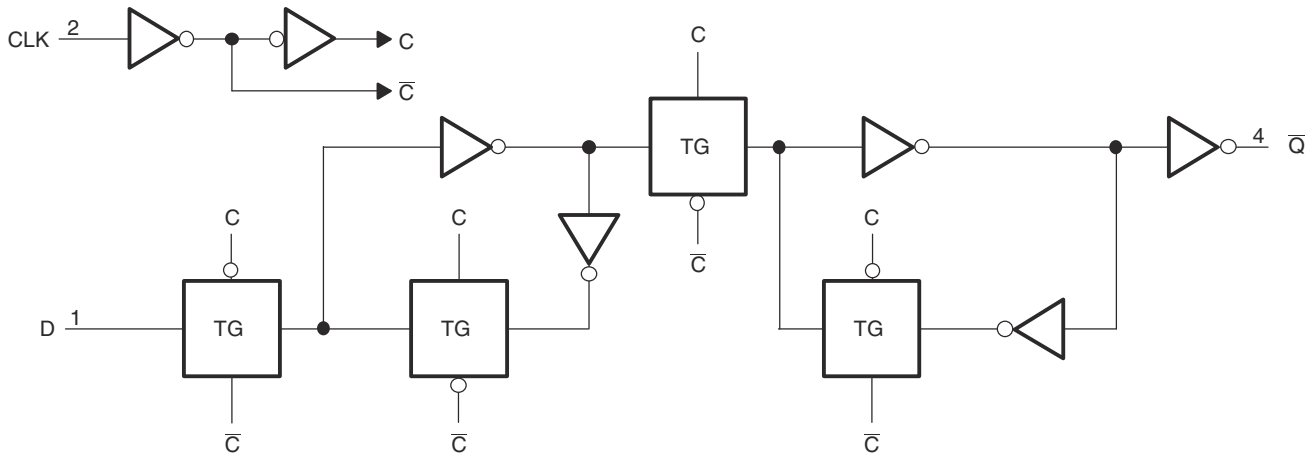
NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN74LVC1G80DBV	SOT-23 (5)	2.90mm × 1.60mm
SN74LVC1G80DCK	SC70 (5)	2.00mm × 1.25mm
SN74LVC1G80YZP	DSBGA (5)	1.41mm × 0.91mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



A. TG - Transmission Gate

Logic Diagram (Positive Logic)

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4 Pin Configuration and Functions

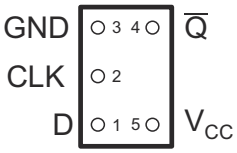


Figure 4-1. YZP Package 5-Pin DSBGA Bottom View

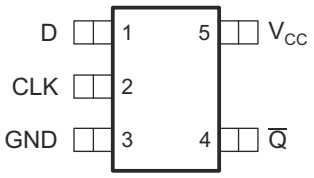


Figure 4-2. DCK Package 5-Pin SC70 Top View

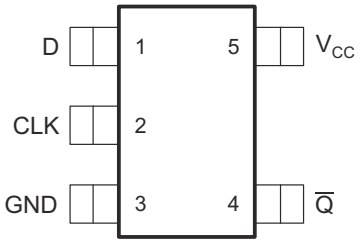


Figure 4-3. DBV Package 5-Pin SOT-23 Top View

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
CLK	2	I	Positive-Edge-Triggered Clock input
D	1	I	Data input
GND	3	—	Ground pin
$\overline{Q}$	4	O	Inverted output
V_{CC}	5	—	Positive Supply

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6.5	V
V_I	Input voltage(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high-impedance or power-off state(2)		–0.5	6.5	V
V_O	Voltage applied to any output in the high or low state(2) (3)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input negative-voltage and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
(3) The value of V_{CC} is provided in *Section 5.3*.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65V to 1.95V	0.65 × V_{CC}		V
		V_{CC} = 2.3V to 2.7V	1.7		
		V_{CC} = 3V to 3.6V	2		
		V_{CC} = 4.5V to 5.5V	0.7 × V_{CC}		
V_{IL}	Low-level input voltage	V_{CC} = 1.65V to 1.95V		0.35 × V_{CC}	V
		V_{CC} = 2.3V to 2.7V		0.7	
		V_{CC} = 3V to 3.6V		0.8	
		V_{CC} = 4.5V to 5.5V		0.3 × V_{CC}	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65V		–4	mA
		V_{CC} = 2.3V		–8	
		V_{CC} = 3V		–16	
				–24	
		V_{CC} = 4.5V		–32	
I_{OL}	Low-level output current	V_{CC} = 1.65V		4	mA
		V_{CC} = 2.3V		8	
		V_{CC} = 3V		16	
				24	
		V_{CC} = 4.5V		32	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 1.8V ± 0.15V, 2.5V ± 0.2V		20	ns/V
		V_{CC} = 3.3V ± 0.3V		10	
		V_{CC} = 5V ± 0.5V		5	
T_J	Junction temperature			150	°C
T_A	Operating free-air temperature	DBV and DCK packages	–40	125	°C
		YZP package	–40	85	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application note, *Implications of Slow or Floating CMOS Inputs*.

5.4 Thermal Information

PACKAGE	PINS	THERMAL METRIC(1)						UNIT
		$R_{\theta JA}$	$R_{\theta JC(top)}$	$R_{\theta JB}$	Ψ_{JT}	Ψ_{JB}	$R_{\theta JC(bot)}$	
DBV (SOT-23)	5	357.1	263.7	264.4	195.6	262.2	-	°C/W
DCK (SOT-SC70)	5	371	297.5	258.6	195.6	256.2	-	°C/W
YZP (DSBGA)	5	136.9	1.3	32.6	6.3	32.6	-	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}	I_{OH} = –100µA	1.65V to 5.5V	V_{CC} – 0.1			V
	I_{OH} = –4mA	1.65V	1.2			
	I_{OH} = –8mA	2.3V	1.9			
	I_{OH} = –16mA	3V	2.4			
	I_{OH} = –24mA		2.3			
	I_{OH} = –32mA	4.5V	3.8			
V_{OL}	I_{OL} = 100µA	1.65V to 5.5V			0.1	V
	I_{OL} = 4mA	1.65V			0.45	
	I_{OL} = 8mA	2.3V			0.3	
	I_{OL} = 16mA	3V			0.4	
	I_{OL} = 24mA				0.55	
	I_{OL} = 32mA	4.5V			0.55	
I_I CLK or D inputs	V_I = 5.5V or GND	0 to 5.5V			±10	µA
I_{off}	V_I or V_O = 5.5V	0			±10	µA
I_{CC}	V_I = 5.5V or GND, I_O = 0	1.65V to 5.5V			10	µA
ΔI_{CC}	One input at V_{CC} – 0.6V, Other inputs at V_{CC} or GND	3V to 5.5V			500	µA
C_i	V_I = V_{CC} or GND, T_A = –40°C to 85°C	3.3V		3.5		pF

(1) All typical values are at V_{CC} = 3.3V, T_A = 25°C.

5.6 Timing Requirements: T_A = –40°C to +85°C

over recommended operating free-air temperature range, T_A = –40°C to +85°C (unless otherwise noted) (see Figure 6-1)

			V_{CC}	MIN	MAX	UNIT
f_{clock}	Clock frequency		V_{CC} = 1.8V ± 0.15V		160	MHz
			V_{CC} = 2.5V ± 0.2V			
			V_{CC} = 3.3V ± 0.3V			
			V_{CC} = 5.5V ± 0.5V			
t_w	Pulse duration, CLK high or low		V_{CC} = 1.8V ± 0.15V	2.5		ns
			V_{CC} = 2.5V ± 0.2V			
			V_{CC} = 3.3V ± 0.3V			
			V_{CC} = 5.5V ± 0.5V			
t_{su}	Setup time before CLK↑	Data high	V_{CC} = 1.8V ± 0.15V	2.3		ns
			V_{CC} = 2.5V ± 0.2V	1.5		
			V_{CC} = 3.3V ± 0.3V	1.3		
			V_{CC} = 5.5V ± 0.5V	1.1		
		Data low	V_{CC} = 1.8V ± 0.15V	2.5		
			V_{CC} = 2.5V ± 0.2V	1.5		
			V_{CC} = 3.3V ± 0.3V	1.3		
			V_{CC} = 5.5V ± 0.5V	1.1		
t_h	Hold time, data after CLK↑		V_{CC} = 1.8V ± 0.15V	0		ns
			V_{CC} = 2.5V ± 0.2V	0.2		
			V_{CC} = 3.3V ± 0.3V	0.9		
			V_{CC} = 5.5V ± 0.5V	0.4		

5.7 Timing Requirements: T_A = –40°C to +125°C

over recommended operating free-air temperature range, T_A = –40°C to +125°C (unless otherwise noted) (see Figure 6-1)

			V_{CC}	MIN	MAX	UNIT
f_{clock}	Clock frequency		V_{CC} = 1.8V ± 0.15V		160	MHz
			V_{CC} = 2.5V ± 0.2V			
			V_{CC} = 3.3V ± 0.3V			
			V_{CC} = 5.5V ± 0.5V			
t_w	Pulse duration, CLK high or low		V_{CC} = 1.8V ± 0.15V	2.5		ns
			V_{CC} = 2.5V ± 0.2V			
			V_{CC} = 3.3V ± 0.3V			
			V_{CC} = 5.5V ± 0.5V			
t_{su}	Setup time before CLK↑	Data high	V_{CC} = 1.8V ± 0.15V	2.3		ns
			V_{CC} = 2.5V ± 0.2V	1.5		
			V_{CC} = 3.3V ± 0.3V	1.3		
			V_{CC} = 5.5V ± 0.5V	1.1		
		Data low	V_{CC} = 1.8V ± 0.15V	2.5		
			V_{CC} = 2.5V ± 0.2V	1.5		
			V_{CC} = 3.3V ± 0.3V	1.3		
			V_{CC} = 5.5V ± 0.5V	1.1		
t_h	Hold time, data after CLK↑		V_{CC} = 1.8V ± 0.15V	0		ns
			V_{CC} = 2.5V ± 0.2V	0.2		
			V_{CC} = 3.3V ± 0.3V	0.9		
			V_{CC} = 5.5V ± 0.5V	0.4		

5.8 Switching Characteristics: T_A = –40°C to +85°C, C_L = 15pF

over recommended operating free-air temperature range, T_A = –40°C to +85°C, C_L = 15pF (unless otherwise noted) (see Figure 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			V_{CC} = 1.8V ± 0.15V	160		MHz
			V_{CC} = 2.5V ± 0.2V			
			V_{CC} = 3.3V ± 0.3V			
			V_{CC} = 5V ± 0.5V			
t_{pd}	CLK	$\overline{Q}$	V_{CC} = 1.8V ± 0.15V	3	9.1	ns
			V_{CC} = 2.5V ± 0.2V	1.5	6	
			V_{CC} = 3.3V ± 0.3V	1.3	4.2	
			V_{CC} = 5V ± 0.5V	1.1	3.8	

5.9 Switching Characteristics: T_A = –40°C to +85°C, C_L = 30pF or 50pF

over recommended operating free-air temperature range, T_A = –40°C to +85°C, C_L = 30pF or 50pF (unless otherwise noted) (see Figure 6-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			V_{CC} = 1.8V ± 0.15V	160		MHz
			V_{CC} = 2.5V ± 0.2V			
			V_{CC} = 3.3V ± 0.3V			
			V_{CC} = 5V ± 0.5V			

over recommended operating free-air temperature range, T_A = –40°C to +85°C, C_L = 30pF or 50pF (unless otherwise noted) (see Figure 6-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
t_{pd}	CLK	$\overline{Q}$	V_{CC} = 1.8V ± 0.15V	4.4	9.9	ns
			V_{CC} = 2.5V ± 0.2V	2.3	7	
			V_{CC} = 3.3V ± 0.3V	2	5.2	
			V_{CC} = 5V ± 0.5V	1.3	4.5	

5.10 Switching Characteristics: T_A = –40°C to +125°C, C_L = 30pF or 50pF

over recommended operating free-air temperature range, T_A = –40°C to +125°C, C_L = 30pF or 50pF (unless otherwise noted) (see Figure 6-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	MAX	UNIT
f_{max}			V_{CC} = 1.8V ± 0.15V	160		MHz
			V_{CC} = 2.5V ± 0.2V			
			V_{CC} = 3.3V ± 0.3V			
			V_{CC} = 5V ± 0.5V			
t_{pd}	CLK	$\overline{Q}$	V_{CC} = 1.8V ± 0.15V	4.4	12.5	ns
			V_{CC} = 2.5V ± 0.2V	2.3	8.5	
			V_{CC} = 3.3V ± 0.3V	2	6	
			V_{CC} = 5V ± 0.5V	1.3	5.5	

5.11 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10MHz	V_{CC} = 1.8V	24	pF
			V_{CC} = 2.5V	24	
			V_{CC} = 3.3V	25	
			V_{CC} = 5V	27	

5.12 Typical Characteristics

This plot shows the different I_{CC} values for various voltages on the data input (D). Voltage sweep on the input is from 0V to 6.5V.

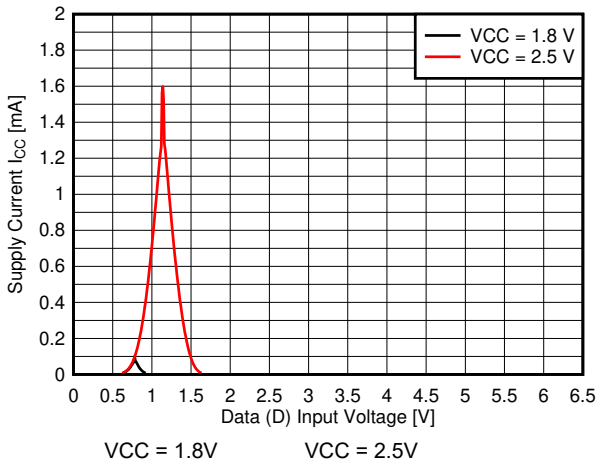


Figure 5-1. Supply Current (I_{CC}) vs Data (D) Input Voltage

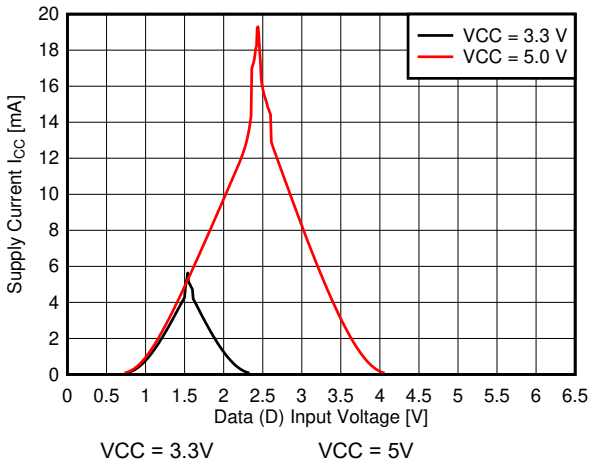
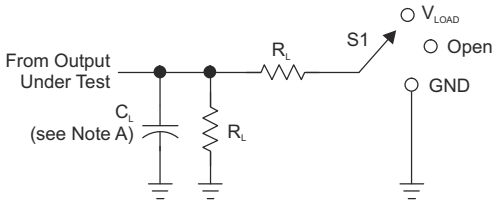


Figure 5-2. Supply Current (I_{CC}) vs Data (D) Input Voltage

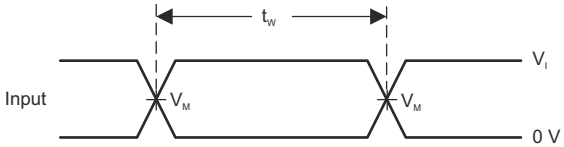
6 Parameter Measurement Information



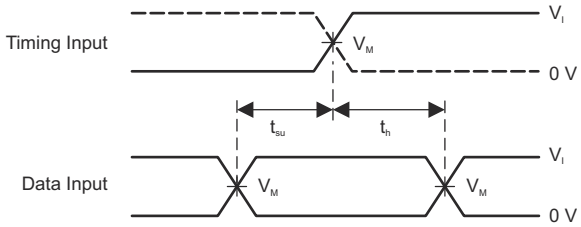
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

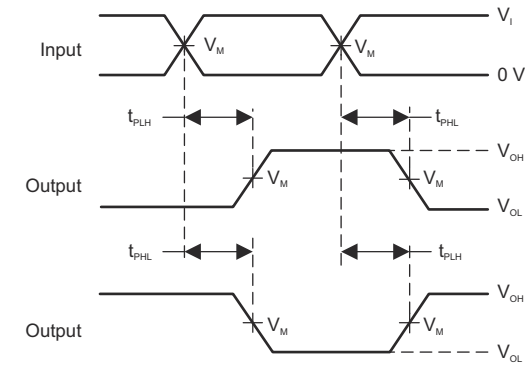
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	£2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MW	0.15 V
2.5 V ± 0.2 V	V_{CC}	£2 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MW	0.15 V
3.3 V ± 0.3 V	3 V	£2.5 ns	1.5 V	6 V	15 pF	1 MW	0.3 V
5 V ± 0.5 V	V_{CC}	£2.5 ns	$V_{CC}/2$	2 × V_{CC}	15 pF	1 MW	0.3 V



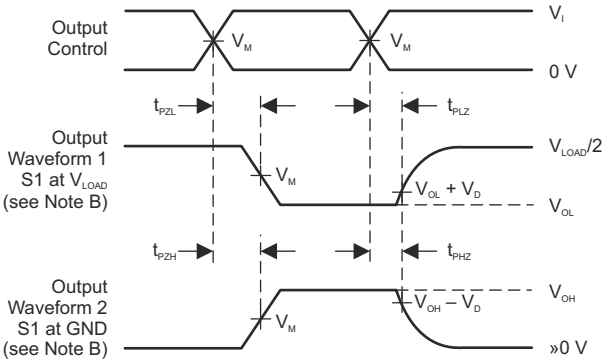
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



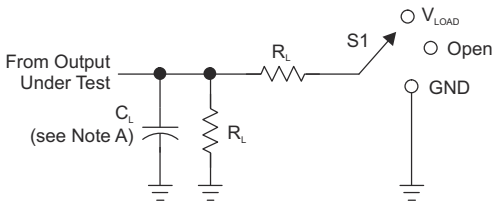
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR £ 10 MHz, Z_o = 50 W.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

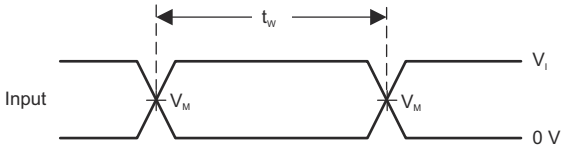
Figure 6-1. Load Circuit and Voltage Waveforms



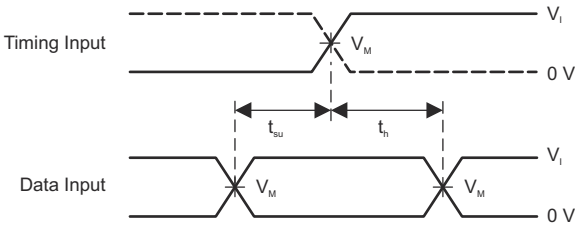
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

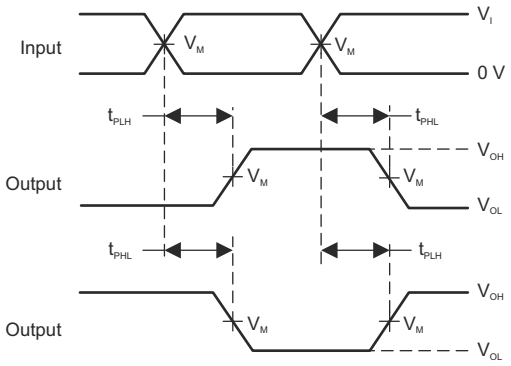
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	£2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kW	0.15 V
2.5 V ± 0.2 V	V_{CC}	£2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 W	0.15 V
3.3 V ± 0.3 V	3 V	£2.5 ns	1.5 V	6 V	50 pF	500 W	0.3 V
5 V ± 0.5 V	V_{CC}	£2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 W	0.3 V



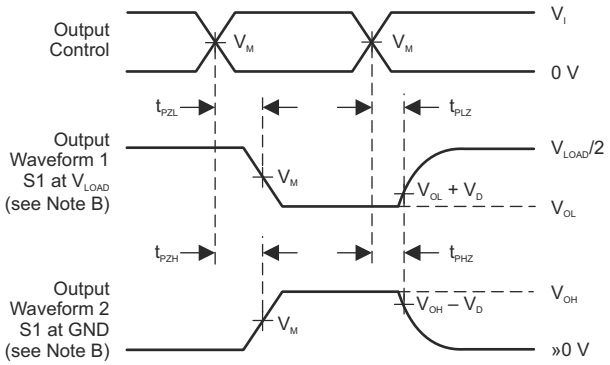
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR £ 10 MHz, Z_O = 50 W.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

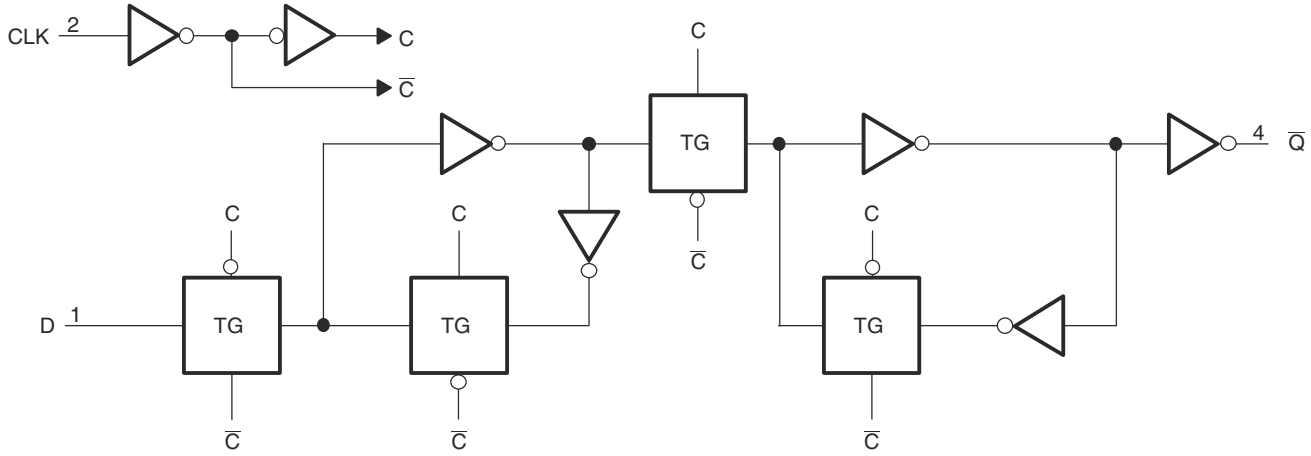
Figure 6-2. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74LVC1G80 is a single positive-edge-trigger D-type flip-flop . Data at the input (D) is transferred to the output ($\overline{Q}$) on the positive-going edge of the clock pulse when the setup time requirement is met. Because the clock triggering occurs at a voltage level, it is not directly related to the rise time of the clock pulse. This allows for data at the input to be changed without affecting the level at the output, following the hold-time interval.

7.2 Functional Block Diagram



Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions must be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. Limit the tower output of the device to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined the in the *Section 5.1* must be followed at all times.

7.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Section 5.5*. The worst case resistance is calculated with the maximum input voltage, given in the *Section 5.3*, and the maximum input leakage current, given in the *Section 5.5*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by Δt/Δv in *Section 5.3* to avoid excessive currents and oscillations. If tolerance to a slow or noisy input signal is required, a device with a Schmitt-trigger input must be used to condition the input signal prior to the standard CMOS input.

7.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Section 5.1* table can cause damage to the device. The input negative-voltage and output voltage ratings can be exceeded if the input and output clamp-current ratings are observed.

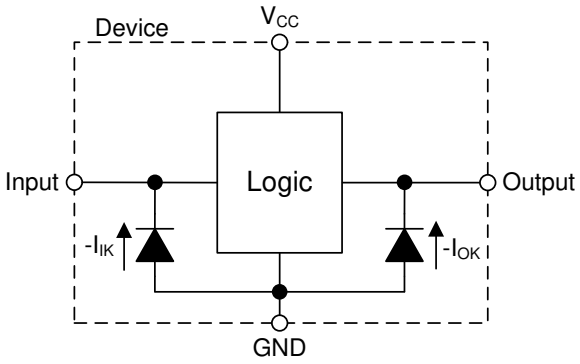


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.4 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Section 5.5*.

7.3.5 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Section 5.1*.

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74LVC1G80.

Table 7-1. Function Table

INPUTS		OUTPUT
CLK	D	$\overline{Q}$
↑	H	L
↑	L	H
L	X	Q_0

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

A useful application for the SN74LVC1G80 is using it as a frequency divider. By feeding back the output ($\overline{Q}$) to the input (D), the output will toggle on every rising edge of the clock waveform. The output goes HIGH once every two clock cycles so essentially the frequency of the clock signal is divided by a factor of two. The SN74LVC1G80 does not have preset or clear functions so the initial state of the output is unknown. This application implements the use of a microcontroller GPIO pin to initially set the input HIGH, so the output LOW. Initialization is not needed, but can be kept in mind. Post initialization, the GPIO pin is set to a high impedance mode. Depending on the microcontroller, the GPIO pin can be set to an input and used to monitor the clock division.

8.2 Typical Application

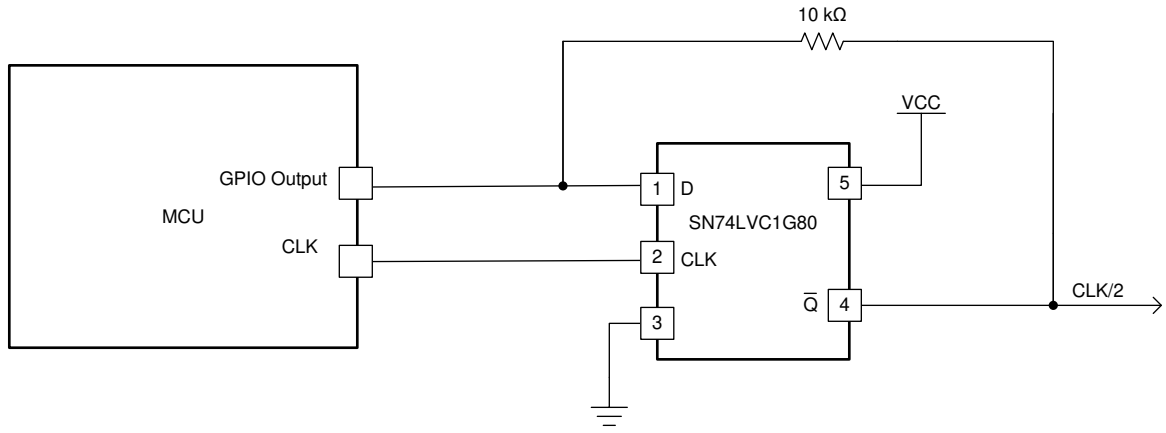


Figure 8-1. Clock Frequency Division

8.2.1 Design Requirements

For this application, a resistor needs to be placed on the feedback line for the initialization voltage from the microcontroller to overpower the signal coming from the output ($\overline{Q}$). Without it the state at the input will be challenged by the GPIO from the microcontroller and from the output of the SN74LVC1G80.

The SN74LVC1G80 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that exceed maximum limits.

8.2.2 Detailed Design Procedure

1. Recommended input conditions:
   - For rise time and fall time specifications, see Δt/Δv in *Section 5.3*.
   - For specified high and low levels, see V_{IH} and V_{IL} in *Section 5.3*.
   - Input voltages are recommended to not go below 0V and not exceed 5.5V for any V_{CC}. See *Section 5.3*.
2. Recommended output conditions:
   - Load currents must not exceed ±50mA. See *Section 5.1*.
   - Output voltages are recommended to not go below 0V and not exceed the V_{CC} voltage. See *Section 5.3*.
3. Feedback resistor:
   - A 10kΩ resistor is chosen here to bias the input so the microcontroller GPIO output can initialize the input and output. The resistor value is important because a resistance too high, say at 1MΩ, would cause too much of a voltage drop, causing the output to no longer be able to drive the input. Conversely, a resistor too low, such as a 1Ω, would not bias enough and might cause current to flow into the microcontroller, possibly damaging the device.

8.2.3 Application Curve

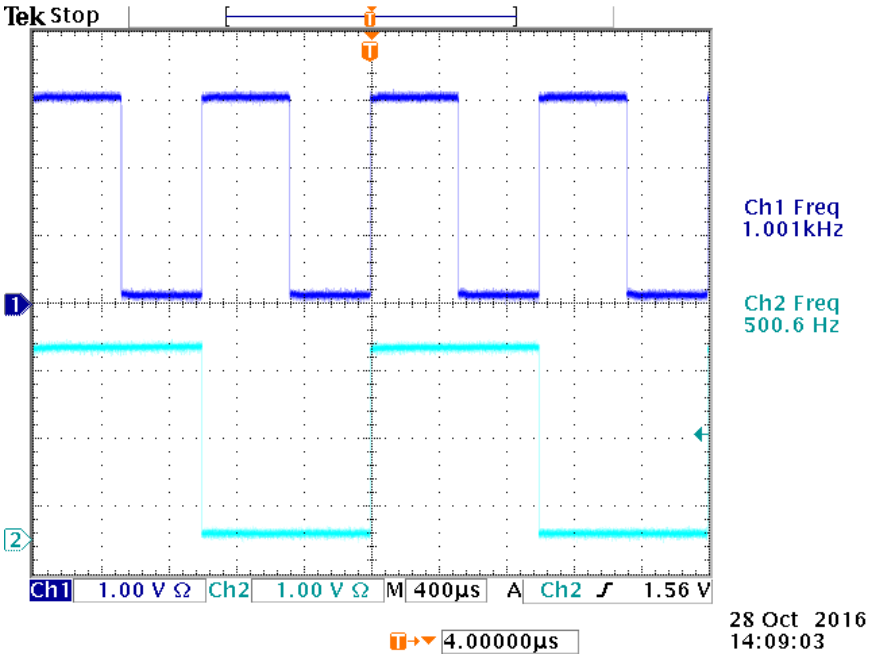


Figure 8-2. Frequency Division

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in *Section 5.3*. A 0.1-µF bypass capacitor is recommended to be connected from the VCC terminal to GND to prevent power disturbance. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must

turn corners. Figure 8-3 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

8.4.2 Layout Example

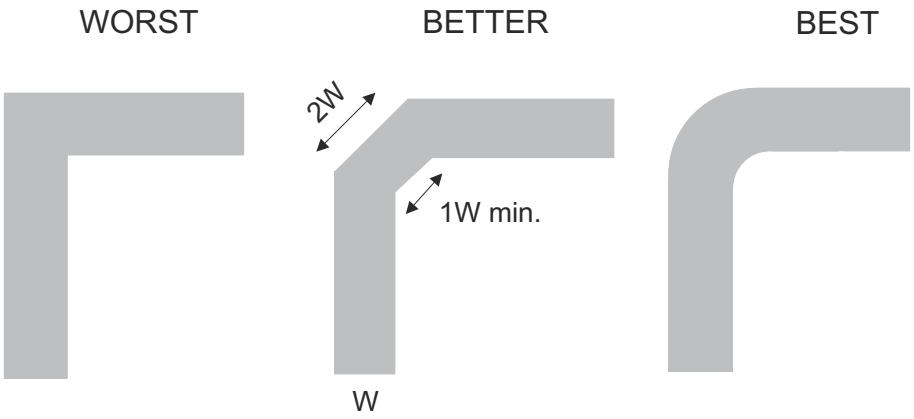


Figure 8-3. Trace Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Community Resources

9.4 Trademarks

NanoFree™ is a trademark of Texas Instruments.
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10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from November 1, 2016 to August 12, 2026 (from Revision S (November 2016) to Revision T (August 2026)) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document..... 1
- Added *Thermal Information* table..... 5
- Changed Junction-to-ambient thermal resistance value for DBV package from: 243.4°C/W to: 357.1°C/W..... 5
- Changed Junction-to-case (top) thermal resistance value for DBV package from: 179°C/W to: 263.7°C/W..... 5
- Changed Junction-to-board characterization value for DBV package from: 77.6°C/W to: 264.4°C/W..... 5
- Changed Junction-to-top characterization value for DBV package from: 58.4°C/W to: 195.6°C/W..... 5
- Changed Junction-to-board characterization value for DBV package from: 77°C/W to: 262.2°C/W..... 5
- Changed Junction-to-ambient thermal resistance value for DCK package from: 278.9°C/W to: 371°C/W..... 5
- Changed Junction-to-case (top) thermal resistance value for DCK package from: 121.3°C/W to: 297.5°C/W.. 5
- Changed Junction-to-board characterization value for DCK package from: 65.6°C/W to: 258.6°C/W..... 5
- Changed Junction-to-top characterization value for DCK package from: 7.5°C/W to: 195.6°C/W..... 5
- Changed Junction-to-board characterization value for DCK package from: 64.9°C/W to: 256.2°C/W..... 5

Changes from Revision R (December 2013) to Revision S (November 2016) **Page**

- Added *Applications* section, *Device Information* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics* section, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section..... 1
- Added max junction temperature to the *Recommended Operating Conditions* table 5
- Added operating free-air temperature for YZP package to the *Recommended Operating Conditions* table 5
- Changed $R_{\theta JA}$ value for DBV package from: 206°C/W to: 243.4°C/W..... 5
- Changed $R_{\theta JA}$ value for DCK package from: 252°C/W to: 278.9°C/W..... 5
- Changed $R_{\theta JA}$ value for YZP package from: 132°C/W to: 136.9°C/W..... 5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G80DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C805, C80F, C80J, C80R)
SN74LVC1G80DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C805, C80F, C80J, C80R)
SN74LVC1G80DBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C805, C80F, C80J, C80R)
SN74LVC1G80DBVRE4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C80F
SN74LVC1G80DBVRG4	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C80F
SN74LVC1G80DBVRG4.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C80F
SN74LVC1G80DBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C805, C80F, C80J, C80R)
SN74LVC1G80DBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C805, C80F, C80J, C80R)
SN74LVC1G80DBVTG4	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C80F
SN74LVC1G80DBVTG4.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C80F
SN74LVC1G80DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(CX5, CXF, CXJ, CXK, CXR)
SN74LVC1G80DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CX5, CXF, CXJ, CXK, CXR)
SN74LVC1G80DCKR.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CX5, CXF, CXJ, CXK, CXR)
SN74LVC1G80DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CX5
SN74LVC1G80DCKRG4.B	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CX5
SN74LVC1G80DCKT	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(CX5, CXF, CXJ, CXK, CXR)
SN74LVC1G80DCKT.B	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CX5, CXF, CXJ, CXK, CXR)
SN74LVC1G80YZPR	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CX7, CXN)
SN74LVC1G80YZPR.B	Active	Production	DSBGA (YZP) | 5	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CX7, CXN)

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC1G80 :

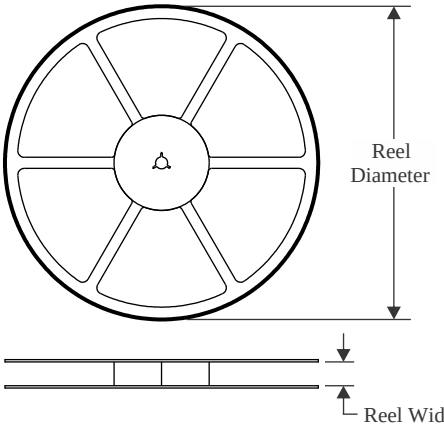
- Automotive : SN74LVC1G80-Q1

NOTE: Qualified Version Definitions:

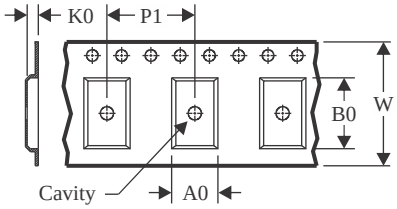
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

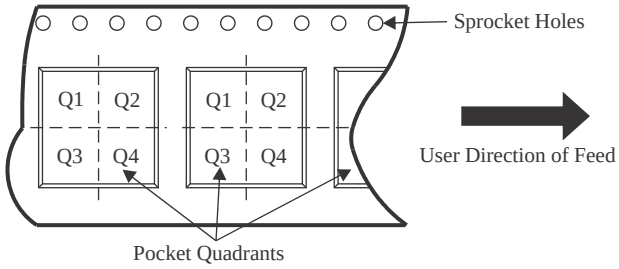


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

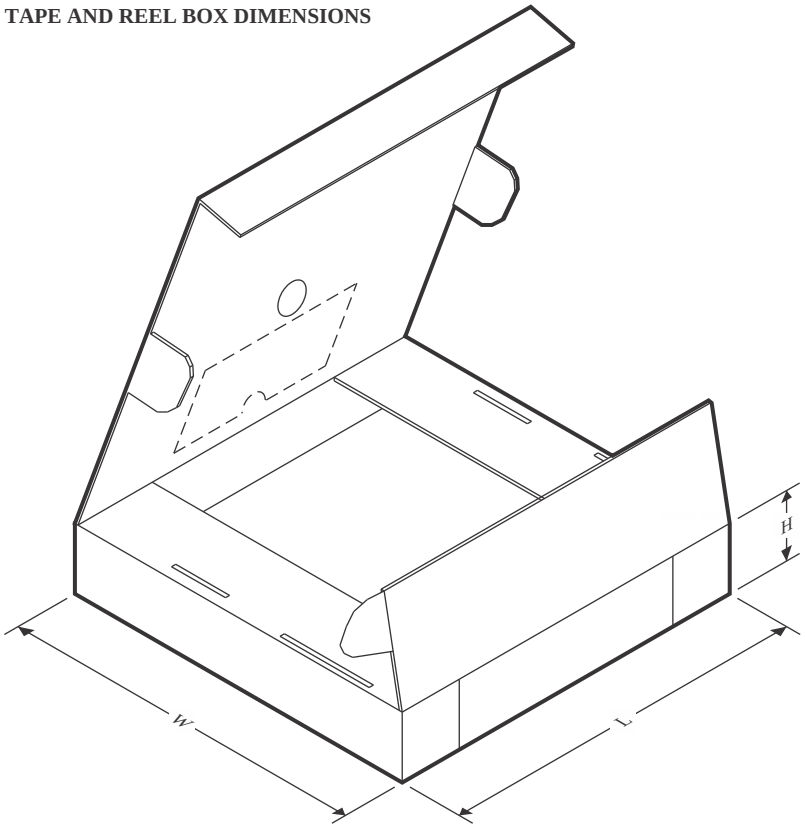


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G80DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G80DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G80DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G80DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G80DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G80DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G80DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G80DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74LVC1G80DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G80DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G80DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G80DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G80DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G80DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G80DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G80DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G80DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G80YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G80DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74LVC1G80DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G80DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G80DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G80DBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
SN74LVC1G80DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G80DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74LVC1G80DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G80DCKR	SC70	DCK	5	3000	208.0	191.0	35.0
SN74LVC1G80DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G80DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74LVC1G80DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G80DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G80DCKR	SC70	DCK	5	3000	210.0	185.0	35.0

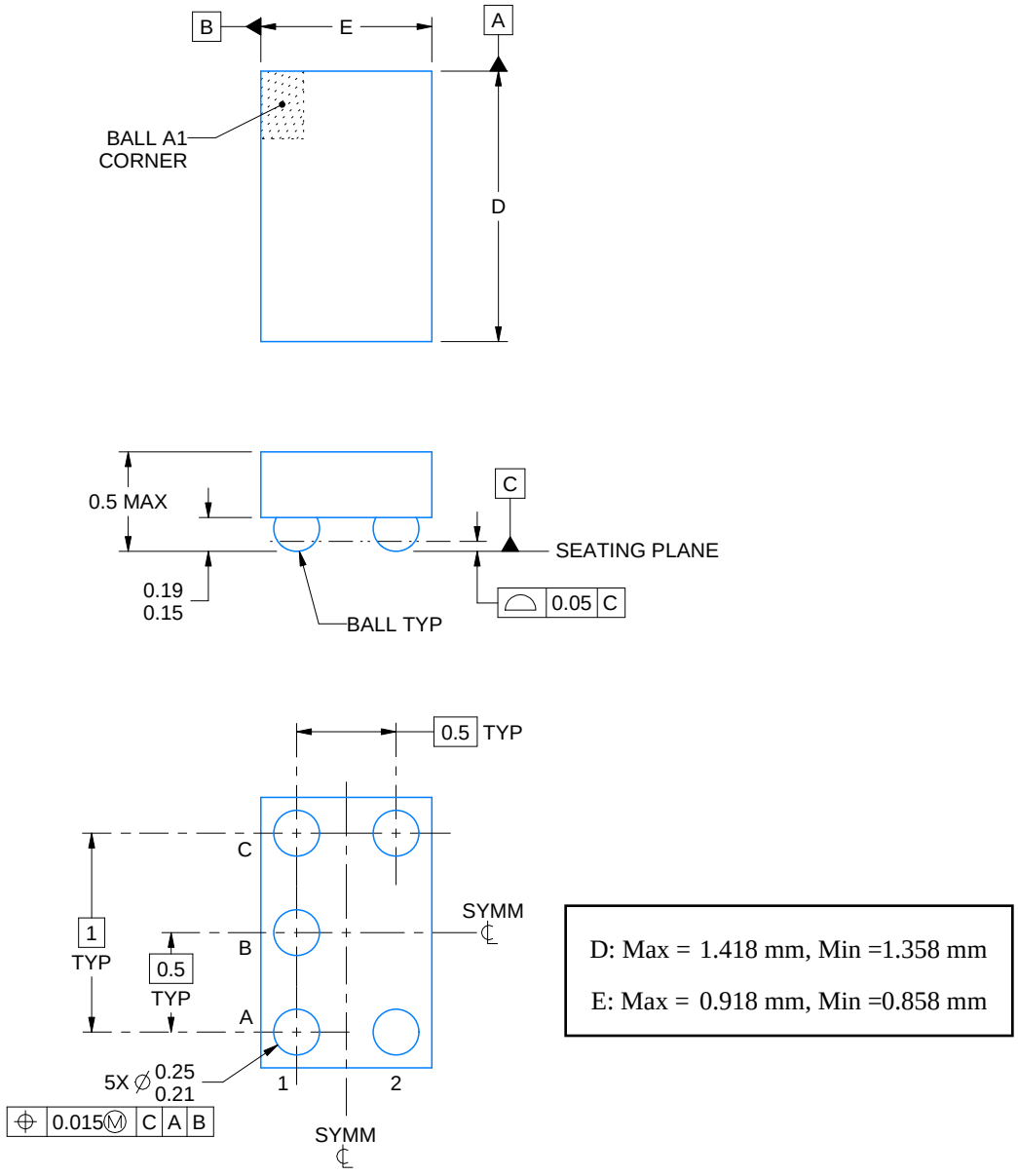
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G80DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G80DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G80DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G80DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G80YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

PACKAGE OUTLINE

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



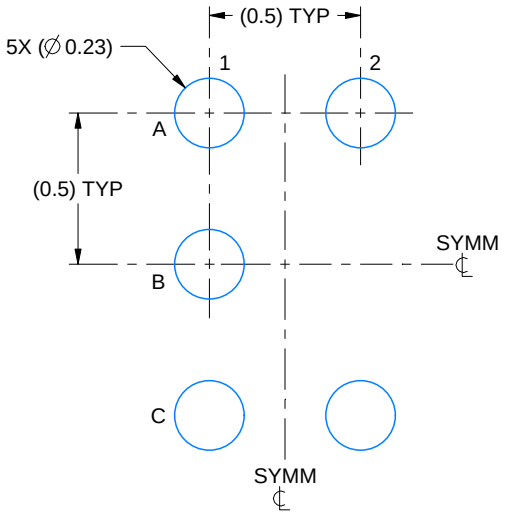
D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

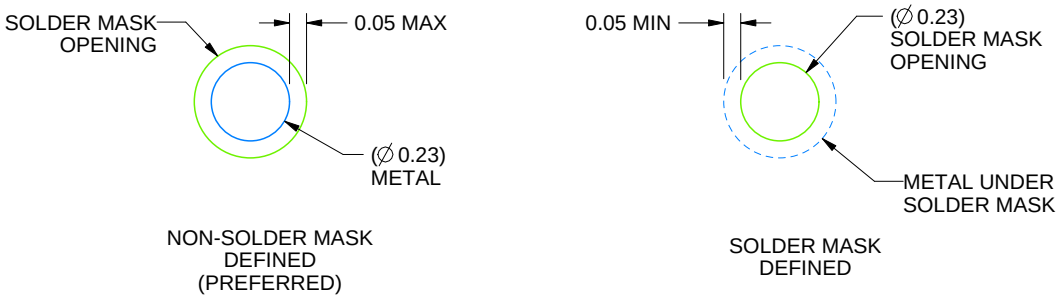
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

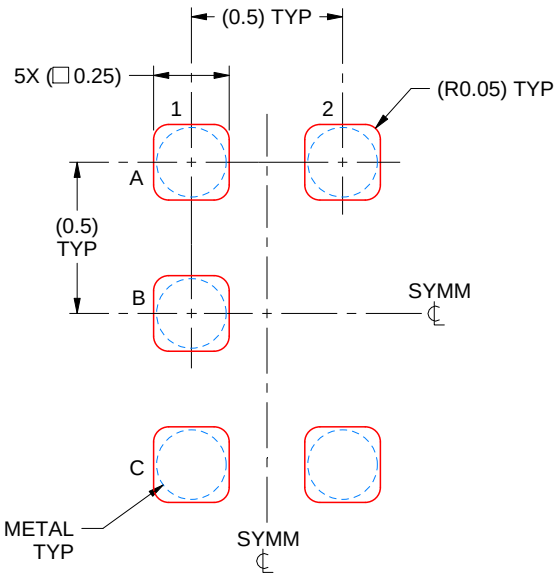


SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

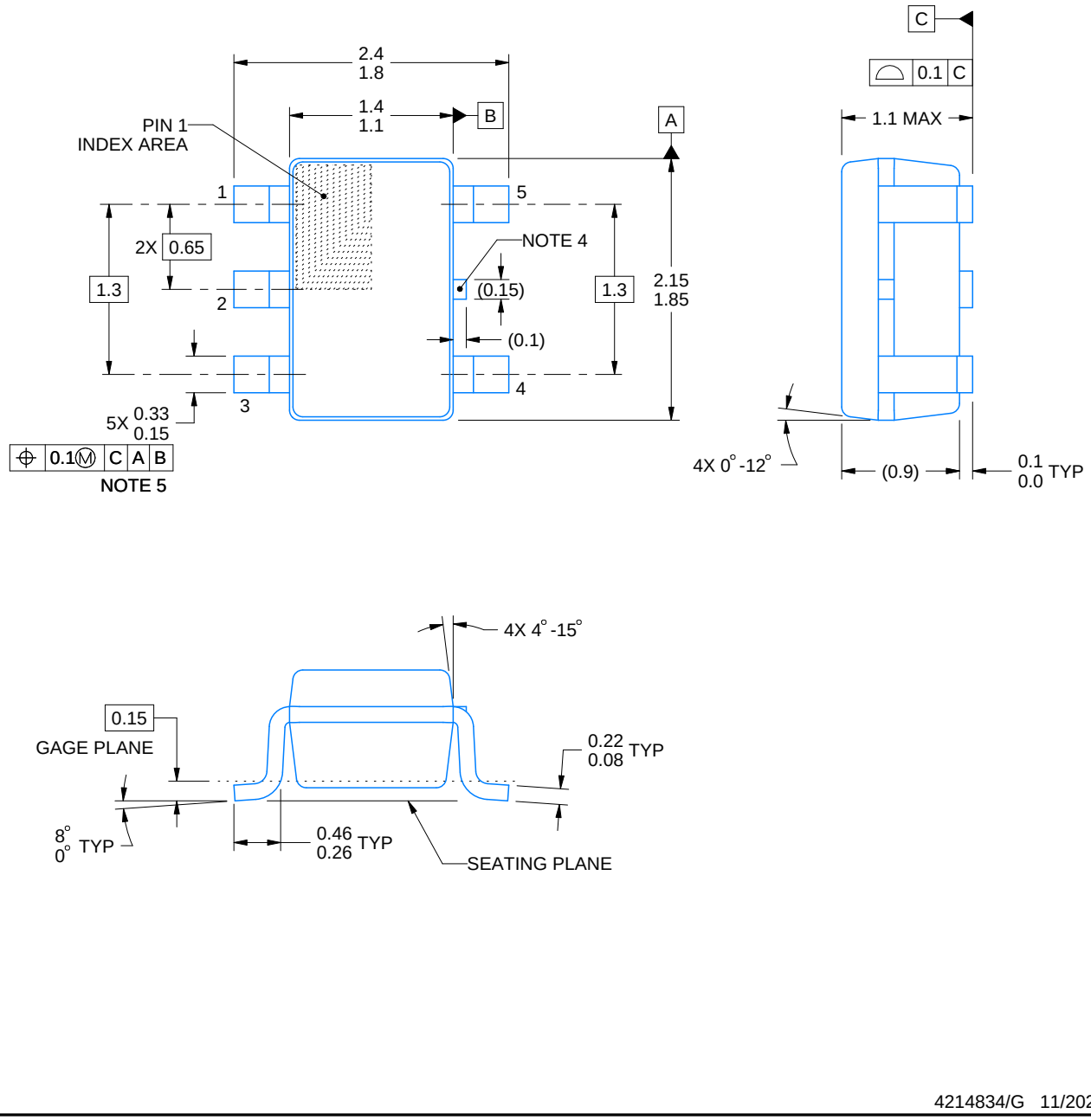
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

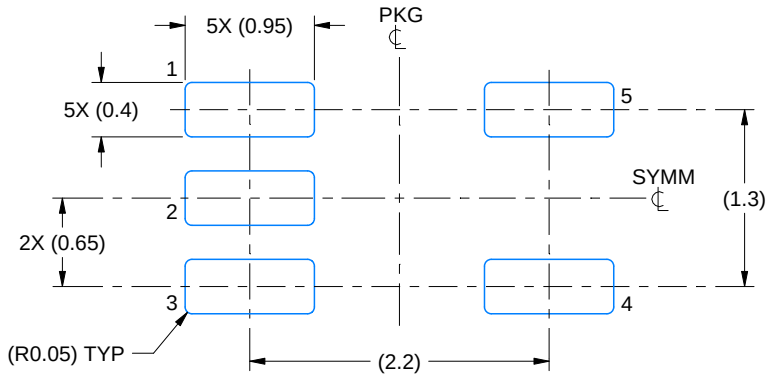
SMALL OUTLINE TRANSISTOR



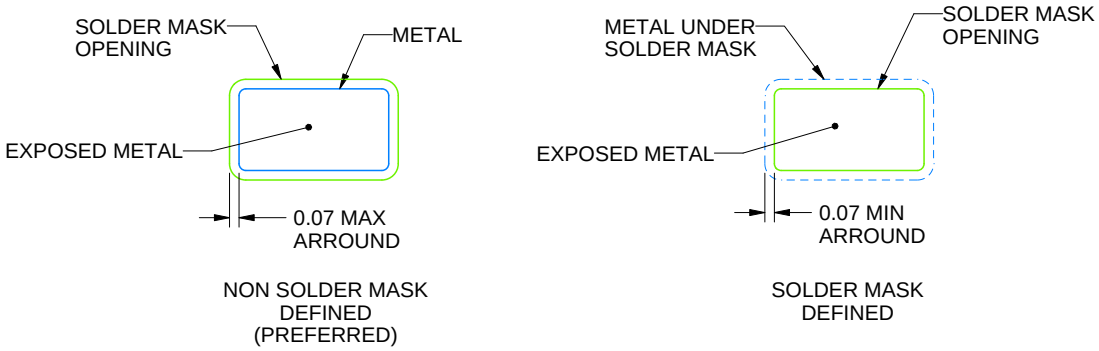
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

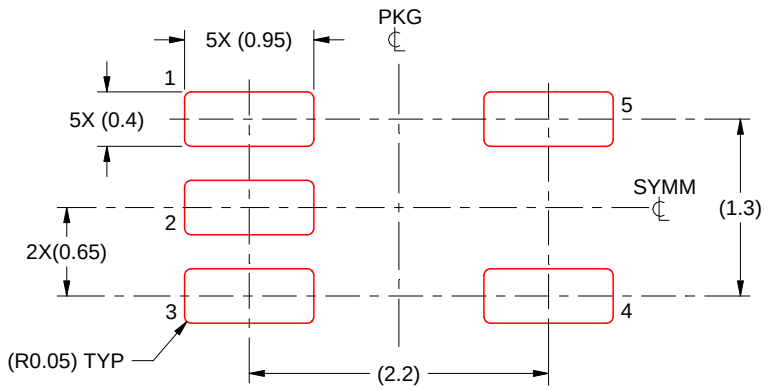


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

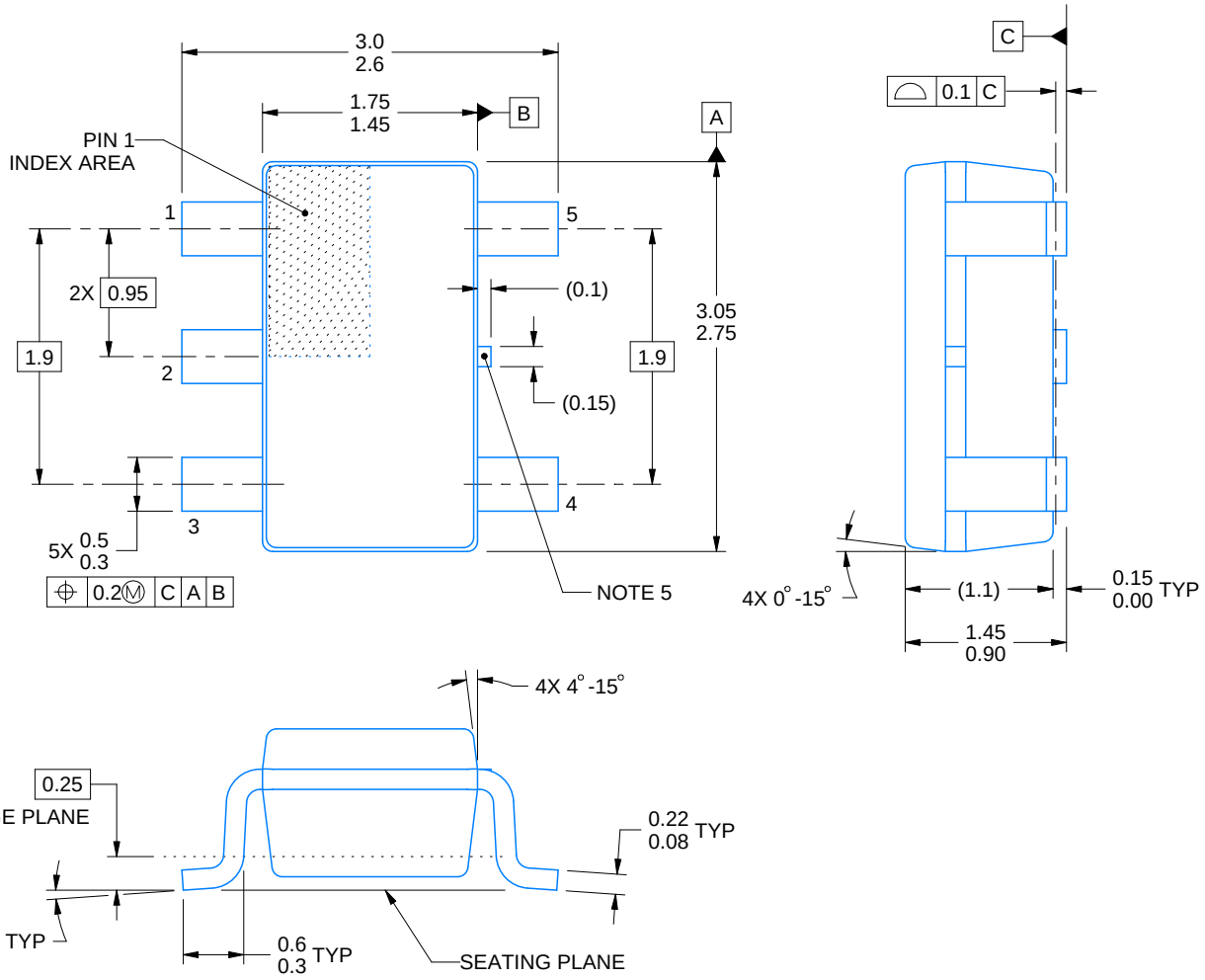
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

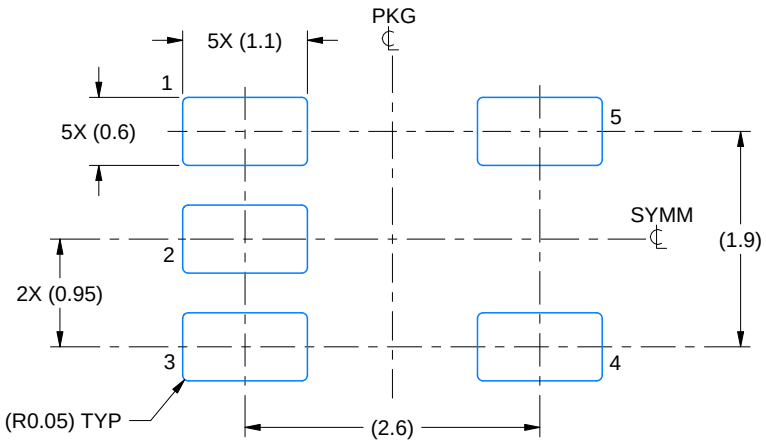
SMALL OUTLINE TRANSISTOR



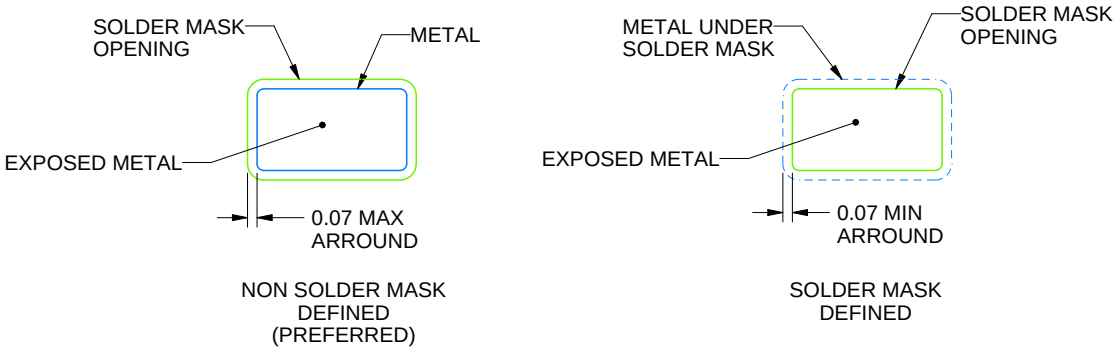
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

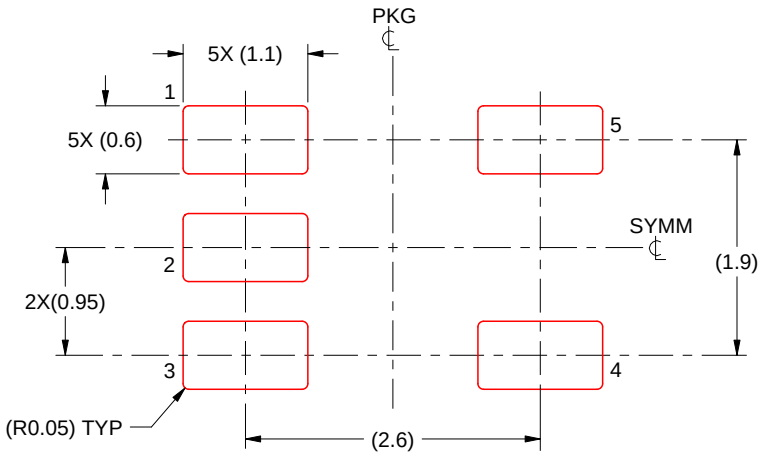


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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