TEXAS INSTRUMENTS

SN74LVCH162244A

SCAS545L – OCTOBER 1995 – REVISED JUNE 2014

SN74LVCH162244A 16-Bit Buffer/Driver with 3-State Outputs

1 Features

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.4 ns at 3.3 V
- Output Ports Have Equivalent 26-Ω Series Resistors, so No External Resistors are Required
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- Bus Hold on Data Inputs Eliminates the Need for External Pullup or Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Servers
- PCs and Notebooks
- Network Switches
- Wireless and Telecom Infrastructures
- TV Set-top Boxes
- Electronic Points of Sale

3 Description

This 16-bit buffer/driver is designed for 1.65-V to 3.6-V V_{CC} operation.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.
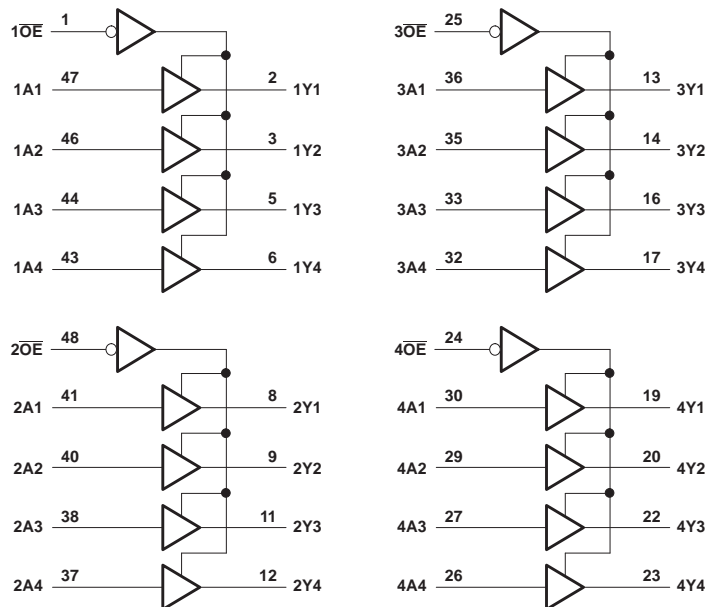
The SN74LVCH162244A device is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVCH162244A	SSOP (48)	15.88 mm × 7.49 mm
	TSSOP (48)	12.50 mm × 6.10 mm
	TVSOP (48)	9.70 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

Table of Contents

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

6 Pin Configuration and Functions

DL, DGG, OR DGV PACKAGE
(TOP VIEW)

Pin		Pin
1$\overline{\text{OE}}$	1	48	2$\overline{\text{OE}}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V$_{CC}$	7	42	V$_{CC}$
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V$_{CC}$	18	31	V$_{CC}$
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4$\overline{\text{OE}}$	24	25	3$\overline{\text{OE}}$

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1$\overline{\text{OE}}$	I	Output Enable 1
2	1Y1	O	1Y1 Output
3	1Y2	O	1Y2 Output
4	GND	—	Ground pin
5	1Y3	O	1Y3 Output
6	1Y4	O	1Y4 Output
7	VCC	—	Power Pin
8	2Y1	O	2Y1 Output
9	2Y2	O	2Y2 Output
10	GND	—	Ground Pin
11	2Y3	O	2Y3 Output
12	2Y4	O	2Y4 Output
13	3Y1	O	3Y1 Output
14	3Y2	O	3Y2 Output
15	GND	—	Ground Pin
16	3Y3	O	3Y3 Output
17	3Y4	O	3Y4 Output
18	VCC	—	Power Pin
19	4Y1	O	4Y1 Output
20	4Y2	O	4Y2 Output

Product Folder Links: *SN74LVCH162244A*

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
21	GND	—	Ground Pin
22	4Y3	O	4Y3 Output
23	4Y4	O	4Y4 Output
24	4$\overline{\text{OE}}$	I	Output Enable 4
25	3$\overline{\text{OE}}$	I	Output Enable 3
26	4A4	I	4A4 Input
27	4A3	I	4A3 Input
28	GND	—	Ground Pin
29	4A2	I	4A2 Input
30	4A1	I	4A1 Input
31	VCC	—	Power Pin
32	3A4	I	3A4 Input
33	3A3	I	3A3 Input
34	GND	—	Ground Pin
35	3A2	I	3A2 Input
36	3A1	I	3A1 Input
37	2A4	I	2A4 Input
38	2A3	I	2A3 Input
39	GND	—	Ground Pin
40	2A2	I	2A2 Input
41	2A1	I	2A1 Input
42	VCC	—	Power Pin
43	1A4	I	1A4 Input
44	1A3	I	1A3 Input
45	GND	—	Ground Pin
46	1A2	I	1A2 Input
47	1A1	I	1A1 Input
48	2$\overline{\text{OE}}$	I	Output Enable 2

Product Folder Links: *SN74LVCH162244A*

7 Specifications

7.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

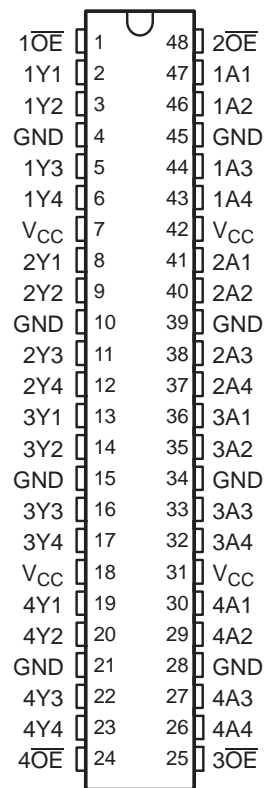|			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6.5	V
V_I	Input voltage range[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2] [3]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CC} or GND			±100	mA

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V		−2	mA
		V_{CC} = 2.3 V		−4	
		V_{CC} = 2.7 V		−8	
		V_{CC} = 3 V		−12	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		2	mA
		V_{CC} = 2.3 V		4	
		V_{CC} = 2.7 V		8	
		V_{CC} = 3 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		−40	125	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

7.4 Thermal Information

THERMAL METRIC[1]		SN74LVCH162244A			UNIT
		DGG	DGV	DL	
		48 PINS	48 PINS	48 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.3	78.4	68.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.6	30.7	34.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	31.5	41.8	41.0	
ψ_{JT}	Junction-to-top characterization parameter	1.1	3.8	12.3	
ψ_{JB}	Junction-to-board characterization parameter	31.2	41.3	40.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{OH}	$I_{OH} = -100$ µA		1.65 V to 3.6 V	$V_{CC} - 0.2$			V
	$I_{OH} = -2$ mA		1.65 V		1.2		
	$I_{OH} = -4$ mA		2.3 V		1.7		
			2.7 V		2.2		
	$I_{OH} = -6$ mA		3 V		2.4		
	$I_{OH} = -8$ mA		2.7 V		2		
	$I_{OH} = -12$ mA		3 V		2		
V_{OL}	$I_{OL} = 100$ µA		1.65 V to 3.6 V			0.2	V
	$I_{OL} = 2$ mA		1.65 V			0.45	
	$I_{OL} = 4$ mA		2.3 V			0.7	
			2.7 V			0.4	
	$I_{OL} = 6$ mA		3 V			0.55	
	$I_{OL} = 8$ mA		2.7 V			0.6	
	$I_{OL} = 12$ mA		3 V			0.8	
I_I	$V_I = 0$ to 5.5 V		3.6 V			±5	µA
$I_{I(hold)}$	$V_I = 0.58$ V		1.65 V	[2]			µA
	$V_I = 1.07$ V		1.65 V	[2]			
	$V_I = 0.7$ V		2.3 V		45		
	$V_I = 1.7$ V		2.3 V		–45		
	$V_I = 0.8$ V		3 V		75		
	$V_I = 2$ V		3 V		–75		
	$V_I = 0$ to 3.6 V[3]		3.6 V			±500	
I_{off}	V_I or $V_O = 5.5$ V		0			±10	µA
I_{OZ}	$V_O = 0$ to 5.5 V		3.6 V			±10	µA
I_{CC}	$V_I = V_{CC}$ or GND	$I_O = 0$	3.6 V			20	µA
	3.6 V ≤ V_I ≤ 5.5 V[4]					20	
ΔI_{CC}	One input at $V_{CC} - 0.6$ V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500	µA
C_i	$V_I = V_{CC}$ or GND		3.3 V		5.5		pF
C_o	$V_O = V_{CC}$ or GND		3.3 V		6		pF

(1) All typical values are at $V_{CC} = 3.3$ V, $T_A = 25$°C.
(2) This information was not available at the time of publication.
(3) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
(4) This applies in the disabled state only.

7.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1	10.2	1	6.4	1	5.6	1.1	4.4	ns
t_{en}	$\overline{OE}$	Y	1	14.8	1	8.2	1	6.9	1	5.5	ns
t_{dis}	$\overline{OE}$	Y	1	12.3	1	7.1	1	6.8	1.8	6.3	ns

7.7 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
			TYP	TYP	TYP	
C_{pd} Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	See[1]	See[1]	35	pF
	Outputs disabled		See[1]	See[1]	4	

(1) This information was not available at the time of publication.
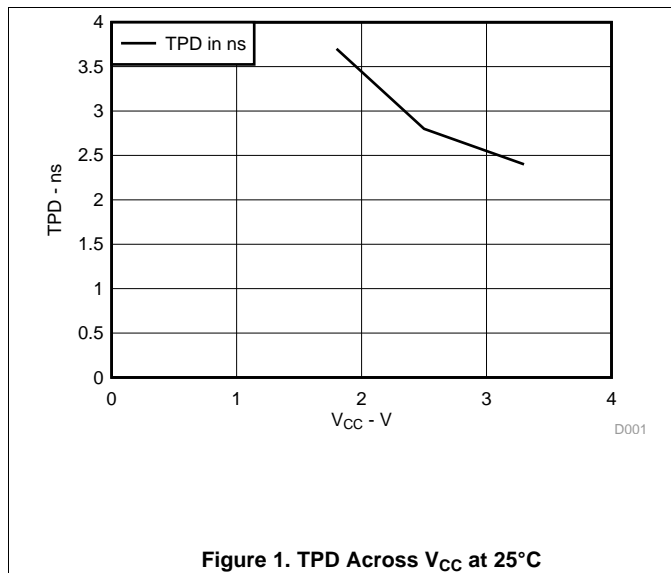
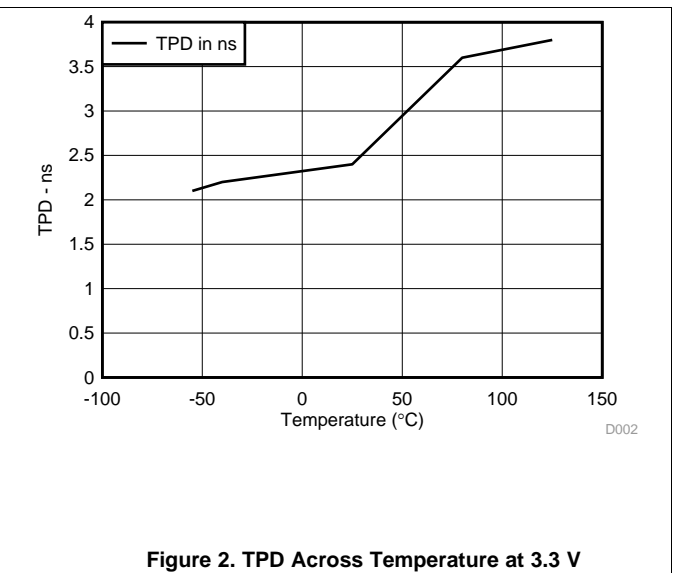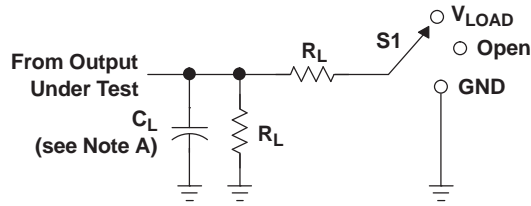## 7.8 Typical Characteristics

Figure 1. TPD Across V_{CC} at 25°C

Figure 2. TPD Across Temperature at 3.3 V

Product Folder Links: *SN74LVCH162244A*

8 Parameter Measurement Information

LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

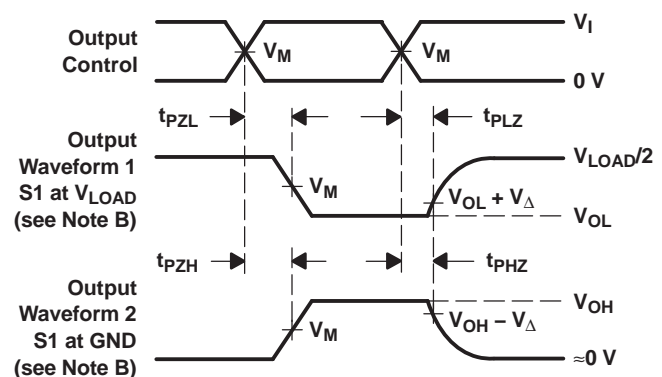| V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V $\pm$ 0.15 V	V_{CC}	$\leq$2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V $\pm$ 0.2 V	V_{CC}	$\leq$2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq$2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V $\pm$ 0.3 V	2.7 V	$\leq$2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
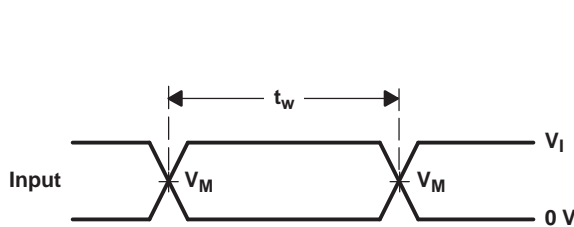
VOLTAGE WAVEFORMS
PULSE DURATION
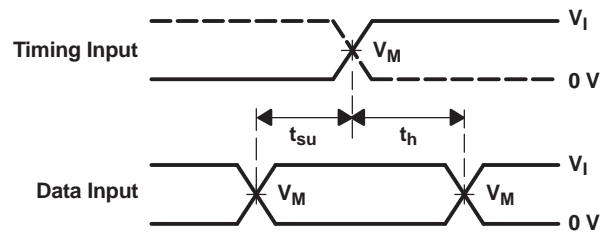
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
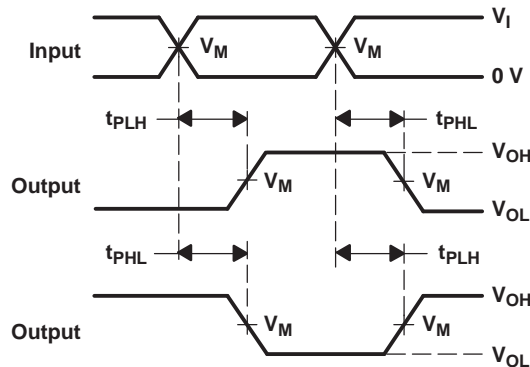
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

9.2 Functional Block Diagram
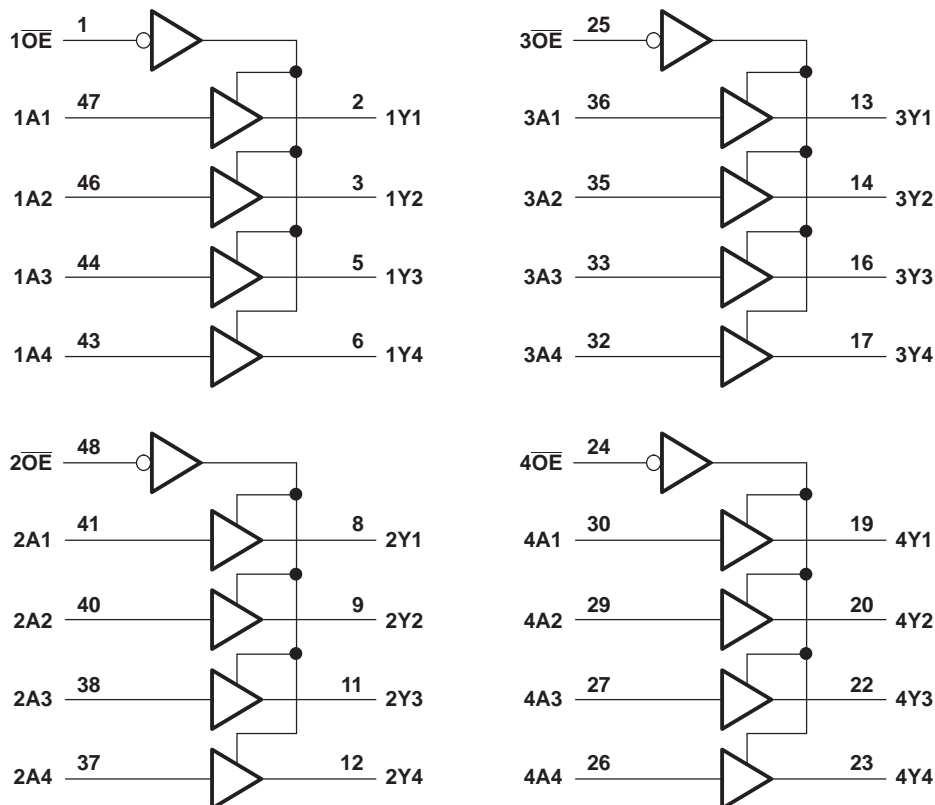
9.3 Feature Description

- Wide operating range
    - Operates from 1.65 V to 3.6 V
- Allows down voltage translation
    - Inputs accept voltages to 5.5 V
- I_{off} feature
    - Allows voltages on the inputs and outputs when V_{CC} is 0 V

9.4 Device Functional Modes

Table 1. Function Table
(Each 4-Bit Buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

10 Application and Implementation

10.1 Application Information

The SN74LVCH16244A device is a 16-bit buffer driver. This device can be used as four 4-bit, two 8-bit, or one 16-bit buffer.

It allows data transmission from the A bus to the Y bus with 4 separate enable pins that control 4 bits each. The output-enable ($\overline{OE}$) input can be used to disable sections of the device so that the buses are effectively isolated.

The SN74LVCH16244A device has 5.5 V tolerant inputs at any valid V_{CC} which allows it to be used in multi-power systems and can be used for down translation. Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

10.2 Typical Application
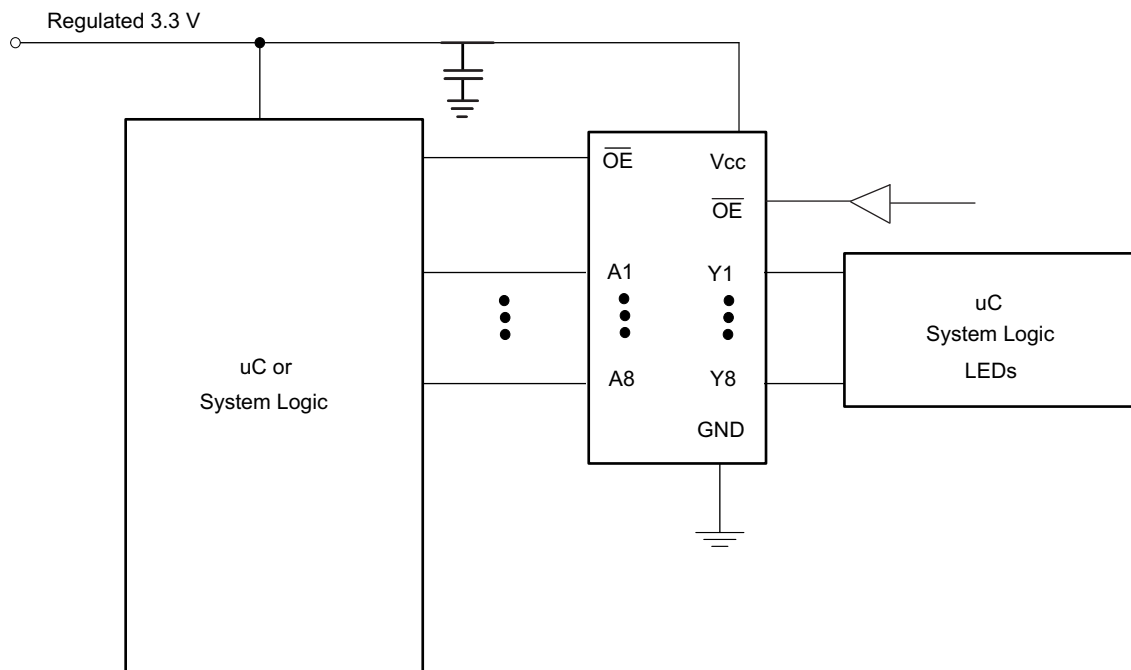
Figure 4. Typical Application Diagram

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   – Rise time and fall time specs: See ($\Delta t/\Delta V$) in the *Recommended Operating Conditions* table.
   – Specified high and low levels: See (V_{IH} and V_{IL}) in the *Recommended Operating Conditions* table.
   – Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommend Output Conditions
   – Load currents should not exceed 25 mA per output and 50 mA total for the part.
   – Outputs should not be pulled above V_{CC}.

Product Folder Links: *SN74LVCH162244A*

Typical Application (continued)

10.2.3 Application Curves

Figure 5. I_{CC} vs Frequency
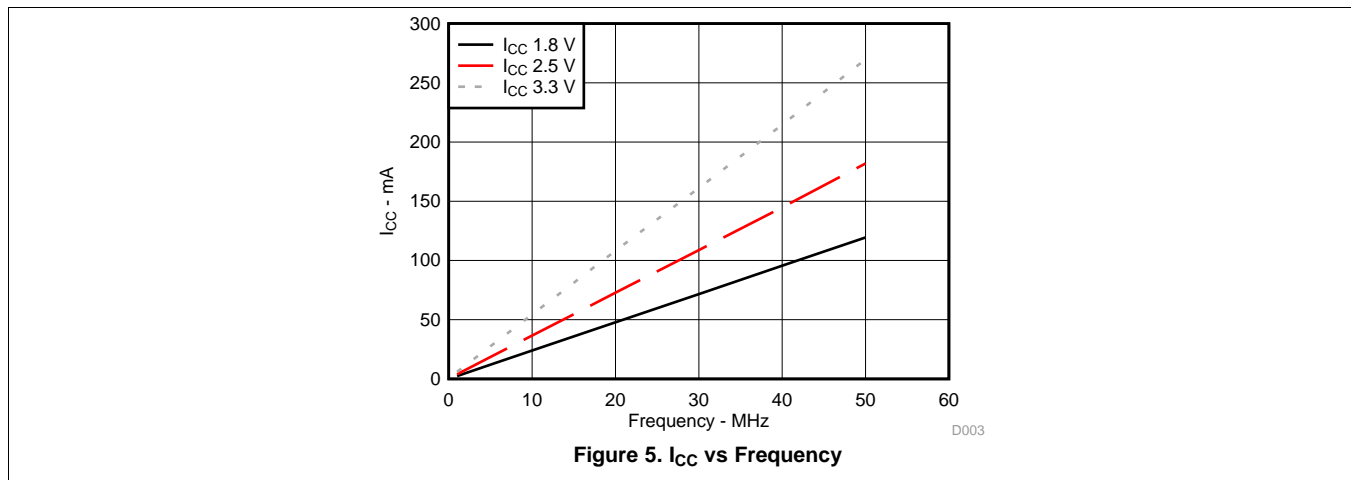
11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µf is recommended; if there are multiple V_{CC} pins, then 0.01 µf or 0.022 µf is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µf and a 1 µf are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 6 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.
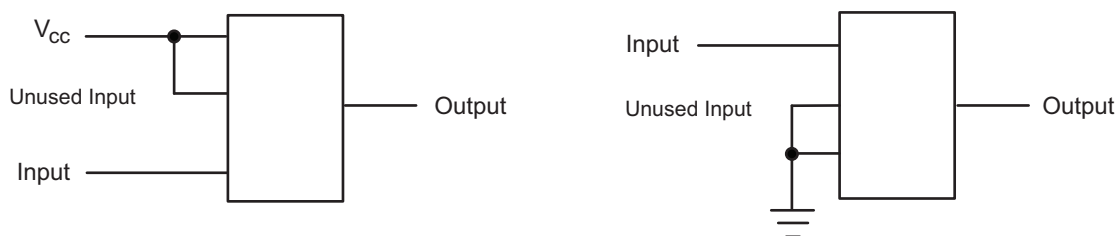
12.2 Layout Example

Figure 6. Layout Diagram

Product Folder Links: *SN74LVCH162244A*

13 Device and Documentation Support

13.1 Trademarks

Widebus is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74LVCH162244AGRG4	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCH162244A
74LVCH162244AGRG4.B	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCH162244A
74LVCH162244AVRG4	Active	Production	TVSOP (DGV) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LN2244A
74LVCH162244AVRG4.B	Active	Production	TVSOP (DGV) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LN2244A
SN74LVCH162244ADL	Active	Production	SSOP (DL) | 48	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCH162244A
SN74LVCH162244ADL.B	Active	Production	SSOP (DL) | 48	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCH162244A
SN74LVCH162244ADLR	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCH162244A
SN74LVCH162244ADLR.B	Active	Production	SSOP (DL) | 48	1000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCH162244A
SN74LVCH162244AGR	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCH162244A
SN74LVCH162244AGR.B	Active	Production	TSSOP (DGG) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCH162244A
SN74LVCH162244AVR	Active	Production	TVSOP (DGV) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LN2244A
SN74LVCH162244AVR.B	Active	Production	TVSOP (DGV) | 48	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LN2244A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.
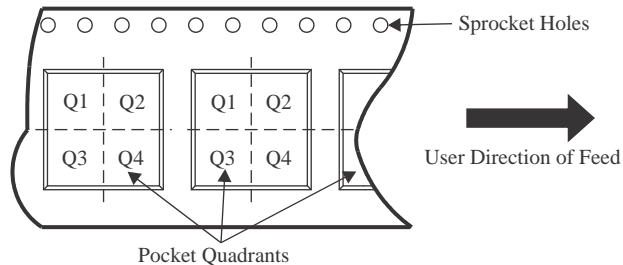
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVCH162244AGRG4	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
74LVCH162244AVRG4	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74LVCH162244ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74LVCH162244AGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVCH162244AVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVCH162244AGRG4	TSSOP	DGG	48	2000	356.0	356.0	45.0
74LVCH162244AVRG4	TVSOP	DGV	48	2000	353.0	353.0	32.0
SN74LVCH162244ADLR	SSOP	DL	48	1000	356.0	356.0	53.0
SN74LVCH162244AGR	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74LVCH162244AVR	TVSOP	DGV	48	2000	353.0	353.0	32.0

PACKAGE MATERIALS INFORMATION

TUBE

T - Tube height

W - Tube width

L - Tube length

B - Alignment groove width
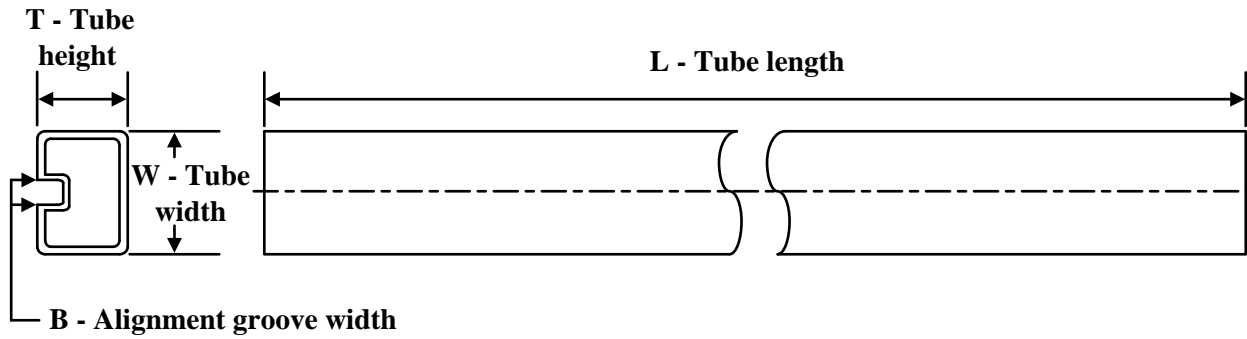
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVCH162244ADL	DL	SSOP	48	25	473.7	14.24	5110	7.87
SN74LVCH162244ADL.B	DL	SSOP	48	25	473.7	14.24	5110	7.87

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN
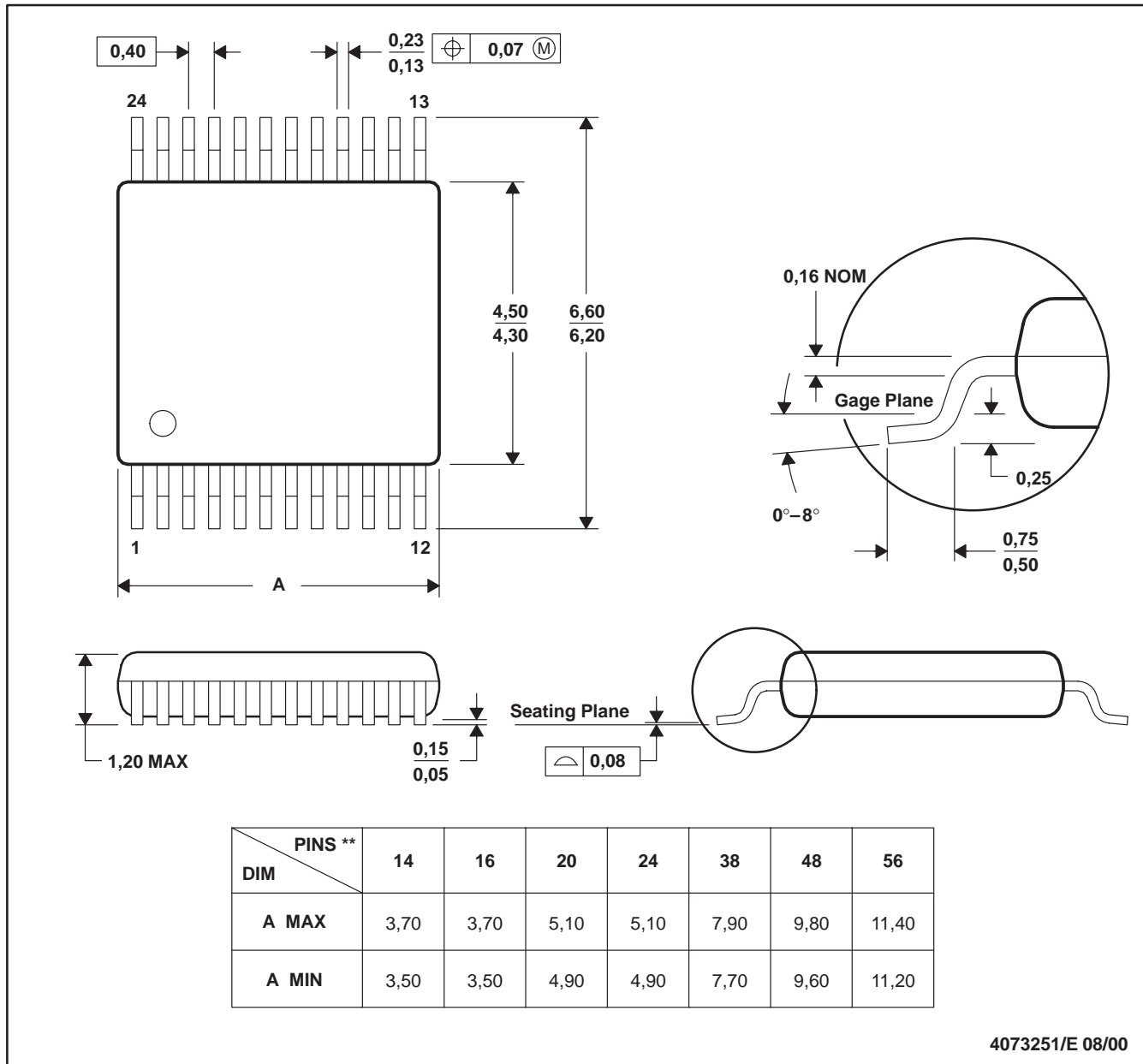
PINS ** DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
        D. Falls within JEDEC: 24/48 Pins – MO-153
                            14/16/20/56 Pins – MO-194

8.3 / 7.9 TYP

A

PIN 1 ID AREA

1

46X 0.5

48

12.6 / 12.4 NOTE 3

2X 11.5

24

25

B

6.2 / 6.0

48X 0.27 / 0.17

⊕ 0.08Ⓜ C A B

C

SEATING PLANE

⌒ 0.1 C

1.2 / 1.0

(0.15) TYP

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

0.75 / 0.50

0.15 / 0.05

DETAIL A
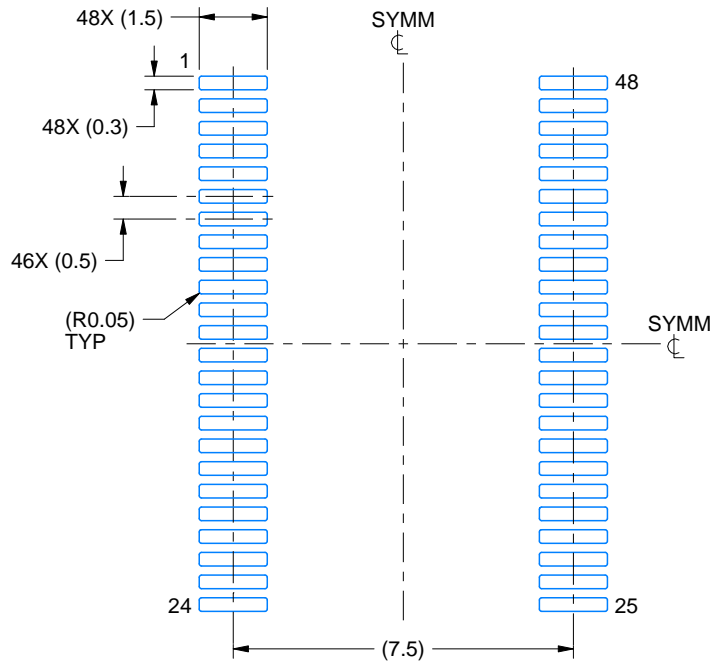TYPICAL
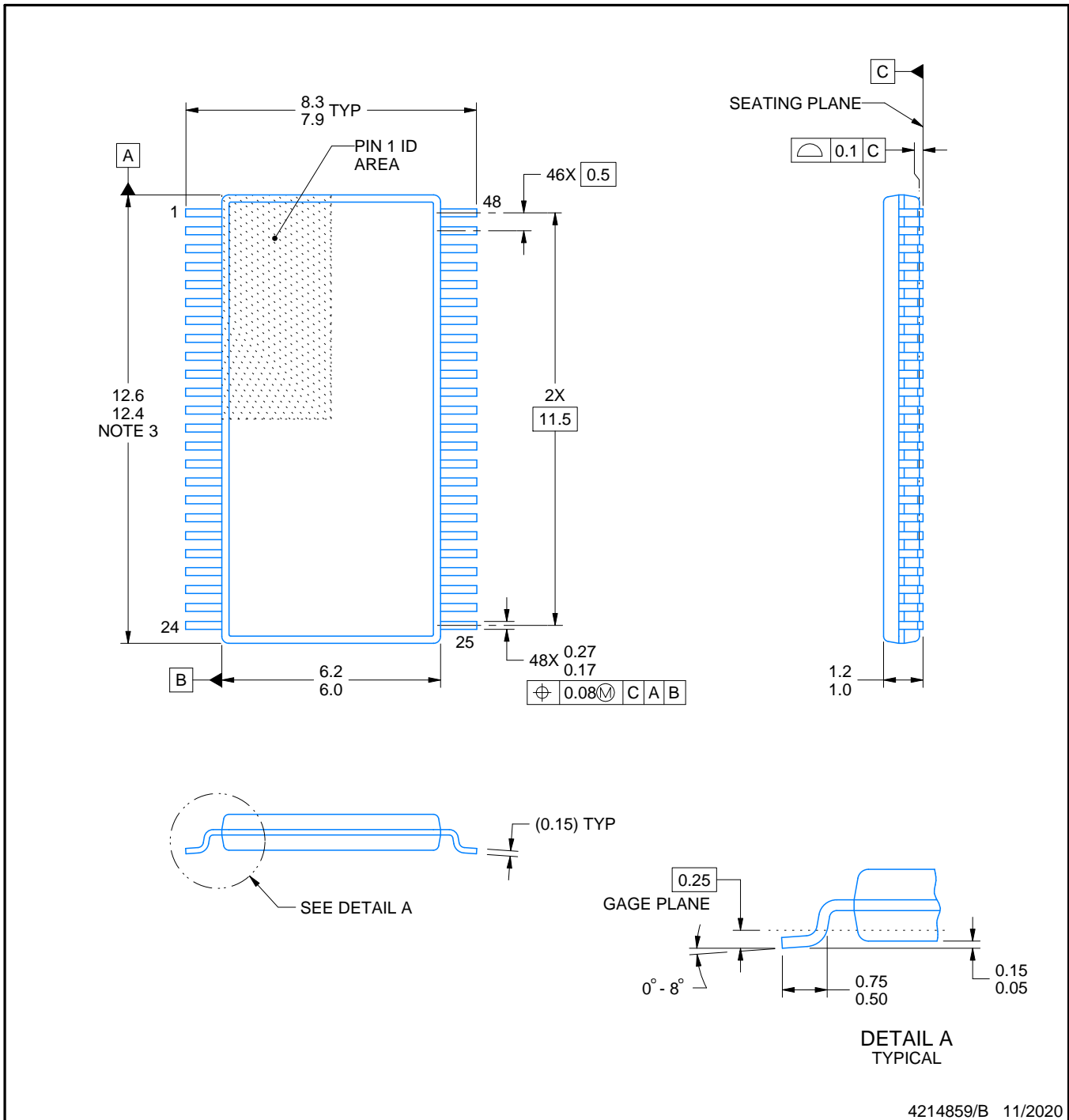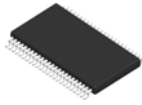
4214859/B   11/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

TEXAS INSTRUMENTS
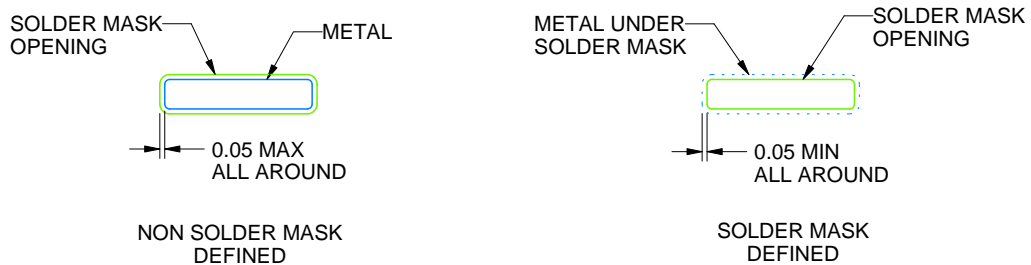www.ti.com

48X (1.5)

1

48X (0.3)

46X (0.5)

(R0.05)
TYP

SYMM

48

SYMM

24

25

(7.5)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

0.05 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

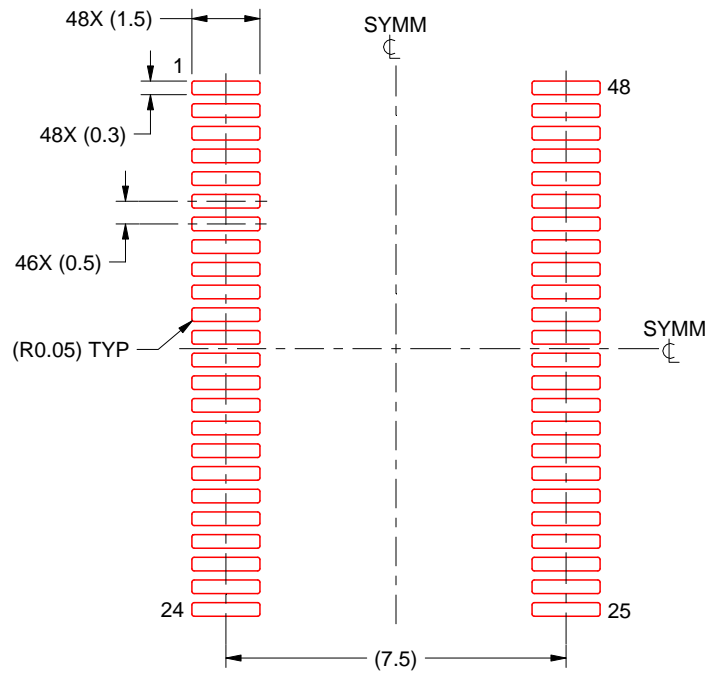4214859/B   11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

48X (1.5)
1
48X (0.3)
46X (0.5)
(R0.05) TYP
SYMM
48
SYMM
24
25
(7.5)

SOLDER PASTE EXAMPLE
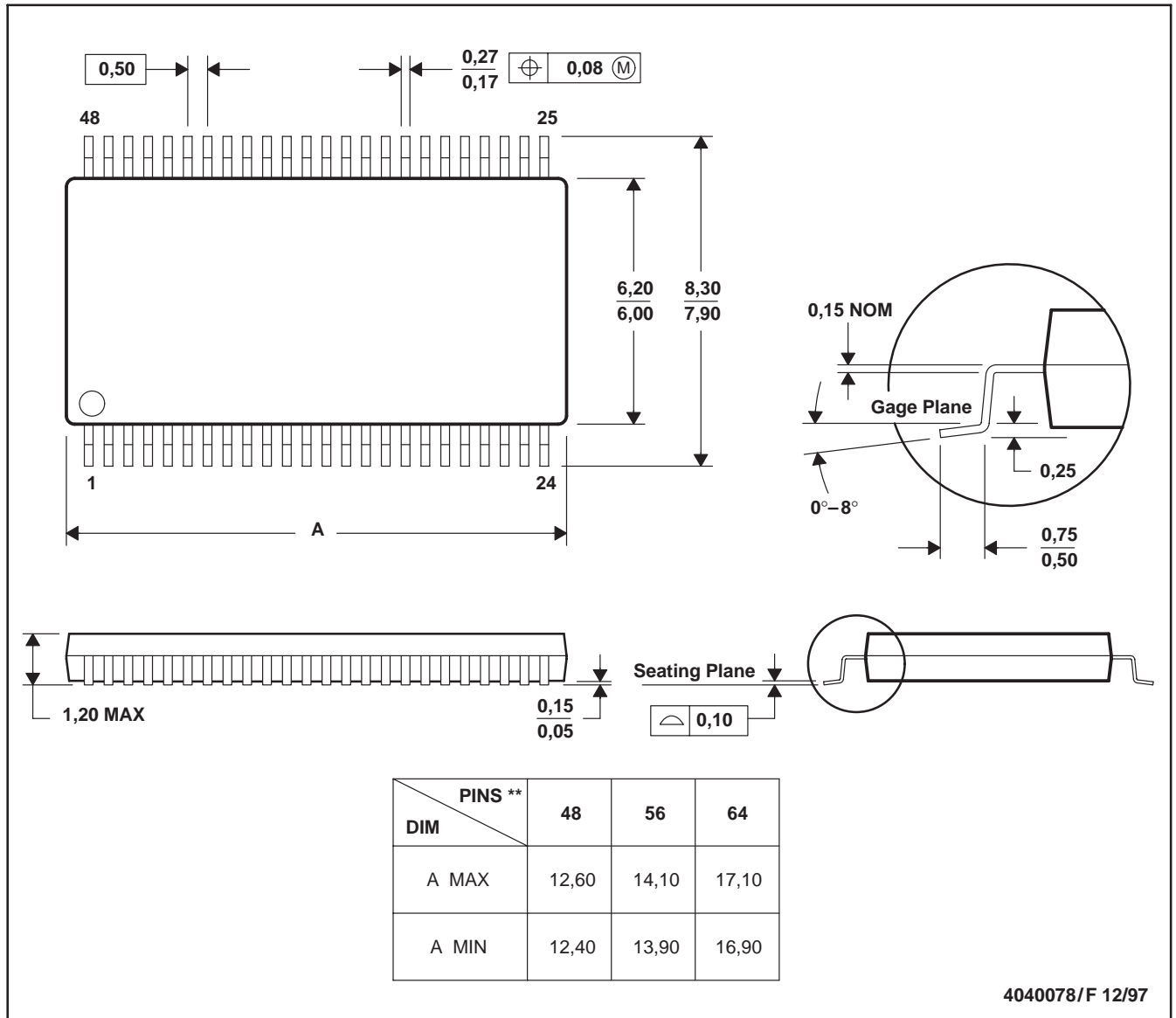BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B   11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)**   PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

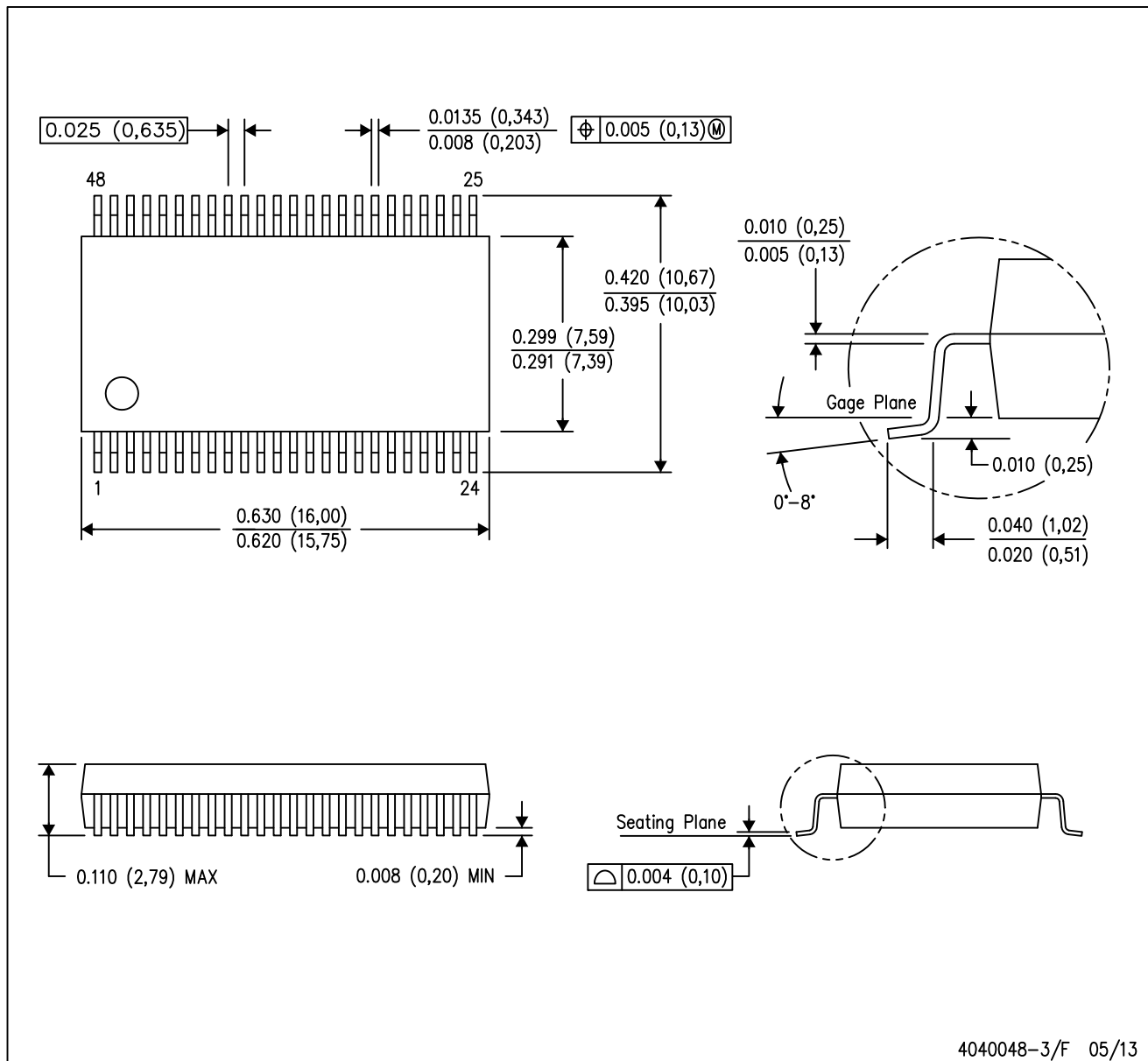| PINS ** DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

DL (R−PDSO−G48)   PLASTIC SMALL−OUTLINE PACKAGE

0.025 (0,635)

0.0135 (0,343)
0.008 (0,203)

⊕ 0.005 (0,13) Ⓜ

48   25

0.420 (10,67)
0.395 (10,03)

0.299 (7,59)
0.291 (7,39)

0.010 (0,25)
0.005 (0,13)

Gage Plane

0.010 (0,25)

0°−8°

0.040 (1,02)
0.020 (0,51)

1   24

0.630 (16,00)
0.620 (15,75)

0.110 (2,79) MAX   0.008 (0,20) MIN

Seating Plane

△ 0.004 (0,10)

4040048−3/F   05/13

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MO−118

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