SNx4LVCH245A Octal Bus Transceivers With Tri-State Outputs

1 Features

- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 6.3 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Bus Hold on Data Inputs Eliminates the Need for External Pullup or Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Servers
- PCs and Notebooks
- Network Switches
- Wearable Health and Wellness Devices
- Telecom Infrastructures
- Electronic Points of Sale

3 Description

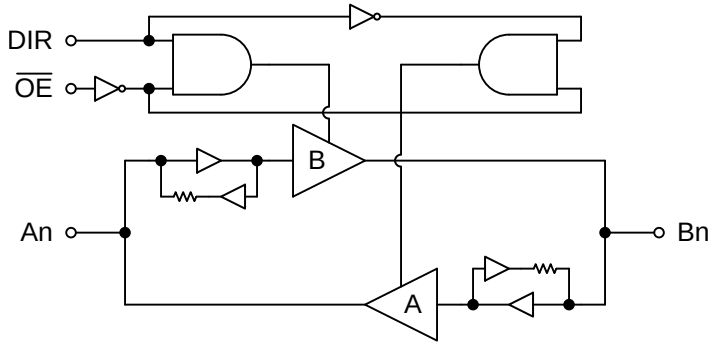
The SN54LVCH245A octal bus transceiver is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVCH245A octal bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation. Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVCH245ADBR	SSOP (20)	7.20 mm × 5.30 mm
SN74LVCH245ADGVR	TVSOP (20)	5.00 mm × 4.40 mm
SN74LVCH245ADWR	SOIC (20)	12.80 mm × 7.50 mm
SN74LVCH245ANSR	SO (20)	12.60 mm × 5.30 mm
SN74LVCH245APWR	TSSOP (20)	6.50 mm × 4.40 mm
SN74LVCH245ARGYR	VQFN (20)	4.50 mm × 3.50 mm
SN74LVCH245AZQNR	BGA MICROSTAR JUNIOR (20)	4.00 mm × 3.00 mm
SN74LVCH245AZXYR	BGA MICROSTAR JUNIOR (20)	3.00 mm × 2.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision P (July 2014) to Revision Q **Page**

- Changed part number column to include specific orderable parts. ... 1
- Removed package name GQN. ... 6
- Added ZXY package pinout section. ... 6
- Changed Handling Ratings to ESD ratings. ... 7
- Deleted storage temperature from ESD Ratings table. ... 7
- Changed only include commercial device specifications in this table. ... 10
- Added new table for military device specifications. ... 11
- Deleted bulleted list of features. ... 16
- Added Output Types, Input Types, Clamp Diode Structure, and Special Features sections. ... 16

Changes from Revision O (December 2005) to Revision P **Page**

- Updated document to new TI data sheet standards. ... 1
- Deleted Ordering Information table. ... 1
- Updated I_{off} Feature bullet. ... 1
- Added Military Disclaimer to Features list. ... 1
- Added Applications. ... 1
- Added Device Information table. ... 1
- Added Handling Ratings table. ... 7
- Changed MAX operating temperature to 125°C. ... 8
- Added Thermal Information table. ... 9
- Added –40°C TO 125°C to Electrical Characteristics table. ... 10
- Added data to –40°C TO 85°C Switching Characteristics table. ... 12
- Added Switching Characteristics table for –40°C to 125°C for SN74LVCH245A. ... 12

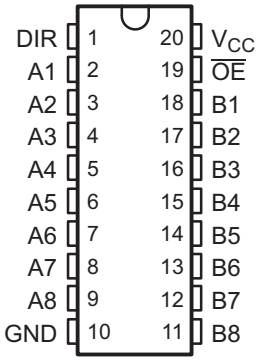
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- Added data to Operating Characteristics table. 13
- Added Typical Characteristics. 13
- Added Detailed Description section..... 16
- Added Application and Implementation section..... 19

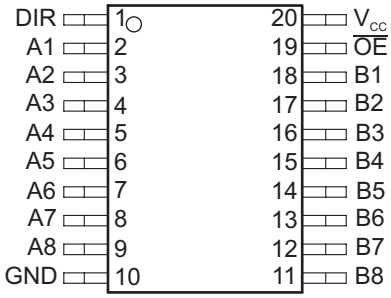
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5 Pin Configuration and Functions

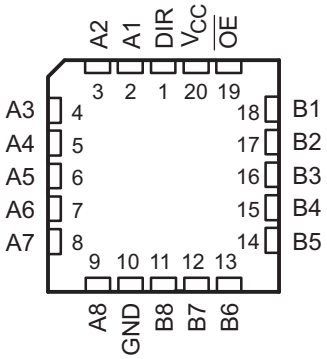
SN54LVCH245A
20-Pin J or W Package
Top View



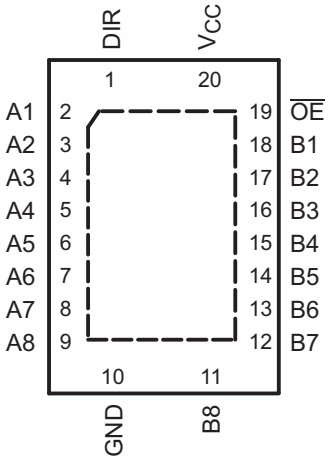
SN74LVCH245A
20-Pin Count DB, DGV. DW, NS or PW Package
Top View



SN54LVCH245A
20-Pin Count FK Package
Top View



SN74LVCH245A
20-Pin Count RGY Package
Top View



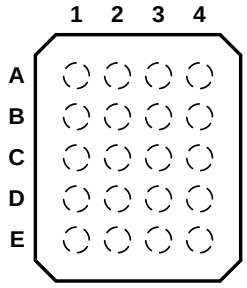
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Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	DIR	I	Direction select
2	A1	I/O	A1 input or output
3	A2	I/O	A2 input or output
4	A3	I/O	A3 input or output
5	A4	I/O	A4 input or output
6	A5	I/O	A5 input or output
7	A6	I/O	A6 input or output
8	A7	I/O	A7 input or output
9	A8	I/O	A8 input or output
10	GND	—	Ground
11	Y8	I/O	Y8 input or output
12	Y7	I/O	Y7 input or output
13	Y6	I/O	Y6 input or output
14	Y5	I/O	Y5 input or output
15	Y4	I/O	Y4 input or output
16	Y3	I/O	Y3 input or output
17	Y2	I/O	Y2 input or output
18	Y1	I/O	Y1 input or output
19	$\overline{OE}$	I	Output enable, active low
20	V_{CC}	—	Positive Supply

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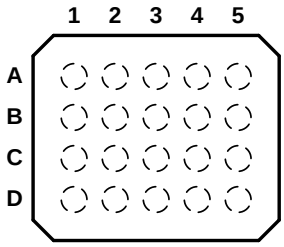
ZQN PACKAGE
(TOP VIEW)



Pin Assignments: ZQN Package

	1	2	3	4
A	A1	DIR	V_{CC}	$\overline{OE}$
B	A3	B2	A2	B1
C	A5	A4	B4	B3
D	A7	B6	A6	B5
E	GND	A8	B8	B7

ZXY PACKAGE
(TOP VIEW)



Pin Assignments: ZXY Package

	1	2	3	4	5
A	A7	A6	A4	A2	DIR
B	A8	A5	A3	A1	V_{CC}
C	GND	B6	B4	B2	$\overline{OE}$
D	B8	B7	B5	B3	B1

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range, V_{CC}		–0.5	6.5	V
Input voltage range, V_I(2)		–0.5	6.5	V
Voltage range applied to any output in the high-impedance or power-off state, V_O(2)		–0.5	6.5	V
Voltage range applied to any output in the high or low state, V_O(2)(3)		–0.5	V_{CC} + 0.5	V
Input clamp current, I_{IK}	V_I < 0		–50	mA
Output clamp current, I_{OK}	V_O < 0		–50	mA
Continuous output current, I_O			±50	mA
Continuous current through V_{CC} or GND			±100	mA
Operating virtual junction temperature, T_j			150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions: SN74LVCH245A

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		Tri-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V		–4	mA
		V_{CC} = 2.3 V		–8	
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		–40	125	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. For more information, see the *Implications of Slow or Floating CMOS Inputs* application report.

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6.4 Recommended Operating Conditions: SN54LVCH245A

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V			V
		V_{CC} = 2.3 V to 2.7 V			
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V			V
		V_{CC} = 2.3 V to 2.7 V			
		V_{CC} = 2.7 V to 3.6 V		0.8	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		Tri-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V			mA
		V_{CC} = 2.3 V			
		V_{CC} = 2.7 V		–12	
		V_{CC} = 3 V		–24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V			mA
		V_{CC} = 2.3 V			
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		–55	125	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. For more information, see the *Implications of Slow or Floating CMOS Inputs* application report.

6.5 Thermal Information

THERMAL METRIC(1)		SN74LVCH245A								UNIT
		DB	DGV	DW	NS	PW	RGY	ZQN	ZXY	
		20 PINS								
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.5	114.7	88.3	74.7	102.5	41.4	129.3	123.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.2	29.8	51.1	40.5	35.9	47.7	75.3	58.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	56.2	50.9	42.3	53.5	17.1	77.6	74.8	
ψ_{JT}	Junction-to-top characterization parameter	18.1	0.8	20.0	14.3	2.2	1.4	2.6	2.0	
ψ_{JB}	Junction-to-board characterization parameter	49.2	55.5	50.5	41.9	52.9	17.1	73.2	74.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	9.8	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

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6.6 Electrical Characteristics: SN74LVCH245A

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	–40°C TO 85°C			–40°C TO 125°C			UNIT
					MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{OH}	High-level output voltage	I_{OH} = –100 µA		1.65 V to 3.6 V	V_{CC} – 0.2			V_{CC} – 0.2			V
		I_{OH} = –4 mA		1.65 V	1.2			1.2			
		I_{OH} = –8 mA		2.3 V	1.7			1.7			
		I_{OH} = –12 mA		2.7 V	2.2			2.2			
				3 V	2.4			2.4			
		I_{OH} = –24 mA		3 V	2.2			2.2			
V_{OL}	Low-level output voltage	I_{OL} = 100 µA		1.65 V to 3.6 V			0.2			0.20	V
		I_{OL} = 4 mA		1.65 V			0.45			0.45	
		I_{OL} = 8 mA		2.3 V			0.7			0.7	
		I_{OL} = 12 mA		2.7 V			0.4			0.4	
		I_{OL} = 24 mA		3 V			0.55			0.55	
I_I	Input current	Control inputs: V_I = 0 to 5.5 V		3.6 V			±5			±5	µA
I_{off}	Input and output power-off leakage current	V_I or V_O = 5.5 V		0 V			±10			±20	µA
$I_{I(hold)}$	Input hold current	V_I = 0.58 V		1.65 V	25			25			µA
		V_I = 1.07 V			–25			–25			
		V_I = 0.7 V		2.3 V	45			45			
		V_I = 1.7 V			–45			–45			
		V_I = 0.8 V		3 V	75			75			
		V_I = 2 V			–75			–75			
		V_I = 0 to 3.6 V(2)		3.6 V			±500			±500	
I_{OZ}(3)	High-impedance state output current	V_O = 0 V or (V_{CC} to 5.5 V)		2.3 V to 3.6 V			±5			±15	µA
I_{CC}	Supply current	V_I = V_{CC} or GND	I_O = 0	3.6 V			10			10	µA
		3.6 V ≤ V_I ≤ 5.5 V(4)	I_O = 0	3.6 V			10			10	
ΔI_{CC}	Supply-current change	One input at V_{CC} – 0.6 V, other inputs at V_{CC} or GND		2.7 V to 3.6 V			500			500	µA
C_i	Input capacitance	Control inputs: V_I = V_{CC} or GND		3.3 V		4					pF
C_{io}	Input and output capacitance	A or B port: V_O = V_{CC} or GND		3.3 V		5.50					pF

(1) All typical values are V_{CC} = 3.3 V, T_A = 25°C.
(2) The bus-hold maximum dynamic current requirement to switch the input from one state to another state.
(3) For the total leakage current in an I/O port, see the $I_{I(hold)}$ specification for the input voltage condition 0 V < V_I < V_{CC}, and the I_{OZ} specification for the input voltage conditions V_I = 0 V or V_I = V_{CC} to 5.5 V. A bus-hold current with an input voltage greater than V_{CC} is negligible.
(4) This only applies when in a disabled state.

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6.7 Electrical Characteristics: SN54LVCH245A

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –100 µA		2.7 V to 3.6 V	V_{CC} – 0.2			V
		I_{OH} = –12 mA		2.7 V	2.2			
				3 V	2.4			
		I_{OH} = –24 mA		3 V	2.2			
V_{OL}	Low-level output voltage	I_{OL} = 100 µA		2.7 V to 3.6 V			0.2	V
		I_{OL} = 12 mA		2.7 V			0.4	
		I_{OL} = 24 mA		3 V			0.55	
I_I	Input current	Control inputs: V_I = 0 to 5.5 V		3.6 V			±5	µA
$I_{I(hold)}$	Input hold current	V_I = 0.8 V		3 V	75			µA
		V_I = 2 V			–75			
		V_I = 0 to 3.6 V(2)		3.6 V			±500	
I_{OZ}(3)	High-impedance state output current	V_O = 0 V or (V_{CC} to 5.5 V)		2.3 V to 3.6 V			±15	µA
I_{CC}	Supply current	V_I = V_{CC} or GND	I_O = 0	3.6 V			10	µA
		3.6 V ≤ V_I ≤ 5.5 V(4)	I_O = 0	3.6 V			10	
ΔI_{CC}	Supply-current change	One input at V_{CC} – 0.6 V, other inputs at V_{CC} or GND		2.7 V to 3.6 V			500	µA
C_i	Input capacitance	Control inputs: V_I = V_{CC} or GND		3.3 V		4	12	pF
C_{io}	Input and output capacitance	A or B port: V_O = V_{CC} or GND		3.3 V		5.5	12	pF

(1) All typical values are V_{CC} = 3.3 V, T_A = 25°C.
(2) The bus-hold maximum dynamic current requirement to switch the input from one state to another state.
(3) For the total leakage current in an I/O port, see the $I_{I(hold)}$ specification for the input voltage condition 0 V < V_I < V_{CC}, and the I_{OZ} specification for the input voltage conditions V_I = 0 V or V_I = V_{CC} to 5.5 V. A bus-hold current with an input voltage greater than V_{CC} is negligible.
(4) This only applies when in a disabled state.

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6.8 Switching Characteristics: SN74LVCH245A, –40°C TO 85°C

over recommended operating free-air temperature range (unless otherwise noted) (see Parameter Measurement Information)

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay time	Input A or B to B or A output		12.7		8.3		7.3	1.5	6.3	ns
t_{en}	Enable time	Input $\overline{OE}$ to A or B output		15.3		10.5		9.5	1.5	8.5	ns
t_{dis}	Disable time	Input $\overline{OE}$ to A or B output		17		9.5		8.5	1.5	7.5	ns
$t_{sk(o)}$	Output skew			1		1		1		1	ns

6.9 Switching Characteristics: SN74LVCH245A, –40°C TO 125°C

over recommended operating free-air temperature range (unless otherwise noted) (see Parameter Measurement Information)

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay time	Input A or B to B or A output		13.7		9.1		7.8	1.5	6.7	ns
t_{en}	Enable time	Input $\overline{OE}$ to A or B output		16.8		12		10	1.5	9.1	ns
t_{dis}	Disable time	Input $\overline{OE}$ to A or B output		18		10.5		8.7	1.5	7.8	ns
t_{PLH}	Propagation delay time (low-level to high-level output)	Input A to Y output C_L = 50 pF	5.4	7.5	1	8.5	1	8.5	1	9.5	ns
t_{PHL}	Propagation delay time (high-level to low-level output)	Input A to Y output C_L = 50 pF	5.4	7.5	1	8.5	1	8.5	1	9.5	
t_{PZH}	Enable time (to high level)	Input $\overline{OE}$ to Y output C_L = 50 pF	6.2	9.3	1	10.5	1	10.5	1	11.5	ns
t_{PZL}	Enable time (to low level)	Input $\overline{OE}$ to Y output C_L = 50 pF	6.2	9.3	1	10.5	1	10.5	1	11.5	
t_{PHZ}	Disable time (to high level)	Input $\overline{OE}$ to Y output C_L = 50 pF	6.7	9.2	1	10.5	1	10.5	1	11	ns
t_{PLZ}	Disable time (to low level)	Input $\overline{OE}$ to Y output C_L = 50 pF	6.7	9.2	1	10.5	1	10.5	1	11	
$t_{sk(o)}$	Output skew	C_L = 50 pF		1 (1)		1		1		1	ns

(1) With products compliant to MIL-PRF-38535, this parameter does not apply.

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6.10 Switching Characteristics: SN54LVCH245A

over recommended operating free-air temperature range (unless otherwise noted) (see Parameter Measurement Information)

PARAMETER		TEST CONDITIONS	V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	Propagation delay time	Input A or B to B or A output		8	1	7	ns
t_{en}	Enable time	Input $\overline{OE}$ to A or B output		9.5	1	8.5	ns
t_{dis}	Disable time	Input $\overline{OE}$ to A or B output		8.5	1	7.5	ns

6.11 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per transceiver	f = 10 MHz	Outputs enabled	42	43	47	pF
			Outputs disabled	1	1	2	

6.12 Typical Characteristics

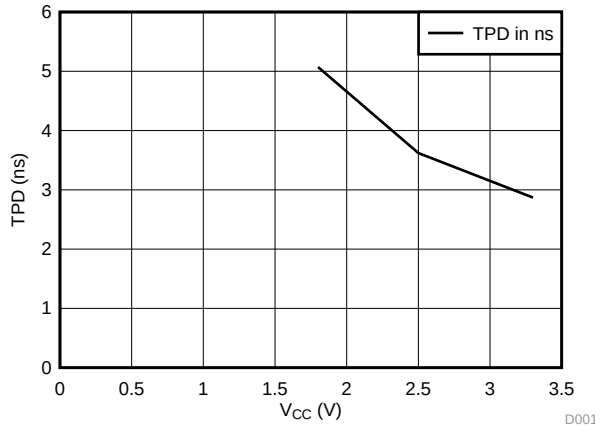


Figure 1. SN74LVCH245A TPD Across V_{CC} at 25°C

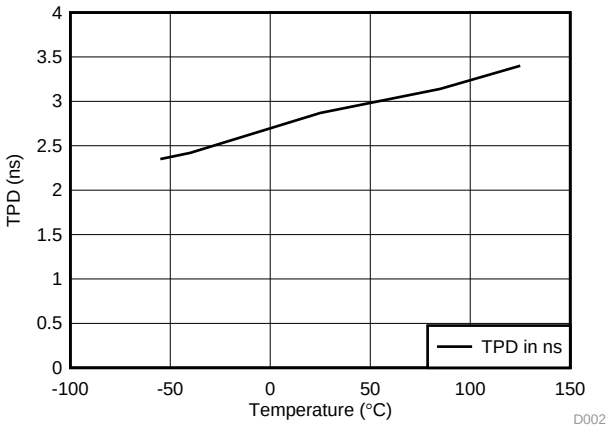


Figure 2. SN74LVCH245A TPD Across Temperature at 3.3 V

7 Parameter Measurement Information

(1) C_L includes probe and jig capacitance.

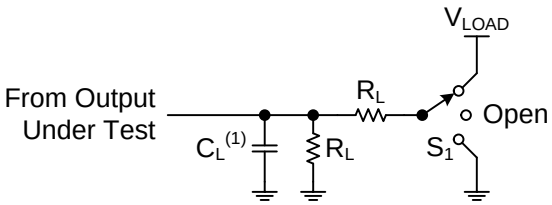


Figure 3. Load Circuit

Table 1. Test Load Switch Position

TEST	S_1
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	V_{LOAD}
t_{PHZ} / t_{PZH}	GND

Table 2. Test and Measurement Conditions

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤ 2 ns	V_{CC} / 2	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤ 2 ns	V_{CC} / 2	2 × V_{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V

(1) Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

(2) t_{PZL} and t_{PZH} are the same as t_{en}.

(3) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

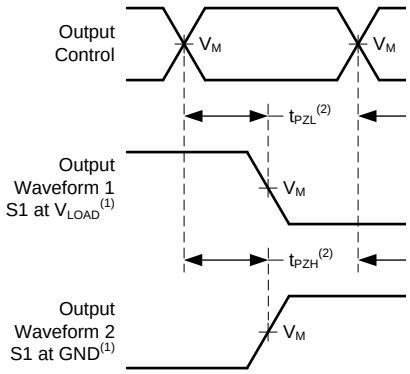


Figure 4. Voltage Waveforms Enable and Disable Times Low- and High-Level Enabling

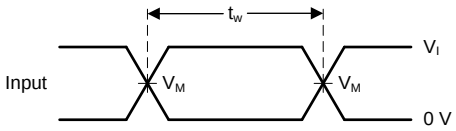


Figure 5. Voltage Waveforms Pulse Duration

(1) t_{PLH} and t_{PHL} are the same as t_{pd}.

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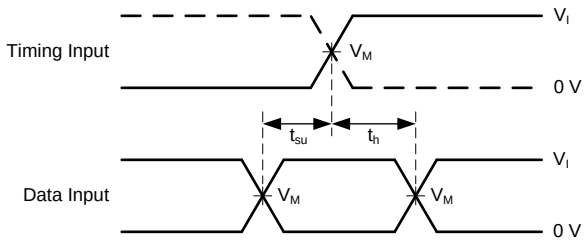


Figure 6. Voltage Waveforms Setup and Hold Times

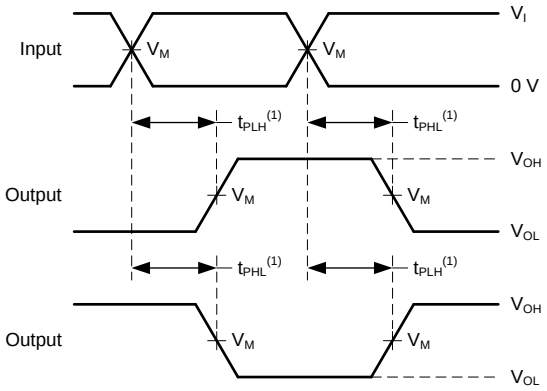


Figure 7. Voltage Waveforms Propagation Delay Times Inverting and Noninverting Outputs

8 Detailed Description

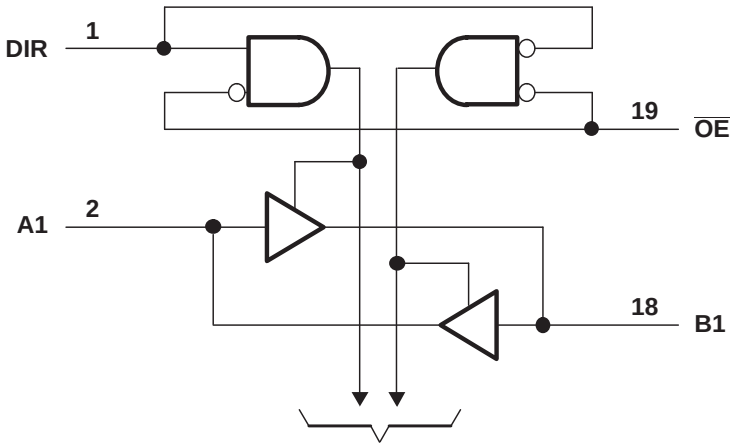
8.1 Overview

The SN54LVCH245A octal bus transceiver is designed for a 2.7-V to 3.6-V V_{CC} operation, and the SN74LVCH245A octal bus transceiver is designed for a 1.65-V to 3.6-V V_{CC} operation. Inputs can be driven from either the 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V or 5-V system environment.

These devices are designed for asynchronous communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device, so the buses are effectively isolated.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs which prevents damaging current backflow through the devices when they are powered down. To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. The bus-hold circuitry is part of the input circuit and is not disabled by $\overline{OE}$ or DIR, so use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads, so routing and load conditions should be taken into consideration to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. The power output of the device must be limited to avoid thermal runaway and damage caused by over-current. Follow the electrical and thermal limits defined in the Absolute Maximum Ratings at all times.

8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance, and these inputs are typically modeled as a resistor in parallel with the input capacitance given in the Electrical Characteristics: SN74LVCH245A. The worst case resistance is calculated with the maximum input voltage, given in the Absolute Maximum Ratings , and the maximum input leakage current, given in the Electrical Characteristics: SN74LVCH245A, using ohm's law (R = V ÷ I).

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Feature Description (continued)

Signals applied to the inputs need to have fast edge rates, as defined by Δt/Δv in Recommended Operating Conditions: SN54LVCH245A to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

8.3.3 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as depicted in Figure 8.

CAUTION

Voltages beyond the values specified in the Absolute Maximum Ratings table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

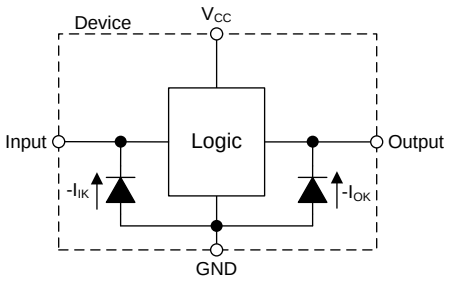


Figure 8. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Bus-Hold Data Inputs

Each data input on this device includes a weak latch that maintains a valid logic level on the input. The state of these latches is unknown at startup and remains unknown until the input has been forced to a valid high or low state. After data has been sent through a channel, the latch then maintains the previous state on the input if the line is left floating.

NOTE

It is highly recommended to not use pull-up or pull-down resistors together with a bus-hold input.

Bus-hold data inputs prevent floating inputs on this device. The *Implications of Slow or Floating CMOS Inputs* application report explains the problems associated with leaving CMOS inputs floating.

These latches remain active at all times, independent of output disable signals such as direction selection or output enables.

The *Bus-Hold Circuit* application report has additional details regarding bus-hold inputs.

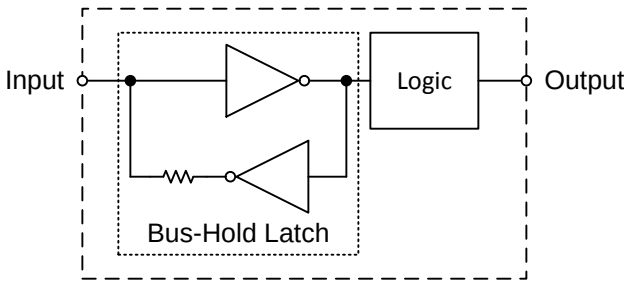


Figure 9. Simplified Schematic For Device With Bus-Hold Data Inputs

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Feature Description (continued)

8.3.5 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the Electrical Characteristics: SN74LVCH245A.

8.3.6 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage, as long as the input signals remain below the maximum input voltage value specified in the Recommended Operating Conditions: SN54LVCH245A .

8.3.7 Output Enable

This device has an output enable (OE) pin that functions according to . When the outputs of the device are disabled, they are placed into a high impedance state where it will neither source nor sink current. High-impedance outputs are also commonly referred to as three-state or tri-state outputs. The maximum leakage for the output in this state is defined by I_{OZ} in the Electrical Characteristics: SN74LVCH245A table.

8.4 Device Functional Modes

Table 3. Function Table

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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9 Application and Implementation

9.1 Application Information

The SN74LVCH245A device is a high-drive CMOS device with bus-hold inputs that can be used for a multitude of bus interface type applications where the data needs to be transmitted and received. The device's output can produce 24 mA of drive current at 3.3 V. Therefore, this device is ideal for driving multiple outputs and for high-speed applications up to 100 MHz. The inputs are 5.5-V tolerant which allows the devices to translate down to V_{CC}.

Figure 10 shows a typical down-translation application in which the device is being used with a fixed direction to reduce an 8-bit 5-V bus to an 8-bit 1.8-V bus.

Figure 11 shows a typical application in which a bus must switch directions for data transfer between a master and a slave device. The SN74LVCH245A allows either V_{CC1} or V_{CC3} to be shut down completely because it has bus-hold inputs that maintains valid states on the floating lines. In this example, V_{CC1}, V_{CC2}, and V_{CC3} all have the same value, but each supply can be delivered by a separate source.

Figure 12 shows a functional diagram for a single channel of the device, including the bus-hold, direction, and output enable logic components. When the direction is set as 'A to B,' the buffer labeled 'A' is disabled and the buffer labeled 'B' is enabled. When the direction is set as 'B to A,' the buffer labeled 'B' is disabled and the buffer labeled 'A' is enabled. When the output enable pin is deasserted, the buffers labeled 'A' and 'B' are both disabled. The bus-hold circuitry remains active at all times.

9.2 Typical Application

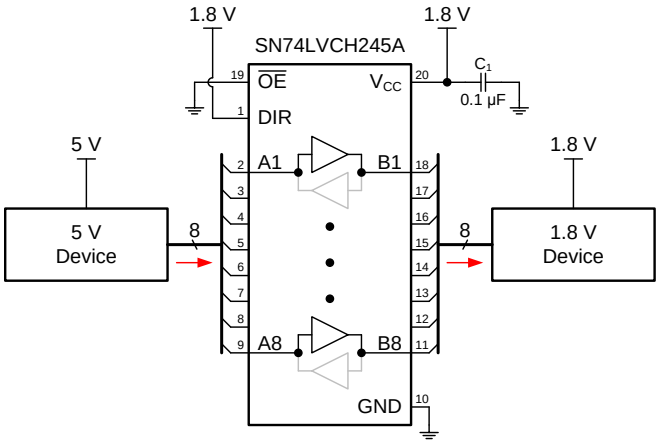


Figure 10. Typical Down-Translation Application

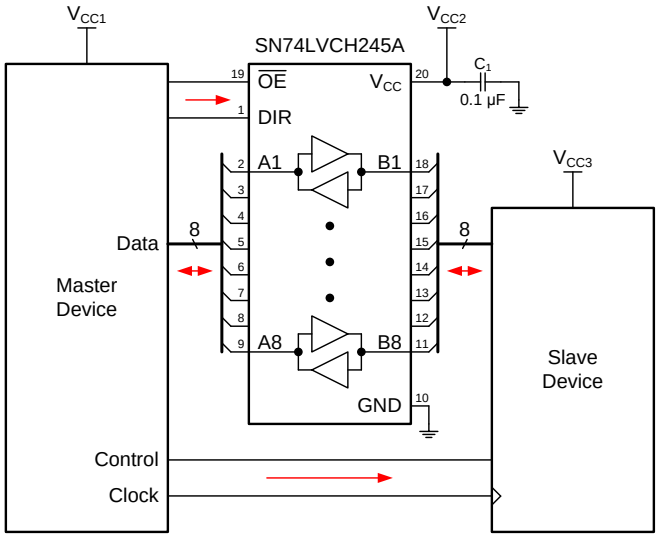


Figure 11. Typical Direction Controlled Application

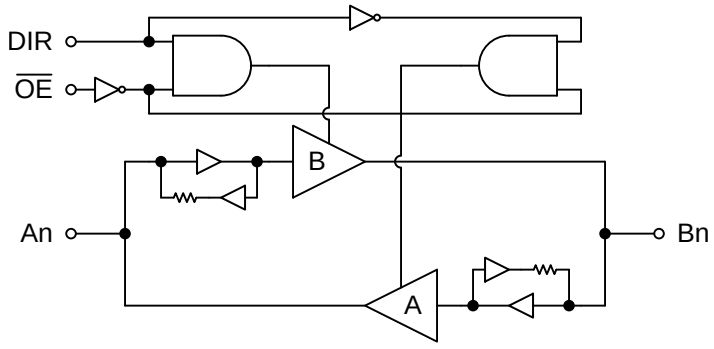


Figure 12. Equivalent Internal Schematic Including Bus-Hold Inputs

Typical Application (continued)

9.2.1 Design Requirements

This device uses CMOS technology and has a balanced output drive. Care should be taken to avoid bus contention because the device's output can drive currents that exceed maximum limits. The high drive also creates fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

This device has bus-hold inputs, which are always active regardless of DIR or $\overline{OE}$ input values. For more information, refer to the Bus-Hold Data Inputs.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions
   - See ($\Delta t/\Delta V$) in the Recommended Operating Conditions: SN54LVCH245A table for the input transition rate specification.
   - See (V_{IH} and V_{IL}) in the Recommended Operating Conditions: SN54LVCH245A table for the input voltage high level and input voltage low level specifications.
   - The inputs are overvoltage tolerant. This allows them to rise up to 5.5 V at any valid V_{CC}.
   - The inputs can be left floating. The internal bus-hold circuits maintains the last valid state at the inputs.
2. Recommended Output Conditions
   - Do not exceed 25 mA per output and 50 mA in total for the device.
   - Do not pull outputs above V_{CC}.

9.2.3 Application Curves

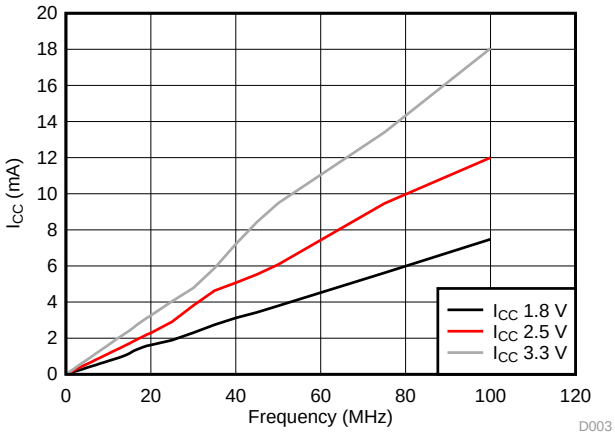


Figure 13. I_{CC} vs Frequency

10 Power Supply Recommendations

The Recommended Operating Conditions: SN54LVCH245A table shows the power supply can be any voltage between the minimum and maximum supply voltage rating that are listed.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended; if there are multiple V_{CC} pins, then 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different noise frequencies. A 0.1 µF and a 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

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11 Layout

11.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused. For example, when two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 14 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally, they will be tied to GND or V_{CC}, the deciding factor is based on whichever makes more sense or is more convenient at the time. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, then asserting the output enable pin will disable the output section of the part. This will not disable the input section of the I/Os, so they cannot float when disabled.

11.2 Layout Example

Figure 14 shows an example layout for the ZXY package. This package has a 0.5-mm pitch and requires either micro-vias or very small traces to access the center pins. In this example, 4-mil vias with 10-mil pads are used to access the center pins. All pins are connected by 5-mil traces except for the supply pins which use 10-mil traces.

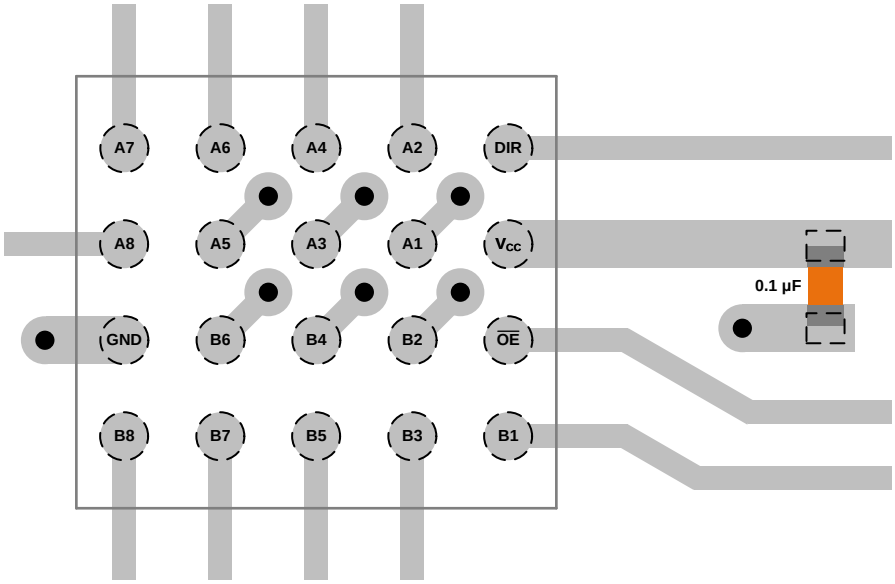


Figure 14. Example Layout of ZXY Package

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LVCH245A	Click here	Click here	Click here	Click here	Click here
SN74LVCH245A	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9754301Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754301Q2A SNJ54LVCH 245AFK
5962-9754301QRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754301QRA SNJ54LVCH245AJ
5962-9754301QSA	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754301QSA SNJ54LVCH245AW
5962-9754301V2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754301V2A SNV54LVCH 245AFK
5962-9754301VRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754301VRA SNV54LVCH245AJ
5962-9754301VSA	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754301VSA SNV54LVCH245AW
SN74LVCH245ADBR	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LCH245A
SN74LVCH245ADBR.B	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LCH245A
SN74LVCH245ADBRE4	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LCH245A
SN74LVCH245ADGVR	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LCH245A
SN74LVCH245ADGVR.B	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LCH245A
SN74LVCH245ADW	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCH245A
SN74LVCH245ADW.B	Active	Production	SOIC (DW) | 20	25 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCH245A
SN74LVCH245ADWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCH245A
SN74LVCH245ADWR.B	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCH245A
SN74LVCH245ANSR	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCH245A
SN74LVCH245ANSR.B	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVCH245A
SN74LVCH245APW	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LCH245A
SN74LVCH245APW.B	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LCH245A

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVCH245APWE4	Active	Production	TSSOP (PW) | 20	70 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LCH245A
SN74LVCH245APWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LCH245A
SN74LVCH245APWR.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LCH245A
SN74LVCH245APWRG4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LCH245A
SN74LVCH245APWRG4.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LCH245A
SN74LVCH245APWT	Active	Production	TSSOP (PW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LCH245A
SN74LVCH245APWT.B	Active	Production	TSSOP (PW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LCH245A
SN74LVCH245ARGYR	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LCH245A
SN74LVCH245ARGYR.B	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LCH245A
SN74LVCH245ARGYRG4	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LCH245A
SNJ54LVCH245AFK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754301Q2A SNJ54LVCH 245AFK
SNJ54LVCH245AJ	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754301QR A SNJ54LVCH245AJ
SNJ54LVCH245AW	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9754301QS A SNJ54LVCH245AW

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LVCH245A, SN54LVCH245A-SP, SN74LVCH245A :

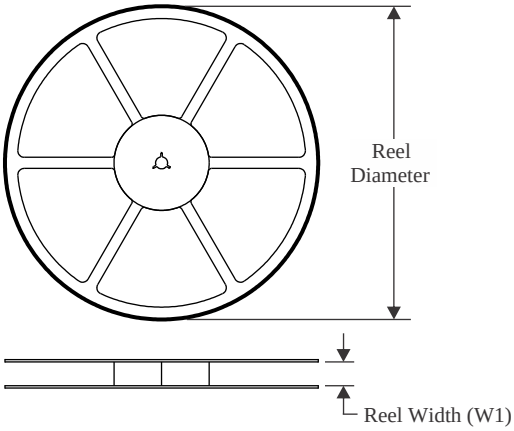
- Catalog : SN74LVCH245A, SN54LVCH245A
- Military : SN54LVCH245A
- Space : SN54LVCH245A-SP

NOTE: Qualified Version Definitions:

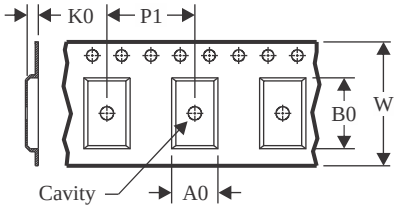
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

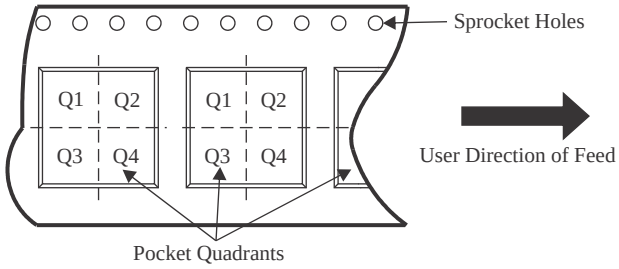


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

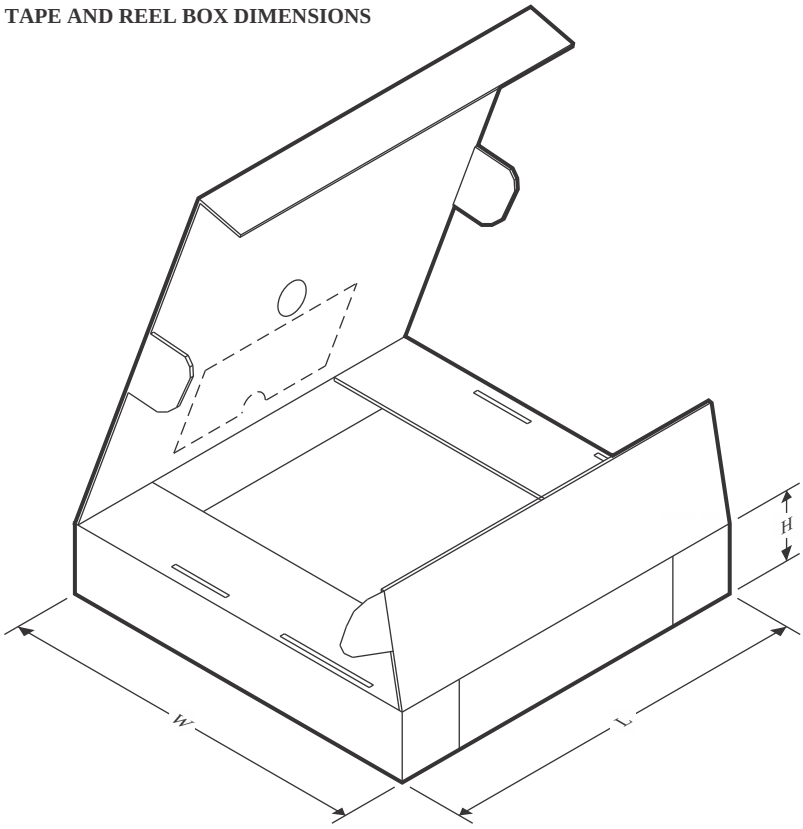
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCH245ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVCH245ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVCH245ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVCH245ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVCH245APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVCH245APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVCH245APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVCH245APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74LVCH245ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1

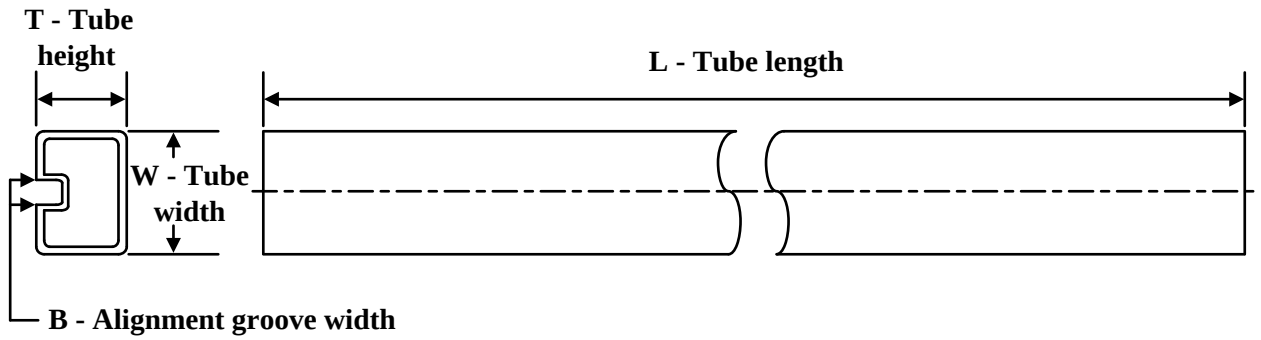
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCH245ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74LVCH245ADGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74LVCH245ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74LVCH245ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74LVCH245APWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LVCH245APWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74LVCH245APWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74LVCH245APWT	TSSOP	PW	20	250	353.0	353.0	32.0
SN74LVCH245ARGYR	VQFN	RGY	20	3000	353.0	353.0	32.0

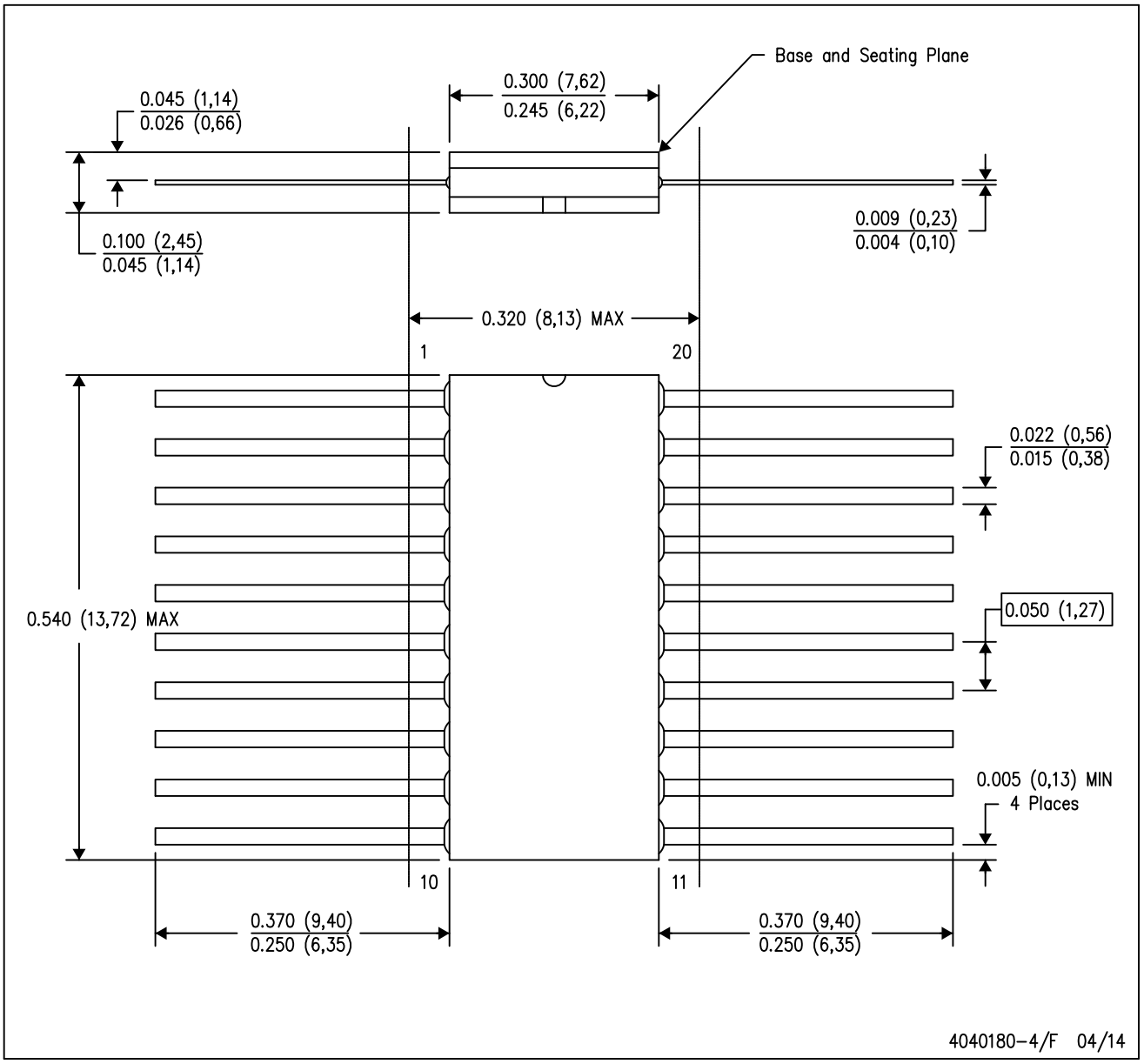
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9754301Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9754301V2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9754301VSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74LVCH245ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVCH245ADW.B	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LVCH245APW	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVCH245APW.B	PW	TSSOP	20	70	530	10.2	3600	3.5
SN74LVCH245APWE4	PW	TSSOP	20	70	530	10.2	3600	3.5
SNJ54LVCH245AFK	FK	LCCC	20	55	506.98	12.06	2030	NA

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



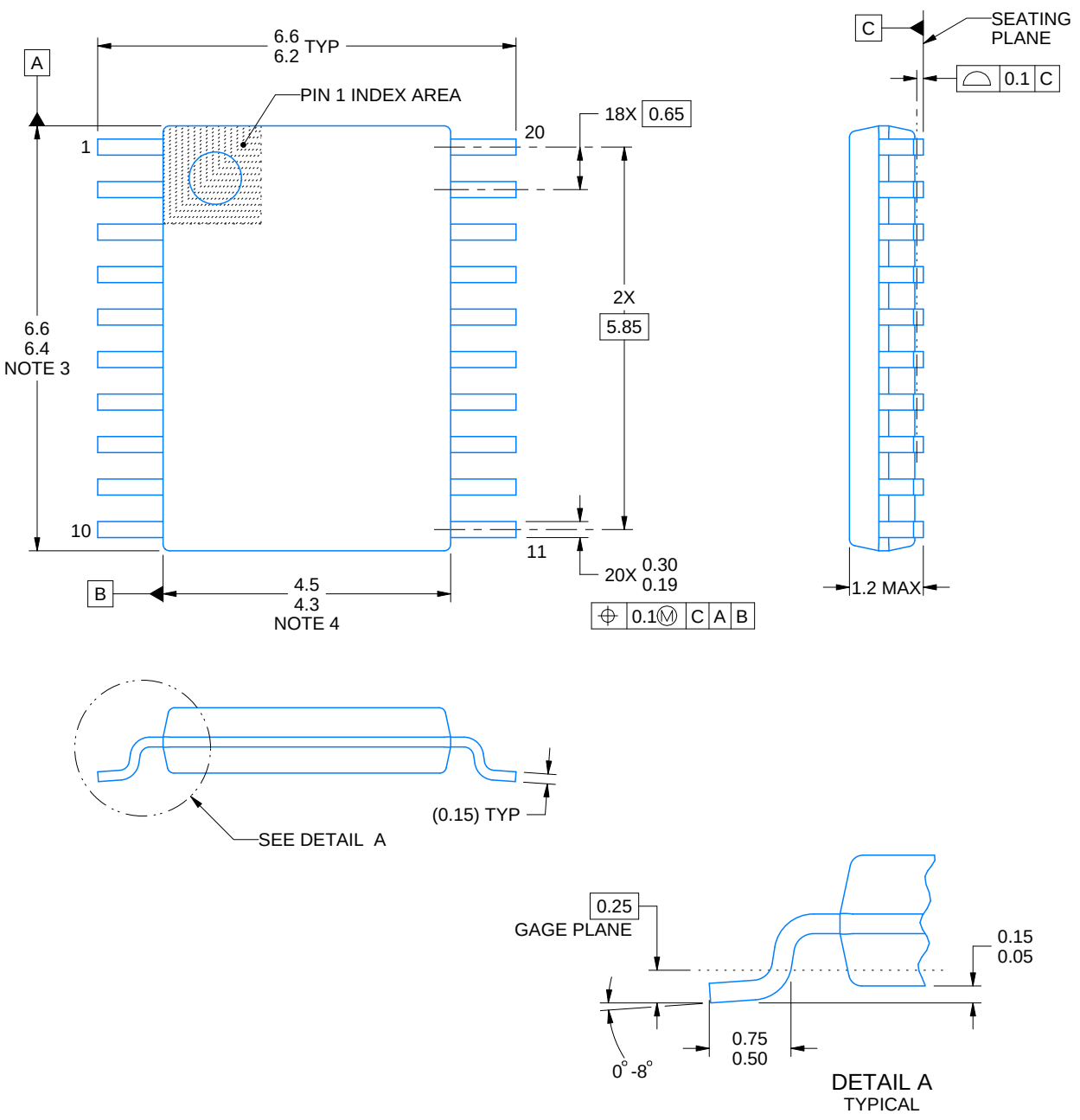
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

PACKAGE OUTLINE

PW0020A

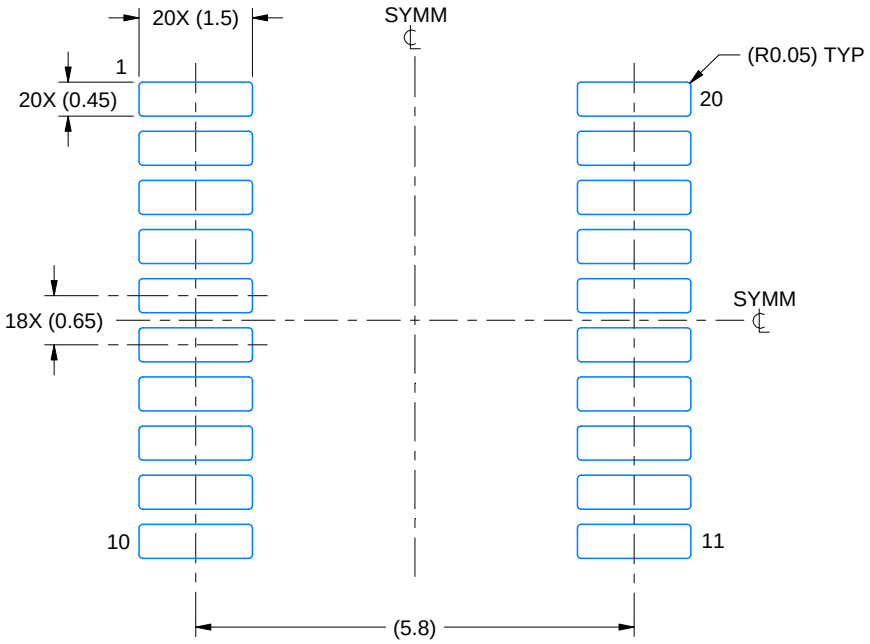
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

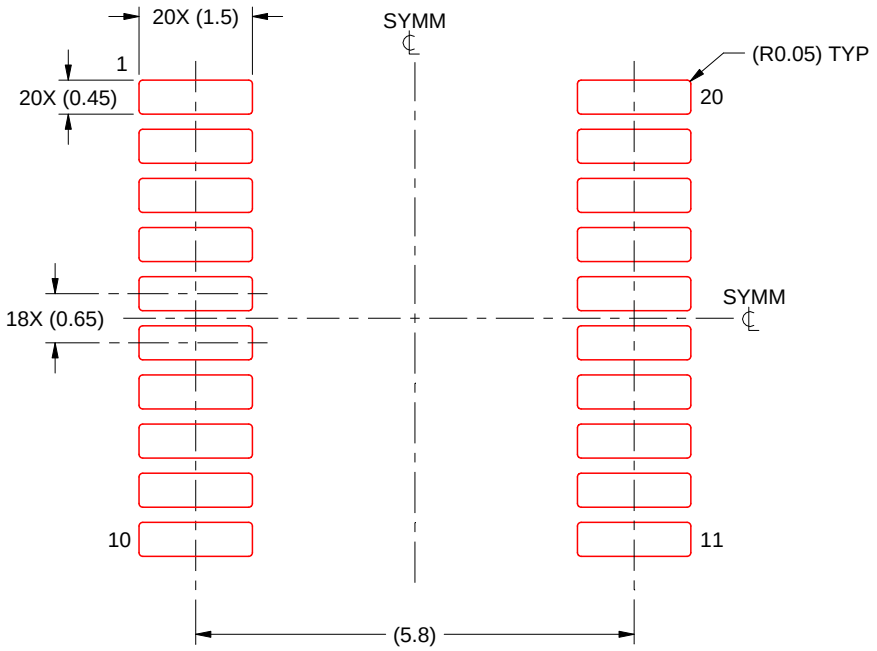


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

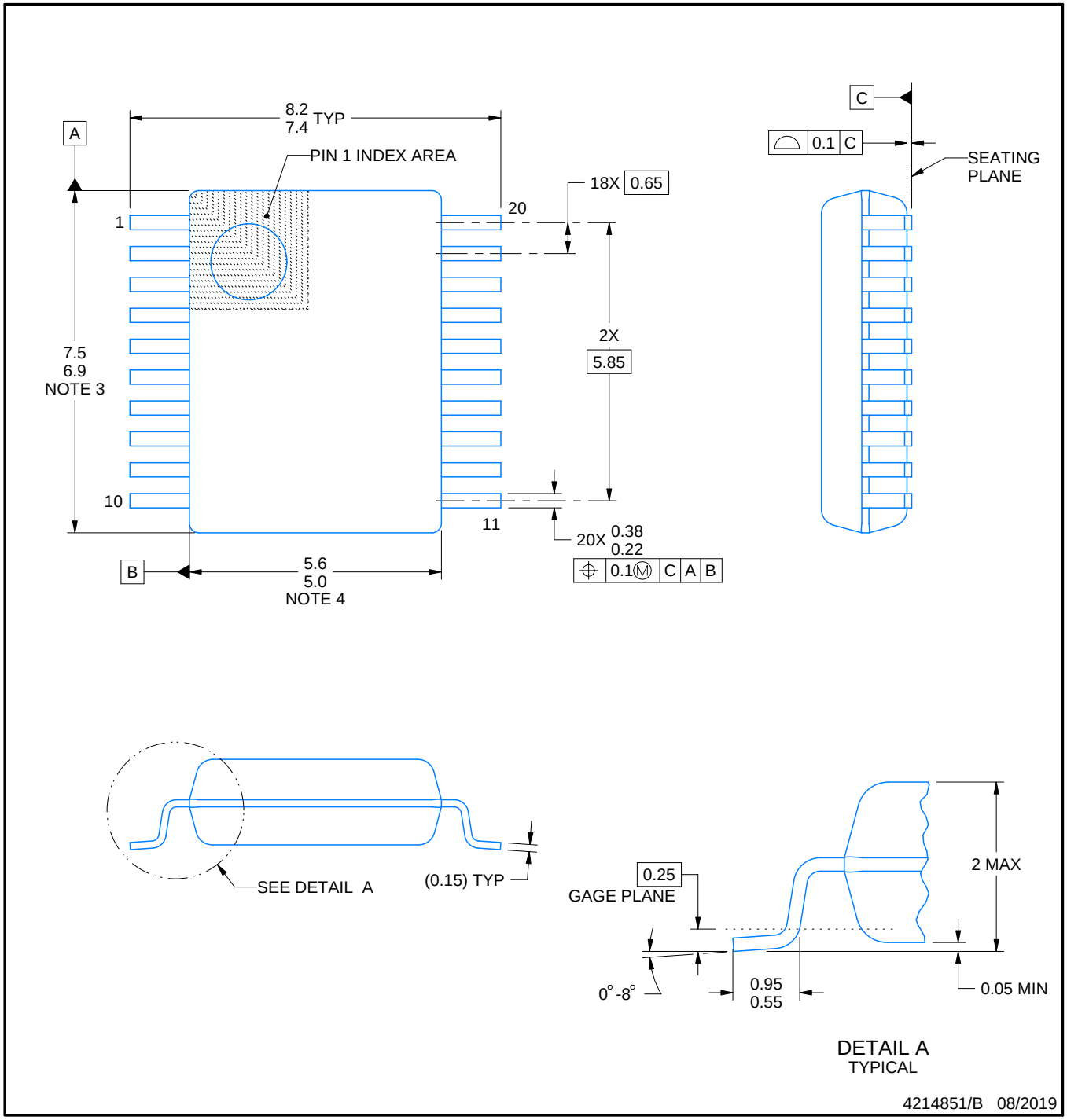
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DB0020A

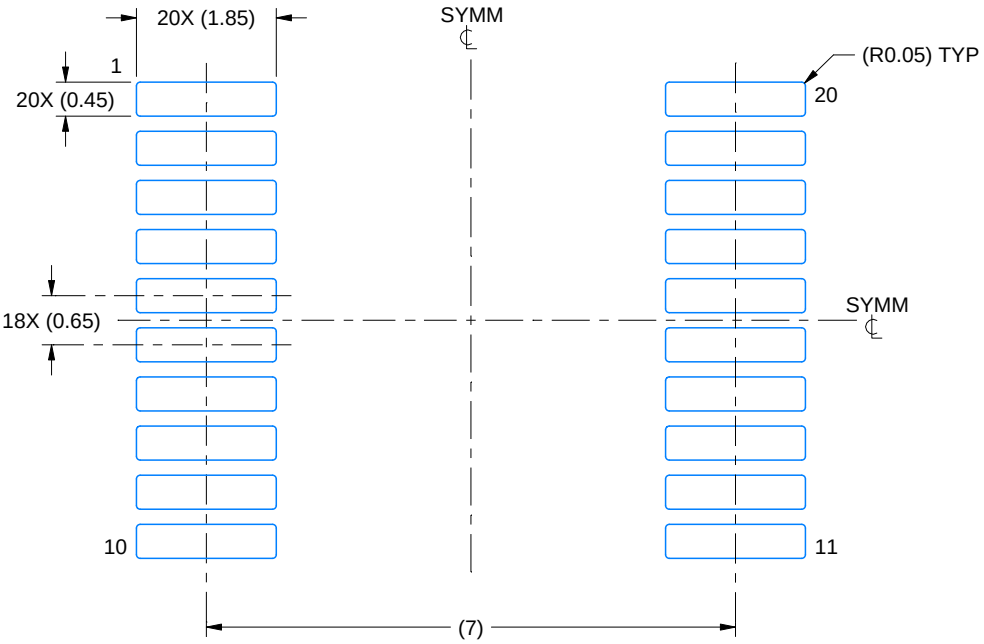
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

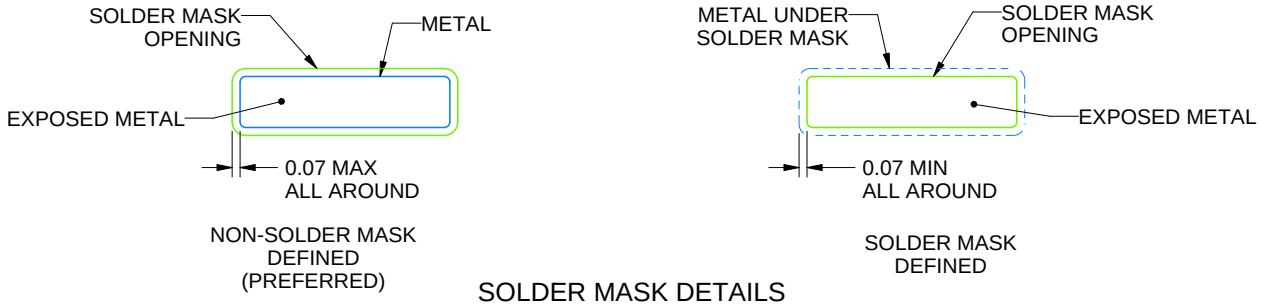


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

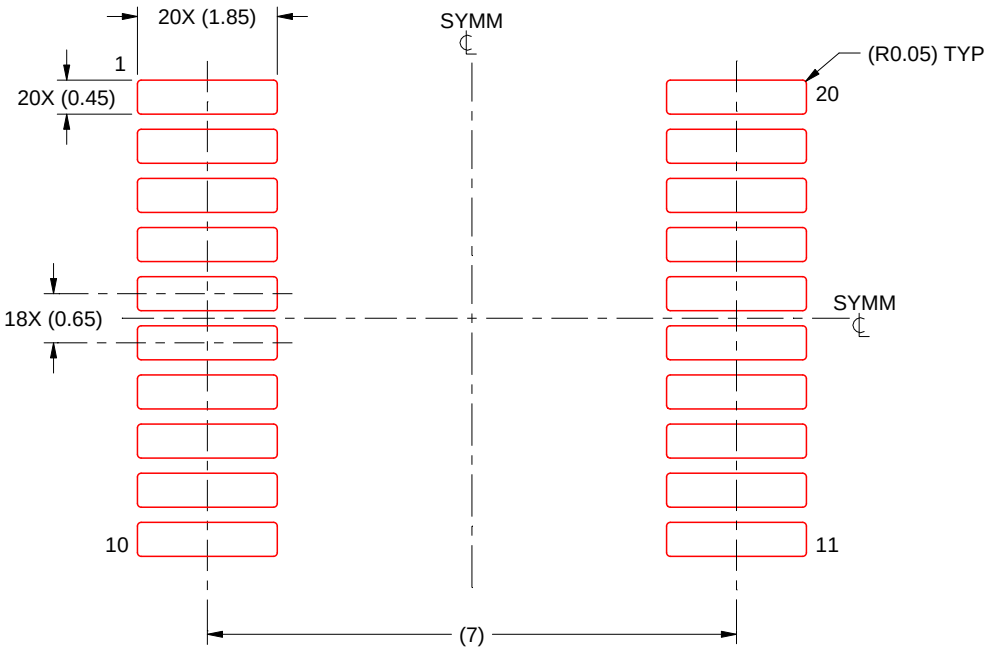
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

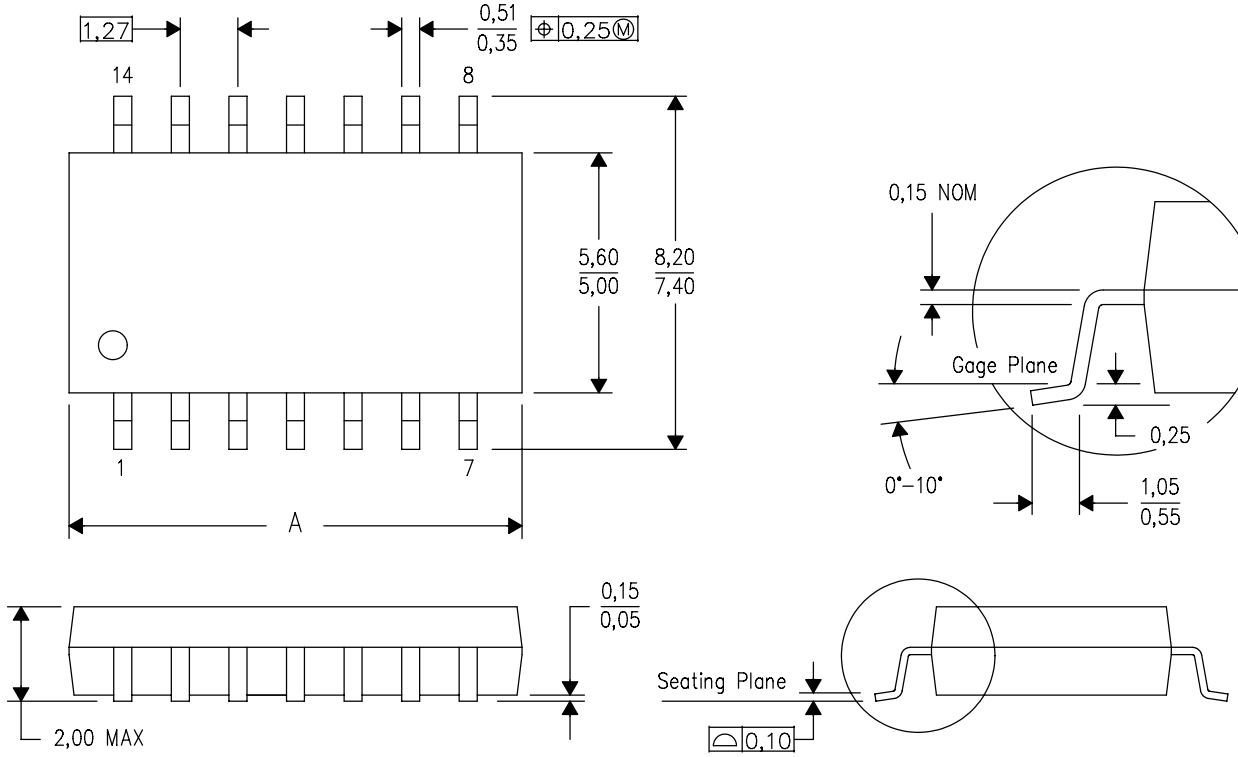
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

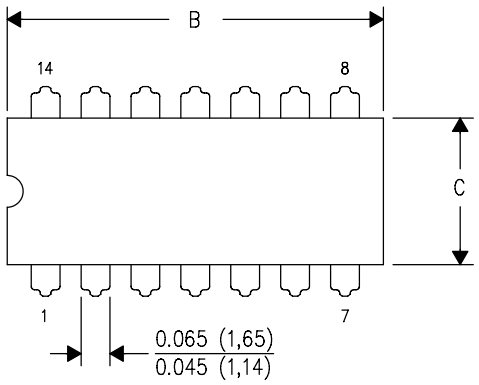
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

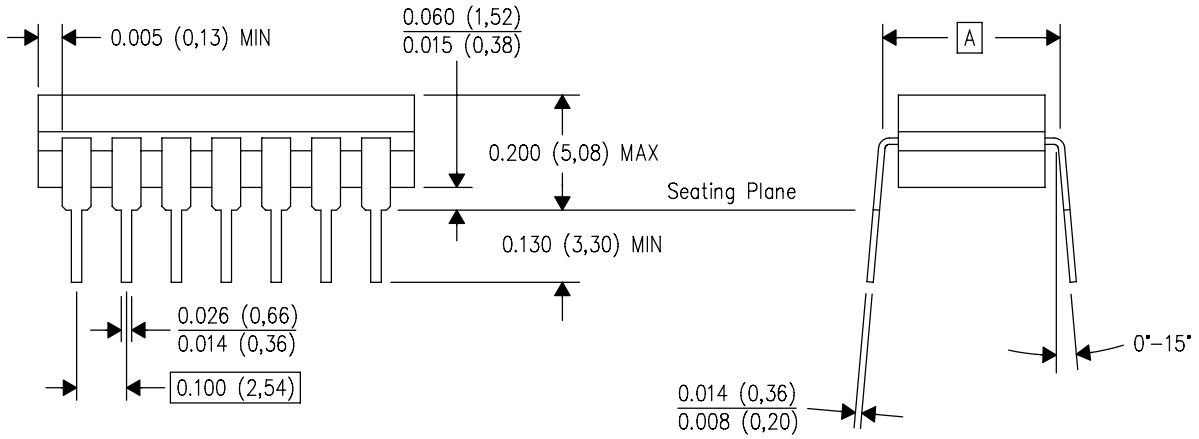
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

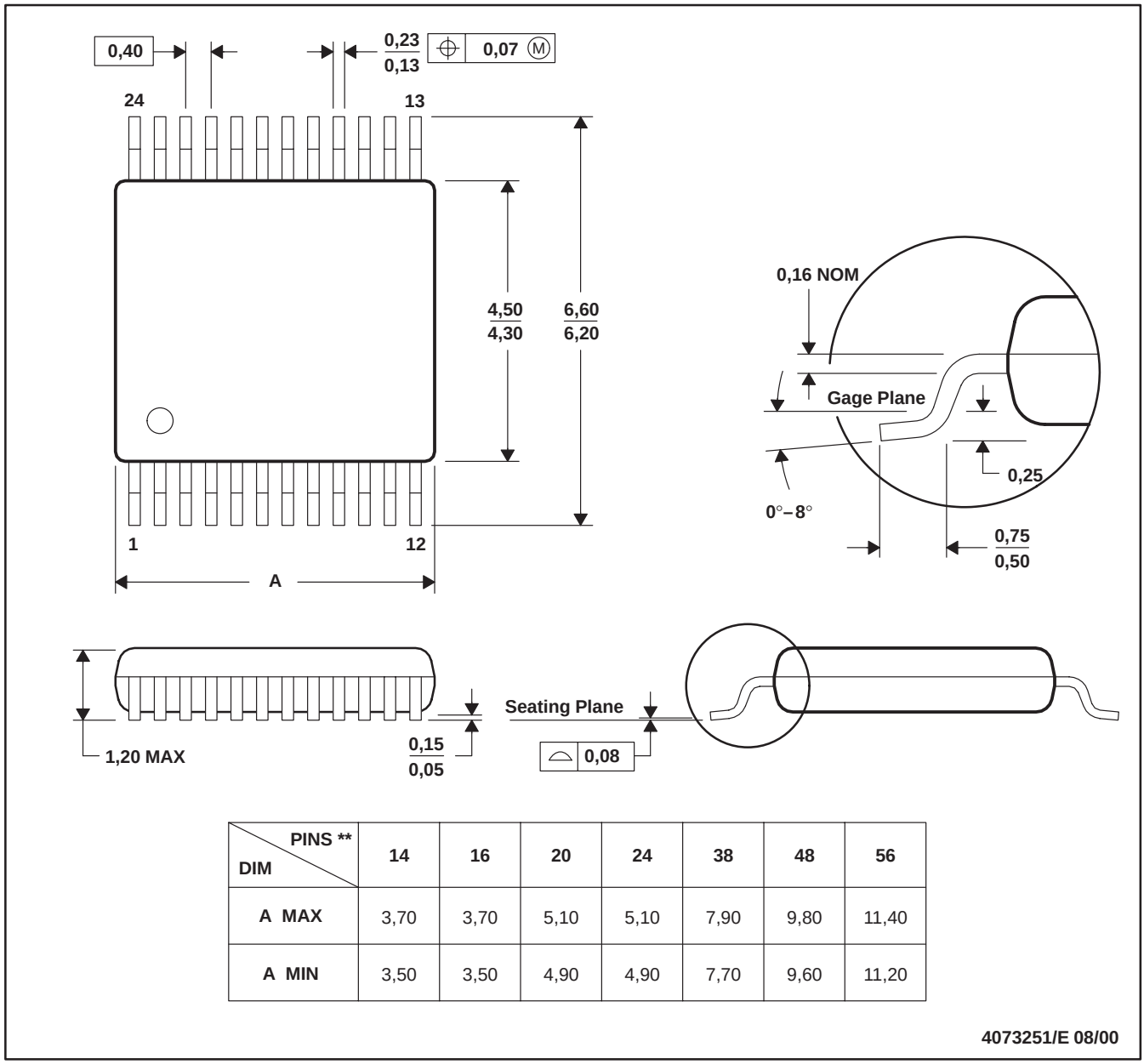


4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

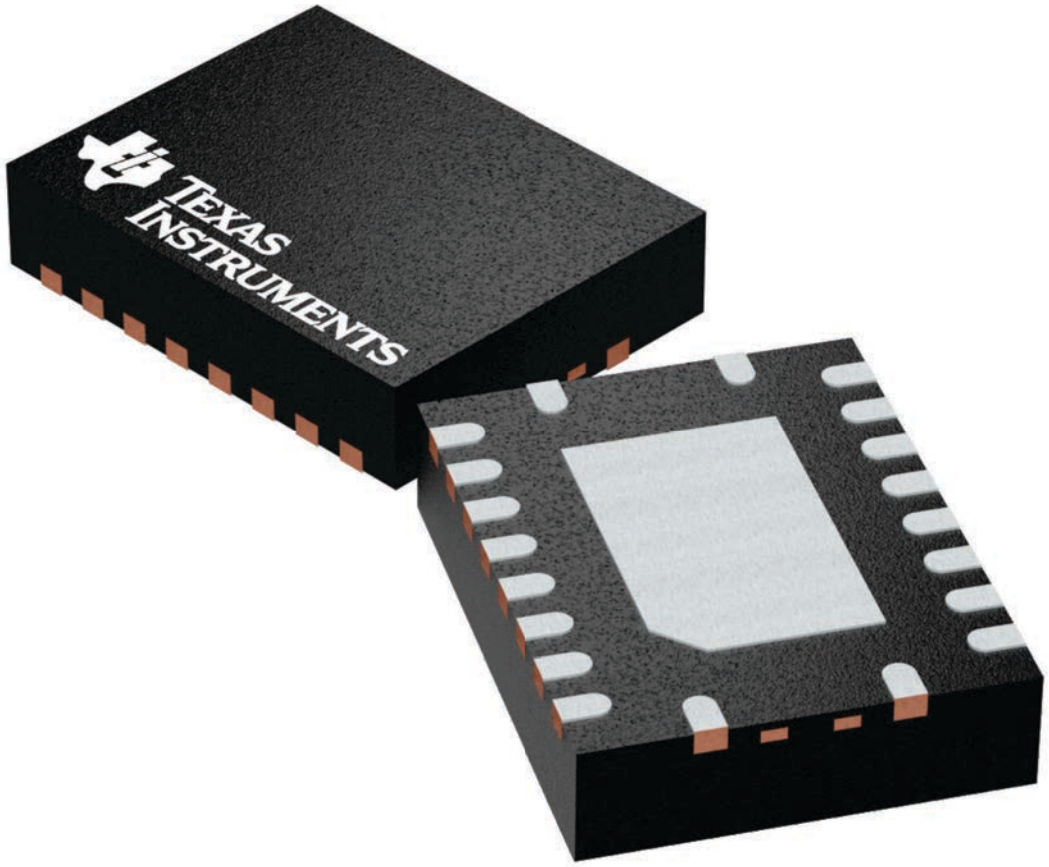
RGY 20

VQFN - 1 mm max height

3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225264/A

GENERIC PACKAGE VIEW

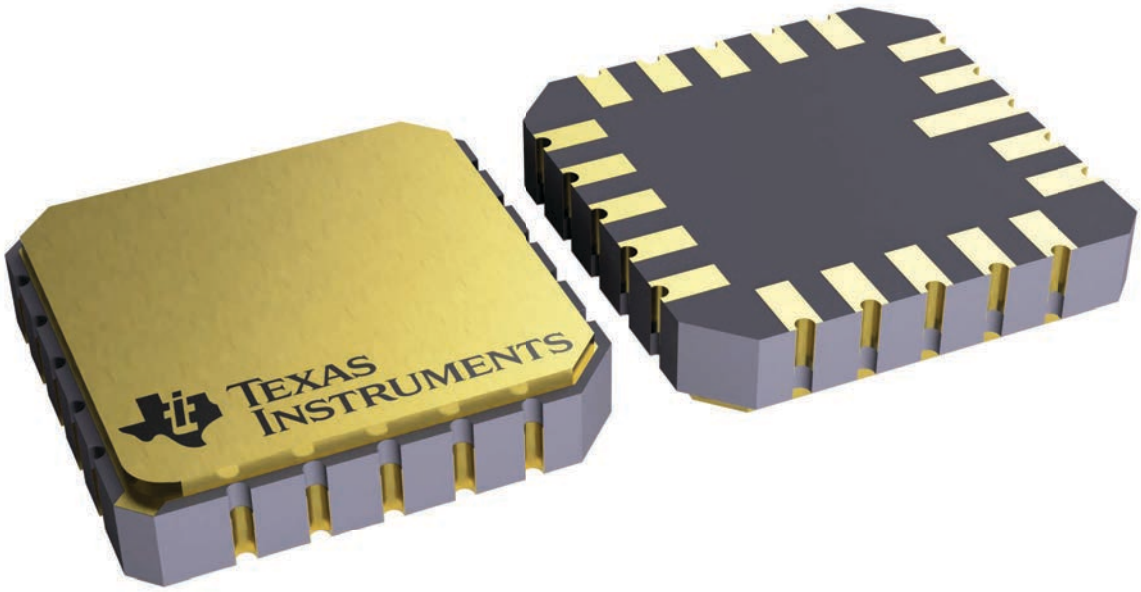
FK 20

LCCC - 2.03 mm max height

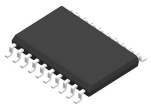
8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

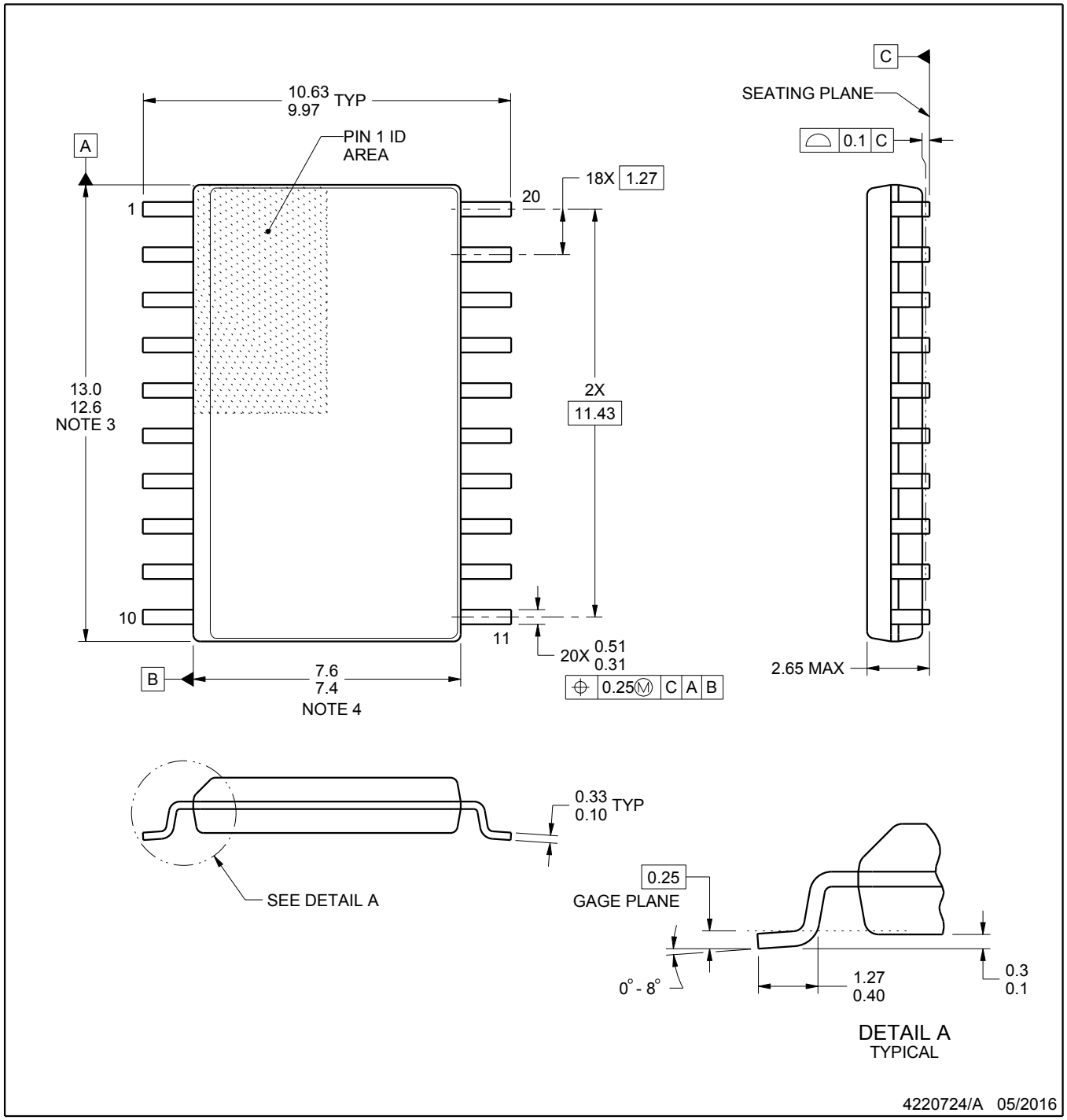


PACKAGE OUTLINE

DW0020A

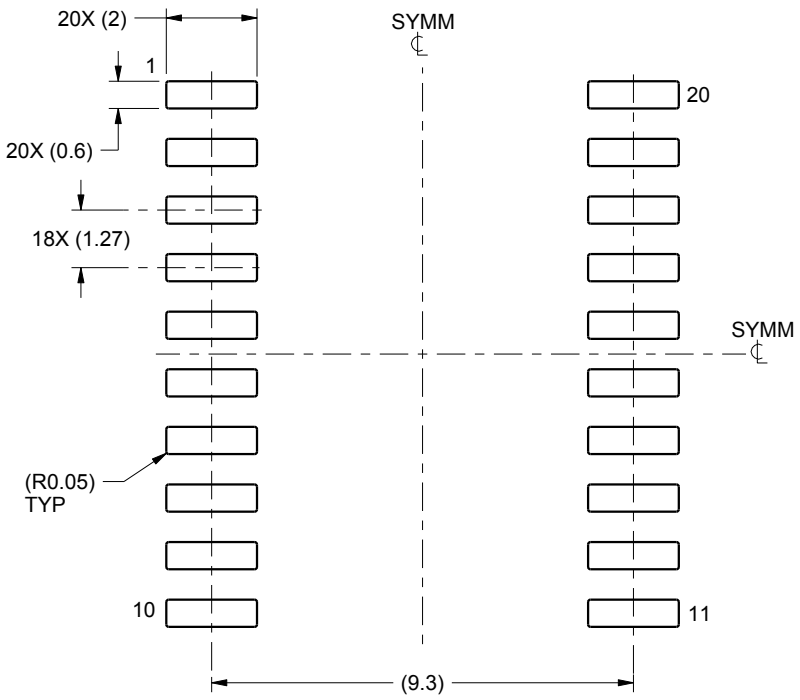
SOIC - 2.65 mm max height

SOIC

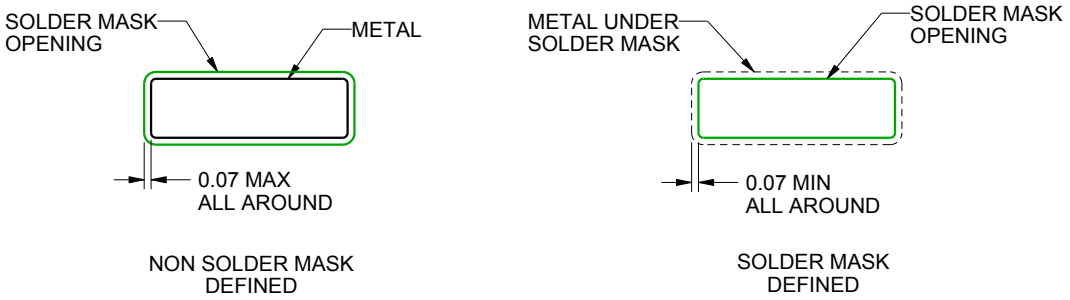


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

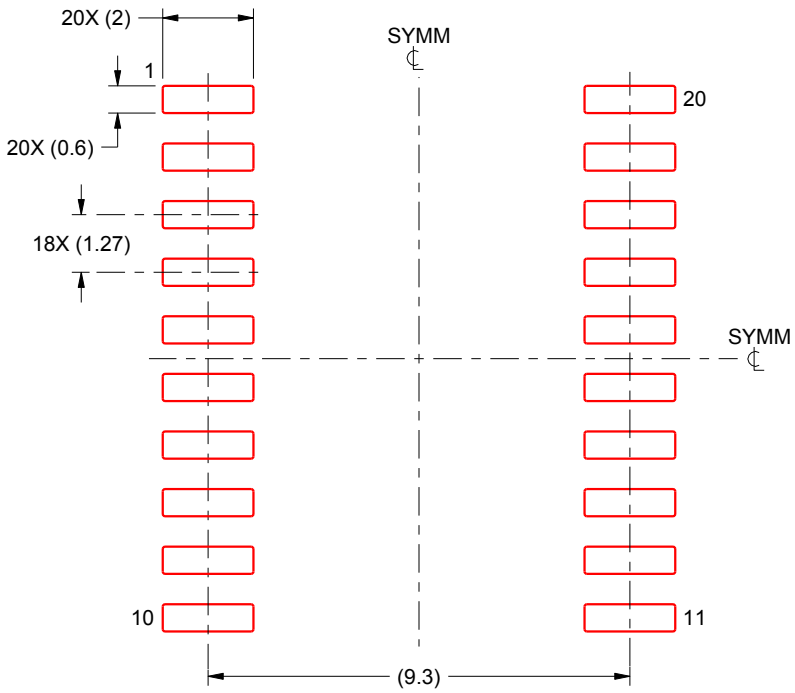


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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