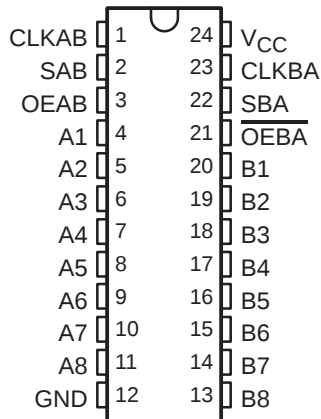


# SN54LVTH652, SN74LVTH652 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

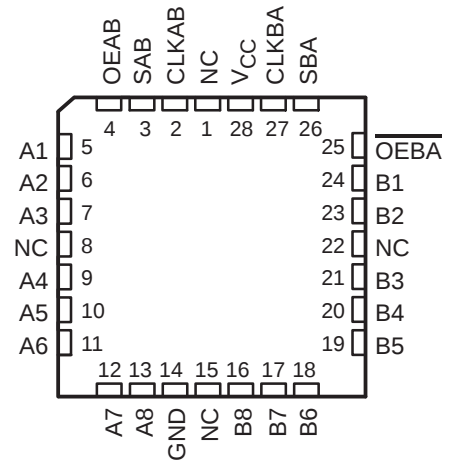
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- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

SN54LVTH652 . . . JT OR W PACKAGE  
SN74LVTH652 . . . DB, DGV, DW, NS, OR PW PACKAGE  
(TOP VIEW)



SN54LVTH652 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

These bus transceivers and registers are designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

## ORDERING INFORMATION

| $T_A$          | PACKAGE†    |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-------------|---------------|-----------------------|------------------|
| -40°C to 85°C  | SOIC – DW   | Tube          | SN74LVTH652DW         | LVTH652          |
|                |             | Tape and reel | SN74LVTH652DWR        |                  |
|                | SOP – NS    | Tape and reel | SN74LVTH652NSR        | LVTH652          |
|                | SSOP – DB   | Tape and reel | SN74LVTH652DBR        | LXH652           |
|                | TSSOP – PW  | Tube          | SN74LVTH652PW         | LXH652           |
|                |             | Tape and reel | SN74LVTH652PWR        |                  |
| -55°C to 125°C | TVSOP – DGV | Tape and reel | SN74LVTH652DGVR       | LXH652           |
|                | CDIP – JT   | Tube          | SNJ54LVTH652JT        | SNJ54LVTH652JT   |
|                | CFP – W     | Tube          | SNJ54LVTH652W         | SNJ54LVTH652W    |
|                | LCCC – FK   | Tube          | SNJ54LVTH652FK        | SNJ54LVTH652FK   |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**TEXAS  
INSTRUMENTS**

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**3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS  
WITH 3-STATE OUTPUTS**

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**description/ordering information (continued)**

The 'LVTH652 devices consist of bus-transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

Output-enable (OEAB and  $\overline{\text{OEBA}}$ ) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input selects real-time data and a high input selects stored data. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVTH652 devices.

Data on the A or B data bus, or both, can be stored in the internal D-type flip-flops by low-to-high transitions at the appropriate clock (CLKAB or CLKBA) inputs, regardless of the select- or enable-control pins. When SAB and SBA are in the real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and  $\overline{\text{OEBA}}$ . In this configuration, each output reinforces its input; therefore, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{\text{OE}}$  should be tied to  $V_{CC}$  through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

This device is fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

**FUNCTION TABLE**

| INPUTS |                          |        |        |                |                | DATA I/O <sup>†</sup>    |                          | OPERATION OR FUNCTION                             |
|--------|--------------------------|--------|--------|----------------|----------------|--------------------------|--------------------------|---------------------------------------------------|
| OEAB   | $\overline{\text{OEBA}}$ | CLKAB  | CLKBA  | SAB            | SBA            | A1–A8                    | B1–B8                    |                                                   |
| L      | H                        | H or L | H or L | X              | X              | Input                    | Input                    | Isolation                                         |
| L      | H                        | ↑      | ↑      | X              | X              | Input                    | Input                    | Store A and B data                                |
| X      | H                        | ↑      | H or L | X              | X              | Input                    | Unspecified <sup>‡</sup> | Store A, hold B                                   |
| H      | H                        | ↑      | ↑      | X <sup>‡</sup> | X              | Input                    | Output                   | Store A in both registers                         |
| L      | X                        | H or L | ↑      | X              | X              | Unspecified <sup>‡</sup> | Input                    | Hold A, store B                                   |
| L      | L                        | ↑      | ↑      | X              | X <sup>‡</sup> | Output                   | Input                    | Store B in both registers                         |
| L      | L                        | X      | X      | X              | L              | Output                   | Input                    | Real-time B data to A bus                         |
| L      | L                        | X      | H or L | X              | H              | Output                   | Input                    | Stored B data to A bus                            |
| H      | H                        | X      | X      | L              | X              | Input                    | Output                   | Real-time A data to B bus                         |
| H      | H                        | H or L | X      | H              | X              | Input                    | Output                   | Stored A data to B bus                            |
| H      | L                        | H or L | H or L | H              | H              | Output                   | Output                   | Stored A data to B bus and stored B data to A bus |

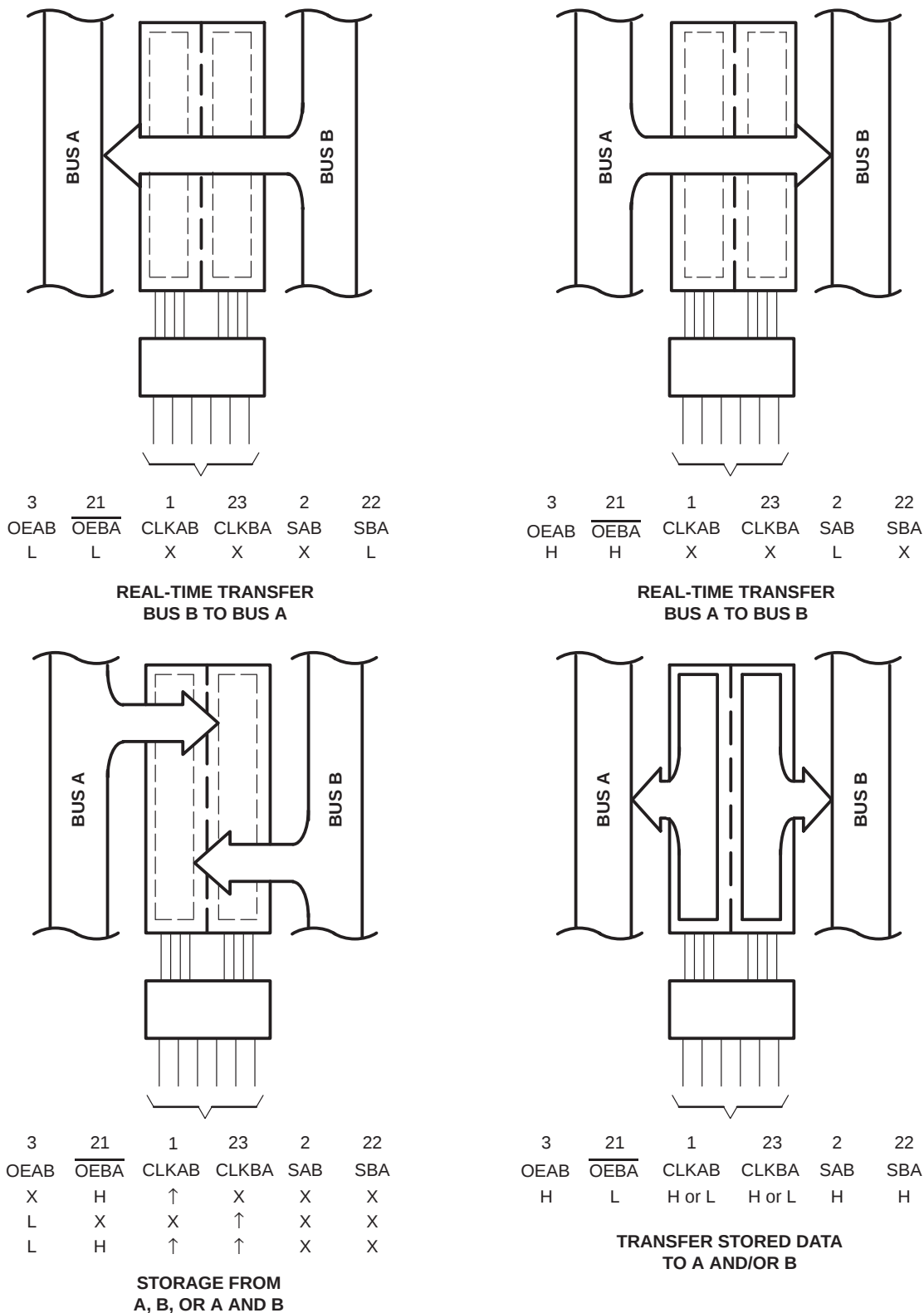
<sup>†</sup> The data-output functions can be enabled or disabled by a variety of level combinations at OEAB or  $\overline{\text{OEBA}}$ . Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

<sup>‡</sup> Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered to load both registers.

# SN54LVTH652, SN74LVTH652 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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Pin numbers shown are for the DB, DGV, DW, JT, NS, PW, and W packages.

**Figure 1. Bus-Management Functions**

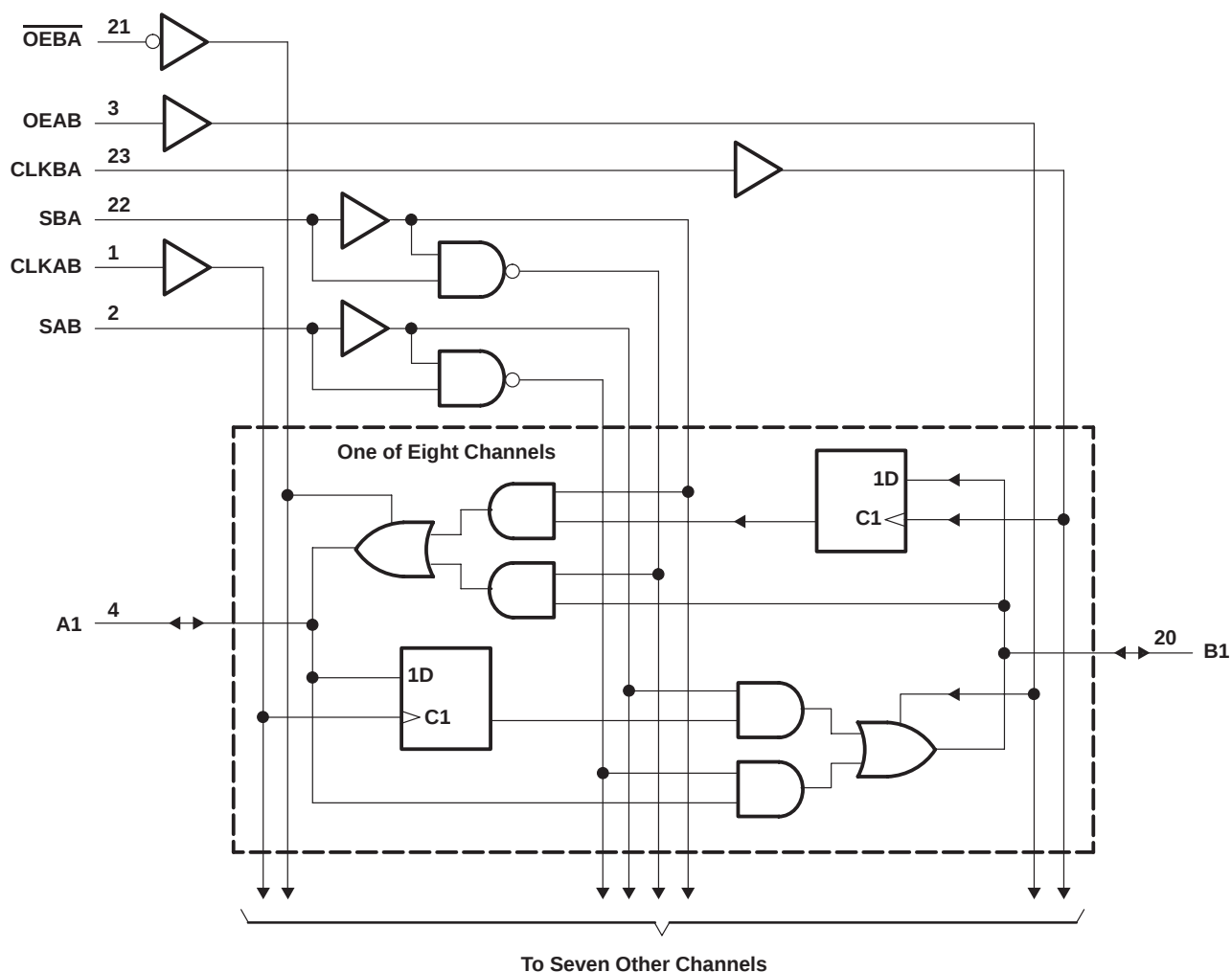
# SN54LVTH652, SN74LVTH652

## 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS

### WITH 3-STATE OUTPUTS

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#### logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, JT, NS, PW, and W packages.

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|                                                                                                  |                            |
|--------------------------------------------------------------------------------------------------|----------------------------|
| Supply voltage range, $V_{CC}$ (see Note 1)                                                      | −0.5 V to 4.6 V            |
| Input voltage range, $V_I$ (see Note 1)                                                          | −0.5 V to 7 V              |
| Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) | −0.5 V to 7 V              |
| Voltage range applied to any output in the high state, $V_O$ (see Note 1)                        | −0.5 V to $V_{CC} + 0.5$ V |
| Current into any output in the low state, $I_O$ : SN54LVTH652                                    | 96 mA                      |
| SN74LVTH652)                                                                                     | 128 mA                     |
| Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH652                       | 8 mA                       |
| SN74LVTH652                                                                                      | 64 mA                      |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                                                      | −50 mA                     |
| Output clamp current, $I_{OK}$ ( $V_O < 0$ )                                                     | −50 mA                     |
| Package thermal impedance, $\theta_{JA}$ (see Note 3): DB package                                | 63°C/W                     |
| DGV package                                                                                      | 86°C/W                     |
| DW package                                                                                       | 46°C/W                     |
| NS package                                                                                       | 65°C/W                     |
| PW package                                                                                       | 88°C/W                     |
| Storage temperature range, $T_{Stg}$                                                             | −65°C to 150°C             |

NOTES:

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
3. The package thermal impedance is calculated in accordance with JEDEC 51-7.

|                     |                                    |                 | SN54LVTH652 |     | SN74LVTH652 |     | UNIT |
|---------------------|------------------------------------|-----------------|-------------|-----|-------------|-----|------|
|                     |                                    |                 | MIN         | MAX | MIN         | MAX |      |
| V <sub>CC</sub>     | Supply voltage                     |                 | 2.7         | 3.6 | 2.7         | 3.6 | V    |
| V <sub>IH</sub>     | High-level input voltage           |                 | 2           |     | 2           |     | V    |
| V <sub>IL</sub>     | Low-level input voltage            |                 |             | 0.8 |             | 0.8 | V    |
| V <sub>I</sub>      | Input voltage                      |                 |             | 5.5 |             | 5.5 | V    |
| I <sub>OH</sub>     | High-level output current          |                 |             | −24 |             | −32 | mA   |
| I <sub>OL</sub>     | Low-level output current           |                 |             | 48  |             | 64  | mA   |
| Δt/Δv               | Input transition rise or fall rate | Outputs enabled |             | 10  |             | 10  | ns/V |
| Δt/ΔV <sub>CC</sub> | Power-up ramp rate                 |                 |             | 200 |             | 200 | μs/V |
| T <sub>A</sub>      | Operating free-air temperature     |                 | −55         | 125 | −40         | 85  | °C   |



# SN54LVTH652, SN74LVTH652

## 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER            |                | TEST CONDITIONS                                                                                              |                                  | SN54LVTH652                 |      |     | SN74LVTH652          |      |      | UNIT |    |
|----------------------|----------------|--------------------------------------------------------------------------------------------------------------|----------------------------------|-----------------------------|------|-----|----------------------|------|------|------|----|
|                      |                |                                                                                                              |                                  | MIN                         | TYP† | MAX | MIN                  | TYP† | MAX  |      |    |
| V <sub>IK</sub>      |                | V <sub>CC</sub> = 2.7 V, I <sub>I</sub> = -18 mA                                                             |                                  | -1.2                        |      |     | -1.2                 |      |      | V    |    |
| V <sub>OH</sub>      |                | V <sub>CC</sub> = 2.7 V to 3.6 V, I <sub>OH</sub> = -100 μA                                                  |                                  | V <sub>CC</sub> -0.2        |      |     | V <sub>CC</sub> -0.2 |      |      | V    |    |
|                      |                | V <sub>CC</sub> = 2.7 V, I <sub>OH</sub> = -8 mA                                                             |                                  | 2.4                         |      |     | 2.4                  |      |      |      |    |
|                      |                | V <sub>CC</sub> = 3 V                                                                                        | I <sub>OH</sub> = -24 mA         | 2                           |      |     |                      |      |      |      |    |
|                      |                |                                                                                                              | I <sub>OH</sub> = -32 mA         |                             |      |     | 2                    |      |      |      |    |
| V <sub>OL</sub>      |                | V <sub>CC</sub> = 2.7 V                                                                                      | I <sub>OL</sub> = 100 μA         | 0.2                         |      |     | 0.2                  |      |      | V    |    |
|                      |                |                                                                                                              | I <sub>OL</sub> = 24 mA          | 0.5                         |      |     | 0.5                  |      |      |      |    |
|                      |                | V <sub>CC</sub> = 3 V                                                                                        | I <sub>OL</sub> = 16 mA          | 0.4                         |      |     | 0.4                  |      |      |      |    |
|                      |                |                                                                                                              | I <sub>OL</sub> = 32 mA          | 0.5                         |      |     | 0.5                  |      |      |      |    |
|                      |                |                                                                                                              | I <sub>OL</sub> = 48 mA          | 0.55                        |      |     |                      |      |      |      |    |
|                      |                |                                                                                                              | I <sub>OL</sub> = 64 mA          |                             |      |     | 0.55                 |      |      |      |    |
| I <sub>I</sub>       | Control inputs | V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub> or GND                                             |                                  | ±1                          |      |     | ±1                   |      |      | μA   |    |
|                      |                | V <sub>CC</sub> = 0 or 3.6 V, V <sub>I</sub> = 5.5 V                                                         |                                  | 10                          |      |     | 10                   |      |      |      |    |
|                      | A or B ports‡  | V <sub>CC</sub> = 3.6 V                                                                                      | V <sub>I</sub> = 5.5 V           |                             | 20   |     |                      | 20   |      |      |    |
|                      |                |                                                                                                              | V <sub>I</sub> = V <sub>CC</sub> |                             | 1    |     |                      | 1    |      |      |    |
|                      |                |                                                                                                              | V <sub>I</sub> = 0               |                             | -5   |     |                      | -5   |      |      |    |
| I <sub>off</sub>     |                | V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V                                           |                                  |                             |      |     | ±100                 |      |      | μA   |    |
| I <sub>I(hold)</sub> | A or B ports   | V <sub>CC</sub> = 3 V                                                                                        | V <sub>I</sub> = 0.8 V           |                             | 75   |     |                      | 75   |      |      | μA |
|                      |                |                                                                                                              | V <sub>I</sub> = 2 V             |                             | -75  |     |                      | -75  |      |      |    |
|                      |                | V <sub>CC</sub> = 3.6 V§                                                                                     |                                  | V <sub>I</sub> = 0 to 3.6 V |      |     |                      |      | ±500 |      |    |
| I <sub>OZPU</sub>    |                | V <sub>CC</sub> = 0 to 1.5 V, V <sub>O</sub> = 0.5 to 3 V, OE/OE = don't care                                |                                  | ±100*                       |      |     | ±100                 |      |      | μA   |    |
| I <sub>OZPD</sub>    |                | V <sub>CC</sub> = 1.5 V to 0, V <sub>O</sub> = 0.5 to 3 V, OE/OE = don't care                                |                                  | ±100*                       |      |     | ±100                 |      |      | μA   |    |
| I <sub>CC</sub>      |                | V <sub>CC</sub> = 3.6 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND                         | Outputs high                     |                             | 0.19 |     |                      | 0.19 |      |      | mA |
|                      |                |                                                                                                              | Outputs low                      |                             | 5    |     |                      | 5    |      |      |    |
|                      |                |                                                                                                              | Outputs disabled                 |                             | 0.19 |     |                      | 0.19 |      |      |    |
| ΔI <sub>CC</sub> ¶   |                | V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND |                                  | 0.2                         |      |     | 0.2                  |      |      | mA   |    |
| C <sub>i</sub>       |                | V <sub>I</sub> = 3 V or 0                                                                                    |                                  | 4                           |      |     | 4                    |      |      | pF   |    |
| C <sub>io</sub>      |                | V <sub>O</sub> = 3 V or 0                                                                                    |                                  | 9                           |      |     | 9                    |      |      | pF   |    |

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Unused terminals at  $V_{CC}\text{ or GND}$

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}\text{ or GND}$ .

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# SN54LVTH652, SN74LVTH652

## 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

|                    |                                               |           | SN54LVTH652                              |     |                         |     | SN74LVTH652                              |     |                         |     | UNIT |
|--------------------|-----------------------------------------------|-----------|------------------------------------------|-----|-------------------------|-----|------------------------------------------|-----|-------------------------|-----|------|
|                    |                                               |           | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | $V_{CC} = 2.7\text{ V}$ |     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | $V_{CC} = 2.7\text{ V}$ |     |      |
|                    |                                               |           | MIN                                      | MAX | MIN                     | MAX | MIN                                      | MAX | MIN                     | MAX |      |
| f <sub>clock</sub> | Clock frequency                               |           | 150                                      |     | 150                     |     | 150                                      |     | 150                     |     | MHz  |
| t <sub>w</sub>     | Pulse duration, CLK high or low               |           | 3.3                                      |     | 3.3                     |     | 3.3                                      |     | 3.3                     |     | ns   |
| t <sub>su</sub>    | Setup time,<br>A or B before CLKAB↑ or CLKBA↑ | Data high | 1.3                                      |     | 1.6                     |     | 1.2                                      |     | 1.5                     |     | ns   |
|                    |                                               | Data low  | 1.9                                      |     | 2.6                     |     | 1.6                                      |     | 2.2                     |     |      |
| t <sub>h</sub>     | Hold time, A or B after CLKAB↑ or CLKBA↑      |           | 1.2                                      |     | 1.2                     |     | 0.8                                      |     | 0.8                     |     | ns   |

switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 2)

| PARAMETER        | FROM<br>(INPUT)          | TO<br>(OUTPUT) | SN54LVTH652                              |     |                         |     | SN74LVTH652                              |      |     |                         | UNIT |     |
|------------------|--------------------------|----------------|------------------------------------------|-----|-------------------------|-----|------------------------------------------|------|-----|-------------------------|------|-----|
|                  |                          |                | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | $V_{CC} = 2.7\text{ V}$ |     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |      |     | $V_{CC} = 2.7\text{ V}$ |      |     |
|                  |                          |                | MIN                                      | MAX | MIN                     | MAX | MIN                                      | TYP† | MAX | MIN                     |      | MAX |
| f <sub>max</sub> |                          |                | 150                                      |     | 150                     |     | 150                                      |      |     | 150                     |      | MHz |
| t <sub>PLH</sub> | CLKBA or CLKAB           | A or B         | 1.7                                      | 5   | 5.9                     |     | 1.8                                      | 3.1  | 4.7 | 5.6                     |      | ns  |
| t <sub>PHL</sub> |                          |                | 1.7                                      | 5   | 5.9                     |     | 1.8                                      | 3.1  | 4.7 | 5.6                     |      |     |
| t <sub>PLH</sub> | A or B                   | B or A         | 1.2                                      | 3.7 | 4.3                     |     | 1.3                                      | 2.3  | 3.5 | 4.1                     |      | ns  |
| t <sub>PHL</sub> |                          |                | 1.2                                      | 3.7 | 4.3                     |     | 1.3                                      | 2.4  | 3.5 | 4.1                     |      |     |
| t <sub>PLH</sub> | SBA or SAB‡              | A or B         | 1.4                                      | 5.2 | 6.3                     |     | 1.5                                      | 3.1  | 4.9 | 6                       |      | ns  |
| t <sub>PHL</sub> |                          |                | 1.4                                      | 5.2 | 6.3                     |     | 1.5                                      | 3.4  | 4.9 | 6                       |      |     |
| t <sub>PZH</sub> | $\overline{\text{OEBA}}$ | A              | 1                                        | 5.4 | 6.7                     |     | 1.1                                      | 2.9  | 5.2 | 6.5                     |      | ns  |
| t <sub>PZL</sub> |                          |                | 1                                        | 5.4 | 6.7                     |     | 1.1                                      | 3.1  | 5.2 | 6.5                     |      |     |
| t <sub>PHZ</sub> | $\overline{\text{OEBA}}$ | A              | 2.2                                      | 5.9 | 6.5                     |     | 2.3                                      | 3.5  | 5.5 | 6.1                     |      | ns  |
| t <sub>PLZ</sub> |                          |                | 2.2                                      | 5.9 | 6.3                     |     | 2.3                                      | 3.7  | 5.5 | 5.9                     |      |     |
| t <sub>PZH</sub> | OEAB                     | B              | 1.2                                      | 4.9 | 5.9                     |     | 1.3                                      | 3    | 4.7 | 5.7                     |      | ns  |
| t <sub>PZL</sub> |                          |                | 1.2                                      | 4.9 | 5.9                     |     | 1.3                                      | 3.3  | 4.7 | 5.7                     |      |     |
| t <sub>PHZ</sub> | OEAB                     | B              | 1.4                                      | 5.8 | 7                       |     | 1.5                                      | 3.6  | 5.6 | 6.7                     |      | ns  |
| t <sub>PLZ</sub> |                          |                | 1.4                                      | 5.9 | 6.6                     |     | 1.5                                      | 3.7  | 5.6 | 6.3                     |      |     |

<sup>†</sup> All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

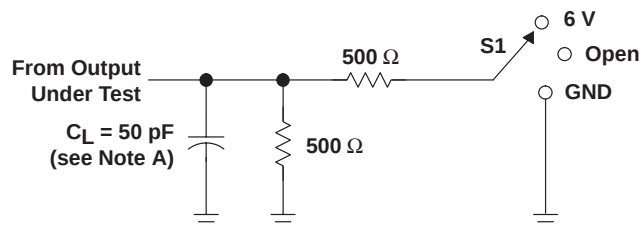
<sup>‡</sup> These parameters are measured with the internal output state of the storage register opposite that of the bus input.

# SN54LVTH652, SN74LVTH652

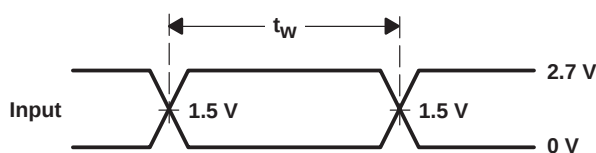
## 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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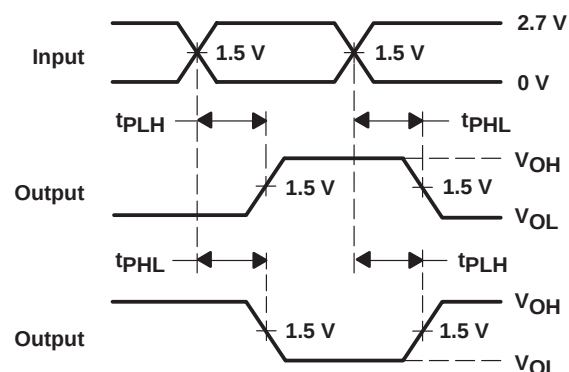
### PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

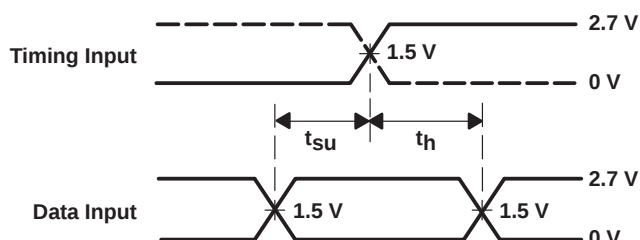


VOLTAGE WAVEFORMS  
PULSE DURATION

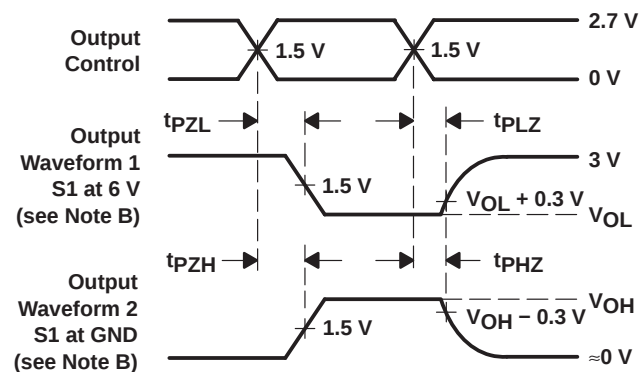


VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS

| TEST              | S1   |
|-------------------|------|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V  |
| $t_{PHZ}/t_{PZH}$ | GND  |



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

| Orderable part number          | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|--------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74LVTH652DW</a>  | Active        | Production           | SOIC (DW)   24  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVTH652             |
| SN74LVTH652DW.B                | Active        | Production           | SOIC (DW)   24  | 25   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LVTH652             |
| <a href="#">SN74LVTH652PW</a>  | Active        | Production           | TSSOP (PW)   24 | 60   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LXH652              |
| SN74LVTH652PW.B                | Active        | Production           | TSSOP (PW)   24 | 60   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LXH652              |
| <a href="#">SN74LVTH652PWR</a> | Active        | Production           | TSSOP (PW)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LXH652              |
| SN74LVTH652PWR.B               | Active        | Production           | TSSOP (PW)   24 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | LXH652              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVTH652PWR | TSSOP        | PW              | 24   | 2000 | 330.0              | 16.4               | 6.95    | 8.3     | 1.6     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

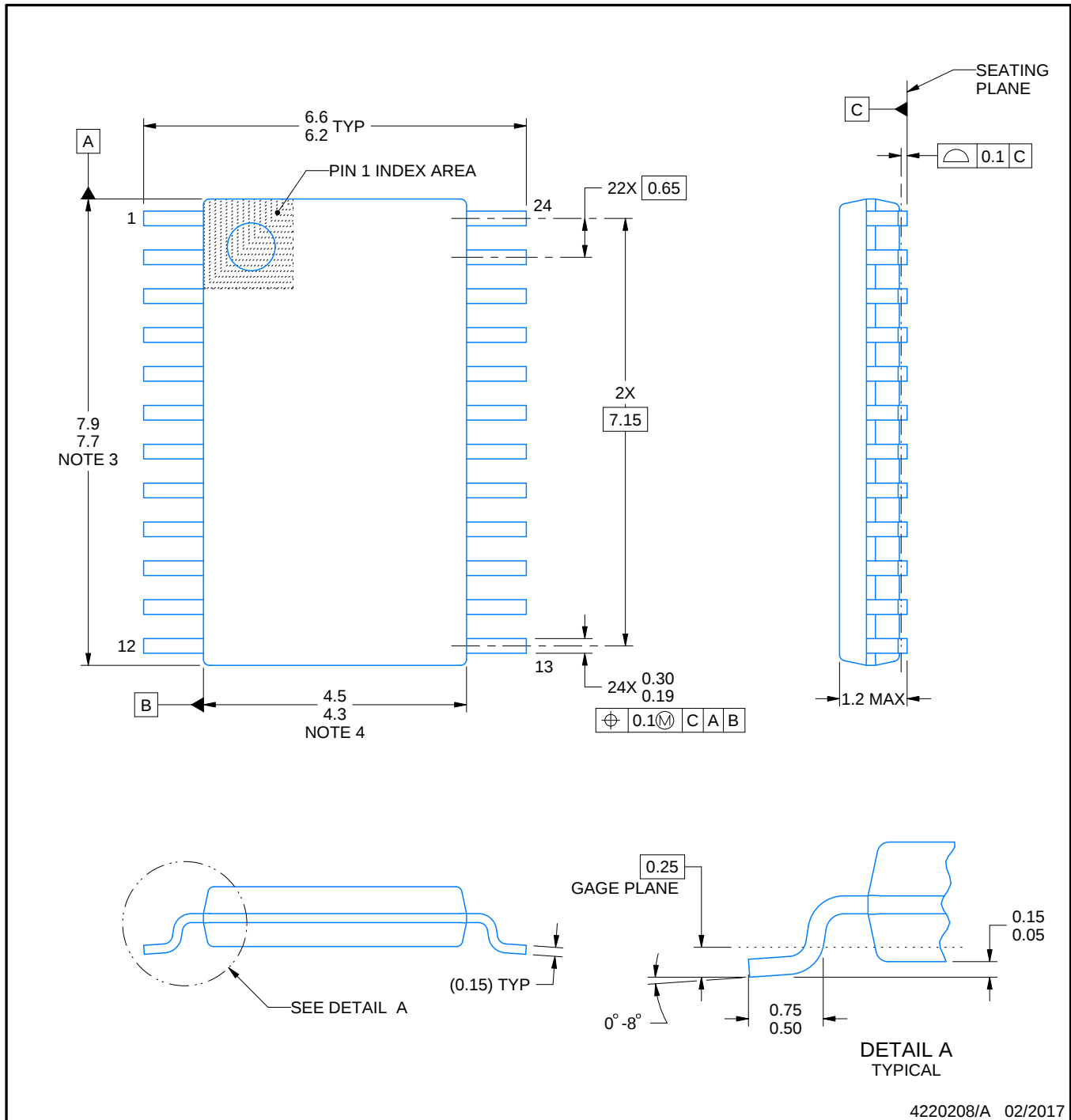
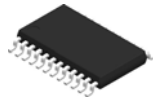
| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVTH652PWR | TSSOP        | PW              | 24   | 2000 | 353.0       | 353.0      | 32.0        |

## TUBE



\*All dimensions are nominal

| Device          | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74LVTH652DW   | DW           | SOIC         | 24   | 25  | 506.98 | 12.7   | 4826   | 6.6    |
| SN74LVTH652DW.B | DW           | SOIC         | 24   | 25  | 506.98 | 12.7   | 4826   | 6.6    |
| SN74LVTH652PW   | PW           | TSSOP        | 24   | 60  | 530    | 10.2   | 3600   | 3.5    |
| SN74LVTH652PW.B | PW           | TSSOP        | 24   | 60  | 530    | 10.2   | 3600   | 3.5    |



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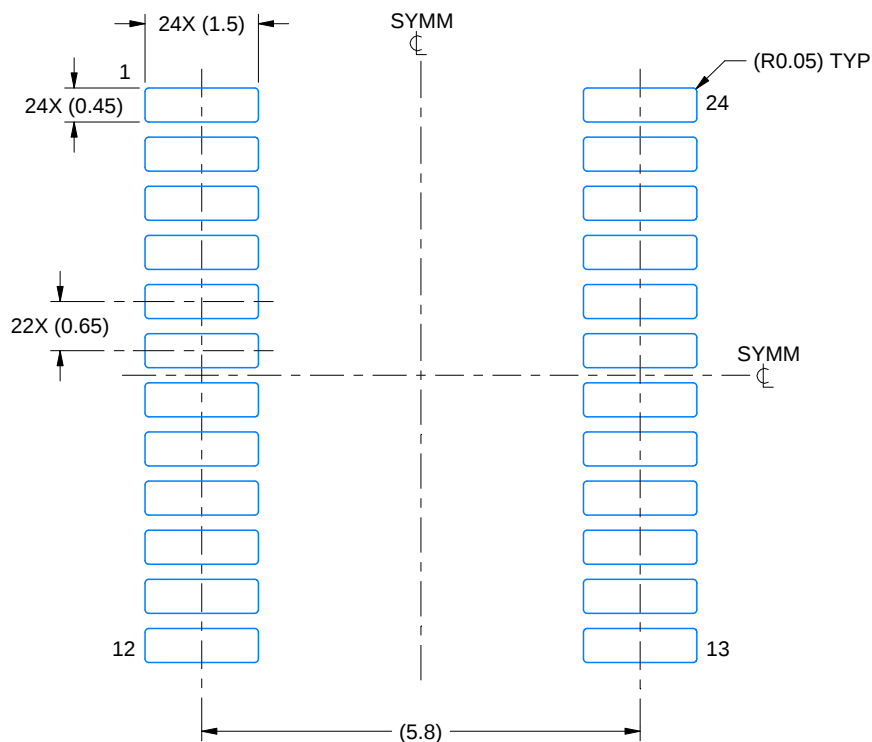
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

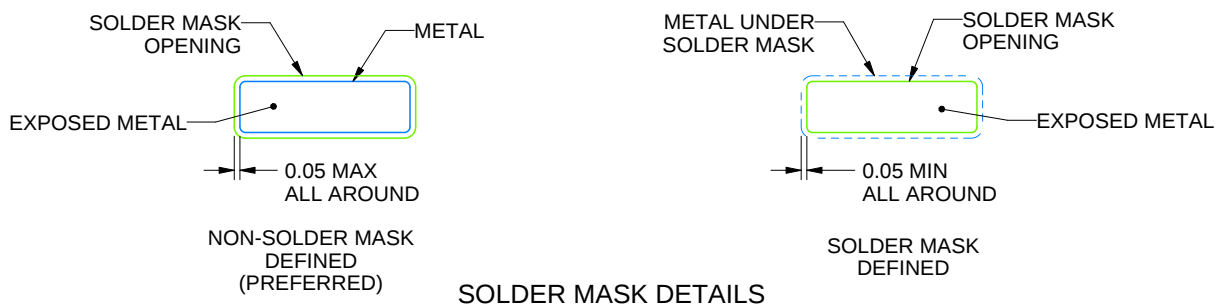
**PW0024A**

## TSSOP - 1.2 mm max height

## SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

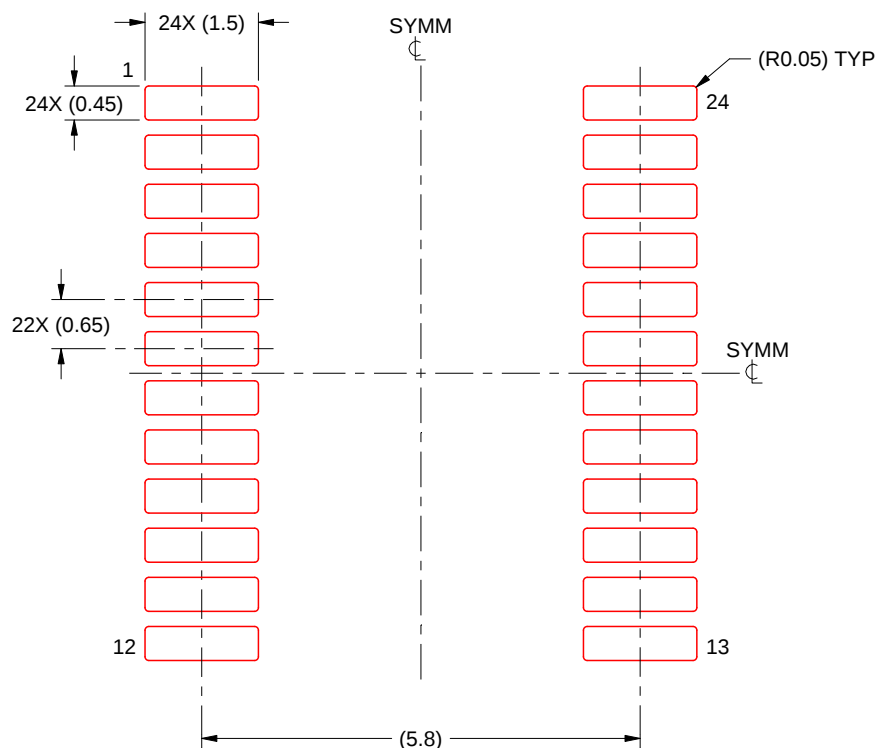
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0024A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

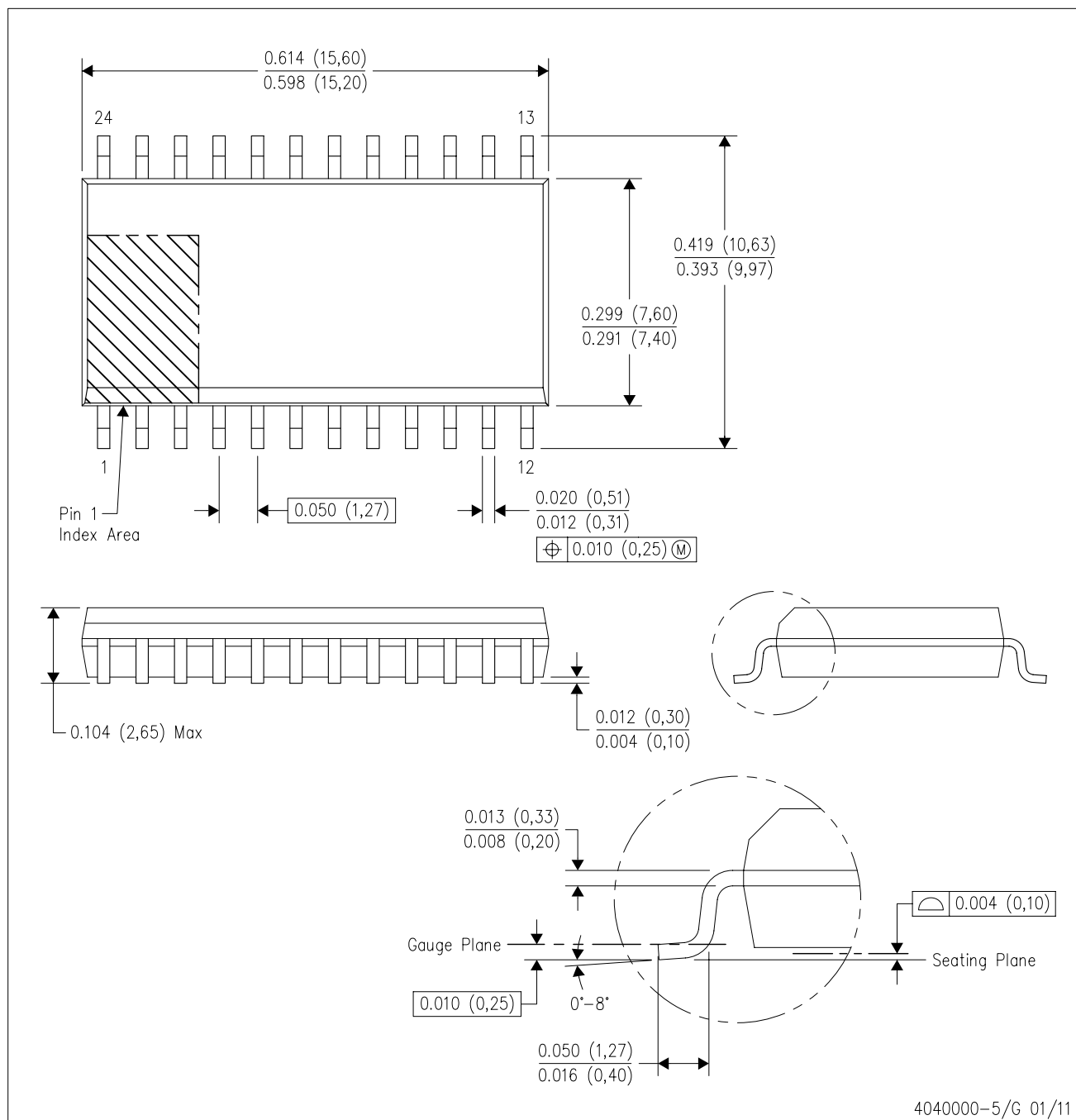
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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R-PDSO-G24)

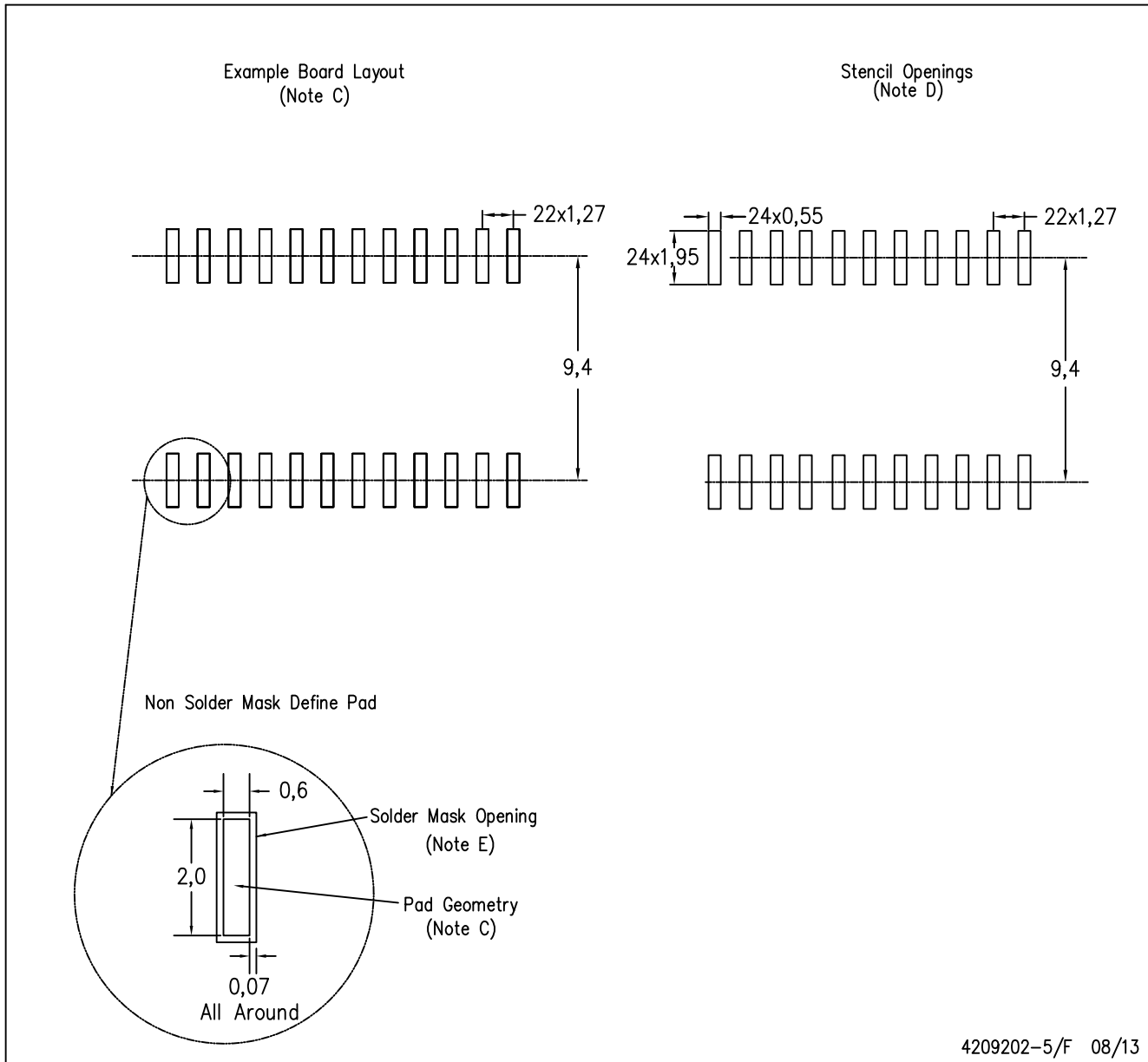
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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