SN74TVC3306 Dual Voltage Clamp

1 Features

- Designed to be used in voltage-limiting applications
- 3.5-ω on-state connection between ports A and B
- Flow-through pinout for ease of printed circuit board trace routing
- Direct interface with GTL+ levels
- Latch-up performance exceeds 100 mA per JESD 78, class II
- ESD protection exceeds JESD 22:
  - 2000-V Human-Body Model
  - 200-V Machine Model
  - 1000-V Charged-Device Model

2 Applications

- Voltage level translation
- Signal switching
- Bus isolation

3 Description

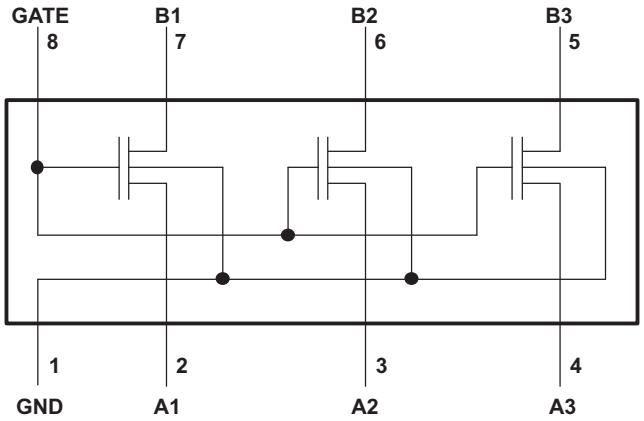
The SN74TVC3306 device provides three parallel NMOS pass transistors with a common unbuffered gate. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device can be used as a dual switch, with the gates cascaded together to a reference transistor. The low-voltage side of each pass transistor is limited to a voltage set by the reference transistor. This is done to protect components with inputs that are sensitive to high-state voltage-level overshoots.

Package Information

PART NUMBER	PACKAGE(1)	PACAKGE SIZE(2)
SN74TVC3306	DCT (SSOP, 8)	2.95 mm × 4 mm
	DCU (VSSOP, 8)	2 mm × 3.1 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



The SN74TVC3306 device has bidirectional capability across many voltage levels. The voltage levels documented in this data sheet are examples.

Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (December 2014) to Revision E (September 2023)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1
• Changed the thermal values to reflect device performance	4
• Changed the switching characteristics to reflect device performance	5

Changes from Revision C (March 2002) to Revision D (December 2014)	Page
• Added *Applications*, *Device Information* table, *Pin Functions* table, *Handling Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1
• Deleted *Ordering Information* table	1
• Changed the R_{ON} parameter in the *Electrical Characteristics* table	5

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5 Pin Configuration and Functions

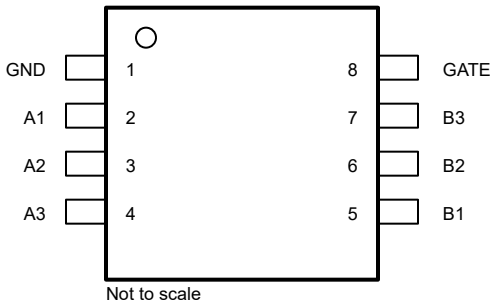


Figure 5-1. DCT or DCU Package, 8-Pin SOP or VSSOP (Top View)

Table 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A1	2	I/O	I/O of gate 1
A2	3	I/O	I/O of gate 1
A3	4	I/O	I/O of gate 1
B1	5	I/O	I/O of gate 2
B2	6	I/O	I/O of gate 2
B3	7	I/O	I/O of gate 2
GATE	8	I	Gate pin. Set high to enable the switches. Connect to B1 (V_{BIAS}) for translation application.
GND	1	—	Ground

(1) I = input, O = output, P = power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_I	Input voltage range(2)		–0.5	7	V
$V_{I/O}$	Input/output voltage range(2)		–0.5	7	V
	Continuous channel current			128	mA
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	5	V
V_{GATE}	GATE voltage	0	5	V
I_{PASS}	Pass transistor current		64	mA
T_A	Operating free-air temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		SN74TVC3306		UNIT
		DCT	DCU	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	254.1	275.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	148.6	127.1 1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	168.8	186.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	70.1	65.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	167.4	185.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IK}	I_I = -18 mA,	V_{GATE} = 0				–1.2	V
I_{IH}	V_I = 5 V,	V_{GATE} = 0				5	µA
$C_{i(GATE)}$	V_I = 3 V or 0				11		pF
$C_{io(off)}$	V_O = 3 V or 0,	V_{GATE} = 0			4	6	pF
$C_{io(on)}$	V_O = 3 V or 0,	V_{GATE} = 3 V			10.5	12.5	pF
R_{on} (2)	V_I = 0,	I_O = 64 mA	V_{GATE} = 4.5 V		3.5	5.5	Ω
			V_{GATE} = 3 V		4.7	7	
			V_{GATE} = 2.3 V		6.3	9.5	
	V_I = 2.4 V,	I_O = 15 mA	V_{GATE} = 4.5 V		4.8	7.5	
	V_I = 1.8 V,	I_O = 15 mA	V_{GATE} = 4.5 V		4.5	5	

(1) All typical values are at T_A = 25°C.
(2) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

6.6 Switching Characteristics (AC, V_{GATE} = 3.3 V, Translating Down)

over recommended operating free-air temperature range, V_{GATE} = 3.3 V, V_{IH} = 3.3 V, V_{IL} = 0, and V_M = 1.15 V (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0	0.8	0	0.6	0	0.3	ns
t_{PHL}			0	1.2	0	1	0	0.75	

6.7 Switching Characteristics (AC, V_{GATE} = 2.5 V, Translating Down)

over recommended operating free-air temperature range, V_{GATE} = 2.5 V, V_{IH} = 2.5 V, V_{IL} = 0, and V_M = 0.75 V (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0	1	0	0.7	0	0.4	ns
t_{PHL}			0	1.3	0	1	0	0.75	

6.8 Switching Characteristics (AC, V_{GATE} = 3.3 V, Translating Up)

over recommended operating free-air temperature range, V_{GATE} = 3.3 V, V_{IH} = 2.3 V, V_{IL} = 0, V_T = 3.3 V, V_M = 1.15 V, and R_L = 300 Ω (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0	0.9	0	0.6	0	0.4	ns
t_{PHL}			0	1.4	0	1.1	0	1.0	

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6.9 Switching Characteristics (AC, V_{GATE} = 2.5 V, Translating Up)

over recommended operating free-air temperature range, V_{GATE} = 2.5 V, V_{IH} = 1.5 V, V_{IL} = 0, V_T = 2.5 V, V_M = 0.75 V, and R_L = 300 Ω (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0	1	0	0.6	0	0.4	ns
t_{PHL}			0	1.3	0	1.3	0	1.3	

6.10 Typical Characteristics

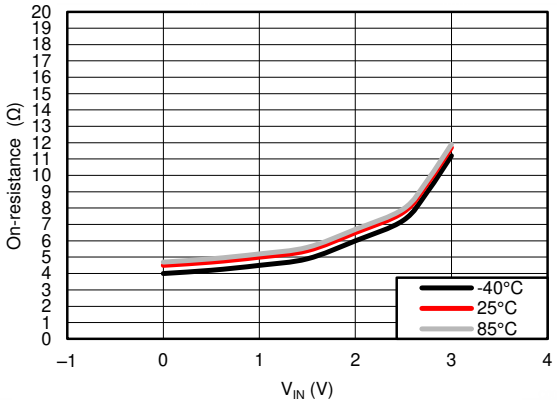
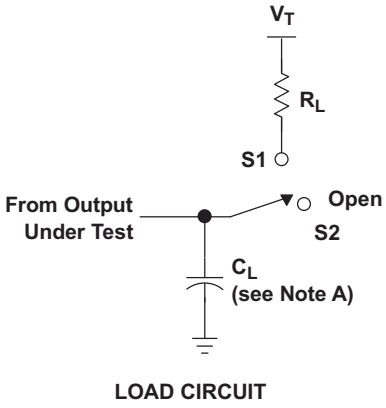


Figure 6-1. R_{ON} vs V_{IN} at I_{IN} = 15 mA.

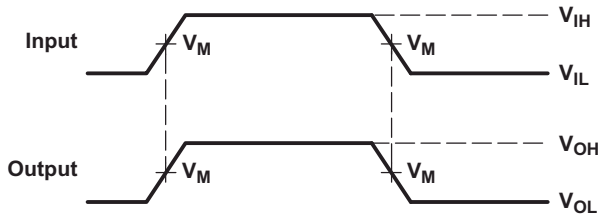
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7 Parameter Measurement Information



LOAD CIRCUIT

USAGE	SWITCH
Translating up	S1
Translating down	S2



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure 7-1. Load Circuit for Outputs

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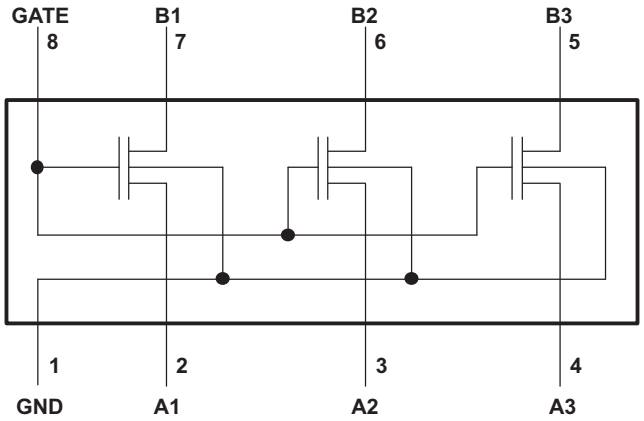
8 Detailed Description

8.1 Overview

The SN74TVC3306 device provides three parallel NMOS pass transistors with a common unbuffered gate. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device can be used as a dual switch, with the gates cascaded together to a reference transistor. The low-voltage side of each pass transistor is limited to a voltage set by the reference transistor. This is done to protect components with inputs that are sensitive to high-state voltage-level overshoots.

8.2 Functional Block Diagram



The SN74TVC3306 device has bidirectional capability across many voltage levels. The voltage levels documented in this data sheet are examples.

8.3 Feature Description

8.3.1 Voltage Clamping

The internal NMOS transistors allow the SN74TVC3306 device to act as a voltage clamp and be configured as a voltage level translator. For more information, see *Application and Implementation*.

8.4 Device Functional Modes

8.4.1 Voltage Clamping

Whenever the signal on the inputs on the side with V_{REF} goes higher than V_{REF}, the voltage clamps on the opposite side to the value of V_{DPU} due to the pullup resistors. In this case, the voltage is translating up. For more information, see *Application and Implementation*.

8.4.2 Voltage Passing

Whenever the signal on the inputs on the VREF side is lower than VREF, the signal will pass to the other side as intended. In this case, the low pulse is staying low (no translation). For more information, see *Application and Implementation*.

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9 Application and Implementation

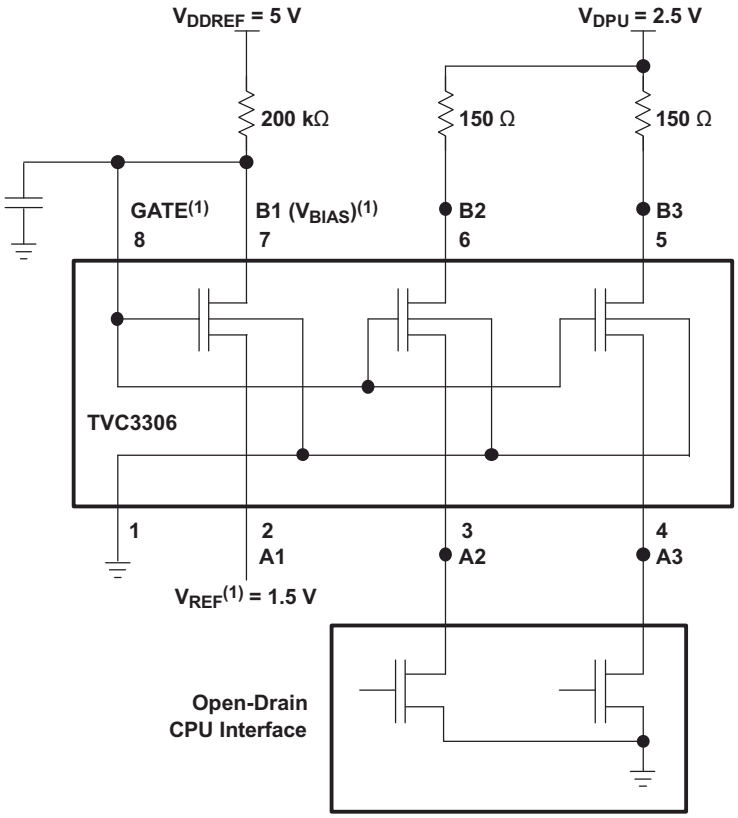
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Because of the voltage-clamping mechanism, the SN74TVC3306 device performs best as a level translator for signals that have sharp edges (as opposed to analog audio signals).

9.2 Typical Application



V_{REF} and V_{BIAS} can be applied to any one of the pass transistors. GATE must be connected externally to V_{BIAS}

Figure 9-1. Typical Application Circuit

9.2.1 Design Requirements

9.2.1.1 Application Operating Conditions

Application Operating Conditions (See Figure 9-1)

		MIN	TYP(1)	MAX	UNIT
V_{BIAS}	BIAS voltage	V_{REF} + 0.6	2.1	5	V
V_{GATE}	GATE voltage	V_{REF} + 0.6	2.1	5	V
V_{REF}	Reference voltage	0	1.5	4.4	V
V_{DPU}	Drain pullup voltage	2.36	2.5	2.64	V
I_{PASS}	Pass-transistor current		14		mA
I_{REF}	Reference-transistor current		5		µA
T_A	Operating free-air temperature	–40		85	°C

(1) All typical values are at T_A = 25°C.

9.2.2 Detailed Design Procedure

For the clamping configuration, the common GATE input must be connected to one side (An or Bn) of any one of the pass transistors, making that the V_{BIAS} connection of the reference transistor and the opposite side (Bn or An) the V_{REF} connection. When V_{BIAS} is connected through a 200-kΩ resistor to a 3-V to 5.5-V V_{CC} supply and V_{REF} is set to 0 V to V_{CC} – 0.6 V, the output of each switch has a maximum clamp voltage equal to V_{REF}. A filter capacitor on V_{BIAS} is recommended.

9.2.3 Application Curves

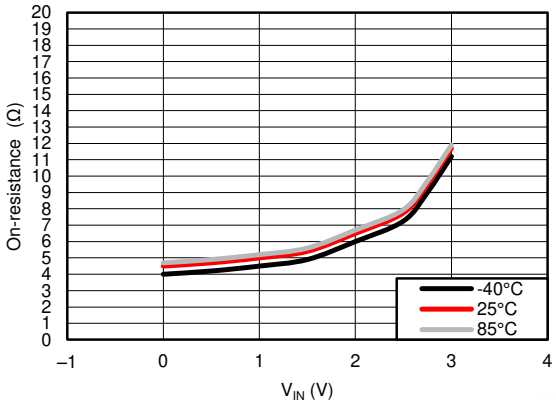


Figure 9-2. On-Resistance vs VIN (A to B, 15 mA Current)

9.3 Power Supply Recommendations

A 200-kΩ resistor is recommended from the input to V_{CC} when the device is being used as a voltage clamp. A filter capacitor is recommended on B1 as well.

9.4 Layout

9.4.1 Layout Guidelines

If used, the filter capacitor should be placed as close to the input of the device as possible.

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9.4.2 Layout Example

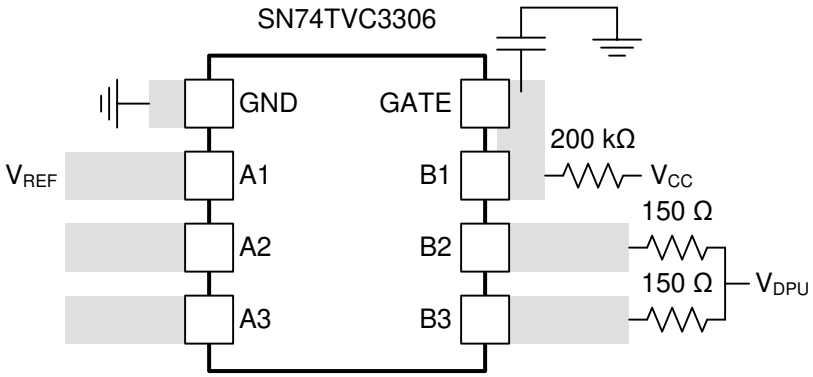


Figure 9-3. Layout Example for Voltage-Clamp Configuration

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.3 Trademarks

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10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74TVC3306DCTR	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	FA6 (S, Y)
SN74TVC3306DCTR.A	Active	Production	SSOP (DCT) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	FA6 (S, Y)
SN74TVC3306DCUR	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(FA6, FA6P, FA6S)
SN74TVC3306DCUR.A	Active	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(FA6, FA6P, FA6S)
SN74TVC3306DCURG4	NRND	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FA6S
SN74TVC3306DCURG4.A	NRND	Production	VSSOP (DCU) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FA6S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

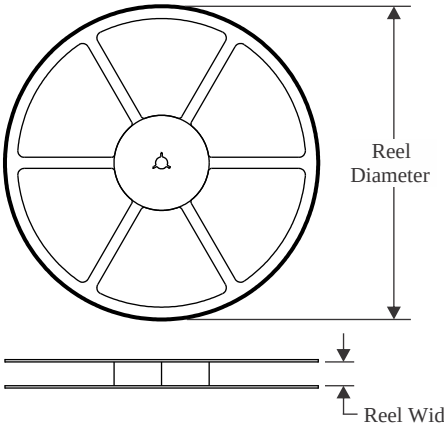
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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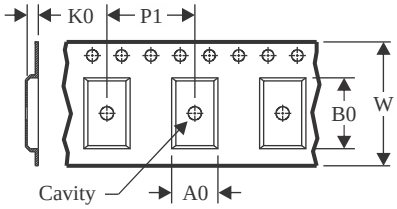
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

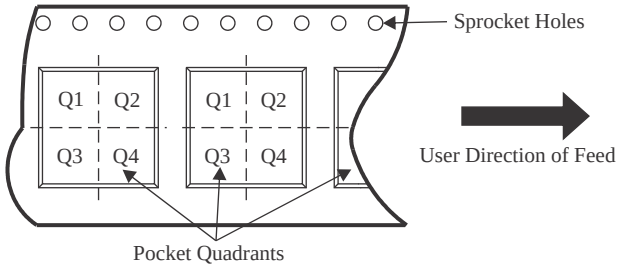


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

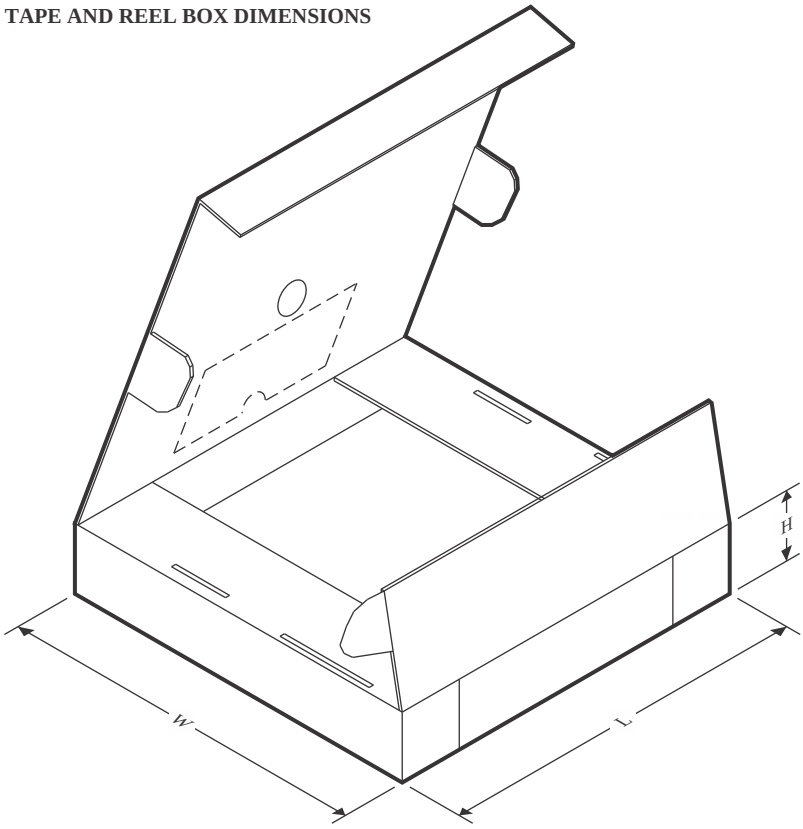
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74TVC3306DCTR	SSOP	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74TVC3306DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74TVC3306DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74TVC3306DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

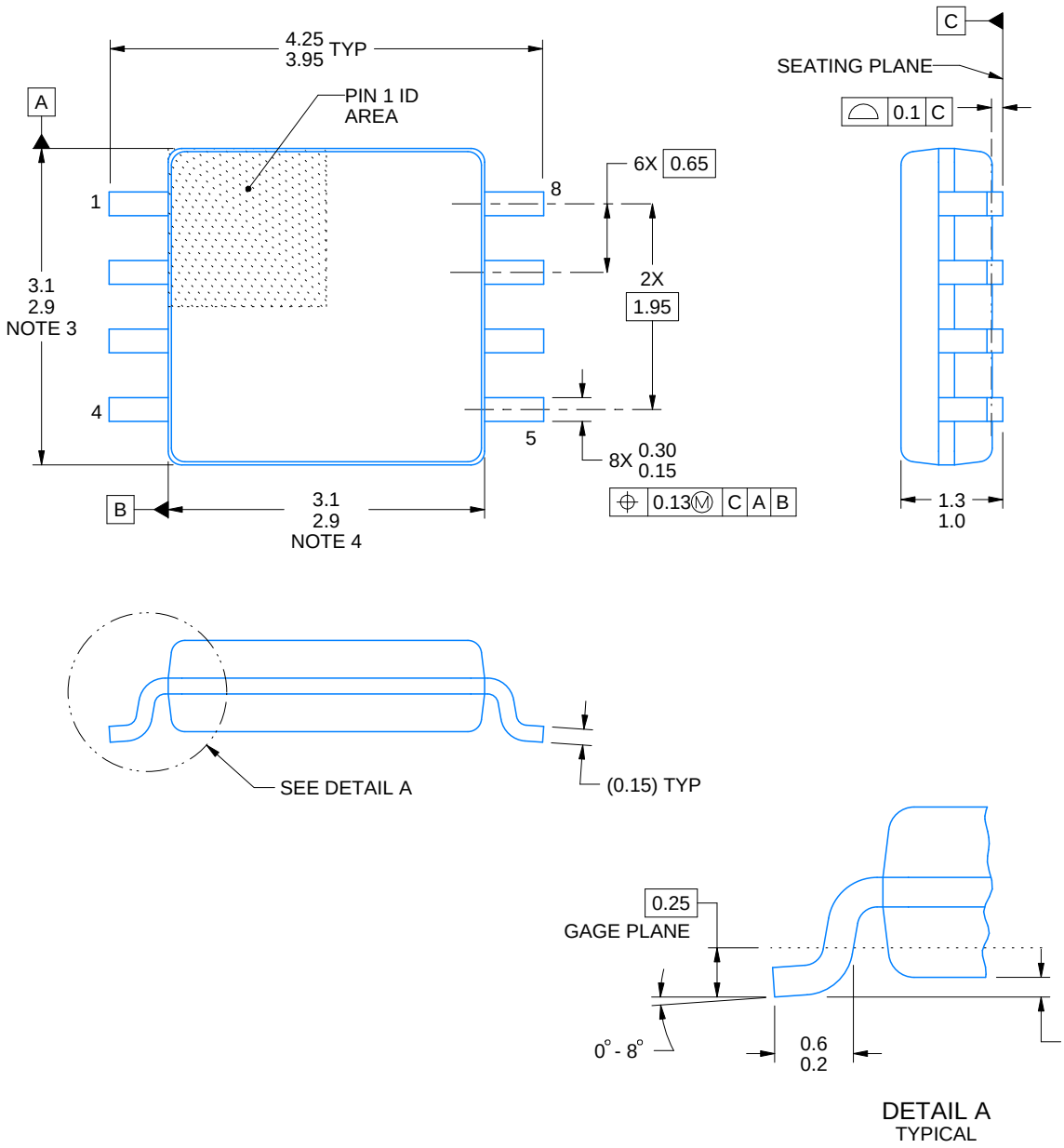
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74TVC3306DCTR	SSOP	DCT	8	3000	190.0	190.0	30.0
SN74TVC3306DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74TVC3306DCUR	VSSOP	DCU	8	3000	213.0	191.0	35.0
SN74TVC3306DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0

PACKAGE OUTLINE

DCT0008A

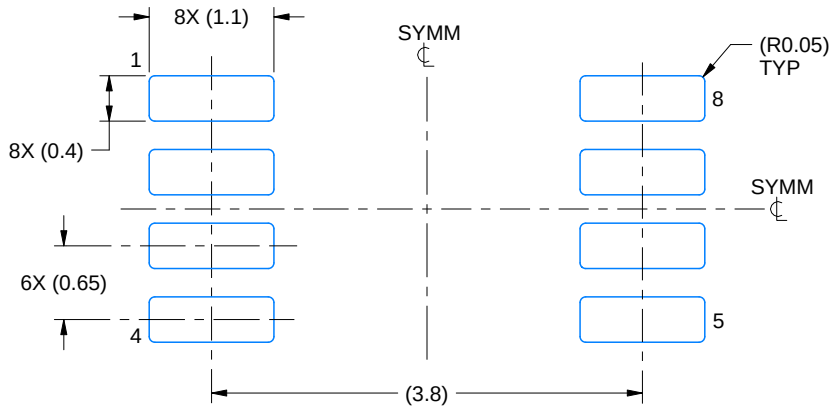
SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE

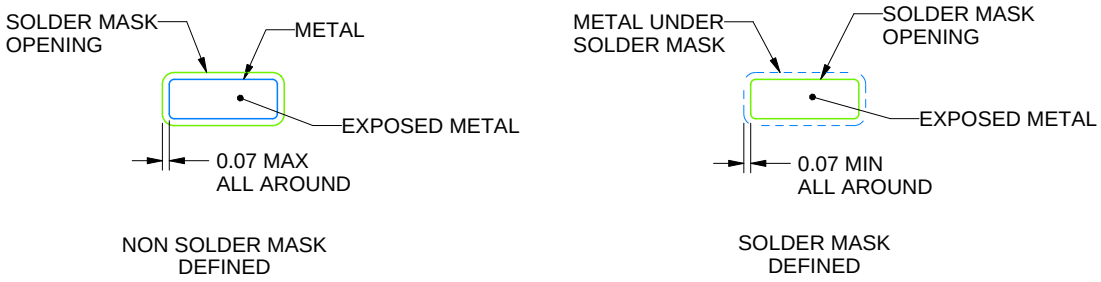


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

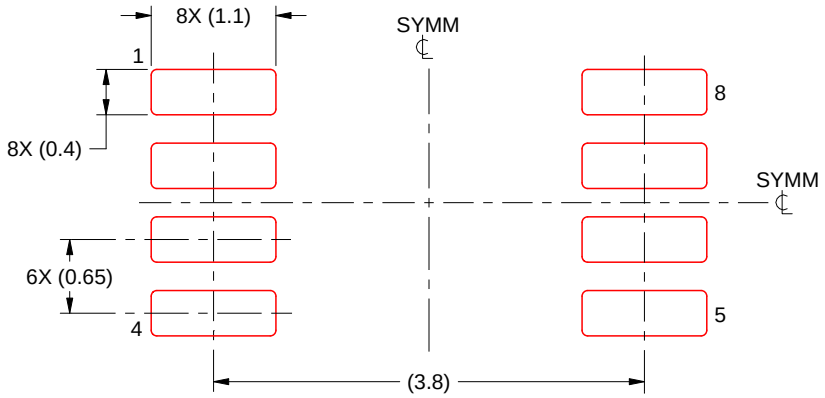


SOLDER MASK DETAILS

4220784/D 10/2025

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/D 10/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

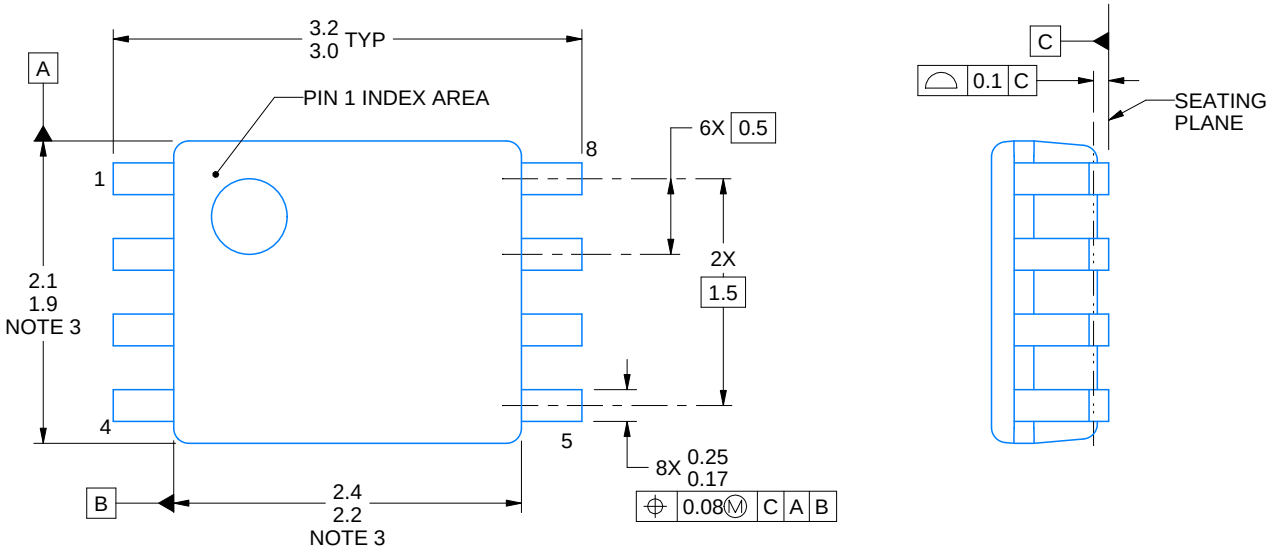
DCU0008A

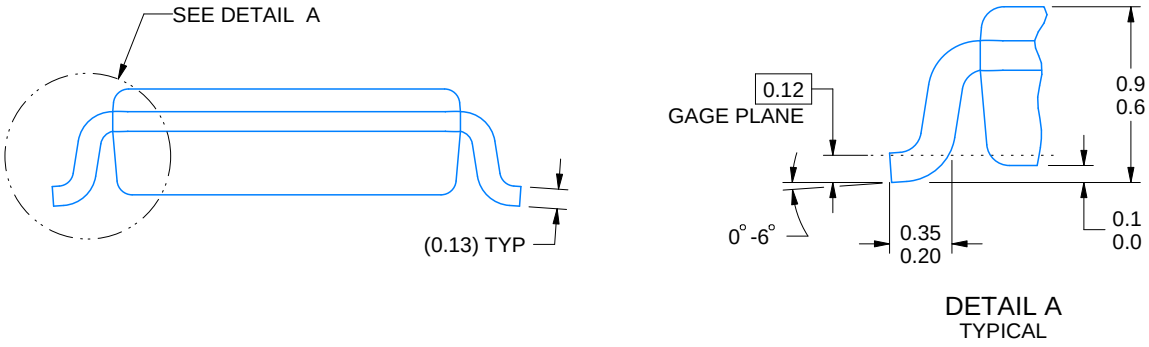


PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

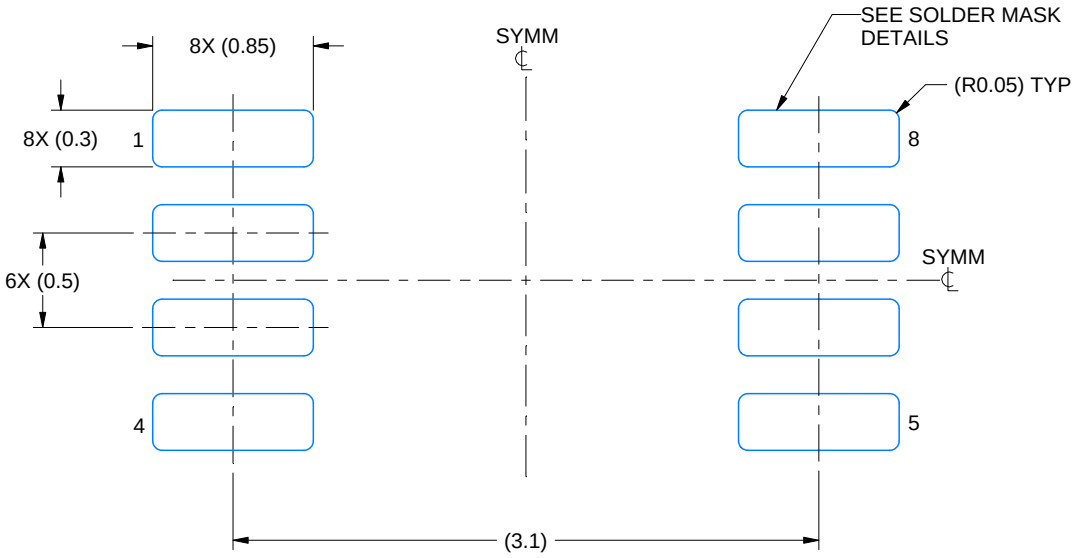




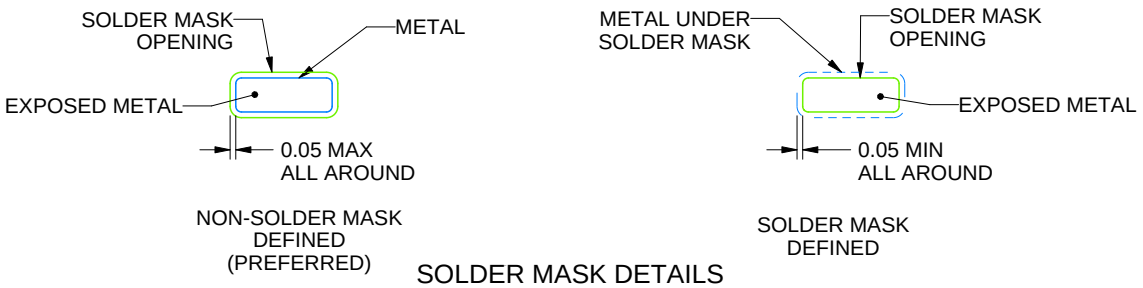
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

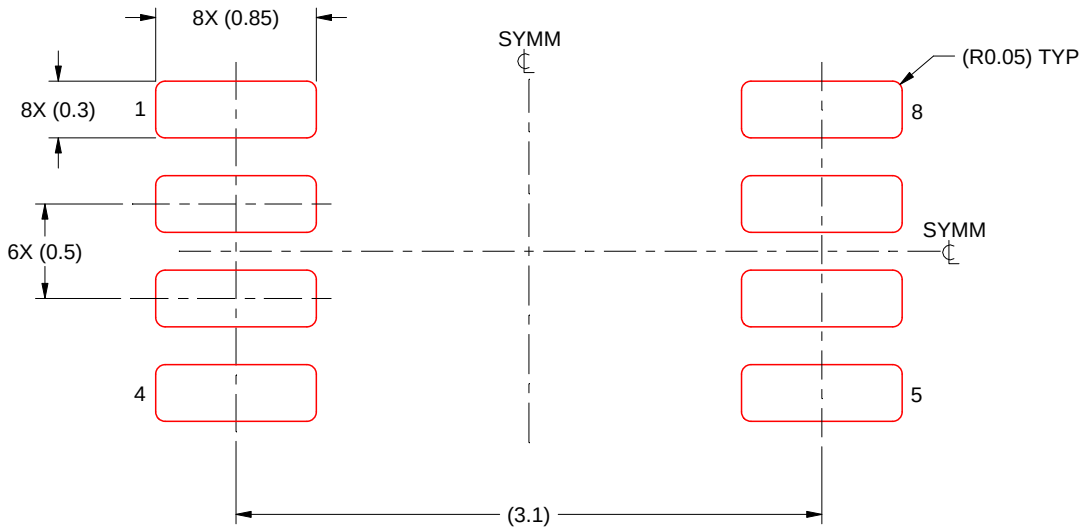


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025