- Meets or Exceeds the Requirements of ANSI TIA/EIA-232-C
- Wide Range of Supply Voltage V_{CC} = ±4.5 V to ±15 V
- Low Power . . . 117 mW (V_{CC} = ±9 V)
- Receiver Output TTL Compatible
- Response Control Provides:
 - Input Threshold Shifting
 - Input Noise Filtering

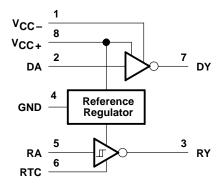
V_{CC}- 1 8 V_{CC+} DA 2 7 DY RY 3 6 RTC GND 4 5 RA

P OR PS PACKAGE

description

The SN751701 line driver and receiver is designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by ANSI TIA/EIA-232-E. The driver used is similar to the SN75188. The receiver used is similar to the SN75189A. The device operates over a wide range of supply voltages ($V_{CC} = \pm 4.5 \text{ V}$ to $\pm 15 \text{ V}$) from the included reference regulator.

logic diagram

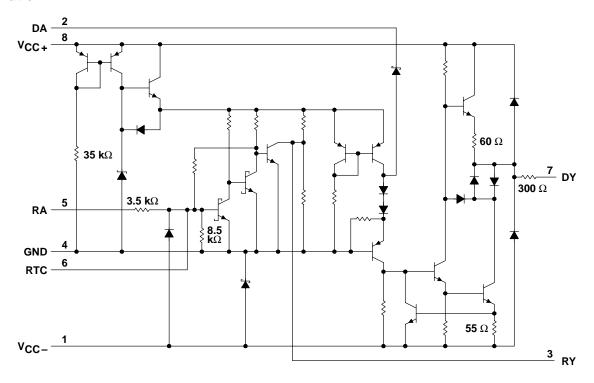




Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC+} (see Note 1)	–0.4 V to 18 V
Supply voltage range, V _{CC} (see Note 1)	0.4 V to –18 V
Input voltage range, V _I : Driver	–5 V to 18 V
Receiver	
Output voltage range, V _O : Driver	
Receiver	0.4 V to 7 V
Output current, I _O (D) Driver	50 mA
Response control current range, I _{RES}	—10 mA to 10 mA
Continuous total power dissipation	See Dissipation Rating Table
Package thermal impedance, θ _{JA} (see Note 2): P package	85°C/W
PS package	95°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 secon	nds 260°C
Storage temperature range, T _{stq}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



recommended operating conditions

			MIN	MAX	UNIT
VCC+	Supply voltage		4.5	15	V
VCC-		-4.5	-15	V	
VI _(D) Input voltage, driver					V
V _{I(R)}	V _{I(R)} Input voltage, receiver				
IRESP	Response control current		-5.5	5.5	mA
IO(R)	Output current, receiver			24	mA
TA	Operating free-air temperature	P package	-20	85	°C
'A		PS package	-20	70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

total device

	PARAMETER	TE	ST CONDITIONS	MIN TYPT	MAX	UNIT
		V _{CC} = ±5 V	$V_{I(D)} = 2 V$	6.3	8.1	
ICCH+	High-level supply current	$V_{CC} = \pm 9 V$	$V_{I(R)} = V_{T+(max)}$	9.1	11.9	mA
		V _{CC} = ±12 V	Output open	10.4	14	
		$V_{CC} = \pm 5 \text{ V}$	$V_{I(D)} = 0.8 \text{ V},$	2.5	3.4	
ICCL+	Low-level supply current	V _{CC} = ±9 V	$V_{I(R)} = V_{T-(min)}$	3.7	5.1	mA
		$V_{CC} = \pm 12 \text{ V}$	Output open	4.1	5.6	
		$V_{CC} = \pm 5 \text{ V}$	$V_{I(D)} = 2 V$	-2.4	-3.1	
ICCH-	ICCH— High-level supply current	$VCC = \pm 9 V$	$V_{I(R)} = V_{T+(max)}$	-3.9	-4.9	mA
		V _{CC} = ±12 V	Output open	-4.8	-6.1	
		$V_{CC} = \pm 5 \text{ V}$	$V_{I(D)} = 0.8 \text{ V},$	-0.2	-0.35	
ICCL-	Low-level supply current	VCC = ±9 V	VI(R) = VT-(min)	-0.25	-0.4	mA
		$V_{CC} = \pm 12 \text{ V}$	Output open	-0.27	-0.45	
loo	Positive supply current		$V_{I(R)} = V_{T+(max)}, V_{I(D)} = 0 V, V_{CC-} = 0 V,$	4.8	6.4	mΔ
ICC+	1 ositive supply current	V _{CC} = ±12 V	Output open	6.7	9.1	mA

[†] All typical values are at $T_A = 25$ °C.

electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 12 V, V_{CC-} = -12 V (unless otherwise noted)

driver section

	PARAMETER	TEST CONDITI	ONS	MIN	TYP	MAX	UNIT
VIH	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
			$V_{CC} = \pm 5 \text{ V}$	3.2	3.7		
Vон	High-level output voltage	$V_{I(D)} = 0.8 \text{ V}, R_L = 3 \text{ k}\Omega$	$V_{CC} = \pm 9 V$	6.5	7.2		V
			$V_{CC} = \pm 12 \text{ V}$	8.9	9.8		
			$V_{CC} = \pm 5 \text{ V}$		-3.6	-3.2	
VOL	Low-level output voltage	$V_{ID)} = 2 V, R_{L} = 3 k\Omega$	$V_{CC} = \pm 9 V$		-7.1	-6.4	V
			$V_{CC} = \pm 12 \text{ V}$		-9.7	-8.8	
lн	High-level input current	$V_{I(D)} = 7 V$				5	μΑ
I _Ι L	Low-level input current	$V_{I(D)} = 0 V$			-0.73	-1.2	mA
los(H)	High-level short-circuit output current	$V_{I(D)} = 0.8 \text{ V}, V_{O(D)} = 0 \text{ V}$		-7	-12	-14.5	mA
IOS(L)	Low-level short-circuit output current	$V_{I(D)} = 2 \text{ V}, V_{O(D)} = 0 \text{ V}$		6.5	11.5	14	mA
rO	Output resistance	$V_{CC+} = 0 \text{ V}, V_{O(D)} = -2 \text{ V to}$	2 V	300			Ω

[†] All typical values are at $T_A = 25$ °C.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = -12 V, T_A = 25°C (unless otherwise noted)

driver section (see Figure 2)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	Propagation delay time, low- to high-level output	$R_1 = 3 k\Omega$, $C_1 = 50 pF$		340	480	20
tPHL	Propagation delay time, high- to low-level output	K[= 3 K22, C[= 50 pr		100	150	ns
tTLH	Transition time, low- to high-level output	$R_1 = 3 k\Omega$, $C_1 = 50 pF$		120	180	20
tTHL	Transition time, high- to low-level output	K[= 3 K22, C[= 50 pr		105	160	ns
tTLH	Transition time, low- to high-level output	R _L = 3 kΩ to 7 kΩ (see Note 3), C _L = 2500 pF		2.1	3	
tTHL	Transition time, high- to low-level output	C _L = 2500 pF		2.1	3	μs

NOTE 3: The time is measured between 3 V and -3 V on output waveform.



electrical characteristics over recommended operating free-air temperature range, V_{CC+} = 12 V, V_{CC-} = -12 V (unless otherwise noted)

receiver section (see Figure 1) (see Note 4)

	PARAMETER	TEST CONDITION	NS	MIN	TYP [†]	MAX	UNIT
V _{IT+}	Positive-going input threshhold voltage			1.2	1.9	2.3	V
V _{IT} _	Negative-going input threshhold voltage			0.6	0.95	1.2	V
V _{hys}	Hystresis voltage (V _{IT+} – V _{IT})			0.6			V
		\(\(\sigma\) = \(\sigma\) = \(\sigma\)	$V_{CC+} = 5 V$	3.7	4.1	4.5	
\/a#\\	High level output voltage		V _{CC+} = 12 V	4.4	4.7	5.2]
VO(H)	High-level output voltage	$V_{I(R)} = V_{T-(min)}$	V _{CC+} = 5 V	3.1	3.4	3.8	
		IOH = -0.4 mA	V _{CC+} = 12 V	3.6	4	4.5	
V _{O(L)}	Low-level output voltage	$V_{I(R)} = V_{T+(max)}$	I _{OL} = 24 mA		0.2	0.3	V
	High level input ourrent	V _{I(R)} = 25 V	V _{I(R)} = 25 V			8.3	mA
l 'IH	High-level input current	$V_{I(R)} = 3 V$	V _{I(R)} = 3 V			1	mA
1	Low level input ourrent	V _{I(R)} = -25 V		-3.6	-6.7	-8.3	mA
¹ı∟	Low-level input current	$V_{I(R)} = -3 V$	-0.43	-0.74	-1	mA	
los	Short-circuit output current	$V_{I(R)} = V_{T-(min)}$			-2.8	-3.7	mA

[†] All typical values are at $T_A = 25$ °C.

NOTE 4: Response Control pin is open.

switching characteristics, $V_{CC+} = 12 \text{ V}$, $V_{CC-} = -12 \text{ V}$, $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

receiver section (see Figure 2)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
^t PLH	Propagation delay time, low- to high-level output	$R_1 = 400 \text{ k}\Omega$, $C_1 = 50 \text{ pF}$		150	240	no
tPHL	Propagation delay time, high- to low-level output	K[= 400 K22, C[= 50 βF		50	100	ns
tTLH	Transition time, low- to high-level output	$R_1 = 400 \text{ k}\Omega$, $C_1 = 50 \text{ pF}$		250	360	no
tTHL	Transition time, high- to low-level output	KL = 400 K22, GL = 50 βF		18	35	ns



PARAMETER MEASUREMENT INFORMATION

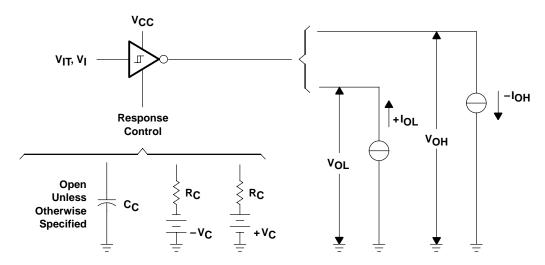
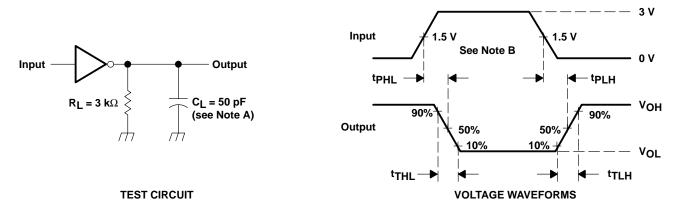


Figure 1. Receiver Section Test Circuit (V_{IT+} , V_{IT-} , V_{OH} , V_{OL})

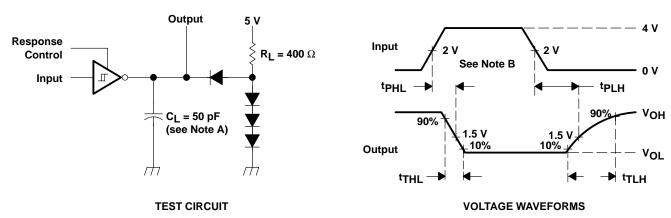


NOTES: A. C_L includes probe and jig capacitance.

B. The input waveform is supplied by a generator having the following characteristics: $Z_O = 50 \Omega$, $t_W = 500 \text{ ns}$, $t_{TLH} \le 5 \text{ ns}$, $t_{THL} \le 5 \text{ ns}$.

Figure 2. Driver Section Switching Test Circuit and Voltage Waveforms

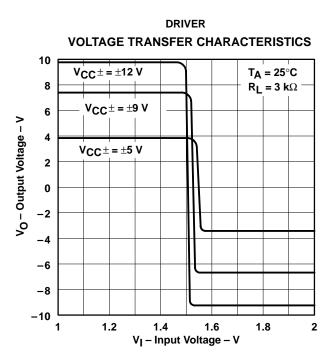
PARAMETER MEASUREMENT INFORMATION



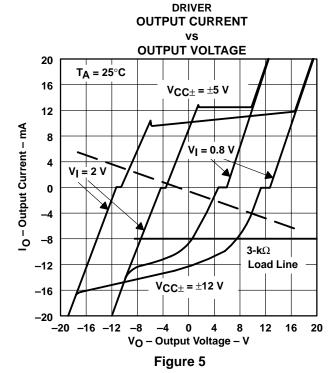
NOTES: A. C_L includes probe and jig capacitance.

B. The input waveform is supplied by a generator having the following characteristics: $Z_O = 50 \Omega$, $t_W = 500 \text{ ns}$, $t_{THL} \le 5 \text{ ns}$, $t_{TLH} \le 5 \text{ ns}$.

Figure 3. Receiver Section Switching Test Circuit and Voltage Waveforms

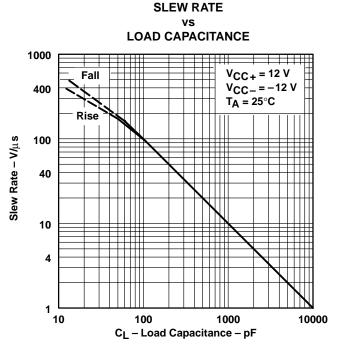






DRIVER SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE 15 los(L) I_{OS}- Short-Circuit Output Current - mA 10 $V_{I(D)} = H$ V_{CC+} = 12 V V_{CC}-=-12 V $V_O = 0$ 5 0 -5 IOS(H) -10 $V_{I(D)} = L$ -15 10 20 30 40 50 70 T_A – Free-Air Temperature – ${}^{\circ}C$

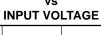
Figure 6



DRIVER

Figure 7

RECEIVER **OUTPUT VOLTAGE** vs



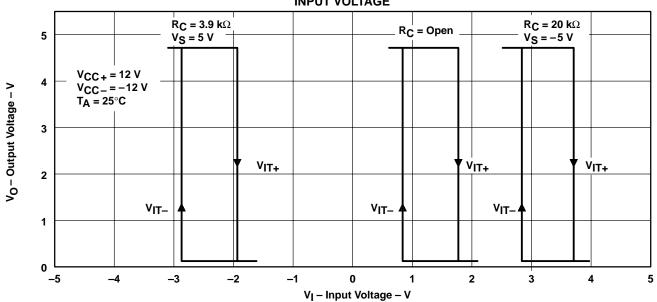


Figure 8

RECEIVER OUTPUT VOLTAGE

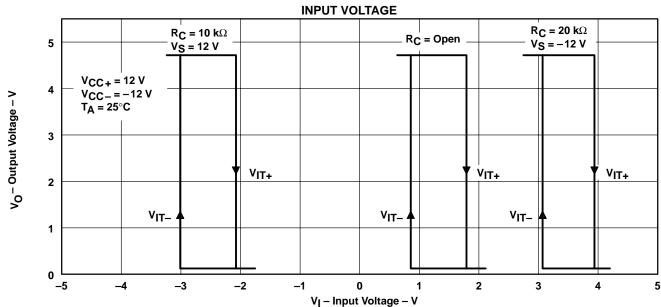
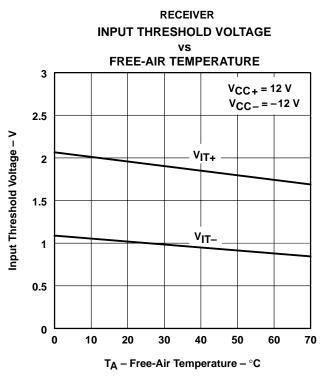


Figure 9





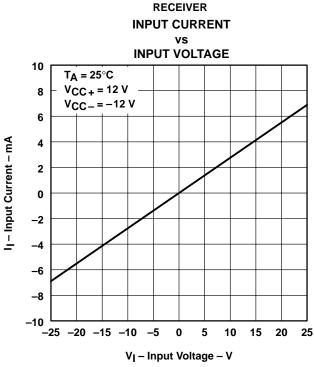
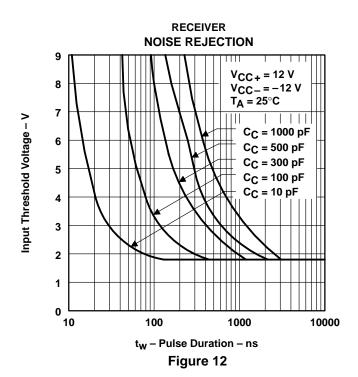
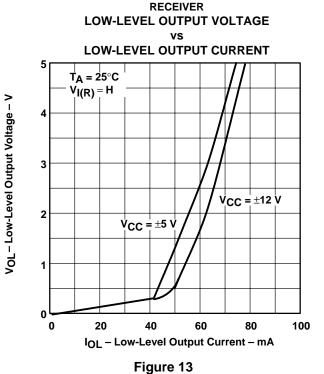


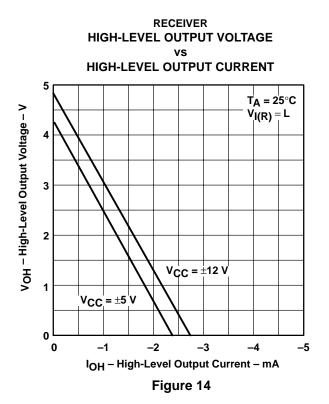
Figure 10

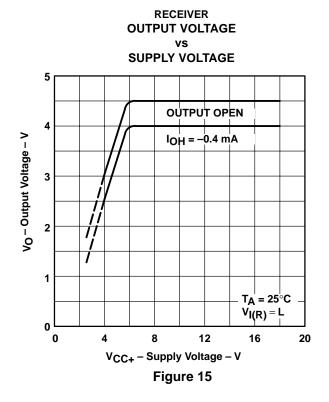






TEXAS INSTRUMENTS





11-Nov-2025

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
						(4)	(5)		
SN751701P	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-20 to 85	SN751701P
SN751701P.A	Active	Production	PDIP (P) 8	50 TUBE	Yes	NIPDAU	N/A for Pkg Type	-20 to 85	SN751701P
SN751701PSR	Active	Production	SO (PS) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 70	A1701
SN751701PSR.A	Active	Production	SO (PS) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-20 to 70	A1701

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

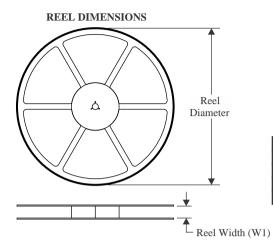
⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

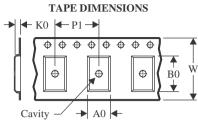
⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

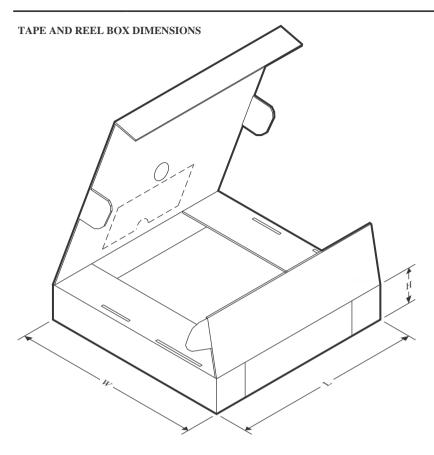


*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN751701PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

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*All dimensions are nominal

Ì	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
ı	SN751701PSR	SO	PS	8	2000	353.0	353.0	32.0	

PACKAGE MATERIALS INFORMATION

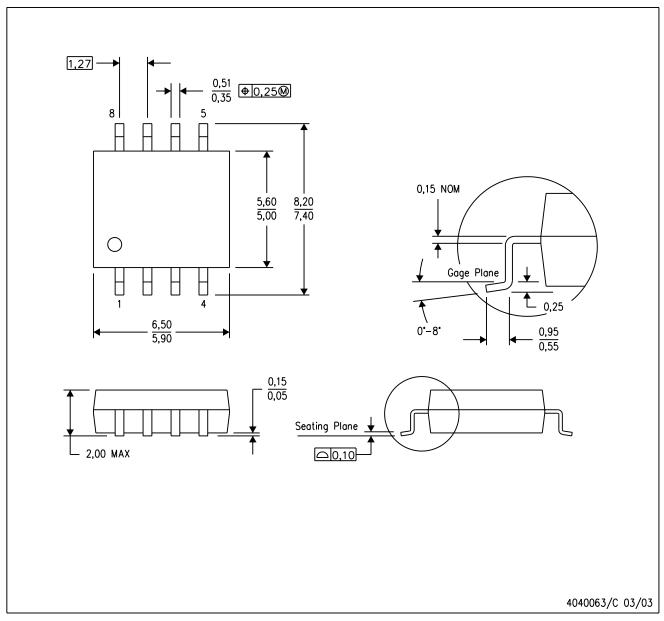
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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN751701P	Р	PDIP	8	50	506	13.97	11230	4.32
SN751701P.A	Р	PDIP	8	50	506	13.97	11230	4.32



NOTES: A. All linear dimensions are in millimeters.

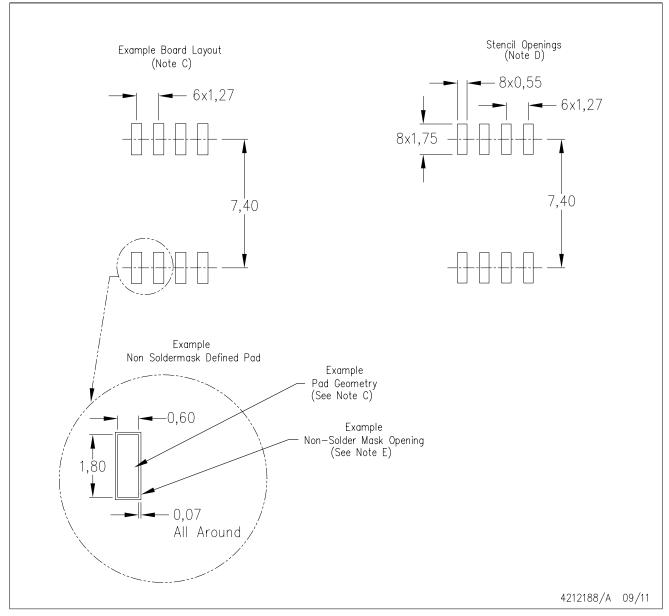
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



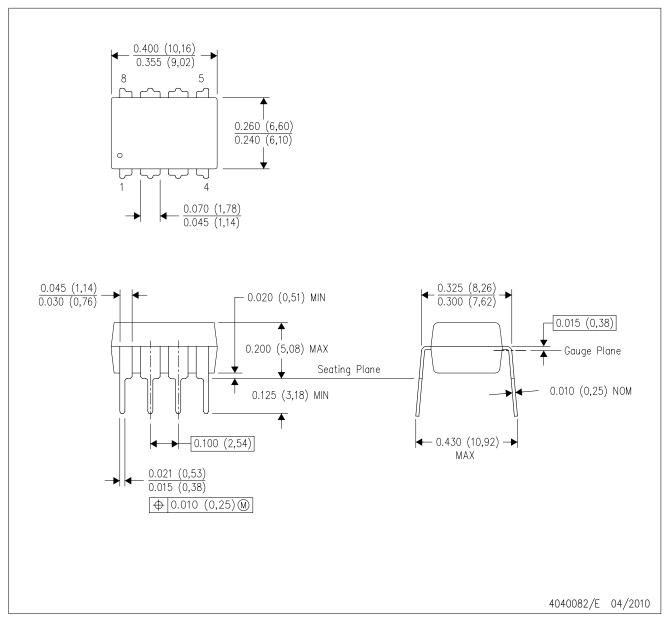
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



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