SN75179B Differential Driver and Receiver Pair

1 Features

- Meets or exceeds the requirements of TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendation V.11
- Bus voltage range: –7V to 12V
- Positive- and negative-current limiting
- Driver output capability: 60mA Max
- Driver thermal-shutdown protection
- Receiver input impedance: 12kΩ Min
- Receiver input sensitivity: ±200mV
- Receiver input hysteresis: 50mV typical
- Operates from single 5V supply
- Low power requirements

2 Description

The SN75179B is a differential driver and receiver pair designed for balanced transmission-line applications and meets TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendation V.11. The device is designed to improve the performance of full-duplex data communications over long bus lines.

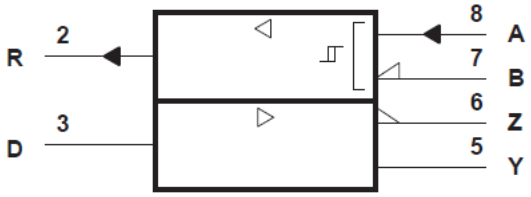
The SN75179B driver output provides limiting for both positive and negative currents. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200mV over a common-mode input voltage range of –7V to 12V. The driver provides thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The SN75179B is designed to drive current loads of up to 60mA maximum.

The SN75179B is characterized for operation from 0°C to 70°C.

Package Information

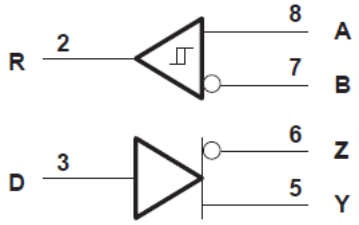
PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN75179B	D (SOIC)	4.9mm x 6mm
	P (PDIP)	9.81mm x 9.43mm
	PS (SOP)	6.2mm x 7.8mm

(1) For all available packages, see Section 9.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



A. This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Logic Symbol



Logic Diagram (Positive Logic)

Table of Contents

3 Pin Configuration and Functions

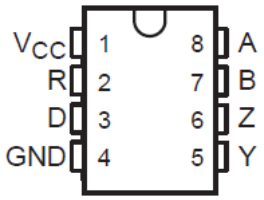


Figure 3-1. D, PS, or P Package
Top View

Table 3-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1	V_{CC}	P	5V Voltage Supply
2	R	O	RS485 Logic Output
3	D	I	RS485 Logic Input
4	GND	G	Ground
5	Y	O	Non-Inverting RS485 Bus Output
6	Z	O	Inverted RS485 Bus Output
7	B	I	Inverted RS485 Bus Input
8	A	I	Non-Inverting RS485 Bus Input

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		7	V
	Voltage range at any bus terminal	–10	15	V
V_{ID}	Differential input voltage (3)		±25	V
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	Driver	2			V
V_{IL}	Low-level input voltage	Driver			0.8	V
V_{IC}	Common-mode input voltage		–7(1)		12	V
V_{ID}	Differential input voltage,				±12	V
I_{OH}	High level output current	Driver			–60	mA
		Receiver			–400	µA
I_{OL}	Low level output current	Driver			60	mA
		Receiver			8	mA
T_A	Operating free-air temperature		0		70	°C

(1) The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage.

4.3 Thermal Information

THERMAL METRIC(1)		SOIC (D)	PDIP (P)	SOP (PS)	UNIT
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	109.5	84.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	53.9	65.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	65.7	62.1	
ψ_{JT}	Junction-to-top characterization parameter	8.8	11.6	31.3	
ψ_{JB}	Junction-to-board characterization parameter	62.6	64.5	60.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

4.4 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100Ω	See Figure 5-1	1/2 V_{OD1}			V
				2(2)			
		R_L = 54Ω	See Figure 5-1	1.5	2.5	5	V
$\|V_{OD3}\|$	Differential output voltage	See (4)		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage					±0.2	V
V_{OC}	Common mode output voltage	R_L = 54Ω or 100Ω,	See Figure 5-1			3	V
						–1	
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(3)					±0.2	V
I_O	Output current	V_{CC} = 0	V_O = -7V to 12V			±100	µA
I_{IH}	High-level input current	V_{IH} = 2.4V				20	µA
I_{IL}	Low-level input current	V_{IL} = 0.4V				–200	µA
I_{OS}	Short circuit output current	V_O = –7V				–250	mA
		V_O = V_{CC}				250	
		V_O = 12V				250	
I_{CC}	Supply current (total package)	No load			57	70	mA

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) The minimum V_{OD2} with 100Ω load is either 1/2 VOD2 or 2V, whichever is greater
(3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(4) See TIA/EIA-485-A, Figure 3.5, Test Termination Measurement 2.

4.5 Switching Characteristics

V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54Ω	See Figure 5-3		15	22	ns
$t_{t(OD)}$	Differential output transition time	R_L = 54Ω	See Figure 5-3		20	30	ns

4.6 Symbol Equivalent

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\| V_{OD1} \|$	V_o	V_o
$\| V_{OD2} \|$	$V_t(R_L$ = 100Ω)	$V_t(R_L$ = 54Ω)
$\| V_{OD3} \|$		V_t (Test Termination Measurement 2)
D $\| V_{OD} \|$	$\| \| V_t \| - \| \overline{V}t_t \| \|$	$\| \| V_t \| - \| \overline{V}_t \| \|$
V_{OC}	$\| V_{os} \|$	$\| V_{os} \|$
D $\| V_{OC} \|$	$\| V_{os} - V_{os} \|$	$\| V_{os} - \overline{V}_{os} \|$
I_{OS}	$\|I_{sa}\|$, $\| I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\| I_{xb}\|$	I_{ia}, I_{ib}

4.7 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7V	I_O = –0.4mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5V	I_O = 8mA		–0.2(2)			V
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT–}$)					50		mV
V_{OH}	High-level output voltage	V_{ID} = 200mV	I_{OH} = -400µA	See Figure 5-2	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = -200mV	I_{OL} = 8mA	See Figure 5-2			0.45	V
I_I	Line input current	Other input at 0V	See (3)	V_I = 12V			1	mA
				V_I = –7V			–0.8	mA
r_I	Input resistance				12			kΩ
I_{OS}	Short-circuit output current				–15		–85	mA
I_{OS}	Supply current (total package)	No load				57	70	mA

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) See TIA/EIA-422-B for exact conditions.

4.8 Switching Characteristics

V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = –1.5V to 1.5V			19	35	ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 15pF	See Figure 5-4		30	40	ns

4.9 Typical Characteristics

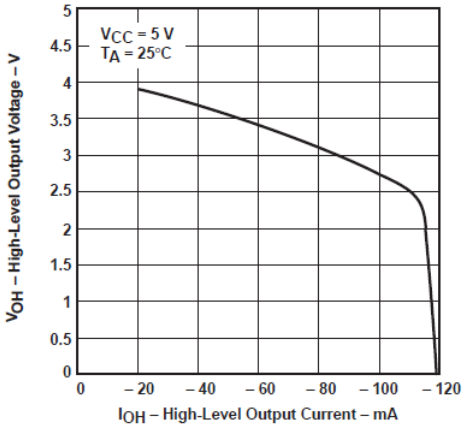


Figure 4-1. Driver High-Level Output Voltage vs High-Level Output Current

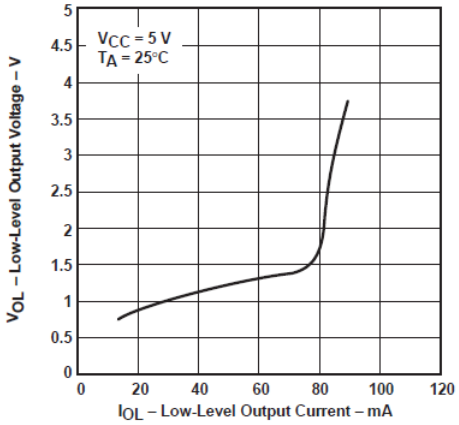


Figure 4-2. Driver Low-Level Output Voltage vs Low-Level Output Current

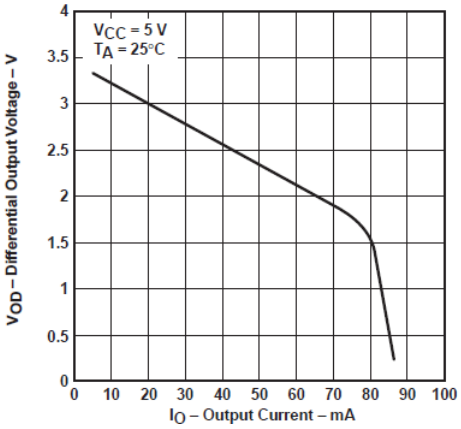


Figure 4-3. Driver Differential Output Voltage vs Output Current

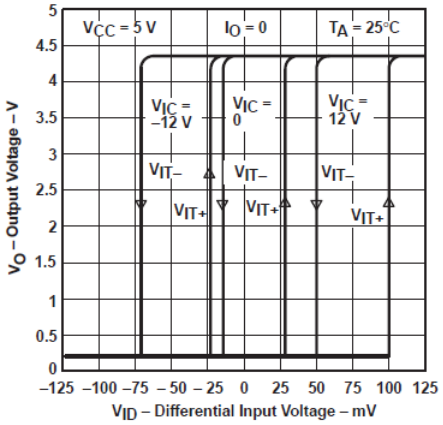


Figure 4-4. Receiver Output Voltage vs Differential Input Voltage

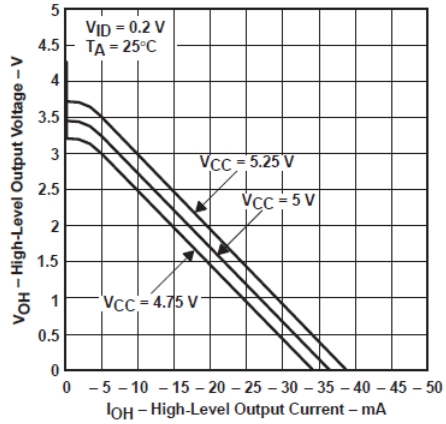


Figure 4-5. High-Level Output Voltage vs High-Level Output Current

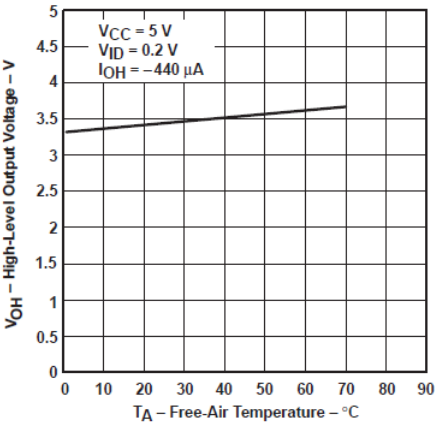


Figure 4-6. High-Level Output Voltage vs Free-Air Temperature

4.9 Typical Characteristics (continued)

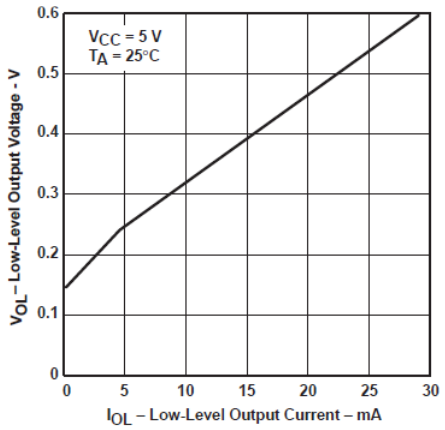


Figure 4-7. Receiver Low-Level Output Voltage vs Low-Level Output Current

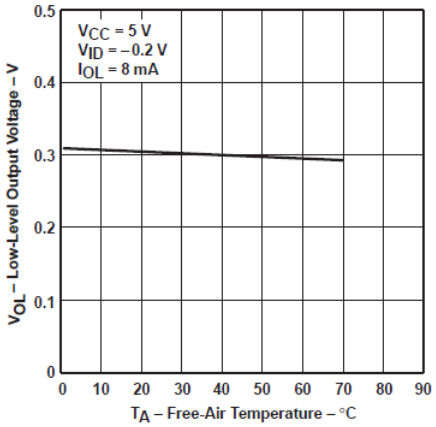


Figure 4-8. Receiver Low-Level Output Voltage vs Free-Air Temperature

5 Parameter Measurement Information

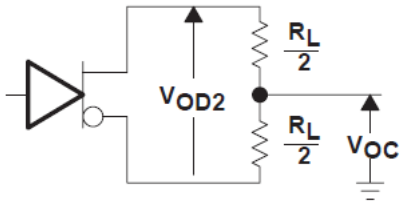


Figure 5-1. Driver V_{DD} and V_{OC}

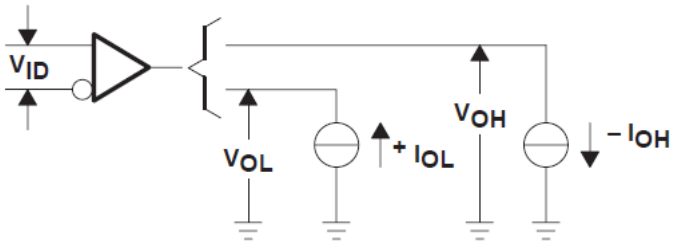
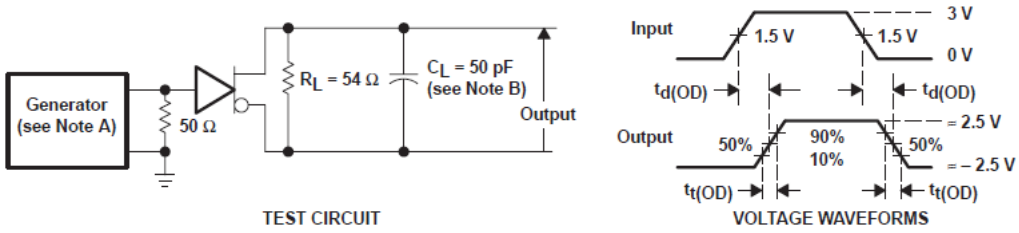


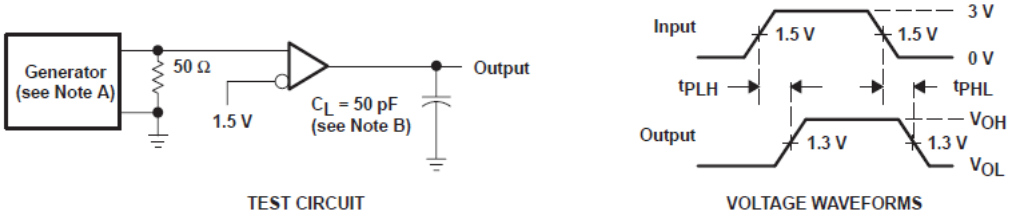
Figure 5-2. Receiver V_{OH} and V_{OL}



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1MHz, 50% duty cycle, t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50Ω.

B. C_L includes probe and jig capacitance.

Figure 5-3. Driver Test Circuit and Voltage Waveforms



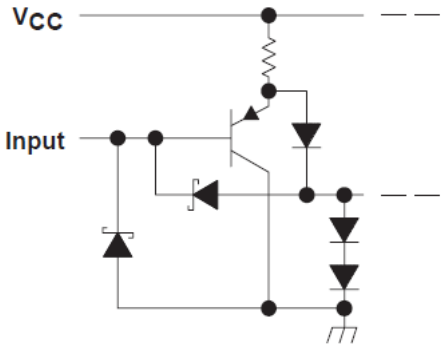
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1MHz, 50% duty cycle, t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50Ω.

B. C_L includes probe and jig capacitance.

Figure 5-4. Receiver Test Circuit and Voltage Waveforms

6 Detailed Description

6.1 Functional Block Diagram



A. Driver input: $R_{(eq)}$ = 3kΩ NOM$R_{(eq)}$ = equivalent resistor

Figure 6-1. Equivalent of Driver Input

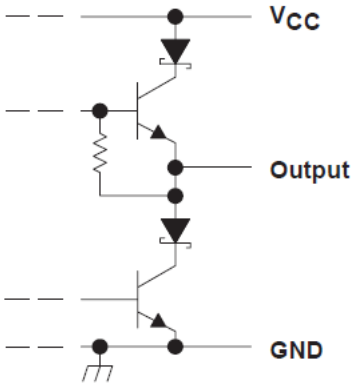


Figure 6-2. Typical of All Driver Outputs

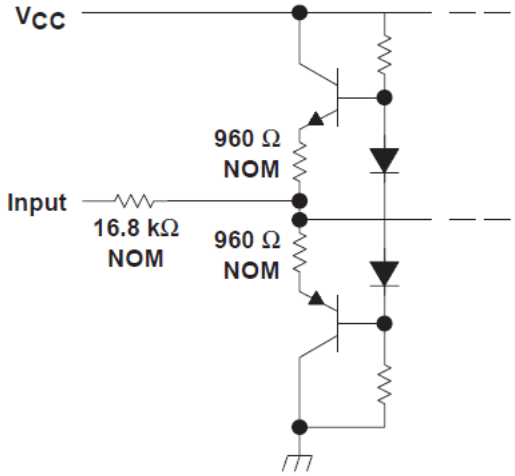


Figure 6-3. Equivalent of Each Receiver Input

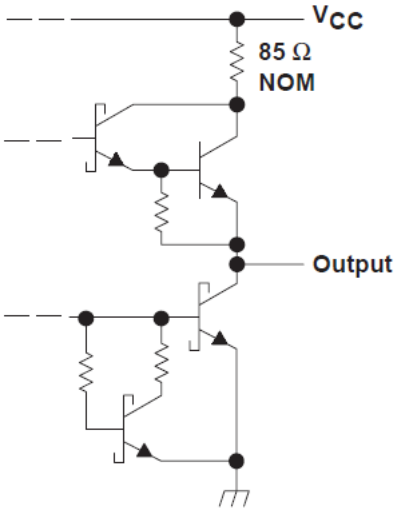


Figure 6-4. Typical of All Receiver Outputs

6.2 Device Functional Modes

Table 6-1. Driver (1)

INPUT D	OUTPUTS	
	Y	Z
H	H	L
L	L	H

(1) H = high level, L = low level, ? = indeterminate

Table 6-2. Receiver

DIFFERENTIAL INPUTS A – B	OUTPUT(1) R
$V_{ID} \geq 0.2V$	H
$-0.2V < V_{ID} < 0.2V$	?
$V_{ID} \leq -0.2V$	L
Open	?

(1) H = high level, L = low level, ? = indeterminate

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Documentation Support

7.1.1 Related Documentation

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (October 2022) to Revision G (April 2025)	Page
• Updated the *Package Information* table	1
• Changed the I_{OH} driver max value from −602mA to −60mA in the *Recommended Operating Conditions*	4

Changes from Revision E (June 2008) to Revision F (October 2022)	Page
• Changed the data sheet format to the latest data sheet format	1
• Changed the *Thermal Information* table	4

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75179BDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75179B
SN75179BDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75179B
SN75179BDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75179B
SN75179BP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75179BP
SN75179BP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75179BP
SN75179BPE4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75179BP
SN75179BPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A179B
SN75179BPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A179B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

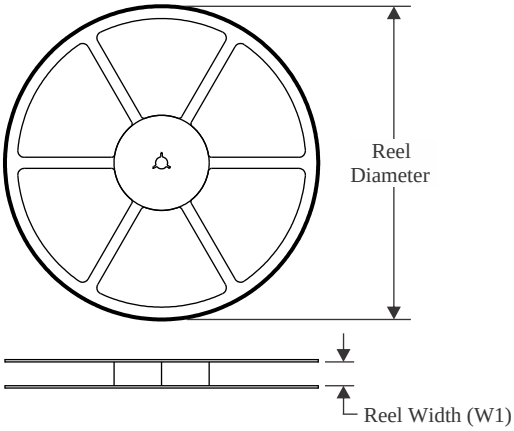
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

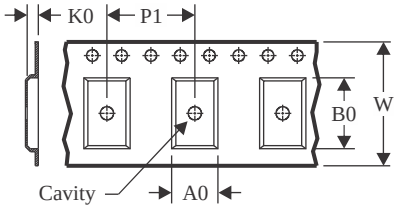
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

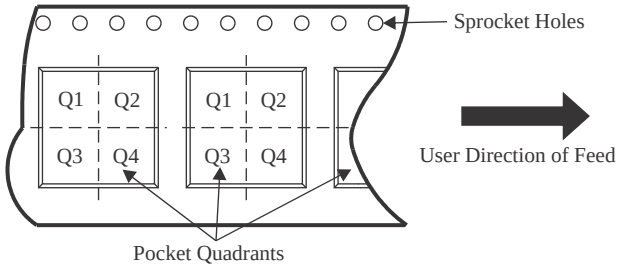


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

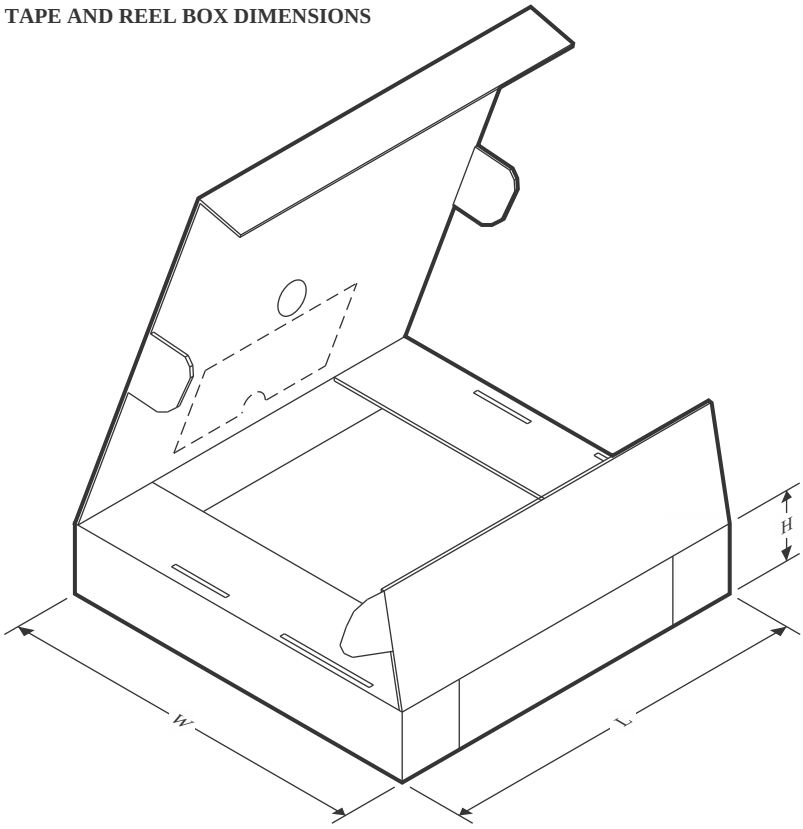
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75179BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75179BPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

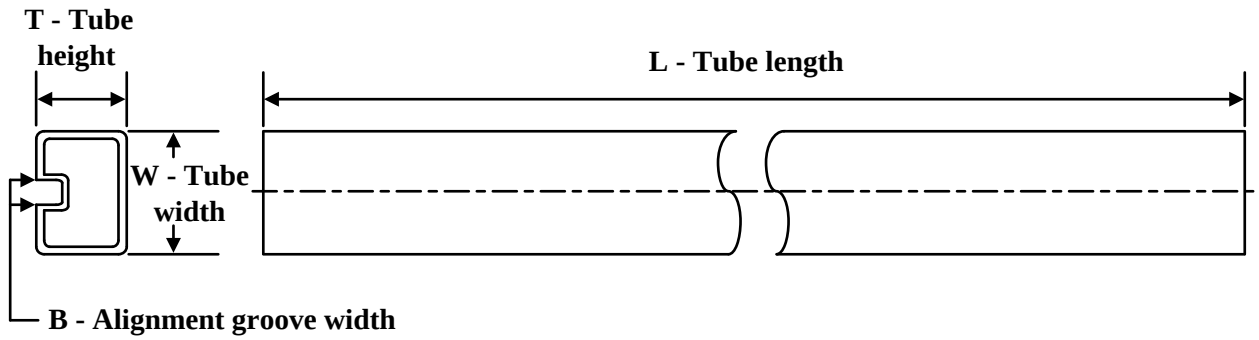
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

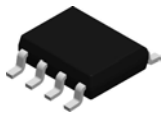
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75179BDR	SOIC	D	8	2500	353.0	353.0	32.0
SN75179BPSR	SO	PS	8	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75179BP	P	PDIP	8	50	506	13.97	11230	4.32
SN75179BP.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75179BPE4	P	PDIP	8	50	506	13.97	11230	4.32

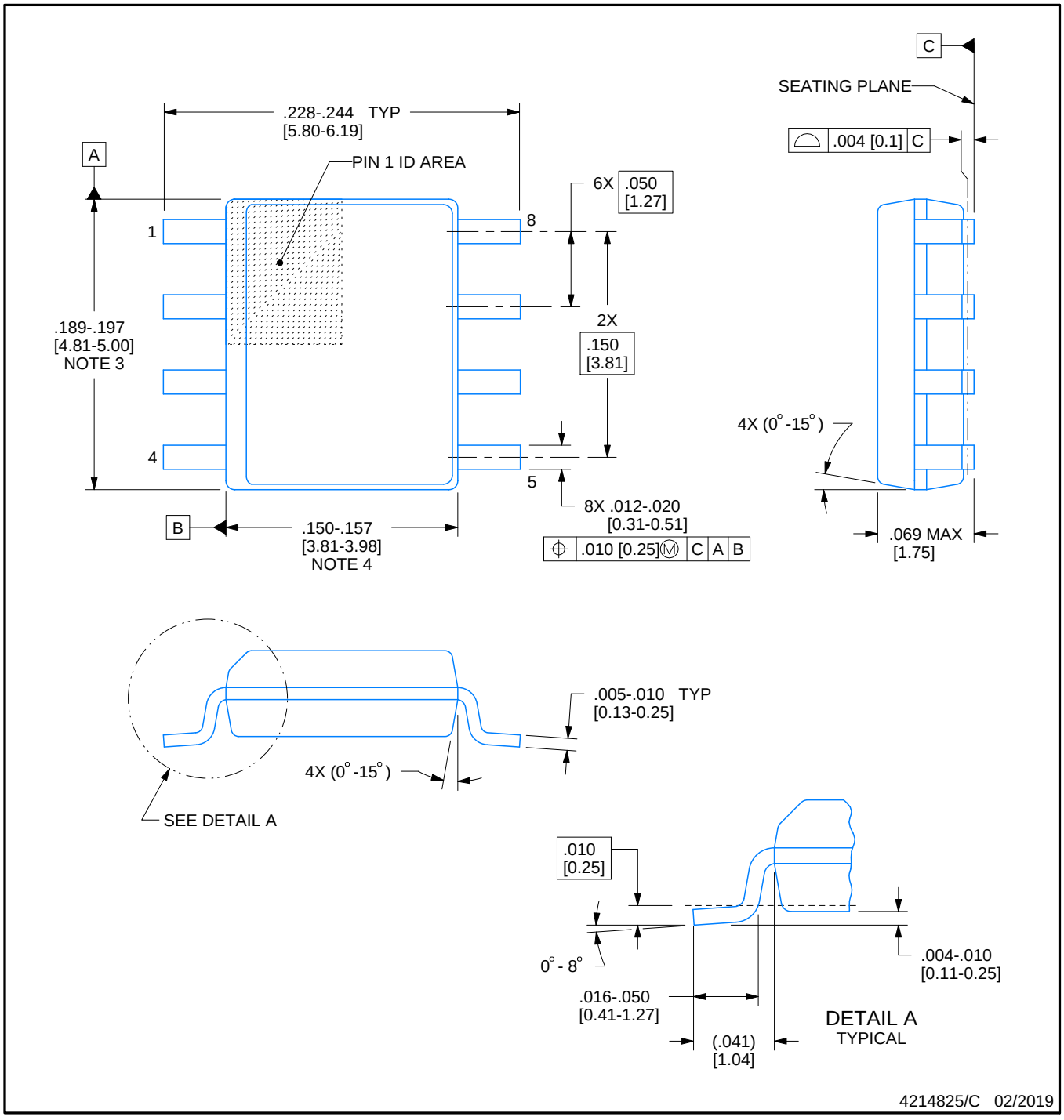


PACKAGE OUTLINE

D0008A

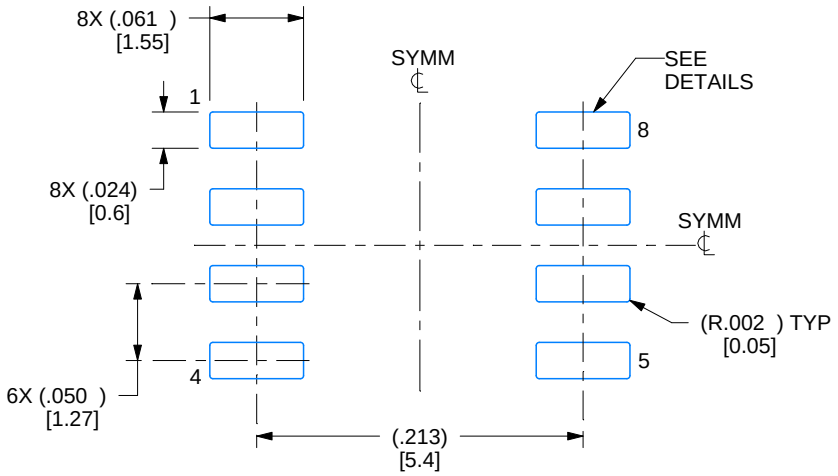
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

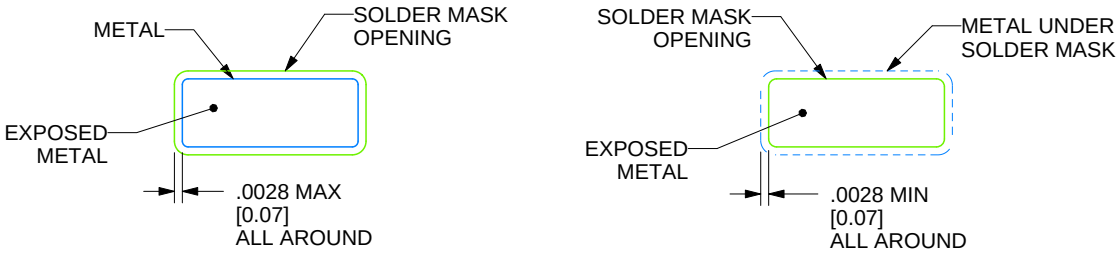


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

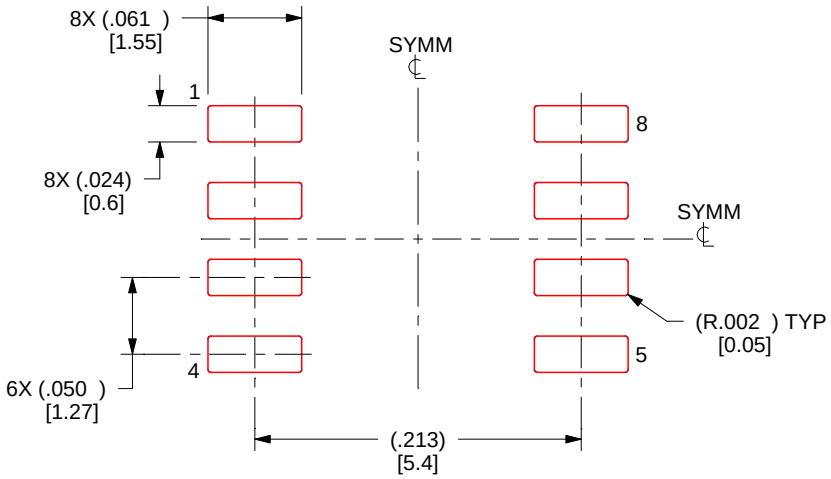
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

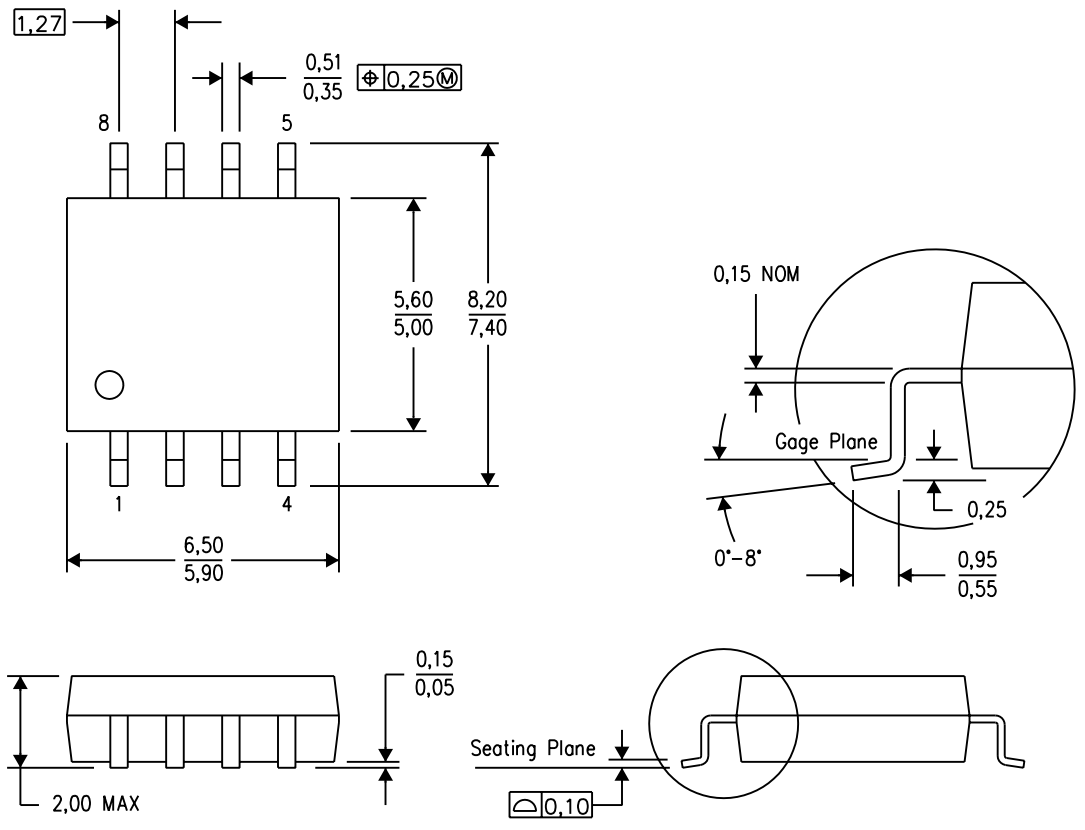
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

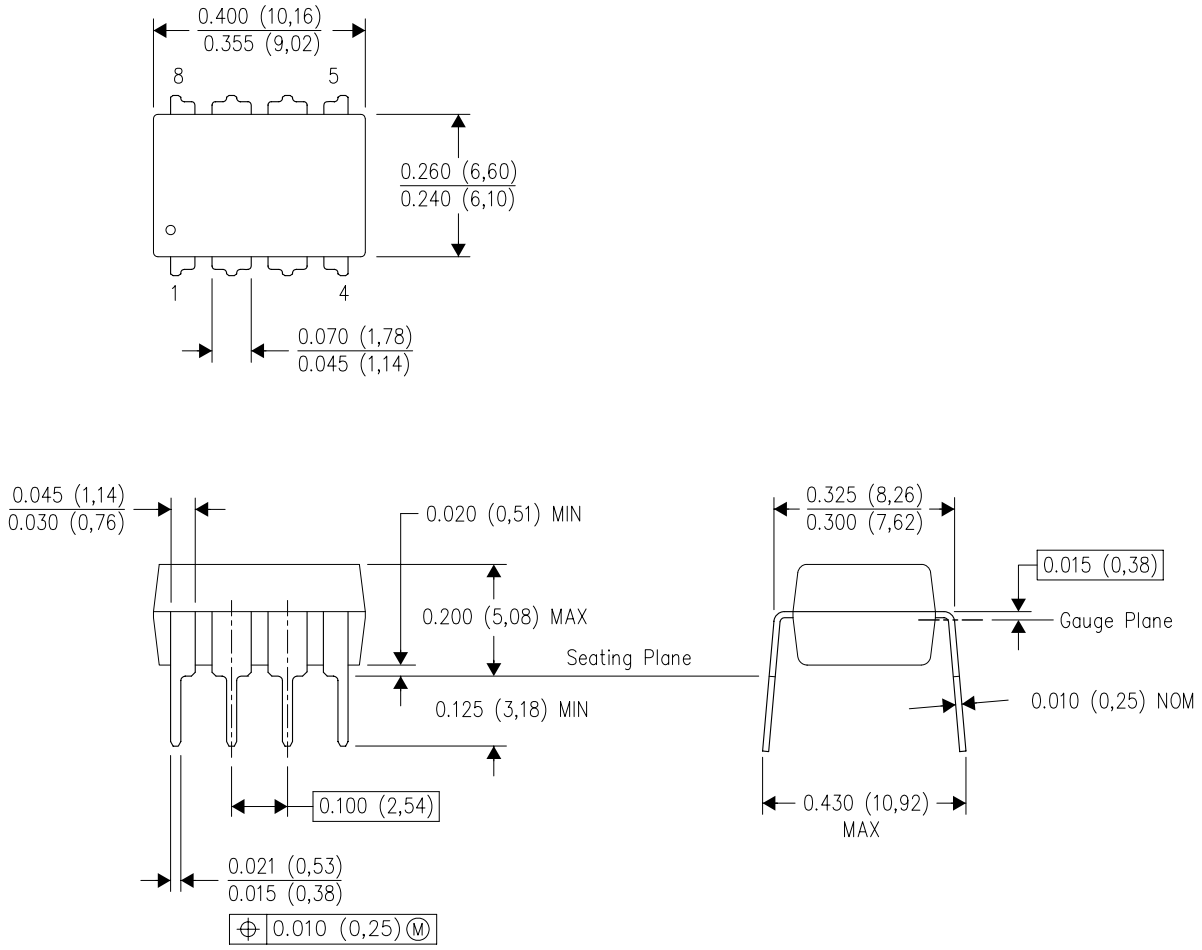
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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