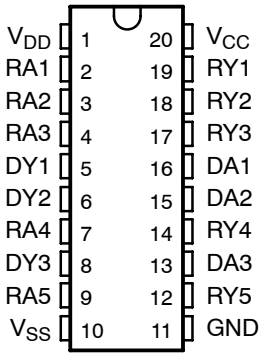
SN75185
MULTIPLE RS-232 DRIVERS AND RECEIVERS

SLLS181D–DECEMBER 1994–REVISED JANUARY 2006

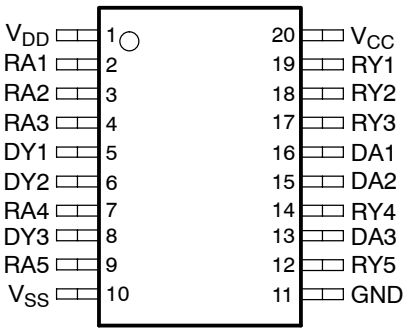
FEATURES

- **Single Chip With Easy Interface Between UART and Serial-Port Connector of IBM™ PC/AT™ and Compatibles**
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Supports Data Rates up to 120 kbit/s**
- **ESD Protection Meets or Exceeds 10 kV on RS-232 Pins and 3.5 kV on All Other Pins (Human-Body Model)**
- **Pin-to-Pin Compatible With the SN75C185**

N PACKAGE
(TOP VIEW)



DB, DW, OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN75185 combines three drivers and five receivers from the TI SN75188 and SN75189 bipolar quadruple drivers and receivers, respectively. The pinout matches the flow-through design of the SN75C185 to decrease the part count, reduce the board space required, and allow easy interconnection of the UART and serial-port connector of IBM™ PC/AT™ and compatibles. The bipolar circuits and processing of the SN75185 provide a rugged low-cost solution for this function at the expense of quiescent power and external passive components relative to the SN75C185.

The SN75185 complies with the requirements of the TIA/EIA-232-F and ITU v.28 standards. These standards are for data interchange between a host computer and peripheral at signaling rates up to 20 kbit/s. The switching speeds of the SN75185 are fast enough to support rates up to 120 kbit/s with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be assured unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates to 120 kbit/s, use of TIA/EIA-423-B (ITU v.10) and TIA/EIA-422-B (ITU v.11) standards is recommended.

The SN75185 is characterized for operation over the temperature range of 0°C to 70°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

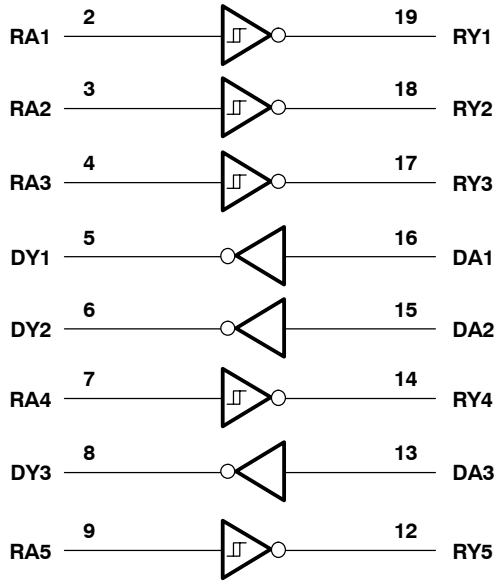
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ORDERING INFORMATION

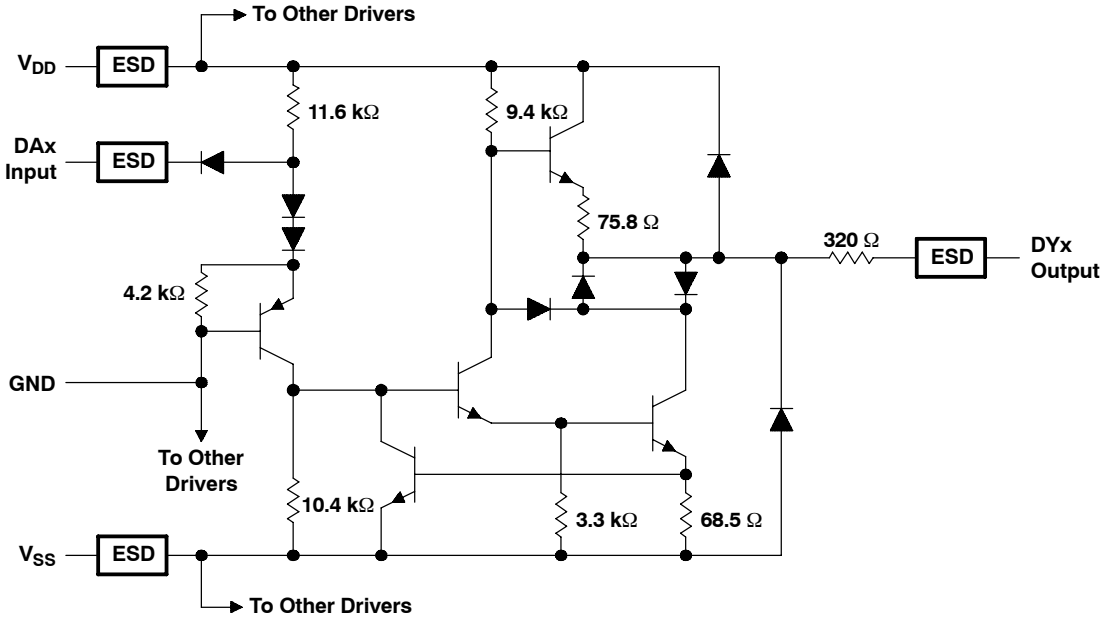
T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube of 20	SN75185N	SN75185N
	SOIC – DW	Tube of 25	SN75185DW	SN75185
		Reel of 2000	SN75185DWR	
	SSOP – DB	Tube of 70	SN75185DB	A185
		Reel of 2000	SN75185DBR	
	TSSOP – PW	Tube of 70	SN75185PW	A185
		Reel of 2000	SN75185PWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

LOGIC DIAGRAM (POSITIVE LOGIC)

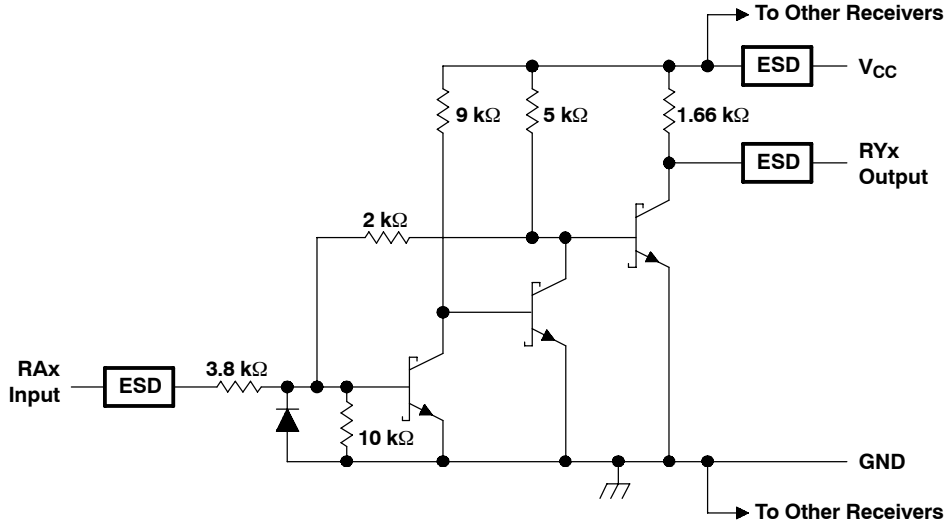


SCHEMATIC OF DRIVERS



Resistor values shown are nominal.

SCHEMATIC (EACH RECEIVER)



Resistor values shown are nominal.

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{CC}	Supply voltage (2)				10	V
V_{DD}	Supply voltage (2)				15	V
V_{SS}	Supply voltage (2)				–15	V
	Input voltage range	Driver		–15	7	V
		Receiver		–30	30	
	Driver output voltage range			–15	15	V
	Receiver low-level output current				20	mA
θ_{JA}	Package thermal impedance (3) (4)	DB package			70	°C/W
		DW package			58	
		N package			69	
		PW package			83	
T_J	Operating virtual junction temperature				150	°C
	Electrostatic discharge	Human-Body Model	RS-232 pins, class 3, A (5)		10	kV
			All pins, class 3, A (6)		3.5	
		Machine Model	RS-232 pins, class 3, B (7)		600	V
			All pins, class 3, B (5)		250	
T_{stg}	Storage temperature range			–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the network ground terminal.
(3) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) RS-232 pins are tested with respect to ground and to each other.
(6) Per MIL-PRF-38535
(7) RS-232 pins are tested with respect to ground.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{DD}	Supply voltage		7.5	9	15	V
V_{SS}	Supply voltage		–7.5	–9	–15	V
V_{IH}	High-level input voltage (drivers only)		1.9			V
V_{IL}	Low-level input voltage (drivers only)				0.8	V
I_{OH}	High-level output current	Drivers			–6	mA
		Receivers			–0.5	
I_{OL}	Low-level output current	Drivers			6	mA
		Receivers			16	
T_A	Operating free-air temperature		0		70	°C

Supply Currents

PARAMETER		TEST CONDITIONS				MIN	MAX	UNIT
I_{CC}	Supply current from V_{CC}	All inputs at 5 V,	No load,	V_{CC} = 5 V			30	mA
I_{DD}	Supply current from V_{DD}	All inputs at 1.9 V,	No load	V_{DD} = 9 V,	V_{SS} = –9 V		15	mA
				V_{DD} = 12 V,	V_{SS} = –12 V		19	
				V_{DD} = 15 V,	V_{SS} = –15 V		25	
		All inputs at 0.8 V,	No load	V_{DD} = 9 V,	V_{SS} = –9 V		4.5	
				V_{DD} = 12 V,	V_{SS} = –12 V		5.5	
				V_{DD} = 15 V,	V_{SS} = –15 V		9	
I_{SS}	Supply current from V_{SS}	All inputs at 1.9 V,	No load	V_{DD} = 9 V,	V_{SS} = –9 V		–15	mA
				V_{DD} = 12 V,	V_{SS} = –12 V		–19	
				V_{DD} = 15 V,	V_{SS} = –15 V		–25	
		All inputs at 0.8 V,	No load	V_{DD} = 9 V,	V_{SS} = –9 V		–3.2	
				V_{DD} = 12 V,	V_{SS} = –12 V		–3.2	
				V_{DD} = 15 V,	V_{SS} = –15 V		–3.2	

DRIVER SECTION

Electrical Characteristics

over recommended operating free-air temperature range, V_{DD} = 9 V, V_{SS} = –9 V, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	R_L = 3 kΩ,	See Figure 1	6	7.5		V
V_{OL}	Low-level output voltage(1)	V_{IH} = 1.9 V,	R_L = 3 kΩ,	See Figure 1		–7.5	–6	V
I_{IH}	High-level input current	V_I = 5 V,	See Figure 2				10	μA
I_{IL}	Low-level input current	V_I = 0,	See Figure 2				–1.6	mA
$I_{OS(H)}$	High-level short-circuit output current(2)	V_{IL} = 0.8 V,	V_O = 0,	See Figure 1	–4.5	–12	–19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current	V_{IH} = 2 V,	V_O = 0,	See Figure 1	4.5	12	19.5	mA
r_o	Output resistance(3)	V_{CC} = V_{DD} = V_{SS} = 0,		V_O = –2 V to 2 V	300			Ω

(1) The algebraic convention, in which the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only (e.g., if –10 V is maximum, the typical value is a more negative voltage).
(2) Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.
(3) Test conditions are those specified by TIA/EIA-232-F and as listed above.

Switching Characteristics

V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = –12 V, T_A = 25°C (see Figure 3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 3 kΩ to 7 kΩ,	C_L = 15 pF		315	500	ns
t_{PHL}	Propagation delay time, high- to low-level output	R_L = 3 kΩ to 7 kΩ,	C_L = 15 pF		75	175	ns
t_{TLH}	Transition time, low- to high-level output	R_L = 3 kΩ to 7 kΩ	C_L = 15 pF		60	100	ns
			C_L = 2500 pF(1)		1.7	2.5	μs
t_{THL}	Transition time, high- to low-level output	R_L = 3 kΩ to 7 kΩ	C_L = 15 pF		40	75	ns
			C_L = 2500 pF(2)		1.5	2.5	μs

(1) Measured between –3-V and 3-V points of the output waveform (TIA/EIA-232-F conditions); all unused inputs are tied either high or low.
(2) Measured between 3-V and –3-V points of the output waveform (TIA/EIA-232-F conditions); all unused inputs are tied either high or low.

RECEIVER SECTION

Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{T+}	Positive-going threshold voltage	See Figure 5	T_A = 25°C	1.75	1.9	2.3	V
			T_A = 0°C to 70°C	1.55		2.3	
V_{T-}	Negative-going threshold voltage			0.75	0.97	1.25	V
V_{hys}	Input hysteresis ($V_{T+} - V_{T-}$)			0.5			V
V_{OH}	High-level output voltage	I_{OH} = –0.5 mA	V_{IH} = 0.75 V	2.6	4	5	V
			Inputs open	2.6			
V_{OL}	Low-level input voltage	I_{OL} = 10 mA,	V_I = 3 V		0.2	0.45	V
I_{IH}	High-level input current	V_I = 25 V,	See Figure 5	3.6		8.3	mA
		V_I = 3 V,	See Figure 5	0.43			
I_{IL}	Low-level output current	V_I = –25 V,	See Figure 5	–3.6		–8.3	mA
		V_I = –3 V,	See Figure 5	–0.43			
I_{OS}	Short-circuit output current	See Figure 4			–3.4	–12	mA

(1) All typical values are at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 9 V, and V_{SS} = –9 V.

Switching Characteristics

V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = -12 V, T_A = 25°C (see Figure 6)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 50 pF,	R_L = 5 kΩ		107	500	ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 50 pF,	R_L = 5 kΩ		42	150	ns
t_{TLH}	Transition time, low- to high-level output	C_L = 50 pF,	R_L = 5 kΩ		175	525	ns
t_{THL}	Transition time, high- to low-level output	C_L = 50 pF,	R_L = 5 kΩ		16	60	ns

PARAMETER MEASUREMENT INFORMATION

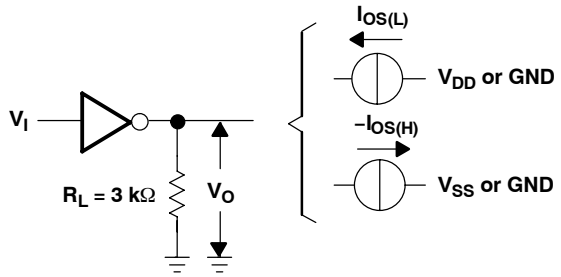


Figure 1. Driver Test Circuit for V_{OH}, V_{OL}, $I_{OS(H)}$, and $I_{OS(L)}$

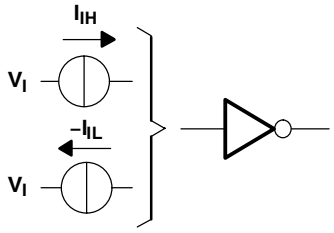
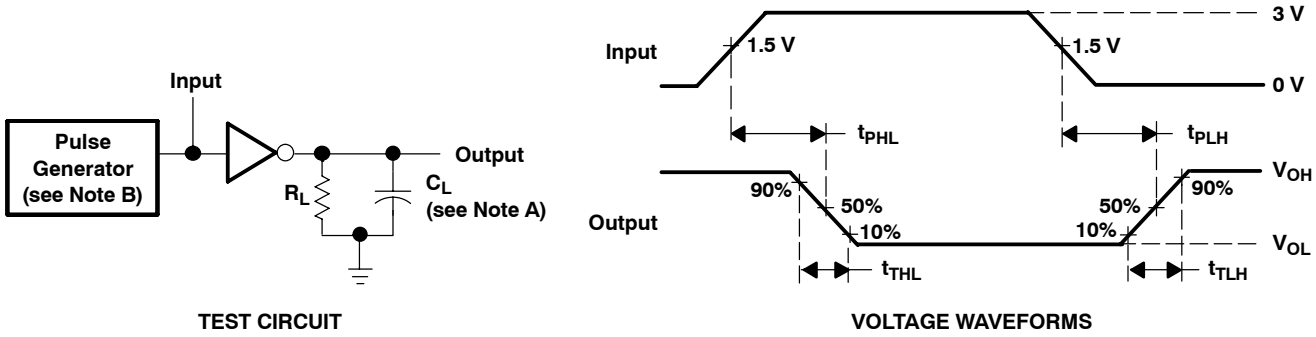


Figure 2. Driver Test Circuit for I_{IH} and I_{IL}



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.

Figure 3. Driver Test Circuit and Voltage Waveforms

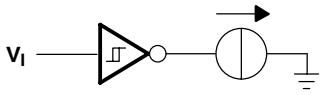


Figure 4. Receiver Test Circuit for I_{OS}

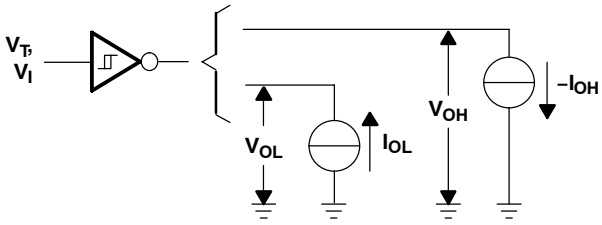
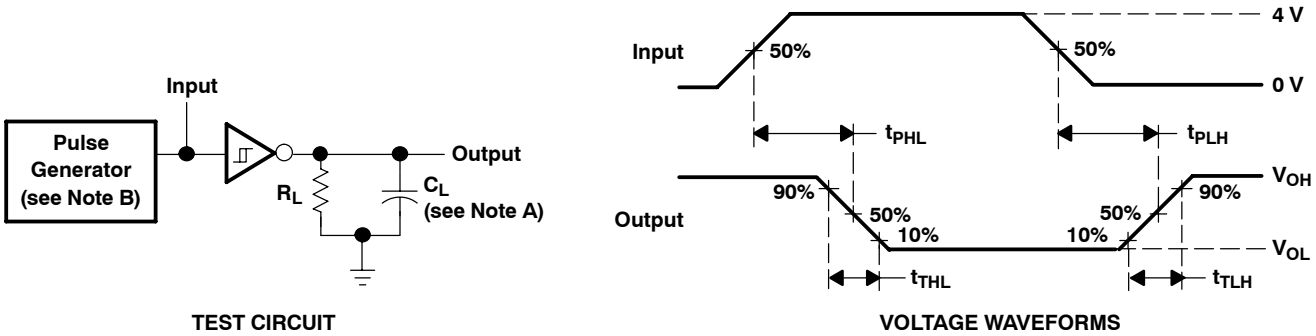


Figure 5. Receiver Test Circuit for V_T, V_{OH}, and V_{OL}

PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: t_w = 25 μs, PRR = 20 kHz, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.

Figure 6. Receiver Propagation and Transition Times

TYPICAL CHARACTERISTICS

DRIVER SECTION

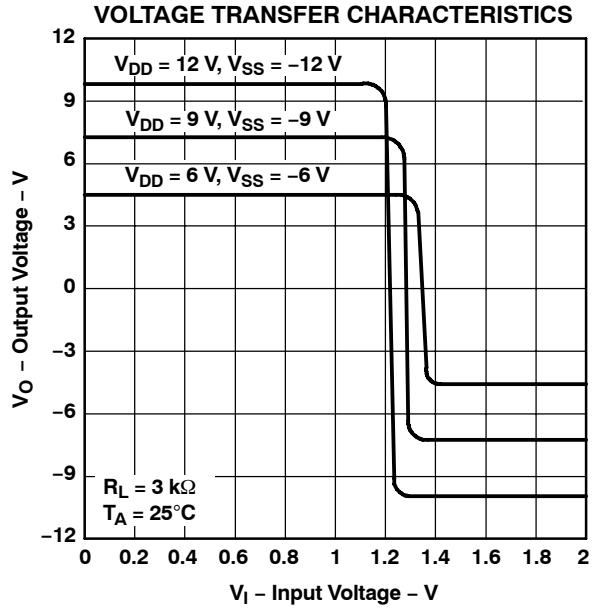


Figure 7.

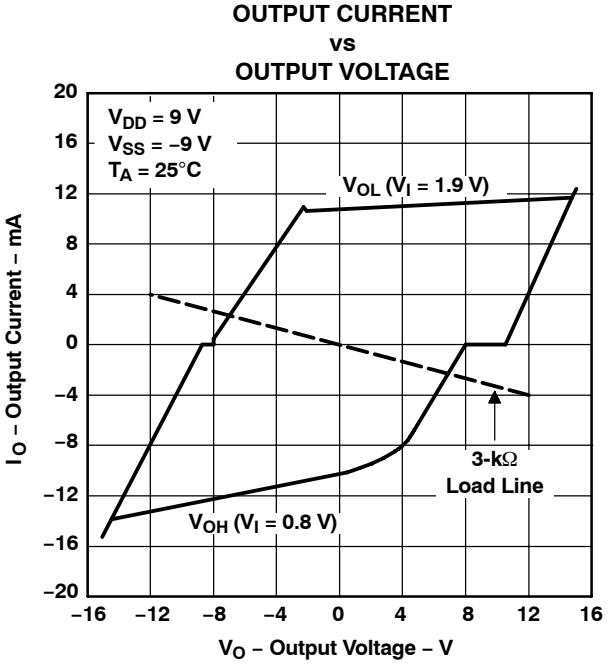


Figure 8.

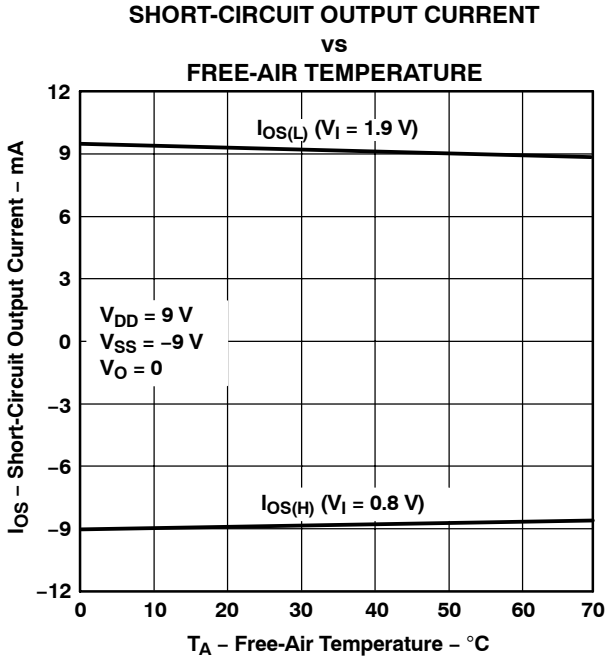


Figure 9.

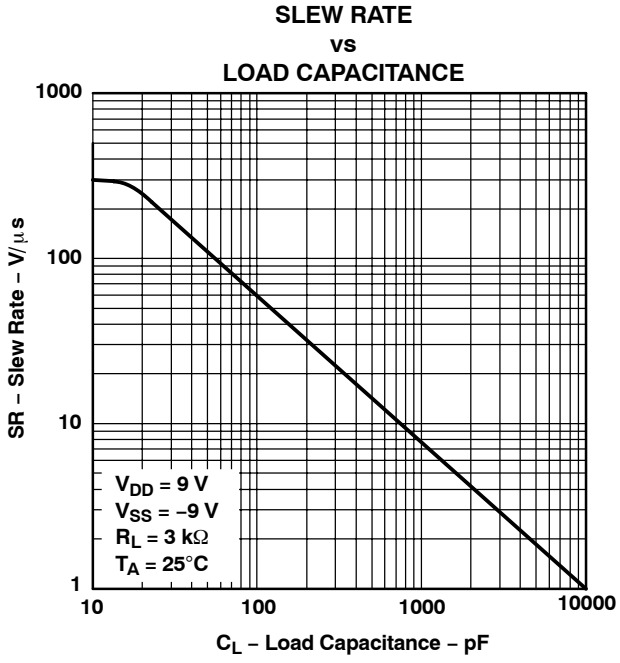


Figure 10.

TYPICAL CHARACTERISTICS

RECEIVER SECTION

INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

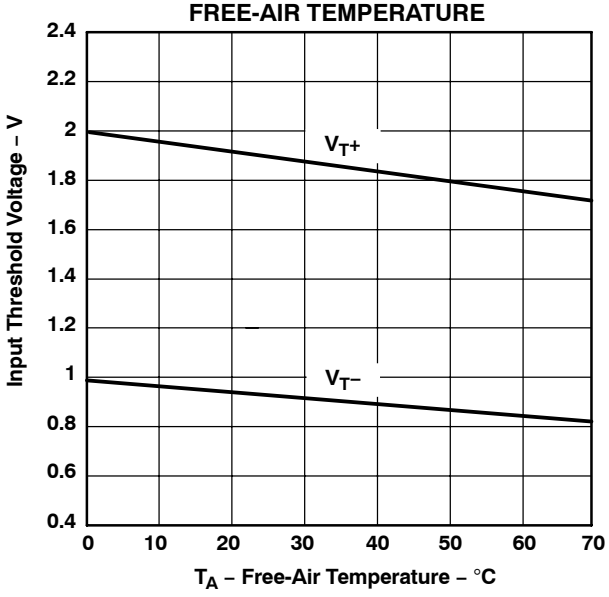


Figure 11.

INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

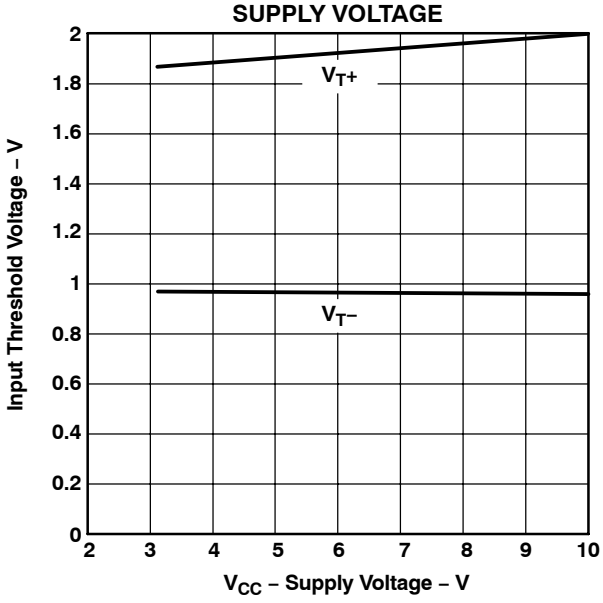
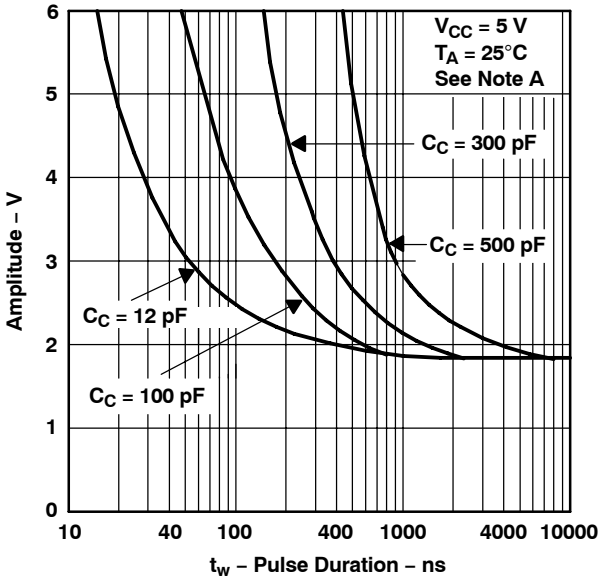


Figure 12.

NOISE REJECTION



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, will not cause a change in the output level.

Figure 13.

MAXIMUM SUPPLY VOLTAGE vs FREE-AIR TEMPERATURE

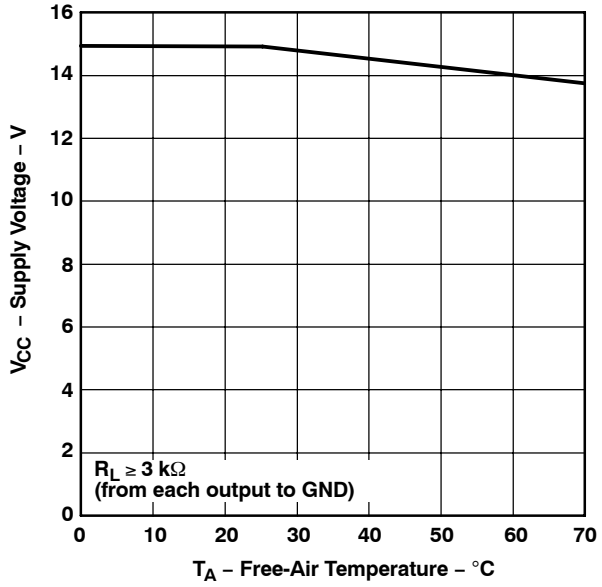


Figure 14.

APPLICATION INFORMATION

Diodes placed in series with the V_{DD} and V_{SS} leads protect the SN75185 in the fault condition. In the fault condition, the device outputs are shorted to ±15 V, and the power supplies are at low and provide low-impedance paths to ground (see Figure 15).

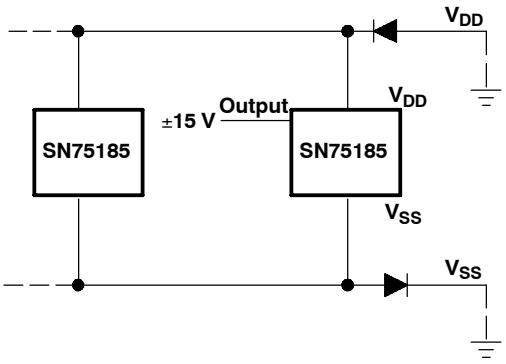
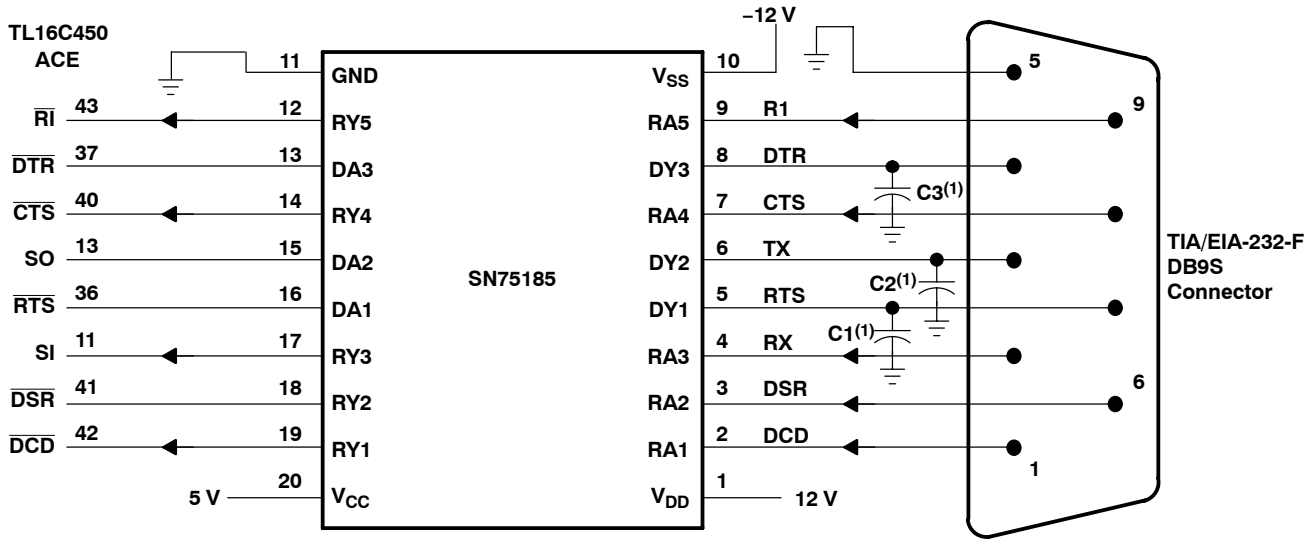


Figure 15. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F



(1) See Figure 10 to select the correct values for the loading capacitors (C1, C2, and C3), which are required to meet the RS-232 maximum slew-rate requirement of 30 V/μs. The value of the loading capacitors required depends on the line length and desired slew rate, but typically is 330 pF.

Figure 16. Typical Connection

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75185DB	Obsolete	Production	SSOP (DB) | 20	-	-	Call TI	Call TI	0 to 70	A185
SN75185DBR	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A185
SN75185DBR.A	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A185
SN75185DW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	0 to 70	SN75185
SN75185DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75185
SN75185DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75185
SN75185N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75185N
SN75185N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75185N
SN75185PWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A185
SN75185PWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A185

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

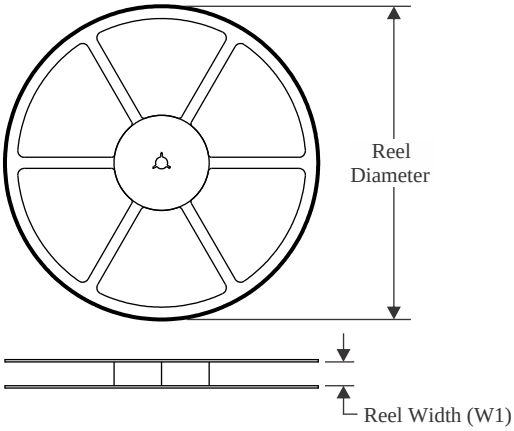
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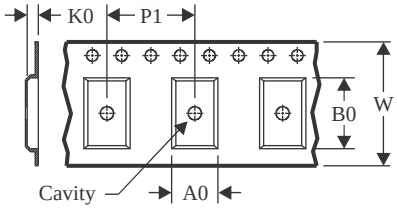
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

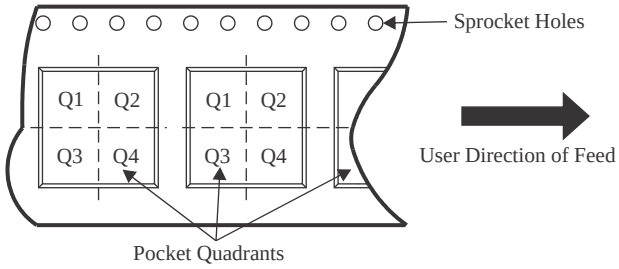


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

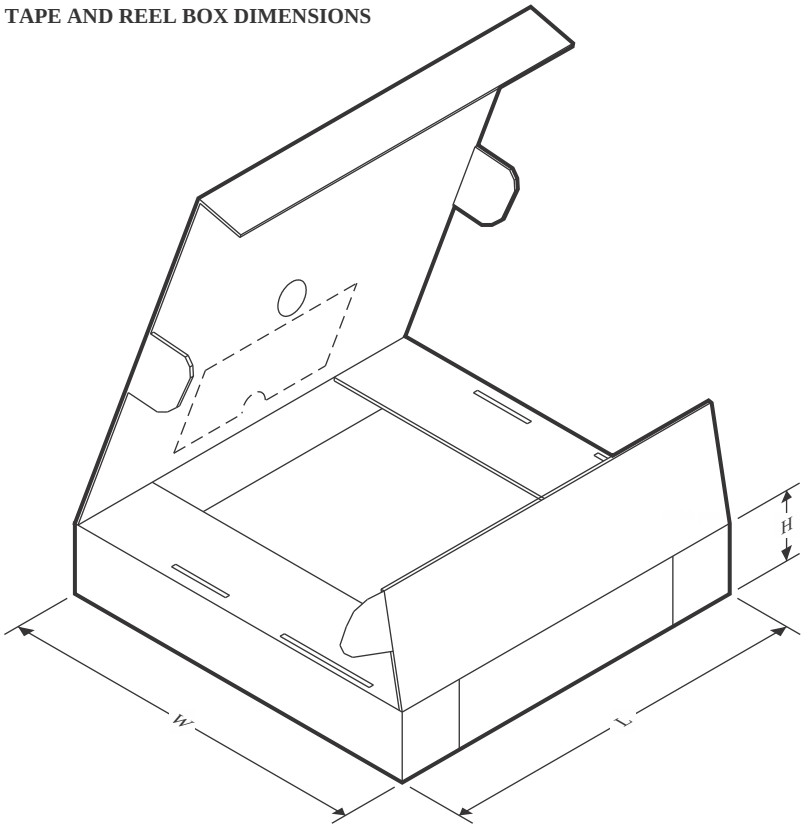
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75185DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN75185DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75185PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

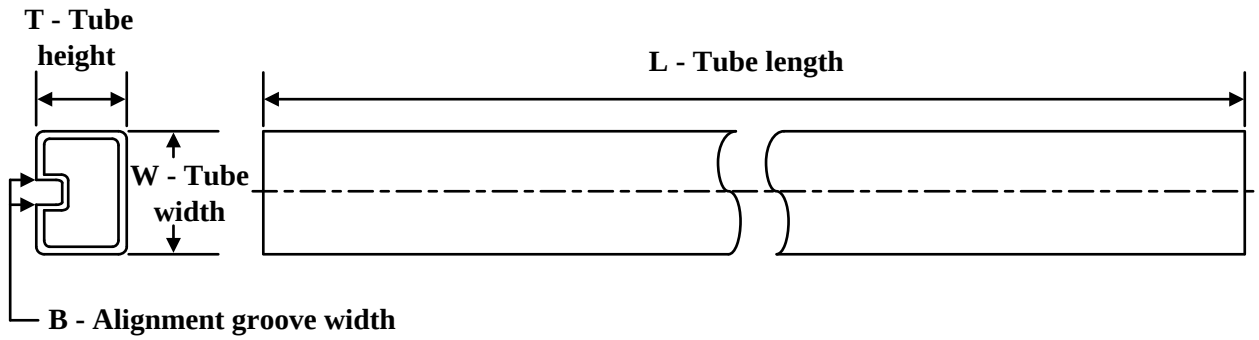
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75185DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN75185DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN75185PWR	TSSOP	PW	20	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

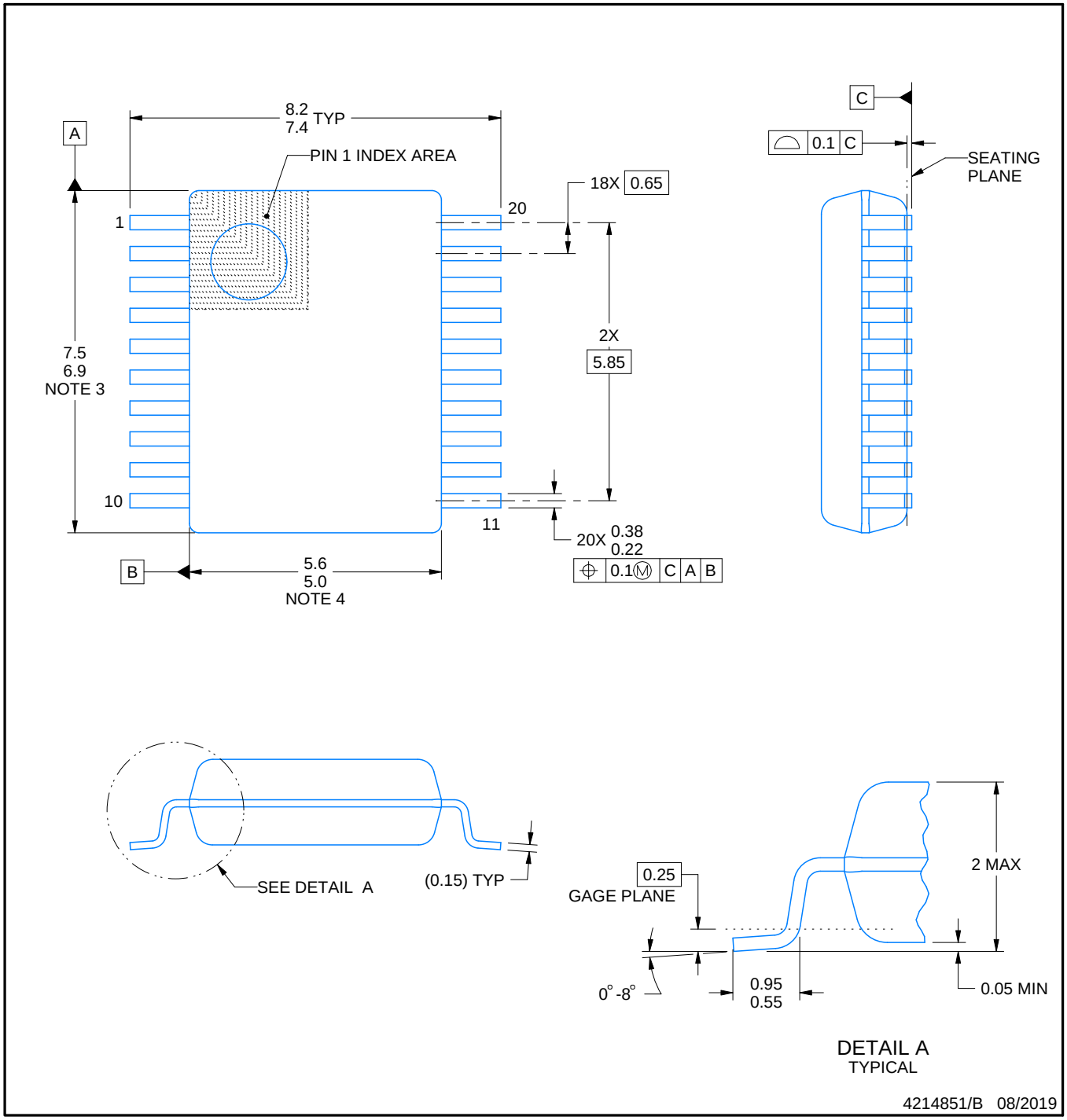
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75185N	N	PDIP	20	20	506	13.97	11230	4.32
SN75185N.A	N	PDIP	20	20	506	13.97	11230	4.32

PACKAGE OUTLINE

DB0020A

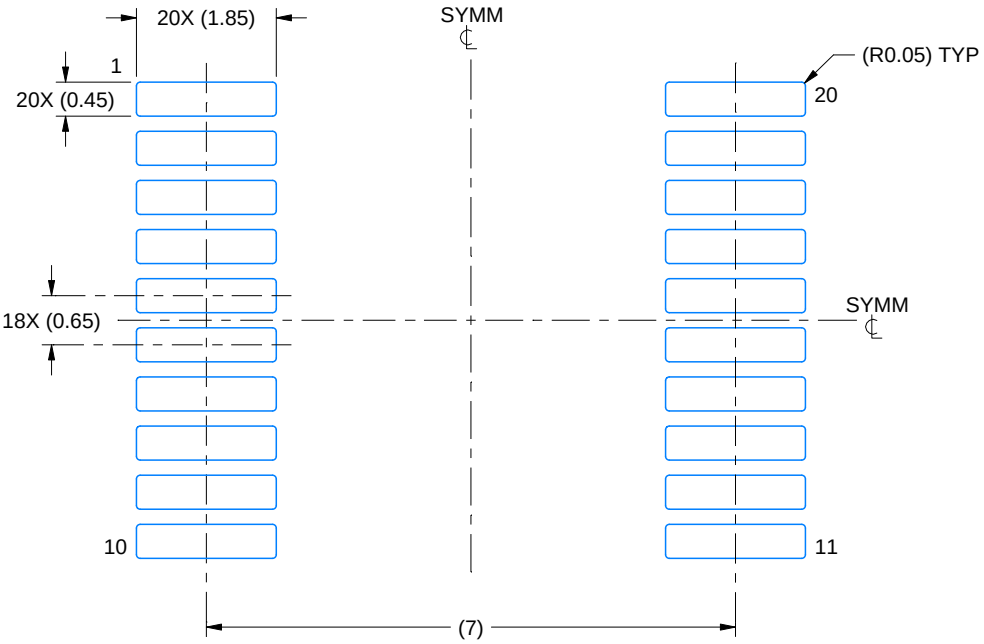
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

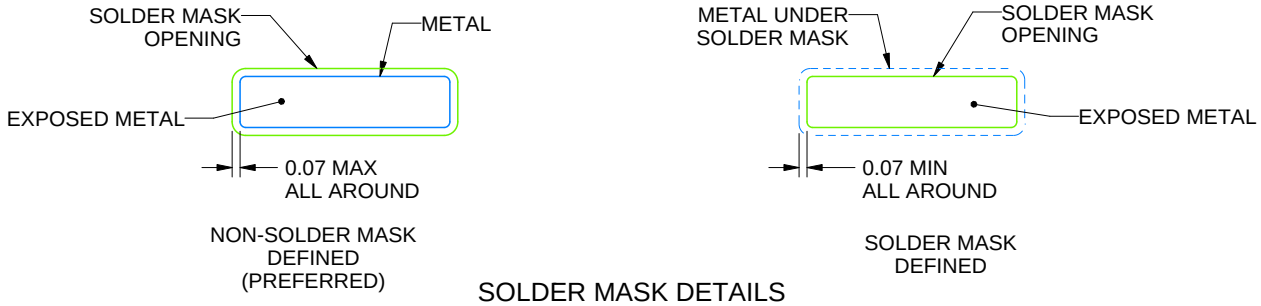


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

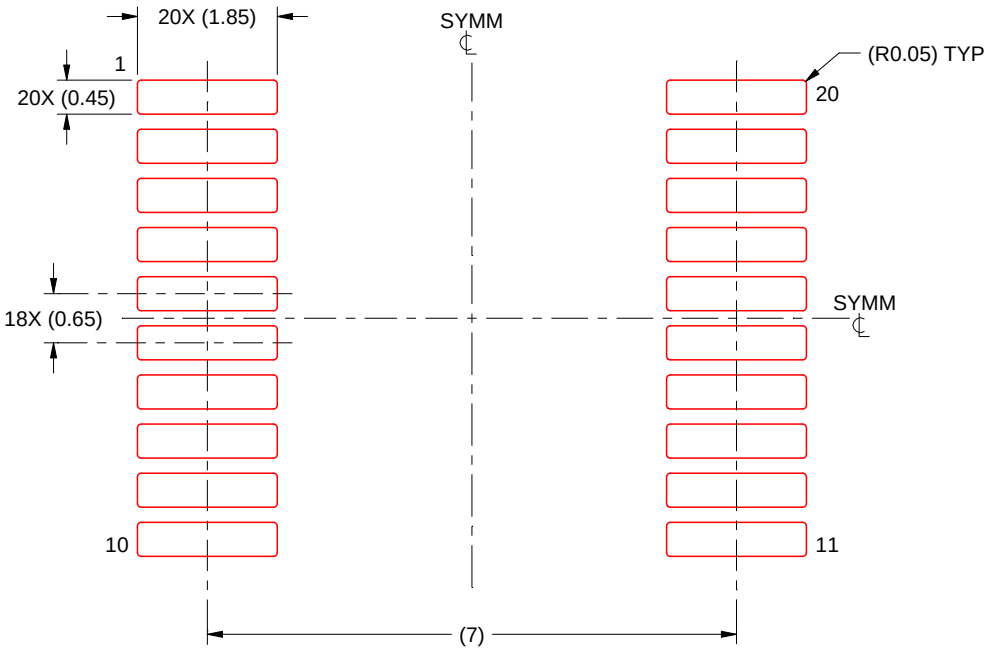
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

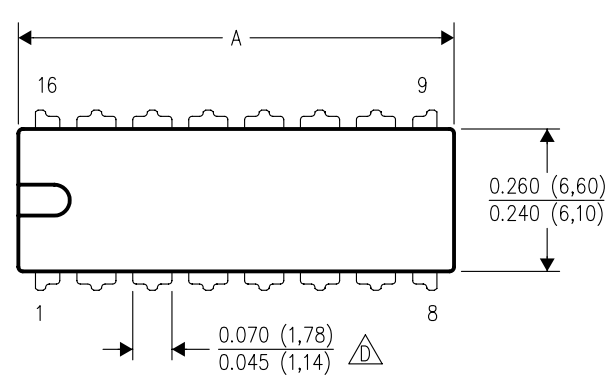
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

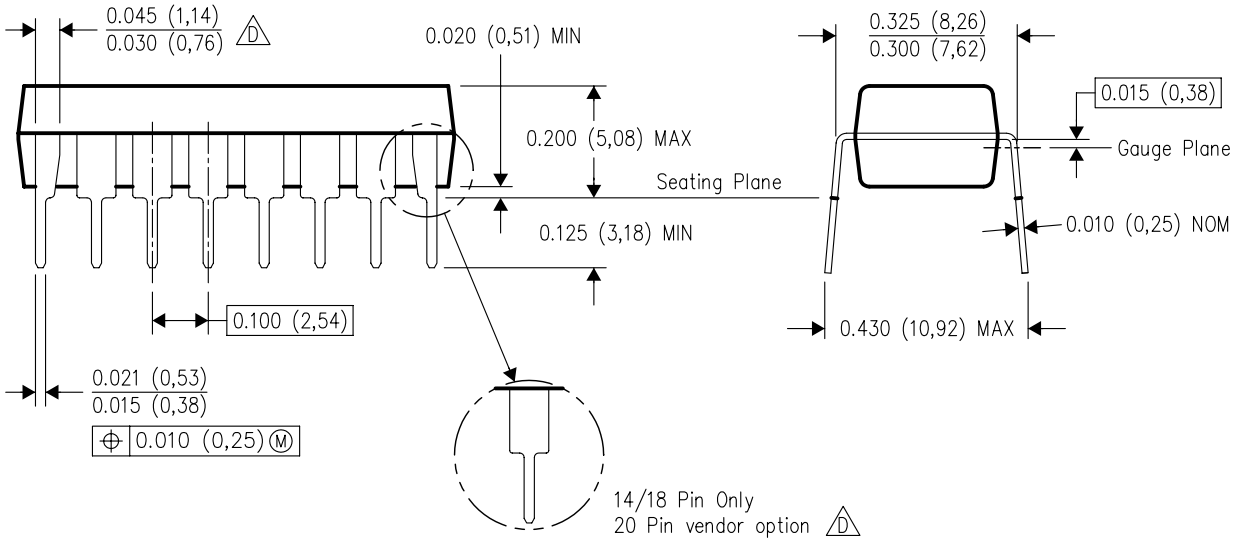
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

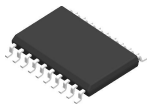


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

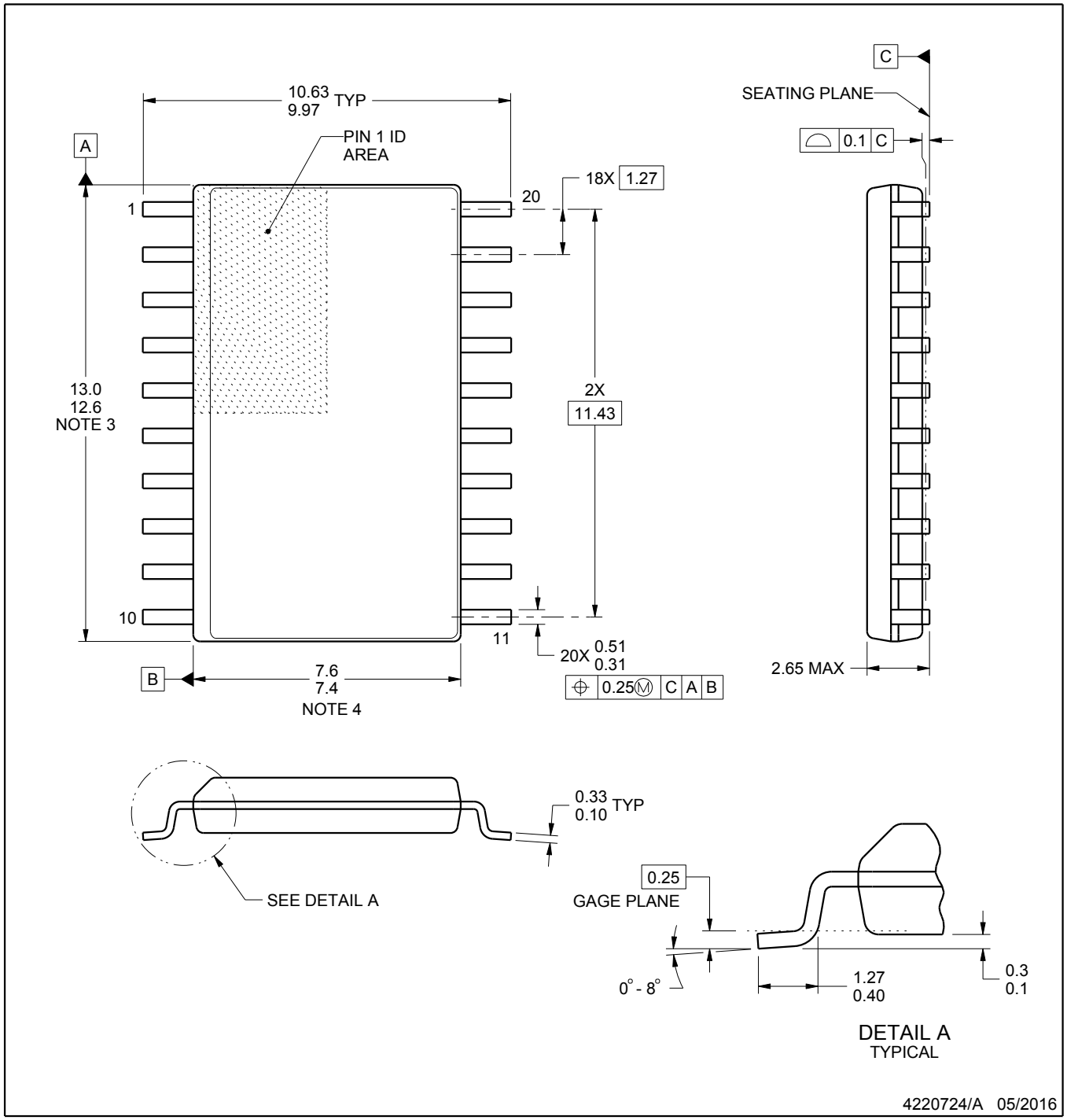


PACKAGE OUTLINE

DW0020A

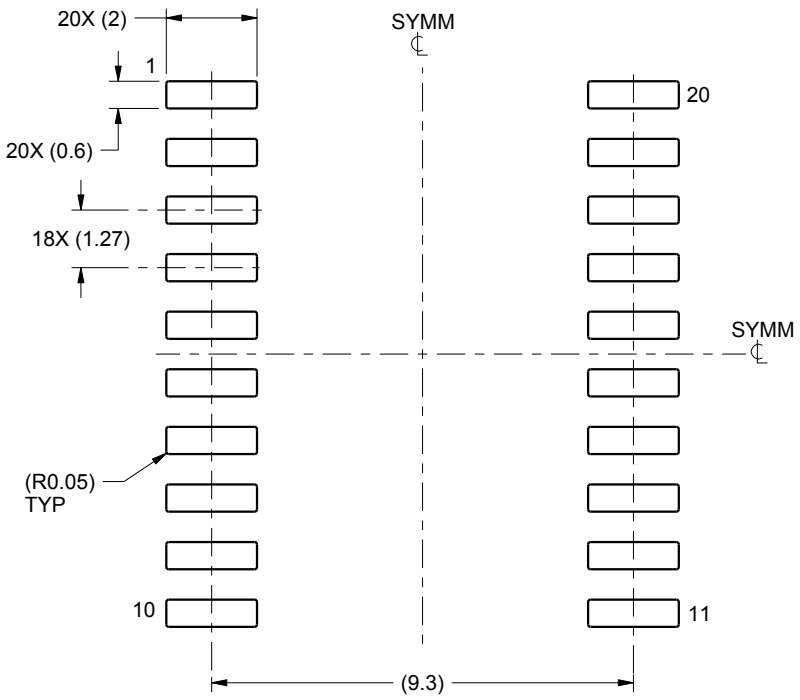
SOIC - 2.65 mm max height

SOIC

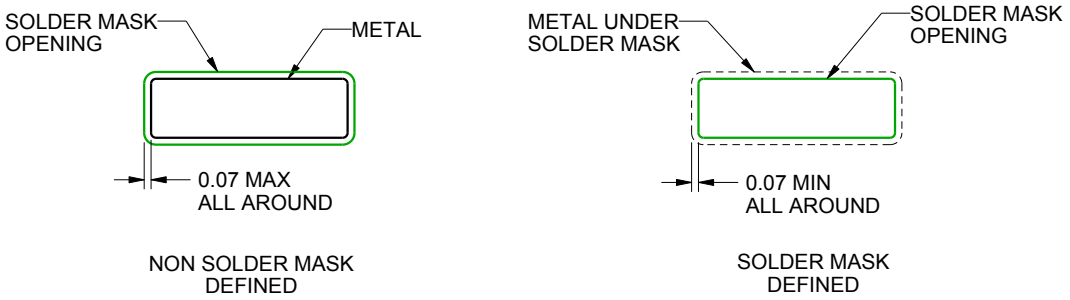


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

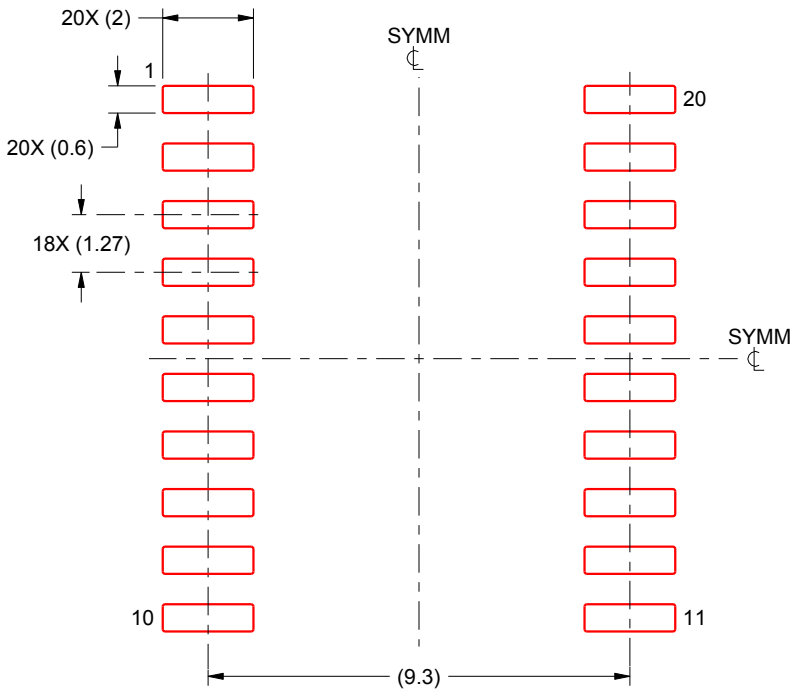


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

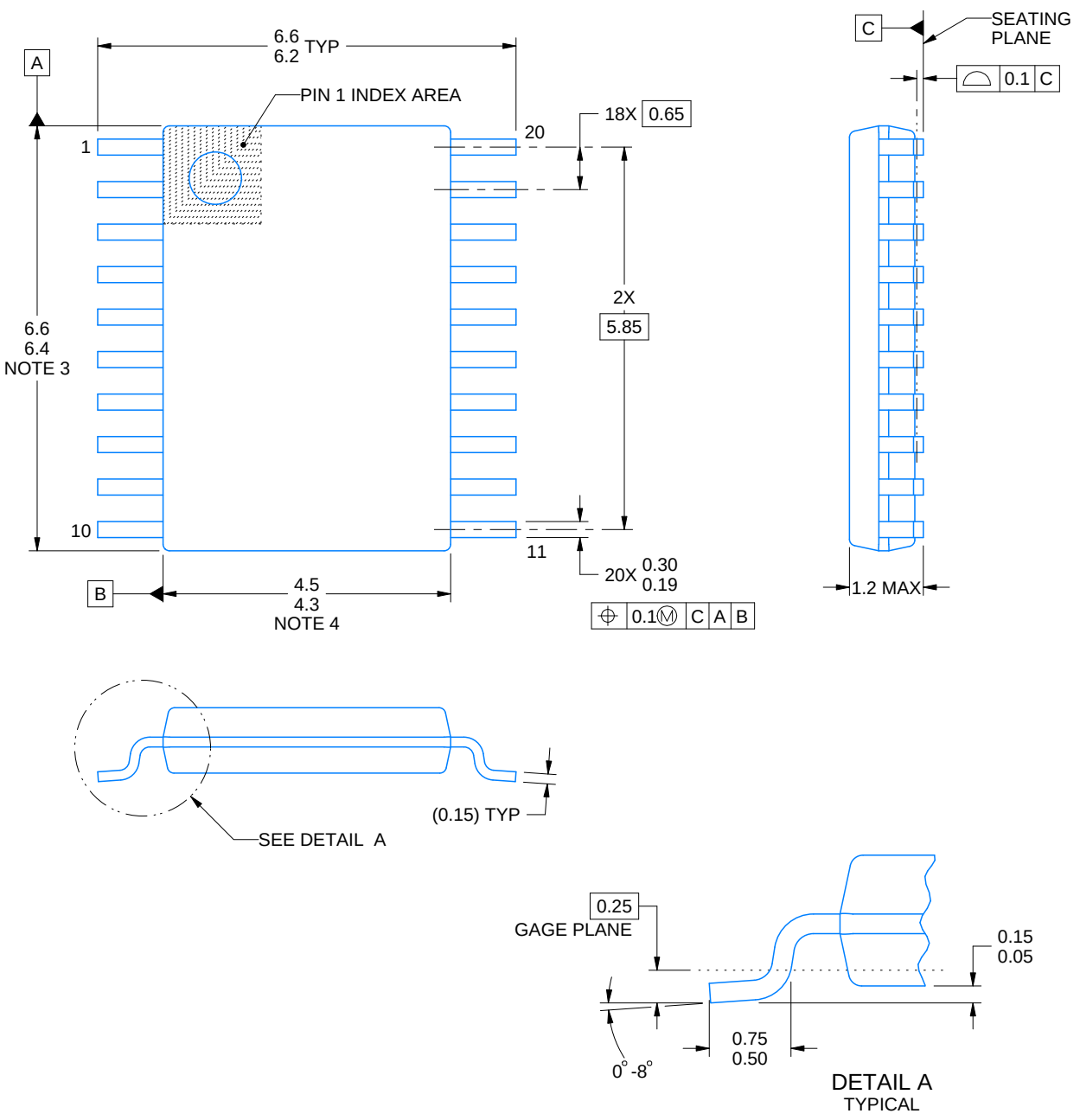
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0020A

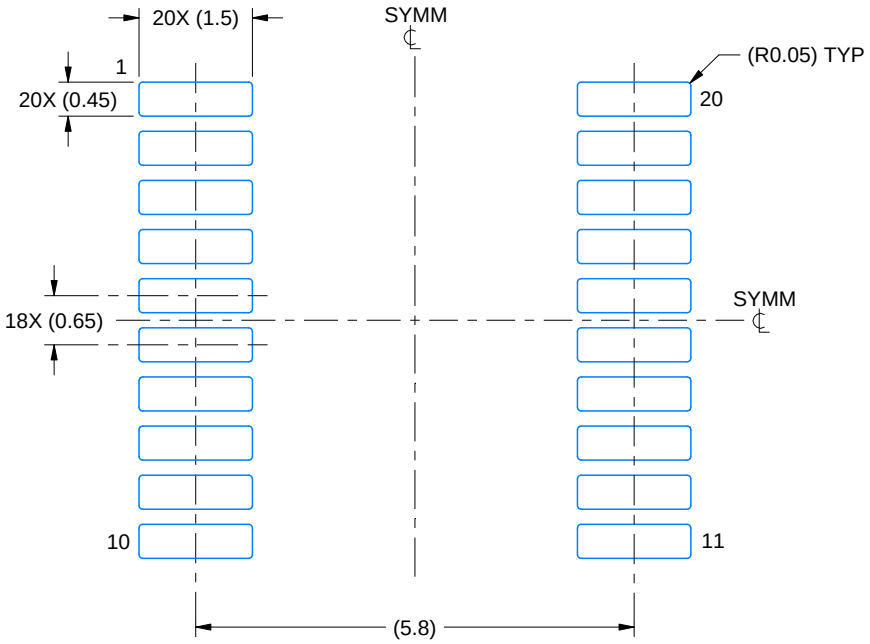
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

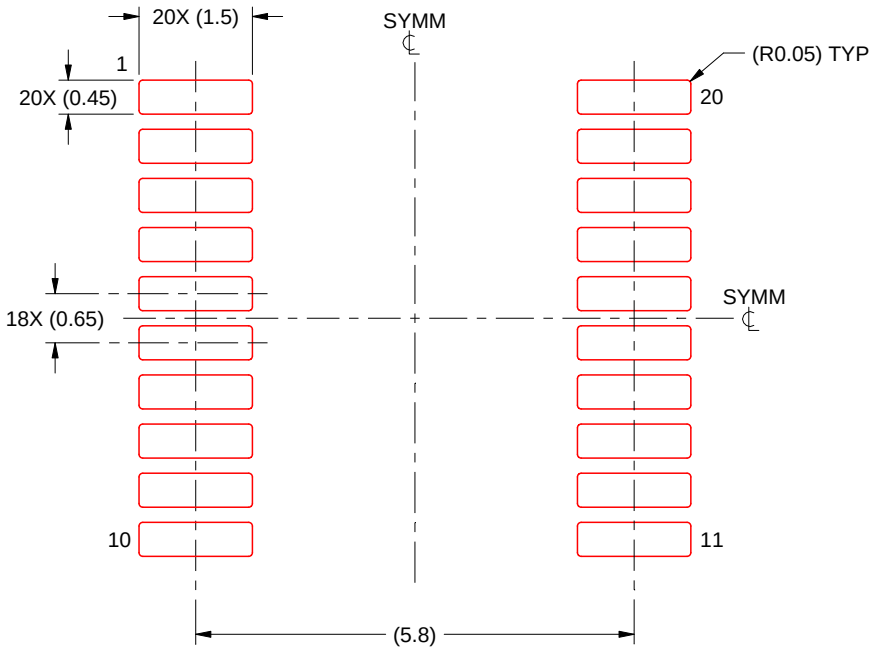


SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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