

# SN65LBC172, SN75LBC172 Quadruple Low-Power Differential Line Driver

## 1 Features

- Exceeds or meets EIA standard RS-485
- Designed for high-speed multipoint transmission on long bus lines in noisy environments
- Supports data rates up to and exceeding ten million transfers per second
- Provides a common-mode output voltage range of -7V to 12V
- Offers positive-and negative-current limiting
- Consumes low power to 1.5mA max (output disabled)
- Functions interchangeably with the SN75172

## 2 Applications

- Motor drives
- Factory automation and control

## 3 Description

The SN65LBC172 and SN75LBC172 are monolithic quadruple differential line drivers with three-state outputs. Both devices are designed to meet the requirements of EIA Standard RS-485. These devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. Each driver features wide positive and negative common- mode output voltage

ranges, current limiting, and thermal-shutdown circuitry which provides a party-line application in noisy environments. Both devices are designed using LinBiCMOS™, facilitating ultra-low power consumption and inherent robustness.

Both the SN65LBC172 and SN75LBC172 provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. These devices offer optimum performance when used with the SN75LBC173 or SN75LBC175 quadruple line receivers. The SN65LBC172 and SN75LBC172 are available in the 16-pin DIP package (N) and the 20-pin wide-body small-outline inline-circuit (SOIC) package (DW).

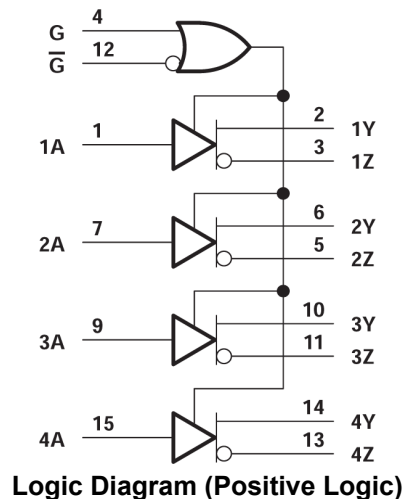
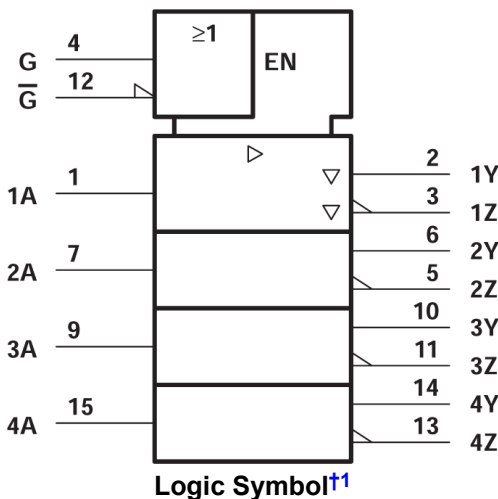
The SN75LBC172 is characterized for operation over the commercial temperature range of 0°C to 70°C. The SN65LBC172 is characterized over the industrial temperature range of -40°C to 85°C.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
SN65LBC172	DW (SOIC, 20)	10.3mm × 10.3mm
SN75LBC172	N (PDIP 16)	19.3mm × 9.4mm

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

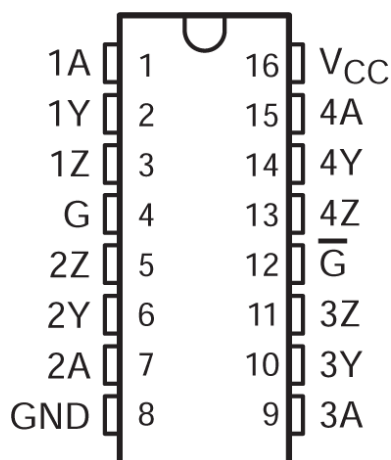
1 Pin numbers shown are for the N package.



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## 4 Pin Configuration and Functions

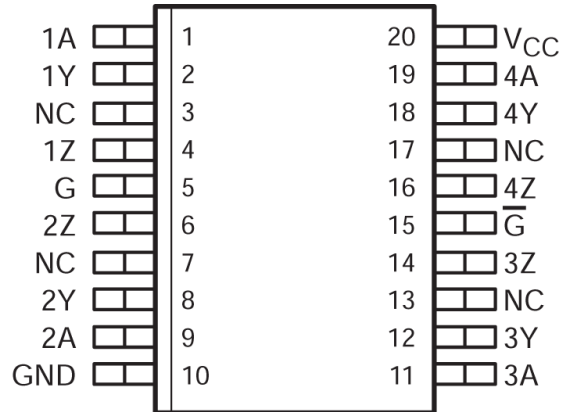


**Figure 4-1. N Package (Top View)**

**Table 4-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1A	1	I	Driver 1 input
1Y	2	O	Driver 1 output
1Z	3	O	Driver 1 inverted output
G	4	I	Active high enable all drivers
2Z	5	O	Driver 2 inverted output
2Y	6	O	Driver 2 output
2A	7	I	Driver 2 input
GND	8	G	Ground pin
3A	9	I	Driver 3 input
3Y	10	O	Driver 3 output
3Z	11	O	Driver 3 inverted output
$\bar{G}$	12	I	Active low enable all drivers
4Z	13	O	Driver 4 inverted output
4Y	14	O	Driver 4 output
4A	15	O	Driver 4 input
V <sub>CC</sub>	16	P	Power pin

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.



NC – No internal connection

**Figure 4-2. DW Package (Top View)****Table 4-2. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1A	1	I	Driver 1 input
1Y	2	O	Driver 1 output
NC	3	-	No Internal Connection
1Z	4	O	Driver 1 inverted output
G	5	I	Active high enable all drivers
2Z	6	O	Driver 2 inverted output
NC	7	-	No Internal Connection
2Y	8	O	Driver 2 output
2A	9	I	Driver 2 input
GND	10	G	Ground pin
3A	11	I	Driver 3 input
3Y	12	O	Driver 3 output
NC	13	-	No Internal Connection
3Z	14	O	Driver 3 inverted output
$\bar{G}$	15	I	Active low enable all drivers
4Z	16	O	Driver 4 inverted output
NC	17	-	No Internal Connection
4Y	18	O	Driver 4 output
4A	19	I	Driver 4 input
V <sub>CC</sub>	20	P	Power pin

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range, (see <sup>(3)</sup> )	-0.3	7	V
V <sub>O</sub>	Output voltage range	-10	15	V
V <sub>I</sub>	Voltage range at A, $\bar{G}$ , G	-0.3	V <sub>CC</sub> + 0.5	V
P <sub>D</sub>	Continuous power dissipation	Internally limited <sup>(2)</sup>		
T <sub>stg</sub>	Storage temperature range	-65	150	°C
T <sub>LEAD</sub>	Lead temperature 1,6mm (1/16 inch) from case for 10 seconds		260	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.
- (3) All voltage values are with respect to GND.

### 5.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC</sub>		4.75	5	5.25	V
High-level input voltage, V <sub>IH</sub>		2			V
Low-level input voltage, V <sub>IL</sub>				0.8	V
Voltage at any bus terminal (separately or common mode), V <sub>O</sub>	Y or Z	-7		12	V
High-level output current, I <sub>OH</sub>	Y or Z			-60	mA
Low-level output current, I <sub>OL</sub>	Y or Z			60	mA
Continuous total power dissipation		See Dissipation Rating Table			
Junction temperature, T <sub>J</sub>				140	°C
Operating free-air temperature, T <sub>A</sub>	SN65LBC172	-40		85	°C
	SN75LBC172	0		70	

### 5.3 Dissipation Rating Table

PACKAGE	THERMAL MODEL	T <sub>A</sub> < 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING
DW	Low K <sup>(1)</sup>	1094mW	10.4mW/°C	625mW	469mW
	High K <sup>(2)</sup>	1669mW	15.9mW/°C	954mW	715mW
N		1150mW	9.2mW/°C	736mW	598mW

- (1) In accordance with the low effective thermal conductivity metric definitions of EIA/JESD 51-3.
- (2) In accordance with the high effective thermal conductivity metric definitions of EIA/JESD 51-7.

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		N (PDIP)	DW (SOIC)	UNIT
		16 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.6	66.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.1	34.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	39.7	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	27.5	8.9	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	40.3	39	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{IK}$	Input clamp voltage	$I_I = -18\text{mA}$				-1.5	V
$ V_{OD} $	Differential output voltage <sup>(2)</sup>	$R_L = 54\Omega$ See <a href="#">Figure 6-1</a>	SN65LBC172	1.1	1.8	5	V
			SN75LBC172	1.5	1.8	5	
		$R_L = 60\Omega$ , See <a href="#">Figure 6-2</a>	SN65LBC172	1.1	1.7	5	
			SN75LBC172	1.5	1.7	5	
$\Delta V_{OD} $	Change in magnitude of common-mode output voltage <sup>(3)</sup>	$R_L = 54\Omega$ ,	See <a href="#">Figure 6-1</a>			$\pm 0.2$	V
$V_{OC}$	Common-mode output voltage			-1		3	V
$\Delta V_{OC} $	Change in magnitude of common-mode output voltage <sup>(3)</sup>					$\pm 0.2$	V
$I_O$	Output current with power off	$V_{CC} = 0$ ,	$V_O = -7\text{V to }12\text{V}$			$\pm 100$	$\mu\text{A}$
$I_{OZ}$	High-impedance-state output current	$V_O = -7\text{V to }12\text{V}$				$\pm 100$	$\mu\text{A}$
$I_{IH}$	High-level input current	$V_I = 2.4\text{V}$				-100	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_I = 0.4\text{V}$				-100	$\mu\text{A}$
$I_{OS}$	Short-circuit output current	$V_O = -7\text{V to }12\text{V}$				$\pm 250$	mA
$I_{CC}$	Supply current (all drivers)	No load	Outputs enabled			7	mA
			Outputs disabled			1.5	

- (1) All typical values are at  $V_{CC} = 5\text{V}$  and  $T_A = 25^\circ\text{C}$ .  
 (2) The minimum  $V_{OD}$  specification does not fully comply with EIA-485 at operating temperatures below  $0^\circ\text{C}$ . The lower output signal should be used to determine the maximum signal-transmission distance.  
 (3)  $\Delta|V_{OD}|$  and  $\Delta|V_{OC}|$  are the changes in magnitude of  $V_{OD}$  and  $V_{OC}$ , respectively, that occur when the input changes from a high level to a low level.

## 5.6 Switching Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	$R_L = 54\Omega$ ,	See <a href="#">Figure 6-3</a>	2	11	20	ns
$t_{t(OD)}$	Differential output transition time			9	15	25	
$t_{PZH}$	Output enable time to high level	$R_L = 110\Omega$ ,	See <a href="#">Figure 6-4</a>		20	30	ns
$t_{PZL}$	Output enable time to low level	$R_L = 110\Omega$ ,	See <a href="#">Figure 6-5</a>		21	30	ns
$t_{PHZ}$	Output disable time from high level	$R_L = 110\Omega$ ,	See <a href="#">Figure 6-4</a>		48	70	ns
$t_{PLZ}$	Output disable time from low level	$R_L = 110\Omega$ ,	See <a href="#">Figure 6-5</a>		21	30	ns

## 5.7 Typical Characteristics

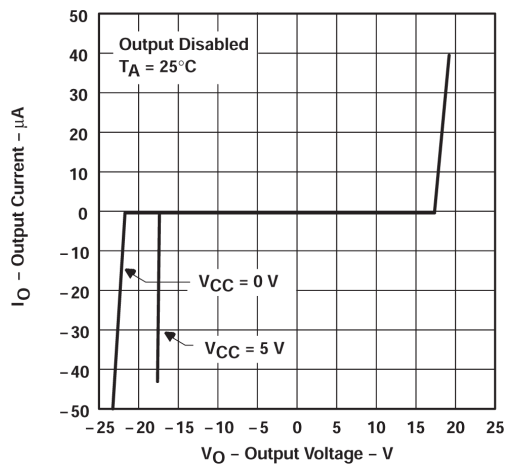


Figure 5-1. Output Current vs Output Voltage

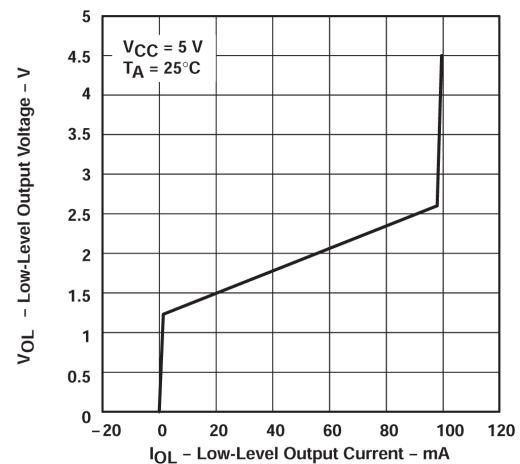


Figure 5-2. Low-level Output Voltage vs Low-level Output Current

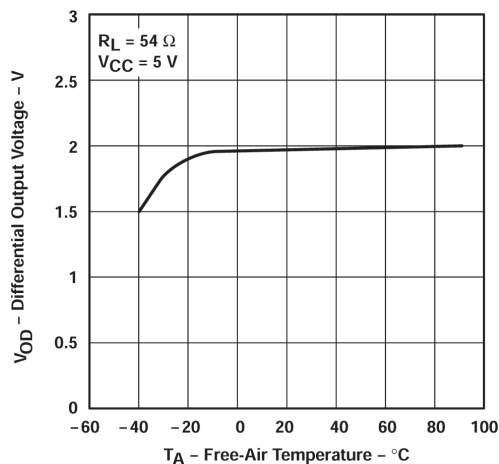


Figure 5-3. Differential Output Voltage vs Free-air Temperature

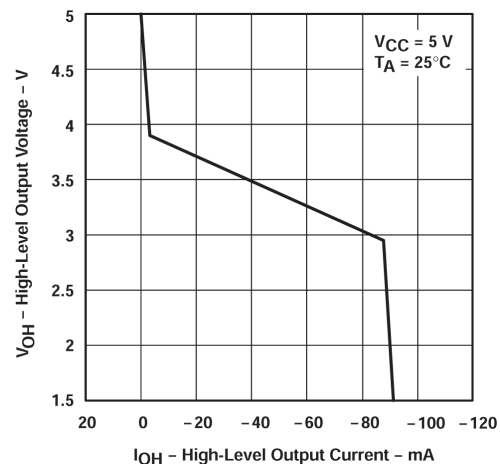


Figure 5-4. High-level Output Voltage vs High-level Output Current

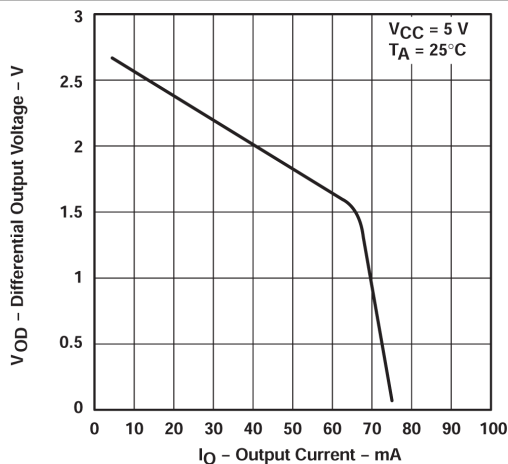


Figure 5-5. Differential Output Voltage vs Output Current

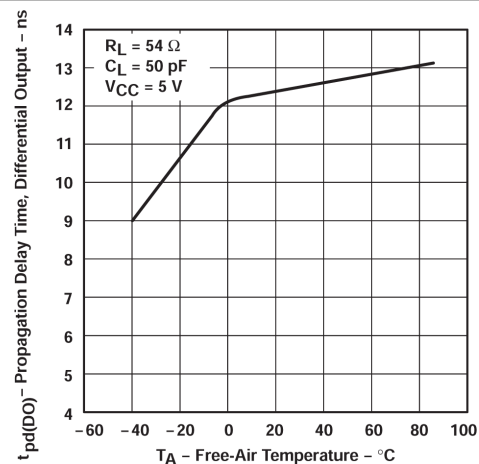
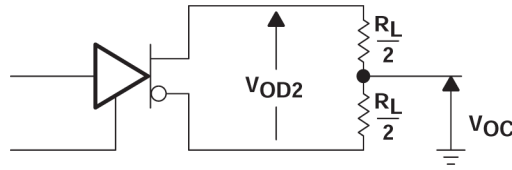


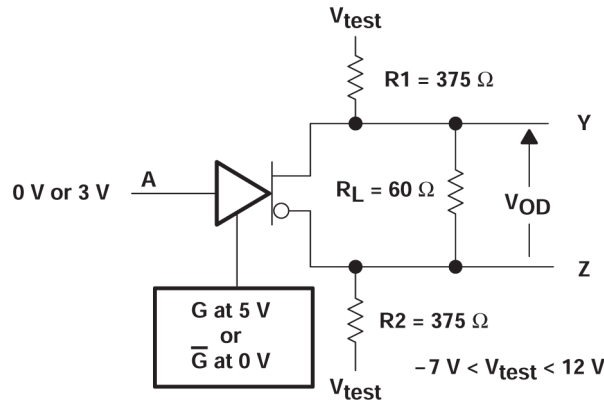
Figure 5-6. Propagation Delay Time, Differential Output vs Free-air Temperature



## 6 Parameter Measurement Information

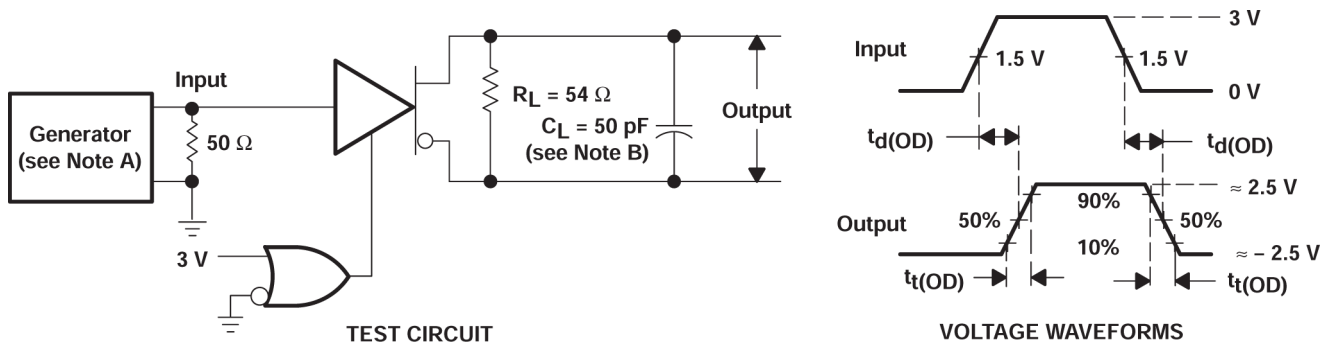


**Figure 6-1. Differential and Common-Mode Output Voltages**



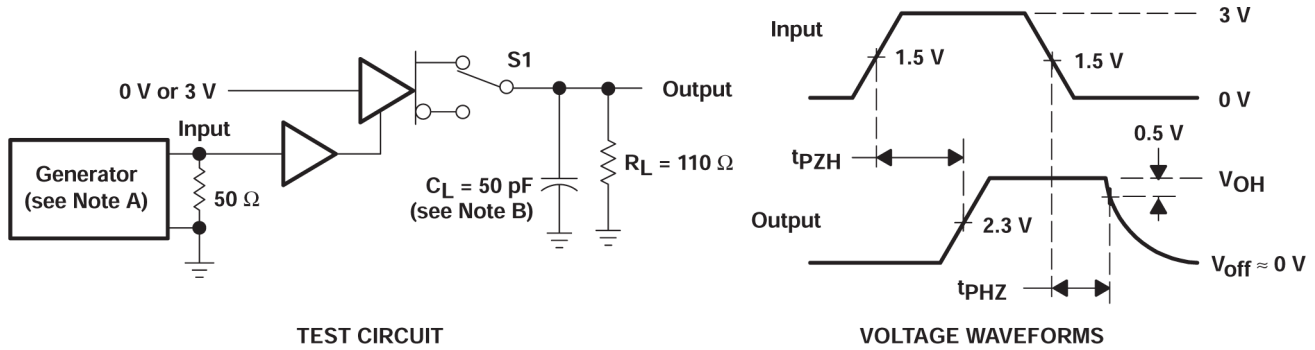
- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, duty cycle = 50%,  $t_r \leq$  5 ns,  $t_f \leq$  5 ns,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes probe and stray capacitance.

**Figure 6-2. Driver  $V_{OD}$  Test Circuit**



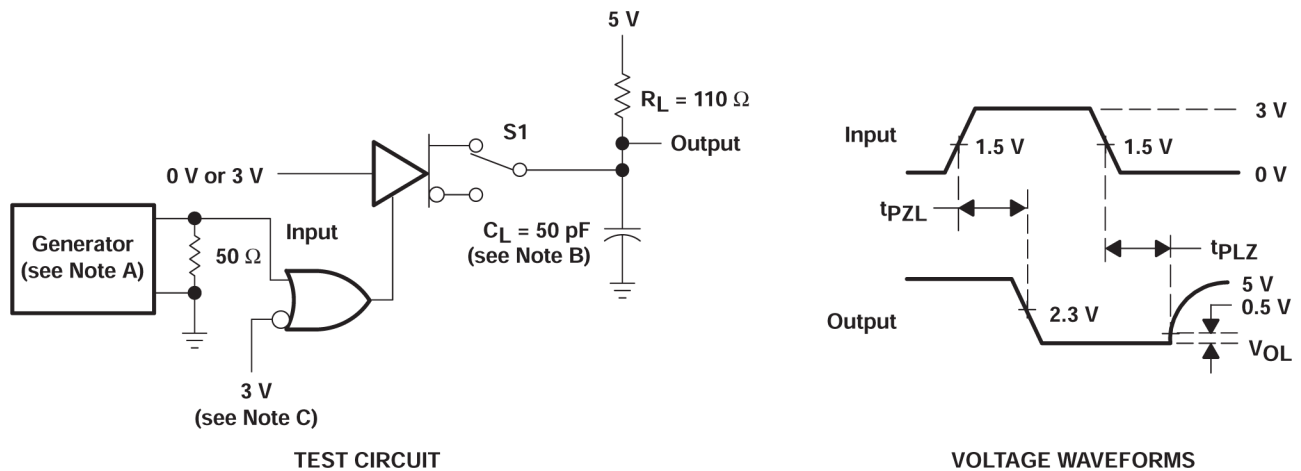
- A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, duty cycle = 50%,  $t_r \leq$  5 ns,  $t_f \leq$  5 ns,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes probe and stray capacitance.

**Figure 6-3. Driver Differential-Output Test Circuit and Delay and Transition-Time Waveforms**



- A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1 \text{ MHz}$ , duty cycle = 50%,  $t_r \leq 5 \text{ ns}$ ,  $t_f \leq 5 \text{ ns}$ ,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes probe and stray capacitance.

**Figure 6-4.  $t_{pZH}$  and  $t_{pHZ}$  Test Circuit and Voltage Waveforms**



- A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1 \text{ MHz}$ , duty cycle = 50%,  $t_r \leq 5 \text{ ns}$ ,  $t_f \leq 5 \text{ ns}$ ,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes probe and stray capacitance
- C. To test the active-low enable  $\overline{G}$ , ground G and apply an inverted waveform to  $\overline{G}$ .

**Figure 6-5.  $t_{pZL}$  and  $t_{pLZ}$  Test Circuit and Waveforms**

## 7 Detailed Description

### 7.1 Thermal Characteristics of Ic Packages

$\Theta_{JA}$  (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power

$\Theta_{JA}$  is NOT a constant and is a strong function of

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

$\Theta_{JA}$  can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures.  $\Theta_{JA}$  is often misused when it is used to calculate junction temperatures for other installations.

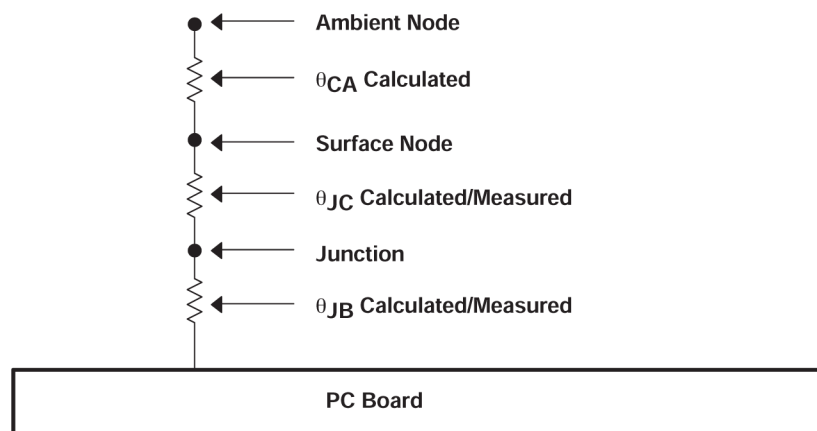
TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance and consists of a single trace layer 25mm long and 2 oz thick copper. The high-k board gives *best case* in-use condition and consists of two 1-oz buried power planes with a single trace layer 25mm long with 2-oz thick copper. A 4% to 50% difference in  $\Theta_{JA}$  can be measured between these two test cards

$\Theta_{JC}$  (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

$\Theta_{JC}$  is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with  $\Theta_{JB}$  in 1-dimensional thermal simulation of a package system.

$\Theta_{JB}$  (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure.  $\Theta_{JB}$  is only defined for the high-k test card.

$\Theta_{JB}$  provides an overall thermal resistance between the die and the PCB. Including a bit for the PCB thermal resistance (especially for BGAs with thermal balls), and can be used for simple 1-dimensional network analysis of package system (see [Figure 7-1](#)).



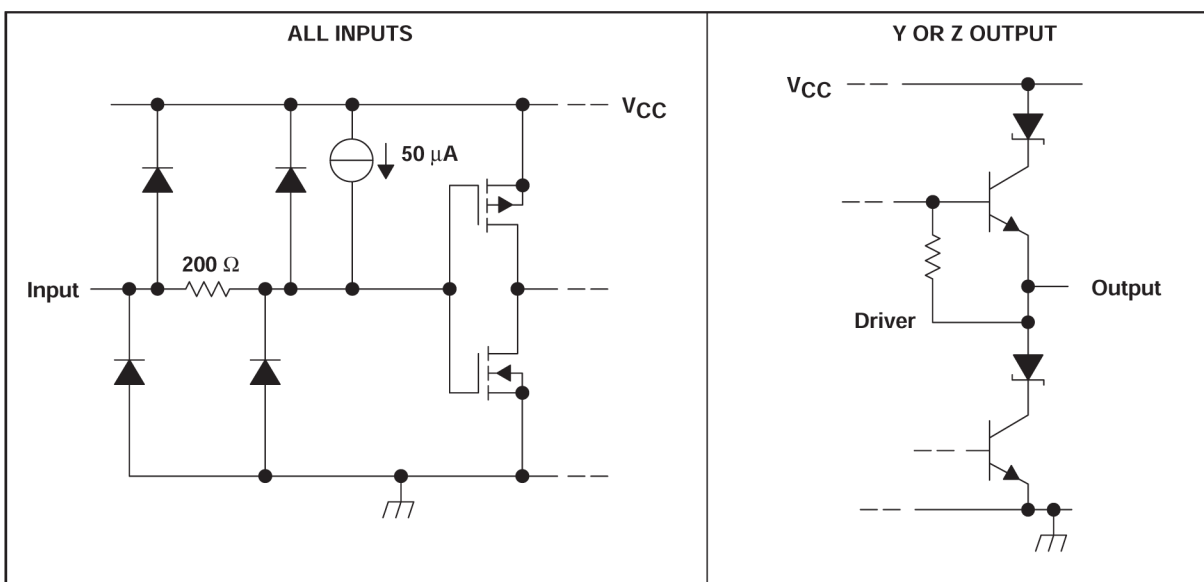
**Figure 7-1. Thermal Resistance**

## 7.2 Device Functional Modes

**Table 7-1. Function Table (Each Driver)**

INPUT A	ENABLES <sup>(1)</sup>		OUTPUTS	
	G	$\bar{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)



**Figure 7-2. Schematic Diagrams of Inputs and Outputs**

## 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 8.3 Trademarks

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### 8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (April 2006) to Revision F (April 2024)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document.....	<a href="#">1</a>
• Added the <i>Thermal Information</i> table.....	<a href="#">6</a>

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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