SN75LVDS82 FlatLink™ Receiver

1 Features

- 4:28 Data Channel Expansion at up to 1904 Mbps Throughput
- Suited for SVGA, XGA, or SXGA Display Data Transmission From Controller to Display With Very Low EMI
- Four Data Channels and Clock Low-Voltage Differential Channels In and 28 Data and Clock Low-Voltage TTL Channels Out
- Operates From a Single 3.3-V Supply With 250 mW (Typical)
- 5-V Tolerant $\overline{\text{SHTDN}}$ Input
- Falling Clock-Edge-Triggered Outputs
- Packaged in Thin Shrink Small-Outline Package (TSSOP) With 20-Mil Terminal Pitch
- Consumes Less Than 1 mW When Disabled
- Pixel Clock Frequency Range of 31 MHz to 68 MHz
- No External Components Required for PLL
- Inputs Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard

2 Applications

- Printers
- Appliances With an LCD
- Digital Cameras
- Laptop and PC Displays Industrial PC, Laptop, and other Factory Automation Displays Patient Monitor and Medical Equipment Displays Projectors Weight Scales

3 Description

The SN75LVDS82 FlatLink™ receiver contains four serial-in, 7-bit parallel-out shift registers, a 7× clock synthesizer, and five low-voltage differential signaling (LVDS) line receivers in a single integrated circuit.

These functions allow receipt of synchronous data from a compatible transmitter, such as the SN75LVDS83B, over five balanced-pair conductors, and expansion to 28 bits of single-ended low-voltage TTL (LVTTL) synchronous data at a lower transfer rate. The SN75LVDS82 can also be used with the SN75LVDS84 for 21-bit transfers.

When receiving, the high-speed LVDS data is received and loaded into registers at the rate of seven times (7×) the LVDS input clock (CLKIN). The data is then unloaded to a 28-bit-wide LVTTL parallel bus at the CLKIN rate. A phase-locked loop (PLL) clock synthesizer circuit generates a 7× clock for internal clocking and an output clock for the expanded data. The SN75LVDS82 presents valid data on the falling edge of the output clock (CLKOUT).

The SN75LVDS82 requires only five line-termination resistors for the differential inputs and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN75LVDS82	TSSOP (56)	14.00 mm × 6.10 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

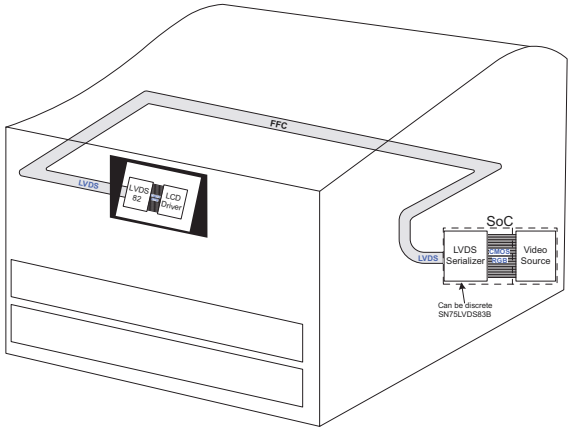


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (April 2011) to Revision J	Page

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Changed *Feature* From: "238 Mbytes/s Throughput" To: "1904 Mbps Throughput" ... 1
- Deleted *Feature*: "Improved Replacement for the National™ DS90C582 " ... 1
- Added item to the *Applications* list: "Laptop and PC Display..." ... 1
- Changed text in the *Description* From: "such as the SN75LVDS81: To: "such as the SN75LVDS83B" ... 1
- Changed text in the *Description* From: "SN75LVDS84 or SN75LVDS85 for 21-bit transfers." To: "SN75LVDS84 for 21-bit transfers" ... 1
- Changed device number SN75LVDS81 To: SN75LVDS83B in Figure 16 ... 16
- Deleted image *18-Bit Color Host to 24-Bit Color LCD Panel Display Application* from the *Application Information* section ... 18

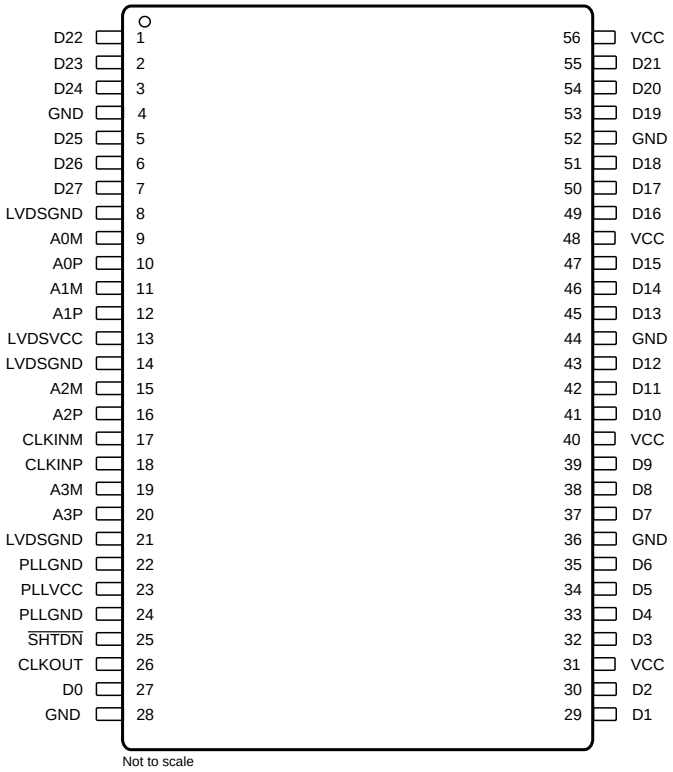
5 Description (continued)

The only possible user intervention is the use of the shutdown/clear ($\overline{\text{SHTDN}}$) active-low input to inhibit the clock and shut off the LVDS receivers for lower power consumption. A low-level on $\overline{\text{SHTDN}}$ clears all internal registers to a low level and places the TTL outputs in a high-impedance state.

The SN75LVDS82 is characterized for operation over ambient air temperatures of 0°C to 70°C.

6 Pin Configuration and Functions

DGG Package
56-Pin TSSOP
Top View



Not to scale

Pin Functions

Pin		I/O	Description
Name	No.		
A0M, A0P	9, 10	LVDS Input	LVDS Data Lane 0
A1M, A1P	11, 12		LVDS Data Lane 1
A2M, A2P	15, 16		LVDS Data Lane 2
A3M, A3P	19, 20		LVDS Data Lane 3
CLKINM, CLKINP			LVDS Clock

Pin Functions (continued)

Pin		I/O	Description
Name	No.		
D0	27	LVTTL Output	Data Bus Output
D1	29		
D2	30		
D3	32		
D4	33		
D5	34		
D6	35		
D7	37		
D8	38		
D9	39		
D10	41		
D11	42		
D12	43		
D13	45		
D14	46		
D15	47		
D16	49		
D17	50		
D18	51		
D19	53		
D20	54		
D21	55		
D22	1		
D23	2		
D24	3		
D25	5		
D26	6		
D27	7		
CLKOUT	26		Clock output for the data bus
$\overline{\text{SHTDN}}$	25	Input	Shutdown Mode; Active-Low
LVDSGND	8, 14, 21	Power	LVDS Ground
$LVDSV_{CC}$	13		LVDS Power supply 3.3 V
PLLGND	22		PLL Ground
$PLLV_{CC}$	23		PLL Power supply 3.3 V
V_{CC}	31,40, 48, 56		Digital Power supply 3.3 V
GND	4, 28, 36, 52		Digital Ground

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.5	4	V
V_O	Output voltage (Dxx terminals)		–0.5	V_{CC} + 0.5	V
V_I	Input voltage	Any terminal except $\overline{SHTDN}$	–0.5	V_{CC} + 0.5	V
		$\overline{SHTDN}$	–0.5	5.5	V
	Continuous total power dissipation		See *Thermal Information*		
T_A	Operating temperature		0	70	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND, unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage ($\overline{SHTDN}$)	2			V
V_{IL}	Low-level input voltage ($\overline{SHTDN}$)			0.8	V
$\lvert V_{ID}\rvert$	Differential input voltage	0.1		0.6	V
V_{IC}	Common-mode input voltage (see Figure 11 and Figure 7)	$\frac{\lvert V_{ID}\rvert}{2}$		$2.4 - \frac{\lvert V_{ID}\rvert}{2}$	V
				$V_{CC} - 0.8$	
T_A	Operating free-air temperature	0		70	°C

7.4 Thermal Information

THERMAL METRIC(1)		SN75LVDS82 DGG (TSSOP) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	57.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage				100	mV
V_{IT-}	Negative-going differential input threshold voltage(2)		–100			mV
V_{OH}	High-level output voltage	I_{OH} = –4 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.4	V
I_{CC}	Quiescent current (average)	Disabled, All inputs open			280	µA
		Enabled, AnP = 1 V, AnM = 1.4 V, t_c = 15.38 ns		60	74	mA
		Enabled, C_L = 8 pF, Grayscale pattern (see Figure 13), t_c = 15.38 ns		74		
		Enabled, C_L = 8 pF, Worst-case pattern (see Figure 14), t_c = 15.38 ns		107		
I_{IH}	High-level input current ($\overline{SHTDN}$)	$V_{IH} = V_{CC}$			±20	µA
I_{IL}	Low-level input current ($\overline{SHTDN}$)	V_{IL} = 0			±20	µA
I_{IN}	Input current (LVDS input terminals A and CLKIN)	0 ≤ V_I ≤ 2.4 V			±20	µA
I_{OZ}	High-impedance output current	V_O = 0 or V_{CC}			±10	µA

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) The algebraic convention, in which the less-positive (more-negative) limit is designed minimum, is used in this data sheet for the negative-going input voltage threshold only.

7.6 Timing Requirements

		MIN	MAX	UNIT
t_c	Cycle time, input clock(1)	14.7	32.3	ns
t_{su1}	Setup time, input (see Figure 2)	600		ps
t_{h1}	Hold time, input (see Figure 2)	600		ps

(1) Parameter t_c is defined as the mean duration of a minimum of 32000 clock cycles.

7.7 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{su2}	Setup time, D0–D27 valid to CLKOUT↓	C_L = 8 pF, See Figure 1	5			ns
t_{h2}	Hold time, CLKOUT↓ to D0–D27 valid	C_L = 8 pF, See Figure 1	5			ns
t_{RSKM}	Receiver input skew margin(2)(see Figure 2)	t_c = 15.38 ns (± 0.2%), |Input clock jitter| < 50 ps(3)	490			ps
t_d	Delay time, CLKIN↑ to CLKOUT↓ (see Figure 2)	t_c = 15.38 ns (± 0.2%), C_L = 8 pF		3.7		ns
$\Delta t_{c(o)}$	Cycle time, change in output clock period(4)	t_c = 15.38 + 0.75 sin (2π500E3t) ± 0.05 ns, See Figure 15		±80		ps
		t_c = 15.38 + 0.75 sin (2π3E6t) ± 0.05 ns, See Figure 15		±300		
t_{en}	Enable time, $\overline{SHTDN}$↑ to Dn valid	See Figure 3		1		ms
t_{dis}	Disable time, $\overline{SHTDN}$↓ to off state	See Figure 4		400		ns
t_t	Transition time, output (10% to 90% t_r or t_f)	C_L = 8 pF		3		ns
t_w	Pulse duration, output clock			0.43 t_c		ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) The parameter $t_{(RSKM)}$ is the timing margin available to the transmitter and interconnection skews and clock jitter. It is defined by $t_c/14 - t_{su1}/t_{h1}$.
(3) |Input clock jitter| is the magnitude of the change in input clock period.
(4) $\Delta t_{c(o)}$ is the change in the output clock period from one cycle to the next cycle observed over 15000 cycles.

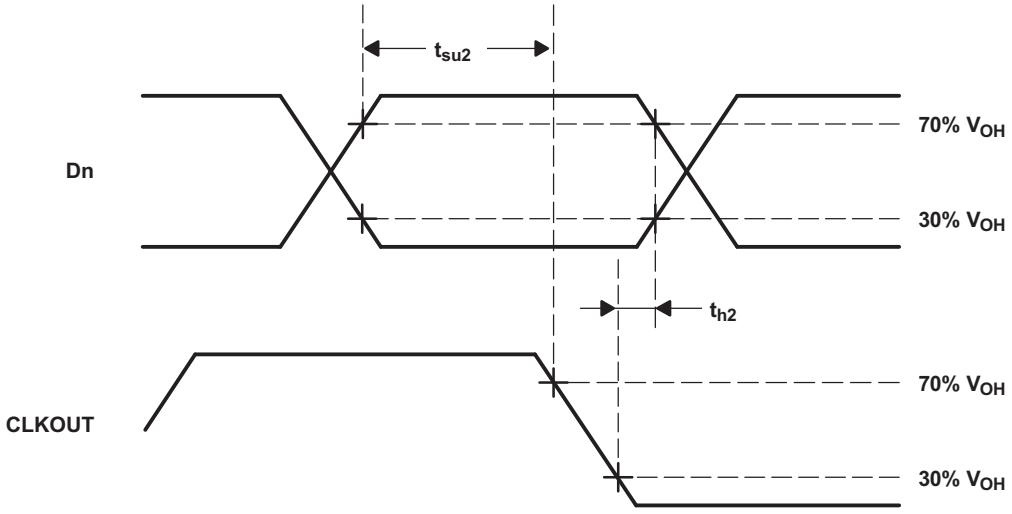


Figure 1. Setup and Hold Time Waveforms

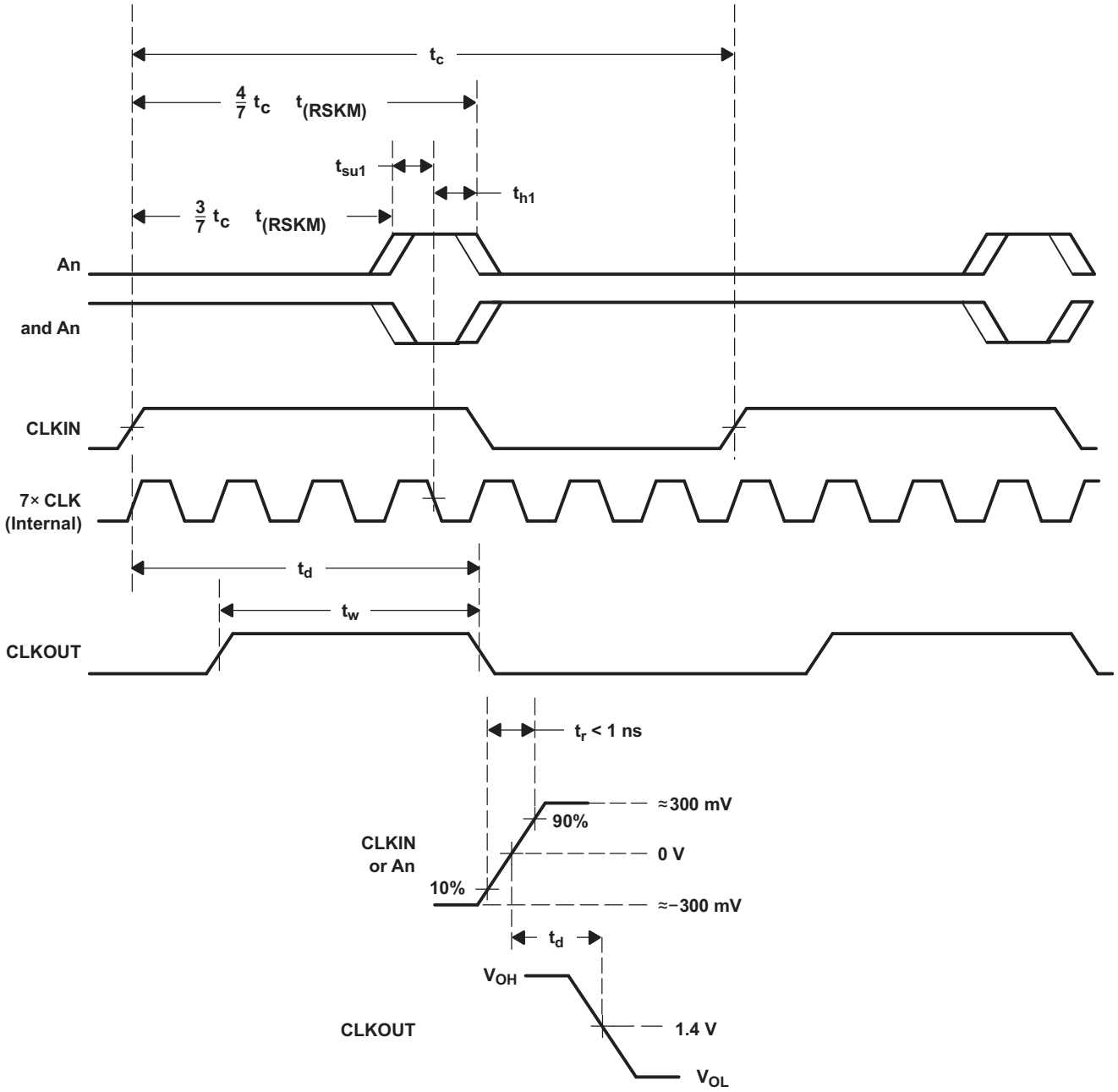


Figure 2. Receiver Input Skew Margin and Delay Timing Waveforms

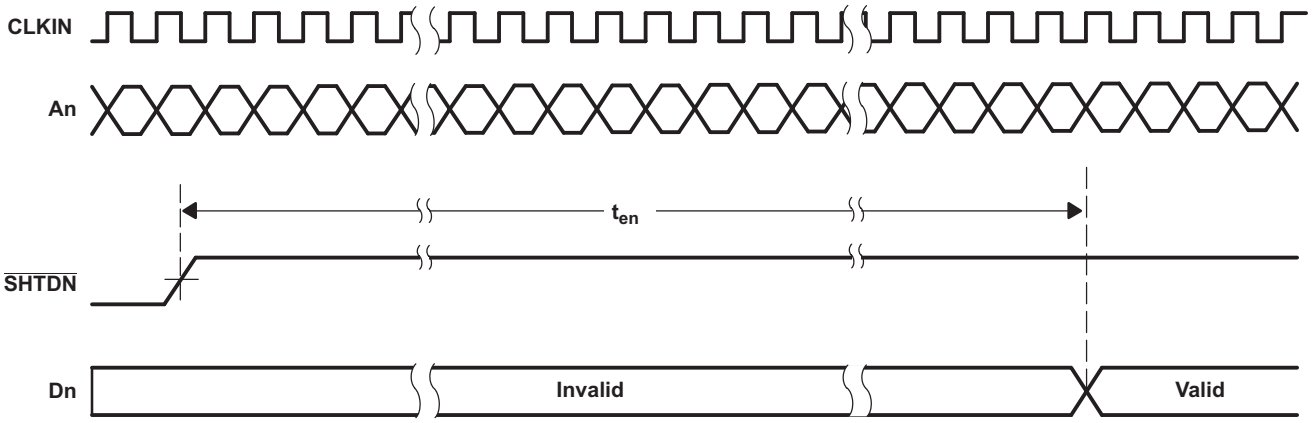


Figure 3. Enable Time Waveforms

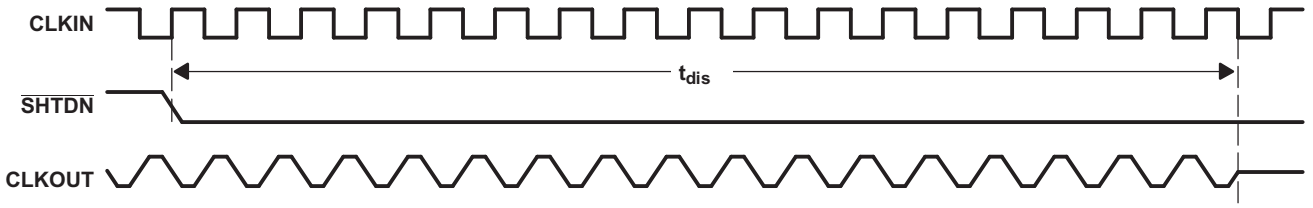


Figure 4. Disable Time Waveforms

7.8 Typical Characteristics

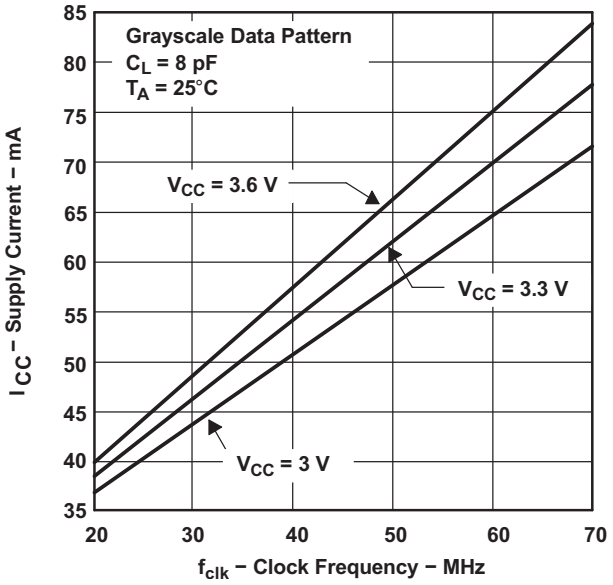


Figure 5. Supply Current vs Clock Frequency

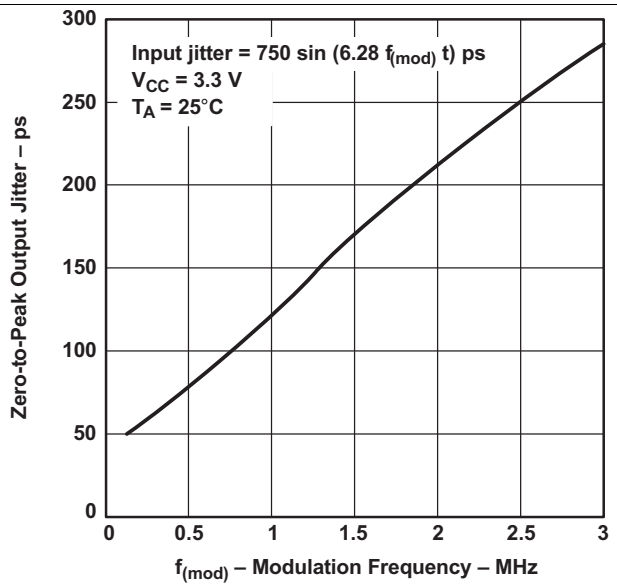


Figure 6. Zero-to-Peak Output Jitter vs Modulation Frequency

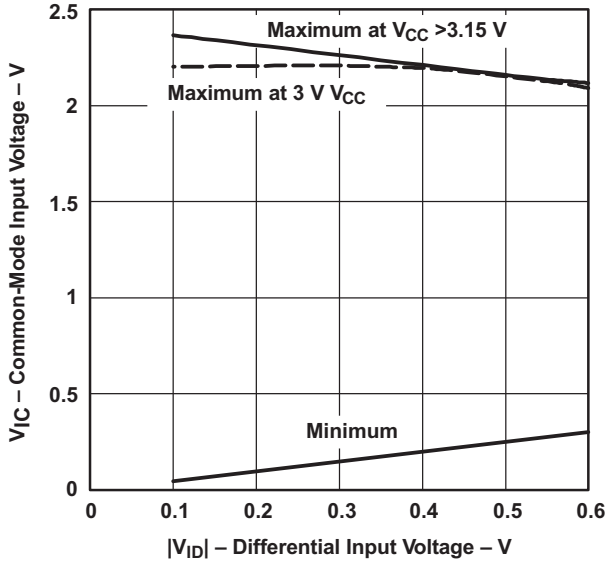


Figure 7. Common-Mode Input Voltage vs Differential Input Voltage

8 Parameter Measurement Information

8.1 Equivalent Input and Output Schematic Diagrams

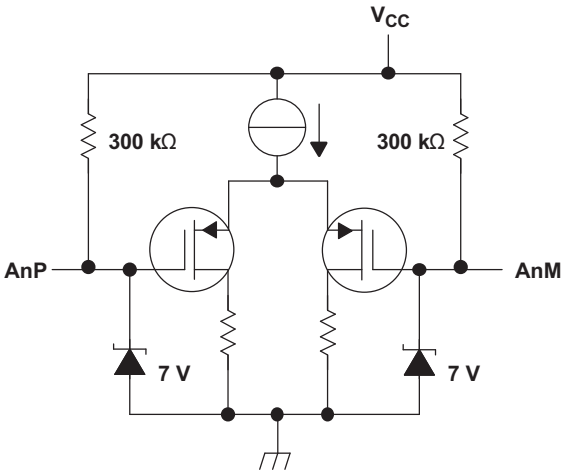


Figure 8. LVDS Input

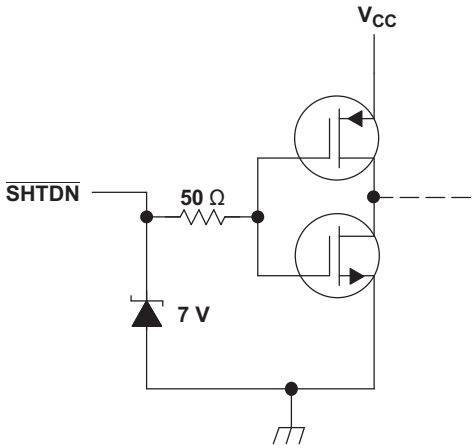


Figure 9. $\overline{SHTDN}$ Input

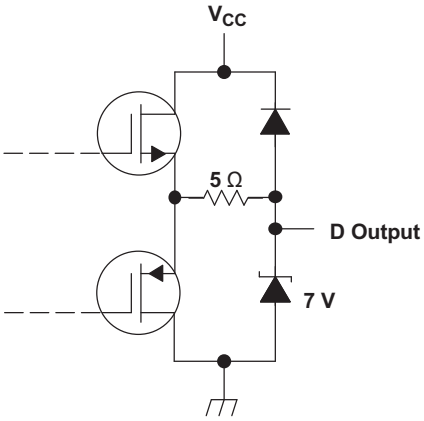


Figure 10. Output

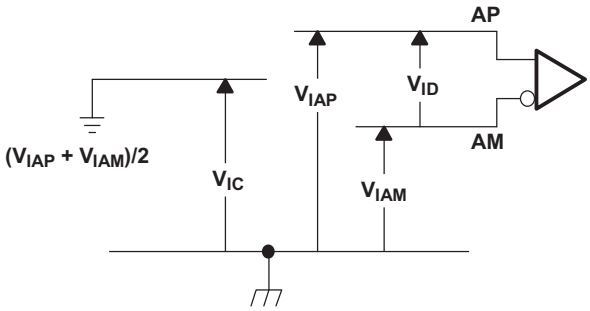


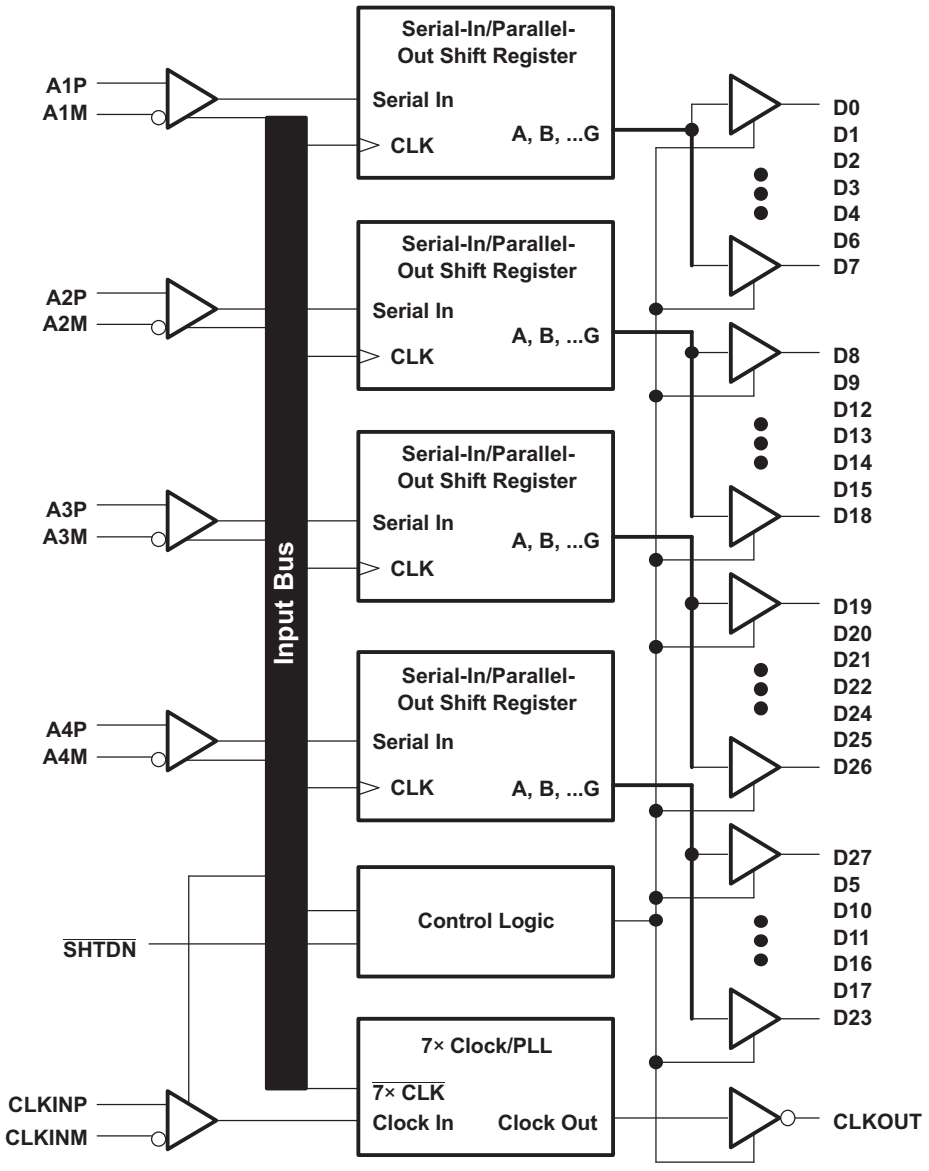
Figure 11. Voltage Definitions

9 Detailed Description

9.1 Overview

The SN75LVDS82 implements five low-voltage differential signal (LVDS) line receivers: 4 data lanes and 1 clock lane. The clock is internally multiplied by 7 and used for sampling LVDS data. Each input lane contains a shift register that converts serial data to parallel. 28 total bits per clock period are deserialized and presented on the LVTTL output bus

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 LVDS Input Data

The SN65LVDS82 is a simple deserializer that ignores bit representation in the LVDS stream. The data inputs to the receiver come from a transmitters such as the SN75LVDS83B and consist of up to 24 bits of video information, a horizontal synchronization bit, a vertical synchronization bit, an enable bit, and a spare bit.

The pixel data assignment is listed in Table 1 for 24-bit, 18-bit, and 12-bit color hosts.

Table 1. Pixel Data Assignment

SERIAL CHANNEL	DATA BITS	8-BIT			6-BIT	4-BIT	
		FORMAT-1	FORMAT-2	FORMAT-3		NON-LINEAR STEP SIZE	LINEAR STEP SIZE
Y0	D0	R0D27	R2	R2	R0	R2	VCC
	D1	R1	R3	R3	R1	R3	GND
	D2	R2	R4	R4	R2	R0	R0
	D3	R3	R5	R5	R3	R1	R1
	D4	R4	R6	R6	R4	R2	R2
	D6	R5	R7	R7	R5	R3	R3
	D7	G0	G2	G2	G0	G2	VCC
Y1	D8	G1	G3	G3	G1	G3	GND
	D9	G2	G4	G4	G2	G0	G0
	D12	G3	G5	G5	G3	G1	G1
	D13	G4	G6	G6	G4	G2	G2
	D14	G5	G7	G7	G5	G3	G3
	D15	B0	B2	B2	B0	B2	VCC
	D18	B1	B3	B3	B1	B3	GND
Y2	D19	B2	B4	B4	B2	B0	B0
	D20	B3	B5	B5	B3	B1	B1
	D21	B4	B6	B6	B4	B2	B2
	D22	B5	B7	B7	B5	B3	B3
	D24	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
	D25	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
	D26	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
Y3	D27	R6	R0	GND	GND	GND	GND
	D5	R7	R1	GND	GND	GND	GND
	D10	G6	G0	GND	GND	GND	GND
	D11	G7	G1	GND	GND	GND	GND
	D16	B6	B0	GND	GND	GND	GND
	D17	B7	B1	GND	GND	GND	GND
	D23	RSVD	RSVD	GND	GND	GND	GND
CLKOUT	CLKIN	CLK	CLK	CLK	CLK	CLK	CLK

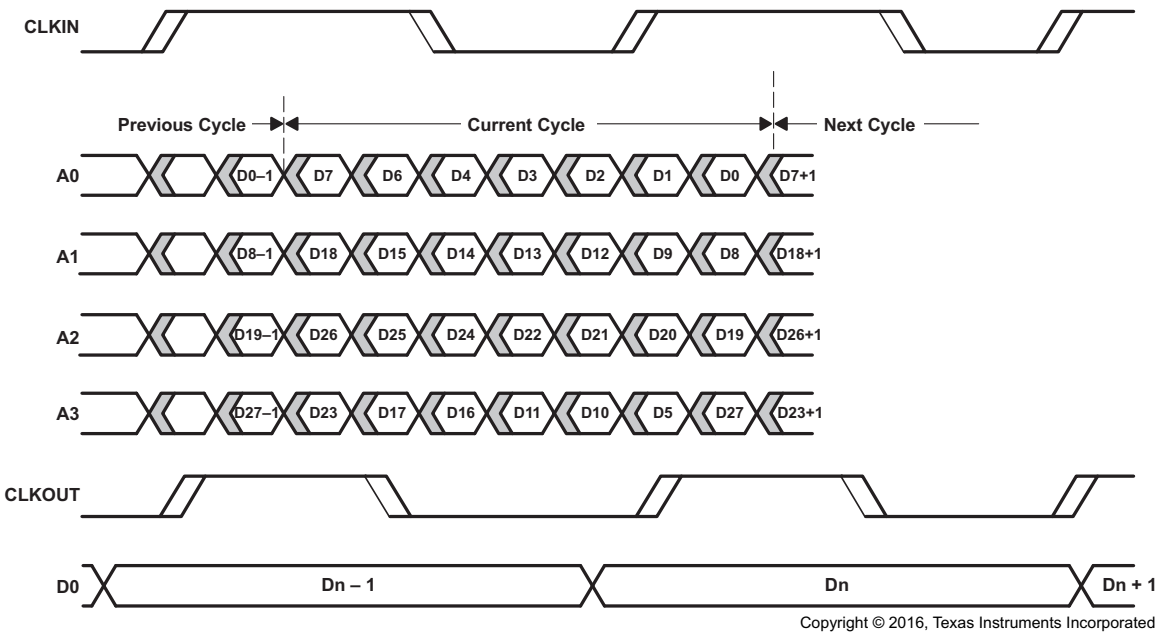


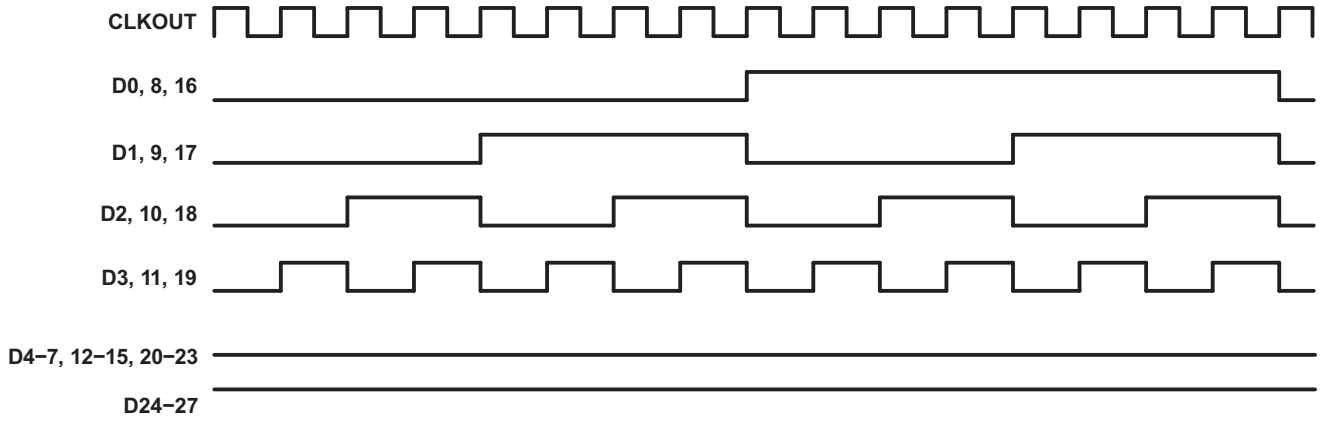
Figure 12. SN75LVDS82 Load and Shift Timing Sequences

9.4 Device Functional Modes

9.4.1 Low Power Mode

The SN75LVDS82 can be put in low-power consumption mode by active-low input $\overline{\text{SHTDN}}$. Connecting pin $\overline{\text{SHTDN}}$ to GND inhibits the clock and shut off the LVDS output drivers for lower power consumption. A low level on this signal clears all internal registers to a low-level. Populate a pull-up to V_{CC} on $\overline{\text{SHTDN}}$ to enable the device for normal operation.

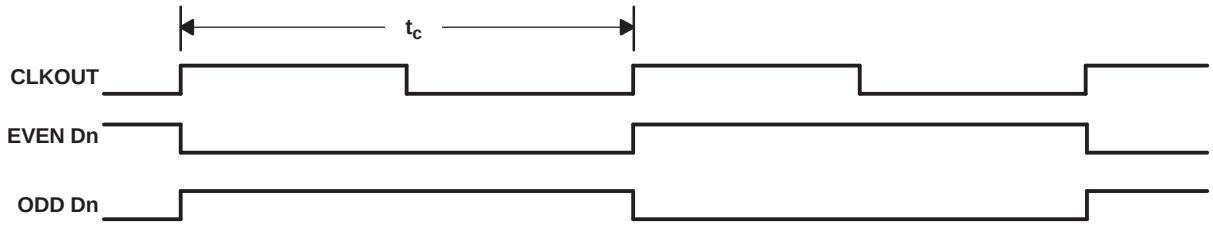
9.4.2 Test Patterns



NOTE A: The 16-grayscale test-pattern tests device power consumption for a typical display pattern.

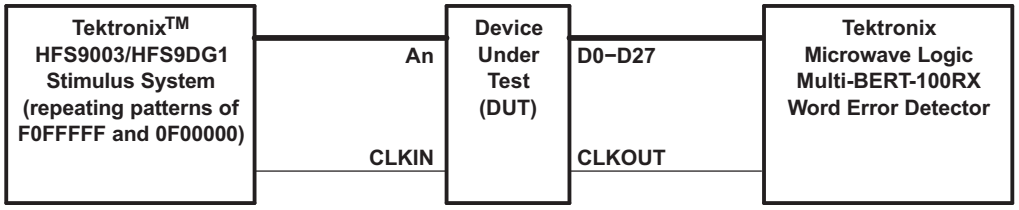
Figure 13. 16-Grayscale Test-Pattern Waveforms

Device Functional Modes (continued)

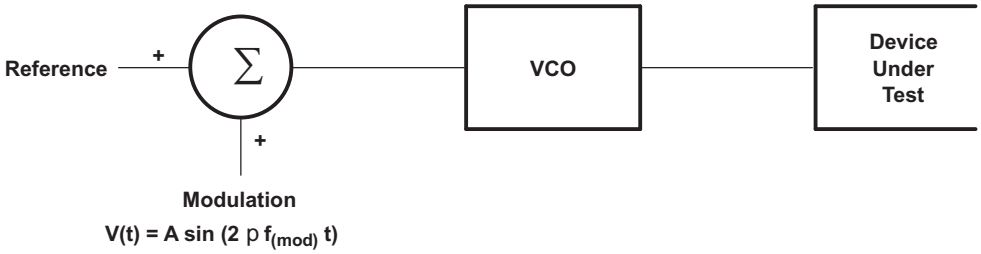


NOTE A: The worst-case test pattern produces the maximum switching frequency for all of the outputs.

Figure 14. Worst-Case Test-Pattern Waveforms



A. CLKIN is advanced or delayed with respect to data until errors are observed at the receiver outputs. The magnitude of the advance or delay is $t_{(RSKM)}$.



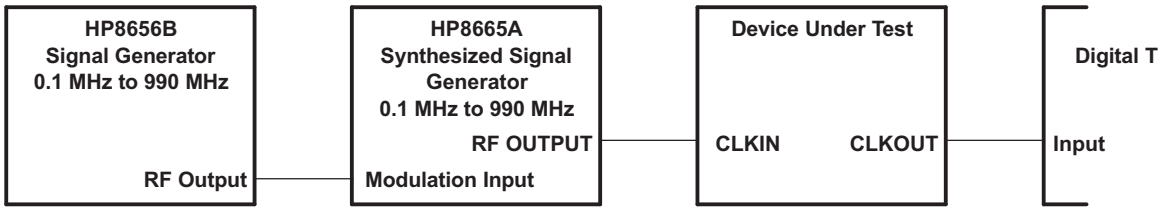


Figure 15. Input Clock Jitter Test

10 Application and Implementation

NOTE

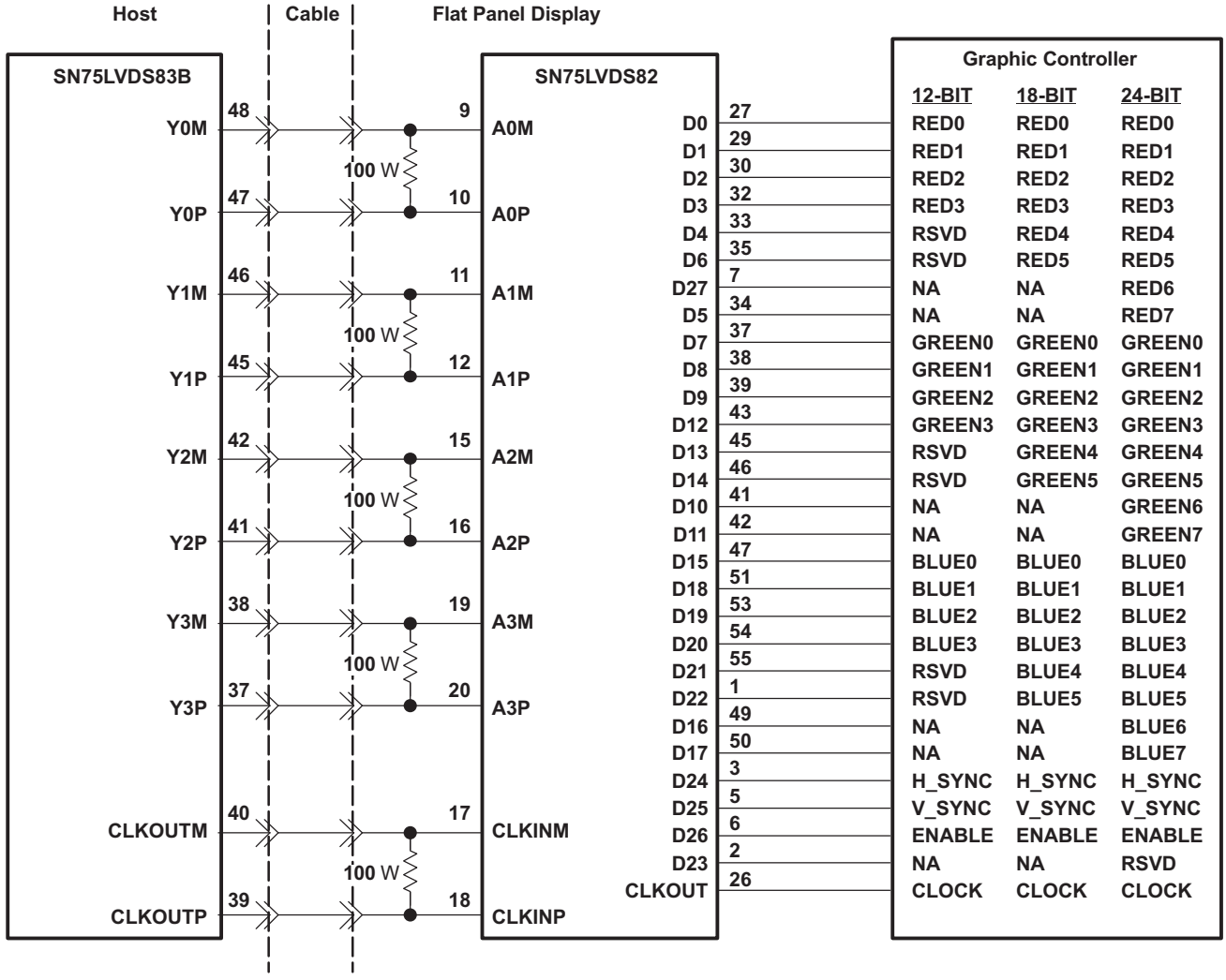
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This section describes provides information on how each signal should be connected from the graphic source through the SN75LVDS83B and the SN75LVDS82 to the LCD panel input.

10.2 Typical Applications

10.2.1 Signal Connectivity



A. The five 100-Ω terminating resistors are recommended to be 0603 types.

B. NA — not applicable, these unused inputs should be left open.

Figure 16. 24-Bit Color Host to 24-Bit LCD Flat Panel Display Application

Typical Applications (continued)

10.2.1.1 Design Requirements

For this design example, use the parameters shown in Table 2.

Table 2. Design Parameters

DESIGN PARAMETERS	VALUE
VDD Main Power Supply	3.3 V
Input LVDS Clock Frequency	31 - 68 MHz
R_L Differential Input Termination Resistance	100 Ω
LVDS Input Lanes	4
Color depth	24 Bit

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Power Up Sequence

The user experience can be impacted by the way a system powers up and powers down an LCD screen. The following sequence is recommended.

Power up sequence (SN75LVDS82 /SHTDN input initially low):

1. Ramp up LCD power (maybe 0.5 ms to 10 ms) but keep backlight turned off.
2. Wait for additional 0-200 ms to ensure display noise will not occur.
3. Enable video source output; start sending black video data.
4. Toggle SN75LVDS82 shutdown to $\overline{SHTDN}$ = V_{IH}.
5. Send > 1 ms of black video data; this allows the SN75LVDS82 to be phase locked, and the display to show black data first.
6. Start sending true image data.
7. Enable backlight.

Power Down sequence (SN75LVDS82 SHTDN input initially high):

1. Disable LCD backlight; wait for the minimum time specified in the LCD data sheet for the backlight to go low
2. Video source output data switch from active video data to black image data (all visible pixel turn black); drive this for > 2 frame times.
3. Set SN75LVDS82 input $\overline{SHTDN}$ = GND; wait for 250 ns.
4. Disable the video output of the video source.
5. Remove power from the LCD panel for lowest system power.

10.2.1.3 Application Curves

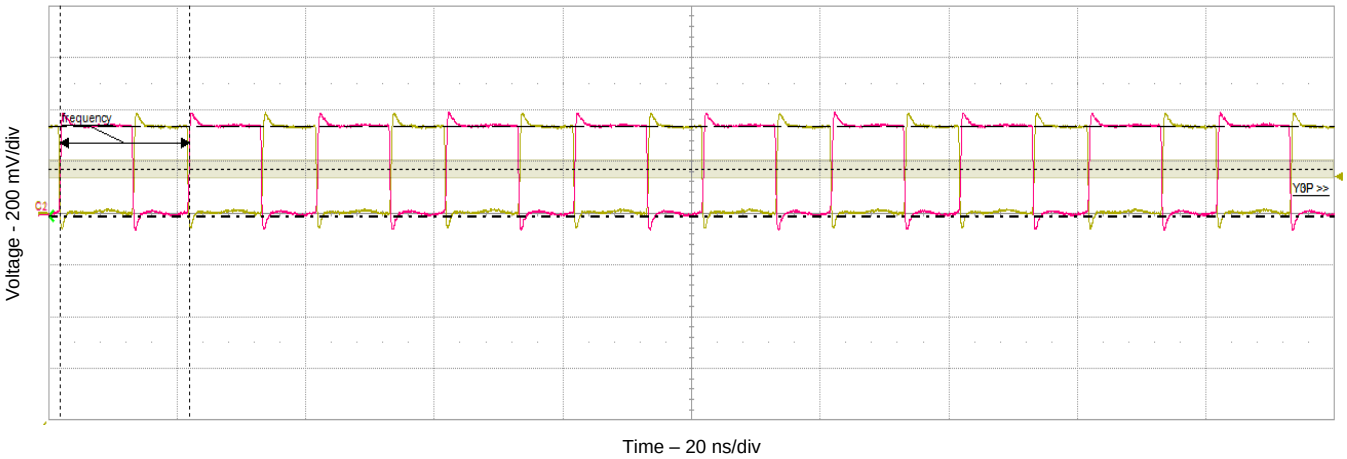


Figure 17. LVDS Clock

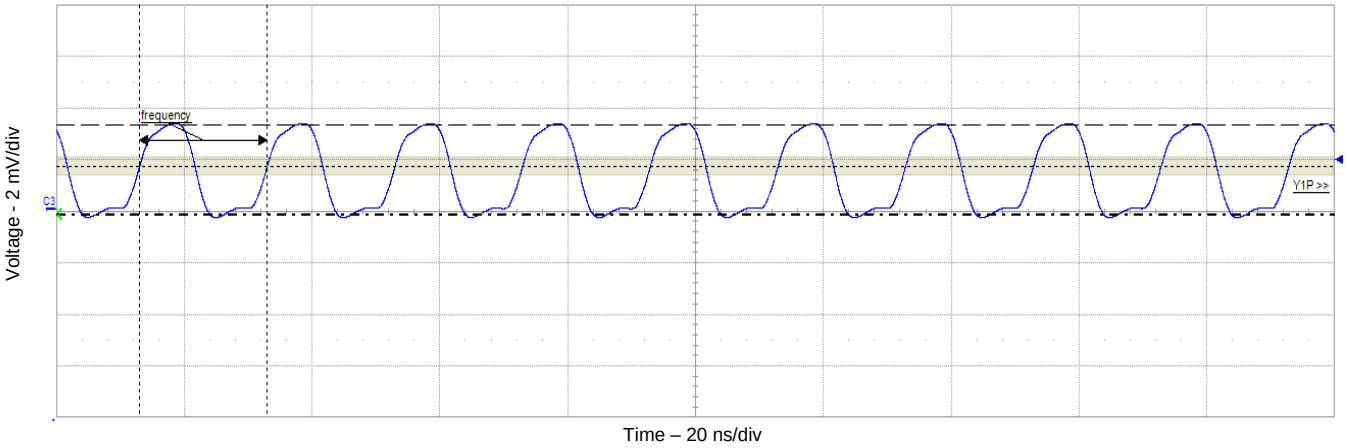


Figure 18. Output Clock

11 Power Supply Recommendations

11.1 Decoupling Capacitor Recommendations

To minimize the power supply noise floor, provide good decoupling near the SN65LVDS82 power pins. It is recommended to place one 0.01-μF ceramic capacitor at each power pin, and two 0.1-μF ceramic capacitors on each power node. The distance between the SN65LVDS82 and capacitors should be minimized to reduce loop inductance and provide optimal noise filtering. Placing the capacitor underneath the SN65LVDS82 on the bottom of the PCB is often a good choice. A 100-pF ceramic capacitor can be put at each power pin to optimize the EMI performance.

12 Layout

12.1 Layout Guidelines

1. Use 45 degree bends (chamfered corners), instead of right-angle (90°) bends. Right-angle bends increase the effective trace width, which changes the differential trace impedance creating large discontinuities. A 45 degree bend is seen as a smaller discontinuity.
2. Place passive components within the signal path, such as source-matching resistors or ac-coupling capacitors, next to each other. Routing as in case a) creates wider trace spacing than in b), the resulting discontinuity, however, is limited to a far narrower area
3. When routing traces next to a via or between an array of vias, make sure that the via clearance section does not interrupt the path of the return current on the ground plane below.
4. Avoid metal layers and traces underneath or between the pads off the DisplayPort connectors for better impedance matching. Otherwise they will cause the differential impedance to drop below 75 Ω and fail the board during TDR testing.
5. Use solid power and ground planes for 100 Ω impedance control and minimum power noise. For a multilayer PCB, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.
6. For 100 Ω differential impedance, use the smallest trace spacing possible, which is usually specified by the PCB vendor.
7. Keep the trace length as short as possible to minimize attenuation.
8. Place bulk capacitors (that is, 10 μF) close to power sources, such as voltage regulators or where the power is supplied to the PCB.

12.2 Layout Example

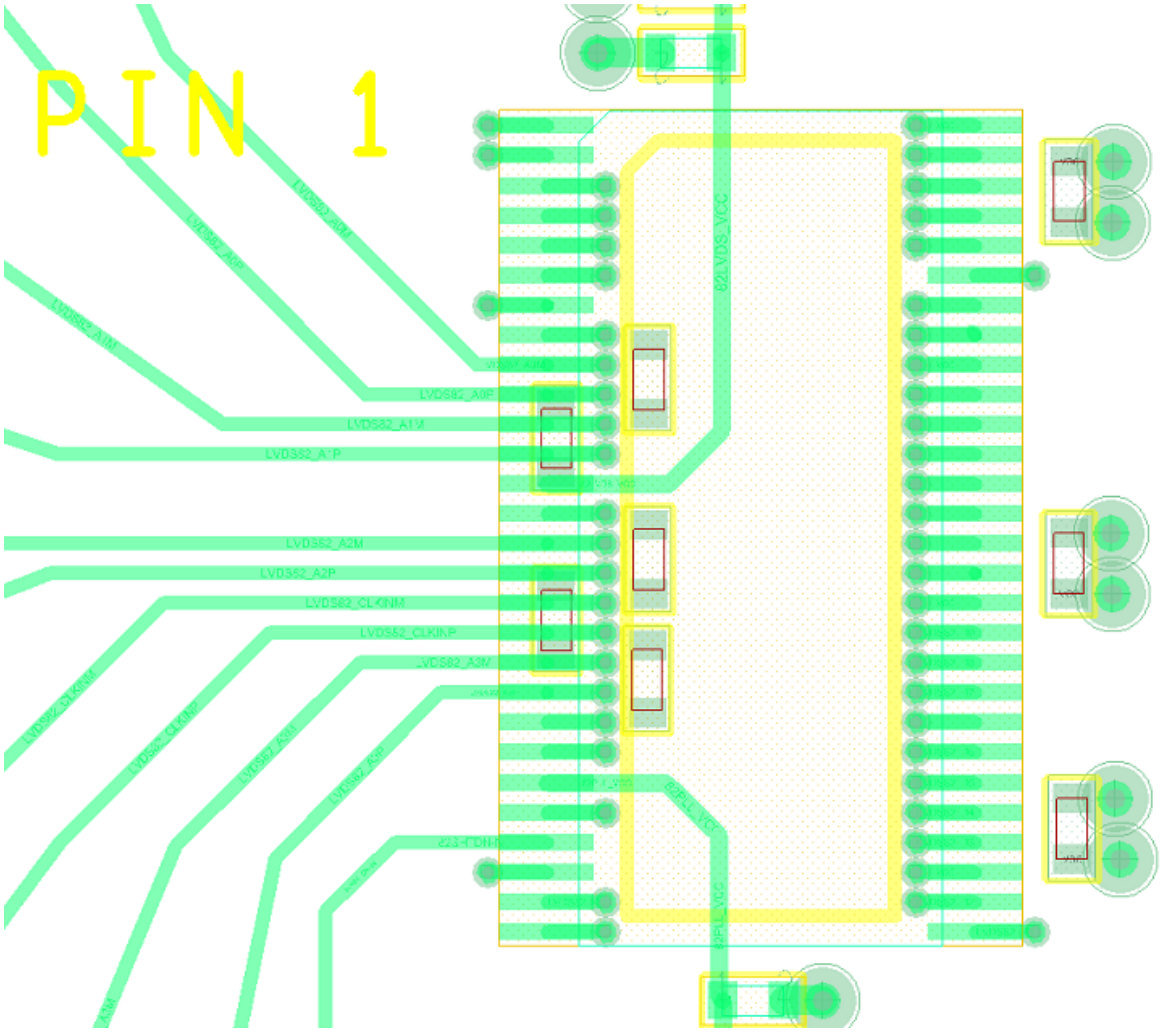


Figure 19. Layout Example

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

FlatLink, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75LVDS82DGG	Active	Production	TSSOP (DGG) | 56	35 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS82
SN75LVDS82DGG.B	Active	Production	TSSOP (DGG) | 56	35 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS82
SN75LVDS82DGGR	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS82
SN75LVDS82DGGR.B	Active	Production	TSSOP (DGG) | 56	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS82

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

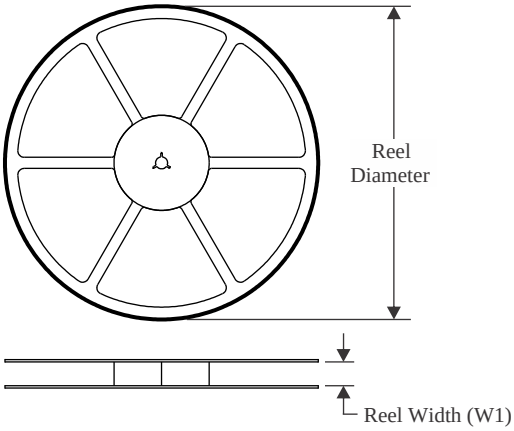
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

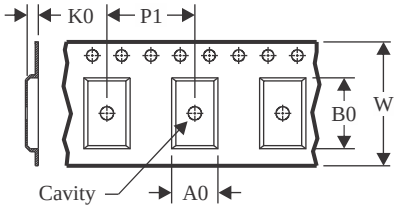
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

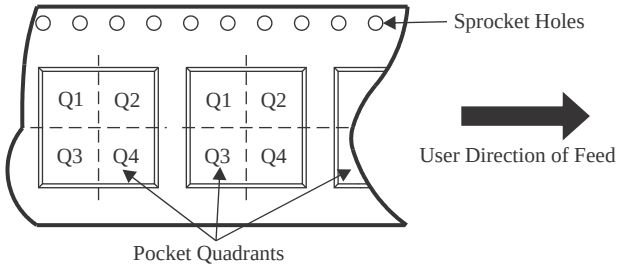


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

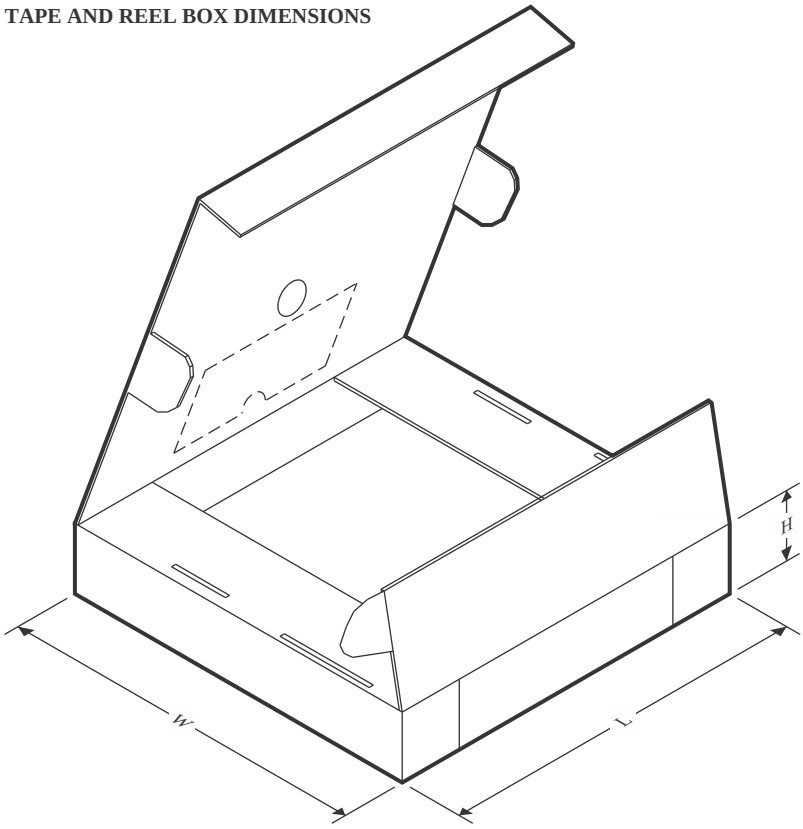
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVDS82DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

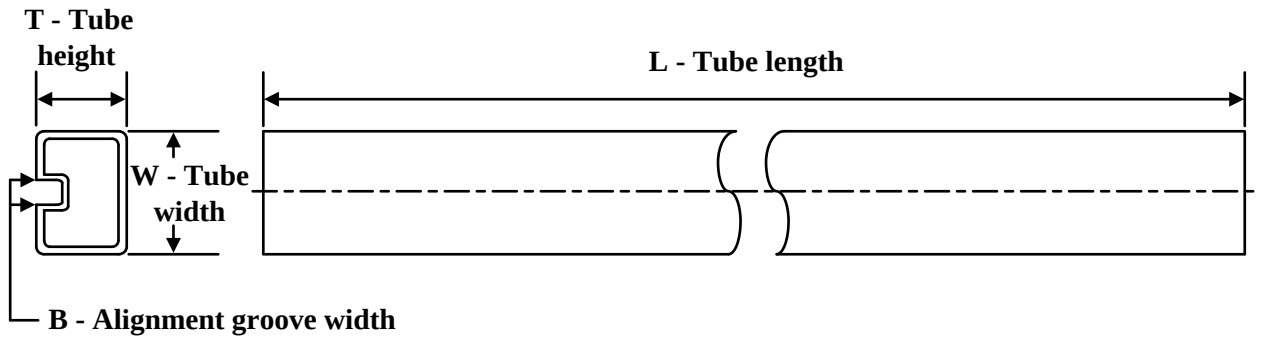
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVDS82DGGR	TSSOP	DGG	56	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

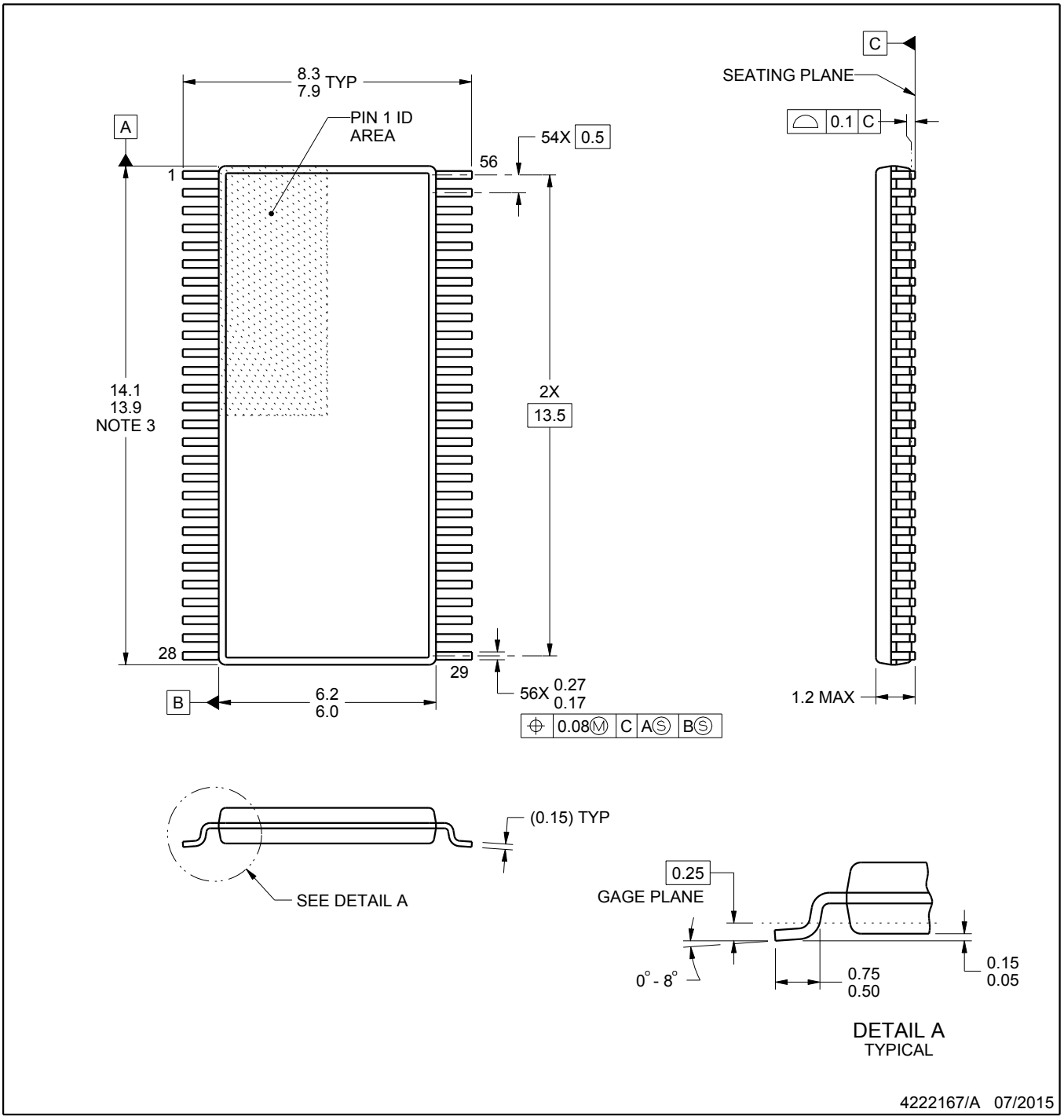
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75LVDS82DGG	DGG	TSSOP	56	35	530	11.89	3600	4.9
SN75LVDS82DGG.B	DGG	TSSOP	56	35	530	11.89	3600	4.9

PACKAGE OUTLINE

DGG0056A

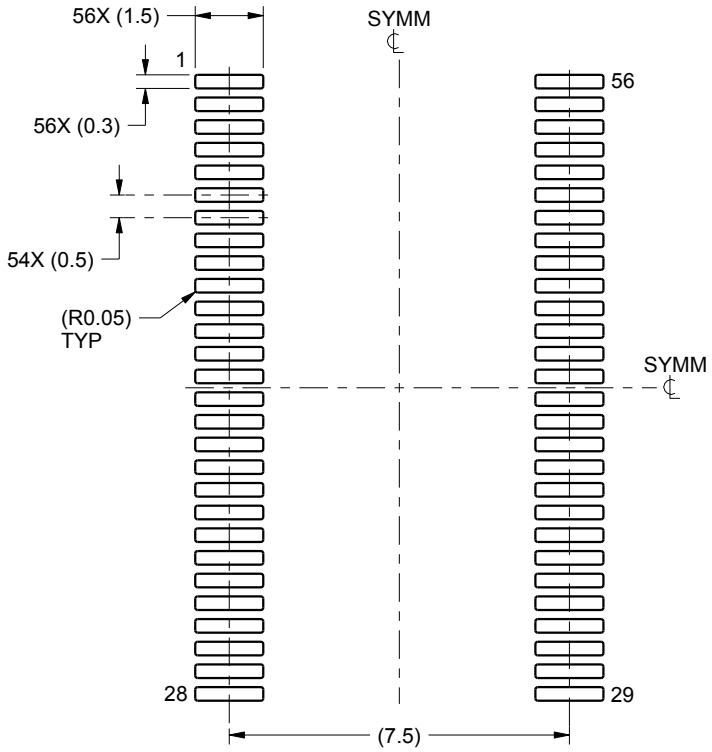
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

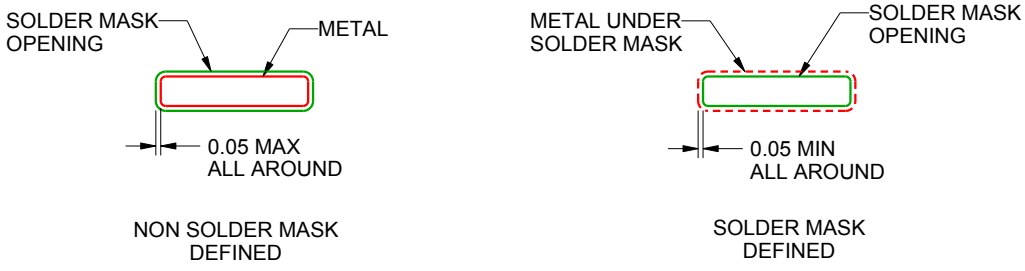


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

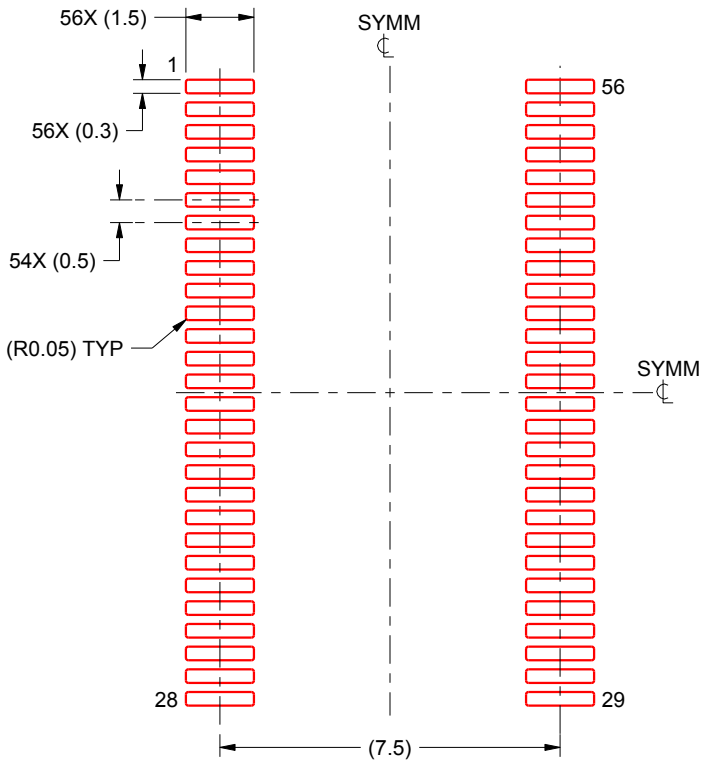


SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025