TAS5720x Digital Input Mono Class-D Audio Amplifier With TDM Support Up To 8 Channels

1 Features

- Mono Class-D Amplifier
  - 20 W at 0.15% THD Continuous into 19 V / 4 Ω
- TDM Audio Input
  - Up to 8 Channels (32-bit, 48 kHz)
- I^2C Control With 8 Selectable I^2C Address
- Power Supplies
  - Power Amplifier: 4.5 V to 16.5 V, TAS5720L
  - Power Amplifier: 4.5 V to 26.4 V, TAS5720M
  - Digital I/O: 3.3 V
- Protection: Thermal and Short-Circuit
- Package: 4 mm × 4 mm, 32-pin VQFN

2 Applications

- Sub Woofers
- Boom Boxes
- Bar Speakers
- Surround Sound Systems

3 Description

The TAS5720x device is a high-efficiency mono Class-D audio power amplifier optimized for high transient power capability to use the dynamic power headroom of small loudspeakers. The device is capable of delivering more than 15 W continuously into a 4-Ω speaker.

The digital time division multiplexed (TDM) interface enables up to eight devices to share the same bus.

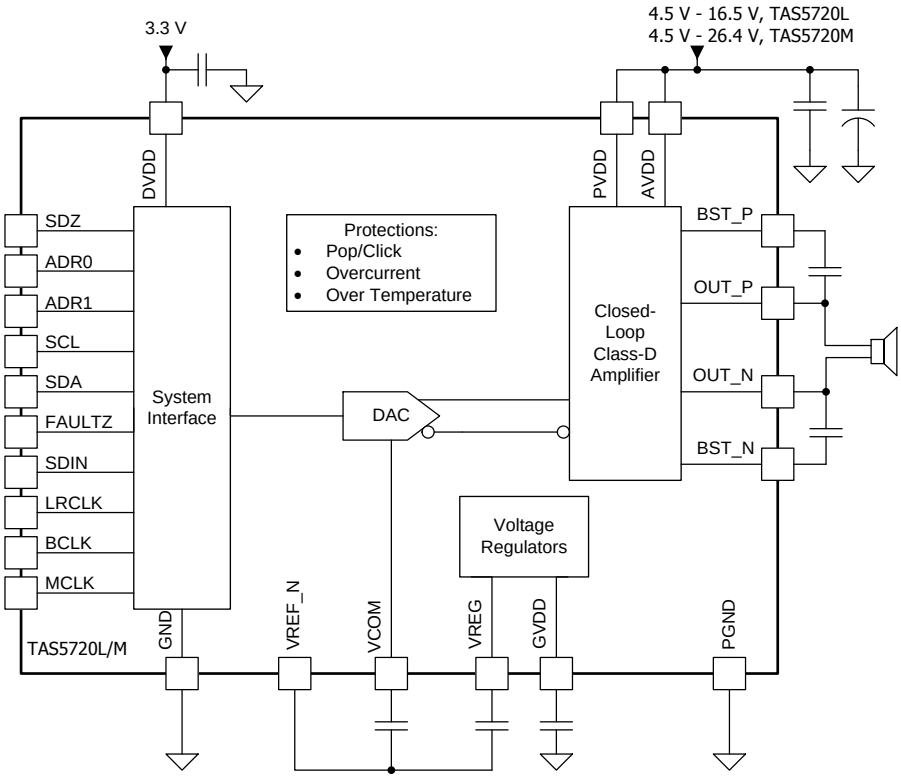
The TAS5720x device is available in a 32-pin, 4 mm × 4 mm, VQFN package for a compact PCB footprint.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TAS5720L	VQFN (32)	4.00 mm × 4.00 mm
TAS5720M		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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4 Revision History

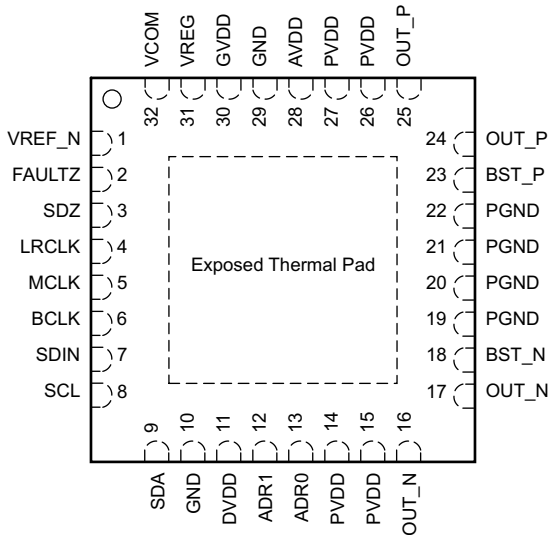
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2015) to Revision B	Page
• Updated Typical Characteristics graphs with new data, new standards.	12
• Added new Layout Example	43

Changes from Original (September 2015) to Revision A	Page
• Production release	1

5 Pin Configuration and Functions

RSM Package
VQFN 32 PINS
Top View



Pin Functions

PIN		I/O/P[1]	DESCRIPTION
NAME	NO.		
ADR1	12	I	I^2C address inputs. Each pin can detect a short to DVDD, a short to GND, a 22-kΩ connection to GND, and a 22-kΩ connection to DVDD.
ADR0	13	I	
AVDD	28	P	Analog power supply input. Connect directly to PVDD.
BST_N	18	P	Class-D Amplifier negative bootstrap. Connect to a capacitor between BST_N and OUT_N.
BST_P	23	P	Class-D Amplifier positive bootstrap. Connect to a capacitor between BST_P and OUT_P.
DVDD	11	P	Digital power supply. Connect to a 3.3-V supply with external decoupling capacitor.
FAULTZ	2	O	Open drain active low fault flag. Pull up on PCB with resistor to DVDD.
LRCLK	4	I	TDM interface frame synchronization.
GND	10 29	P	Ground. Connect to PCB ground plane.
GVDD	30	O	Class-D amplifier gate drive regulator output. Connect decoupling cap to PCB ground plane.
MCLK	5	I	Device master clock.
PGND	19 20 21 22	P	Power ground. Connect to PCB ground plane.
PVDD	14 15 26 27	P	Class-D amplifier power supply input. Connect to PVDD supply and decouple externally.
OUT_N	16 17	O	Class-D amplifier negative output.
OUT_P	24 25	O	Class-D amplifier positive output.
BCLK	6	I	TDM Interface serial bit clock.

(1) I = input, O = output, P = power, I/O = bi-directional

Pin Functions (continued)

PIN		I/O/P(1)	DESCRIPTION
NAME	NO.		
SCL	8	I	I^2C clock Input. Pull up on PCB with a 2.4-kΩ resistor.
SDA	9	I/O	I^2C bi-directional data. Pull up on PCB with a 2.4-kΩ resistor.
SDIN	7	I	TDM interface data input.
SDZ	3	I	Active low shutdown signal. Assert low to hold device inactive.
Thermal Pad	33	G	Connect to GND for best system performance. If not connected to GND, leave floating.
VCOM	32	O	Common mode reference output. Connect decoupling capacitor to the VREF_N pin.
VREF_N	1	P	Negative reference for analog. Connect to VCOM and VREG capacitor negative pins.
VREG	31	O	Analog regulator output. Connect decoupling capacitor to the VREF_N pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage(2)	PVDD, AVDD (TAS5720L)	–0.3	20	V
	PVDD, AVDD (TAS5720M)	–0.3	30	
	DVDD	–0.3	4	
Digital input voltage	Digital inputs referenced to DVDD supply	–0.5	V_{DVDD} + 0.5	V
Ambient operating temperature, T_A		–25	85	°C
Storage temperature, T_{stg}		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) All voltages are with respect to network ground pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001,(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
PVDD/ AVDD	Power supply voltage	TAS5720L	4.5		16.5	V
		TAS5720M	4.5		26.4	V
DVDD	Power supply voltage		3	3.3	3.6	V
$V_{IH(DR)}$	High-level digital input voltage			V_{DVDD}		V
$V_{IL(DR)}$	Low-level digital input voltage			0		V
R_{SPK}	Minimum speaker load		3.2			Ω
T_A	Operating free-air temperature		–25		85	°C
T_J	Operating junction temperature		–25		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TAS5720x RSM (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.3	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	30.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.7	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

T_A = 25ºC, $V_{(PVDD)}$ = 15 V, $V_{(DVDD)}$ = 3.3 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_s = 48 kHz, $f_{(PWM)}$ = 768 kHz, Gain = 20.7 dBV, SDZ = 1, Measured with an Audio Precision SYS-2722 High-Performance Audio Analyzer and using a 15-µH, 0.68-µF reconstruction filter at the device output.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT AND OUTPUT						
V_{IH}	High-level digital input logic voltage threshold	All digital pins	70% V_{DVDD}			
V_{IL}	Low-level digital input logic voltage threshold	All digital pins			30% V_{DVDD}	
I_{IH}	Input logic "high" leakage for digital inputs	All digital pins, excluding SDZ			15	µA
I_{IL}	Input logic "low" leakage for digital inputs	All digital pins, excluding SDZ			–15	µA
$I_{IH(SDZ)}$	Input logic "high" leakage for SDZ inputs	SDZ			1	µA
$I_{IL(SDZ)}$	Input logic "low" leakage for SDZ inputs	SDZ			–1	µA
V_{OL}	Output logic "low" for FAULTZ open drain Output	I_{OL} = –2 mA			10% V_{DVDD}	
C_{IN}	Input capacitance for digital inputs	All digital pins		5		pF
MASTER CLOCK						
$D_{(MCLK)}$	Allowable MCLK duty cycle		45%	50%	55%	
$f_{(MCLK)}$	MCLK input frequency				25	MHz
	Supported single-speed MCLK frequencies	Values: 64, 128, 256, and 512	64 × f_S		512 × f_S	
	Supported double-speed MCLK frequencies	Values: 64, 128, and 256	64 × f_S		256 × f_S	
SERIAL AUDIO PORT						
$D_{(BCLK)}$	Allowable BCLK duty cycle		45%	50%	55%	
$f_{(BCLK)}$	BCLK input frequency				25	MHz
	Supported single-speed BCLK frequencies	Values: 64, 128, 256, and 512	64 × f_S		512 × f_S	
	Supported double-speed BCLK frequencies	Values: 64, 128, and 256	64 × f_S		256 × f_S	
f_S	Supported single-speed input sample rates	Values: 44.1 and 48	44.1		48	kHz
	Supported double-speed input sample rates	Values: 88.2 and 96	88.2		96	kHz
I^2C CONTROL PORT						
$C_{L(I2C)}$	Allowable load capacitance for each I^2C Line				400	pF
f_{SCL}	SCL frequency	No wait states			400	kHz
PROTECTION						
$OTE_{(THRESH)}$	Overtemperature error (OTE) threshold			150		°C
$OTE_{(HYST)}$	Overtemperature error (OTE) hysteresis			15		°C
$OCE_{(THRESH)}$	Overcurrent error (OCE) threshold	$V_{(PVDD)}$ = 16.5 V, T_A = 25°C		6		A
$DCE_{(THRESH)}$	DC error (DCE) threshold	$V_{(PVDD)}$ = 16.5 V, TA = 25°C		2.6		V

Electrical Characteristics (continued)

T_A = 25ºC, $V_{(PVDD)}$ = 15 V, $V_{(DVDD)}$ = 3.3 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_s = 48 kHz, $f_{(PWM)}$ = 768 kHz, Gain = 20.7 dBV, SDZ = 1, Measured with an Audio Precision SYS-2722 High-Performance Audio Analyzer and using a 15-µH, 0.68-µF reconstruction filter at the device output.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
AMPLIFIER PERFORMANCE						
P_{OUT}	Continuous average power	R_L= 4 Ω, 10% THD+N, $V_{(PVDD)}$ = 7.2 V, f_{IN} = 1 kHz		6.6		W
		R_L= 8 Ω, 10% THD+N, $V_{(PVDD)}$ = 7.2 V, f_{IN} = 1 kHz		3.7		
		R_L= 4 Ω, 10% THD+N, $V_{(PVDD)}$ = 12 V, f_{IN} = 1 kHz		17.8		
		R_L= 8 Ω, 10% THD+N, $V_{(PVDD)}$ = 12 V, f_{IN} = 1 kHz		10.1		
		R_L= 4 Ω, 10% THD+N, $V_{(PVDD)}$ = 15 V, f_{IN} = 1 kHz, T_A= 60°C		27.4		
		R_L= 8 Ω, 10% THD+N, $V_{(PVDD)}$ = 15 V, f_{IN} = 1 kHz		15.8		
		R_L= 4 Ω, 10% THD+N, $V_{(PVDD)}$ = 19 V, f_{IN} = 1 kHz		27		
		R_L= 8 Ω, 10% THD+N, $V_{(PVDD)}$ = 19 V, f_{IN} = 1 kHz		25.3		
		R_L= 4 Ω, 10% THD+N, $V_{(PVDD)}$ = 24 V, f_{IN} = 1 kHz		22.1		
		R_L= 8 Ω, 10% THD+N, $V_{(PVDD)}$ = 24 V, f_{IN} = 1 kHz		39.8		
THD+N	Total harmonic distortion plus noise	R_L= 4 Ω,$V_{(PVDD)}$ = 7.2 V, P_{OUT} = 1 W, f_{IN} = 1 kHz		0.033%		
		R_L= 8 Ω,$V_{(PVDD)}$ = 7.2 V, P_{OUT} = 1 W, f_{IN} = 1 kHz		0.015%		
		R_L= 4 Ω, $V_{(PVDD)}$= 12 V, P_{OUT} = 1 W, f_{IN} = 1 kHz		0.03%		
		R_L= 8 Ω, $V_{(PVDD)}$= 12 V, P_{OUT} = 1 W, 20 Hz ≤ f_{IN} ≤ 20 kHz		0.013v		
		R_L= 4 Ω, $V_{(PVDD)}$ = 15 V, P_{OUT} = 1 W, 20 Hz ≤ f_{IN}≤ 20 kHz		0.028%		
		R_L= 8 Ω, $V_{(PVDD)}$ = 15 V, P_{OUT} = 1 W, 20 Hz ≤ f_{IN}≤ 20 kHz		0.012%		
		R_L= 4 Ω, $V_{(PVDD)}$ = 19 V, P_{OUT} = 1 W, 20 Hz ≤ f_{IN} ≤ 20 kHz		0.026%		
		R_L= 8 Ω, $V_{(PVDD)}$ = 19 V, P_{OUT} = 1 W, 20 Hz ≤ f_{IN} ≤ 20 kHz		0.013%		
		R_L= 4 Ω, $V_{(PVDD)}$ = 24 V, P_{OUT} = 1 W, 20 Hz ≤ f_{IN} ≤ 20 kHz		0.026%		
		R_L= 8 Ω, $V_{(PVDD)}$ = 24 V, P_{OUT} = 1 W, 20 Hz ≤ f_{IN} ≤ 20 kHz		0.016%		
P_{EFF}	Power efficiency	R_L= 8 Ω, $V_{(PVDD)}$ = 12 V, P_{OUT} = 9 W		91%		
		R_L= 8 Ω, $V_{(PVDD)}$ = 12 V, P_{OUT} = 9 W; f_{PWM} = 384 kHz		90%		
		R_L= 8 Ω, $V_{(PVDD)}$ = 24 V, P_{OUT} = 40 W		90%		
V_N	Integrated noise floor voltage	A-Weighted,R_L= 8 Ω, Gain = 20.7 dBV		50		µVrms
φ_{CC}	Channel-to-channel phase shift	Output phase shift between multiple devices from 20 Hz to 20 kHz. Across all sample frequencies and SAIF operating modes.		0.2		deg
$A_{(RIPPLE)}$	Frequency response	Maximum deviation above or below passband gain.		±0.15		dB
	-3 dB Output Cutoff Frequency			0.47 × f_S		Hz

Electrical Characteristics (continued)

T_A = 25ºC, $V_{(PVDD)}$ = 15 V, $V_{(DVDD)}$ = 3.3 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_s = 48 kHz, $f_{(PWM)}$ = 768 kHz, Gain = 20.7 dBV, SDZ = 1, Measured with an Audio Precision SYS-2722 High-Performance Audio Analyzer and using a 15-µH, 0.68-µF reconstruction filter at the device output.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
$AV_{(00)}$	Amplifier analog gain(1)	ANALOG_GAIN[1:0] register bits set to "00"		19.2		dBV
$AV_{(01)}$		ANALOG_GAIN[1:0] register bits set to "01"		20.7		
$AV_{(10)}$		ANALOG_GAIN[1:0] register bits set to "10"		23.5		
$AV_{(11)}$		ANALOG_GAIN[1:0] register bits set to "11"		26.3		
$AV_{(ERROR)}$	Amplifier analog gain error				±0.15	dB
V_{OS}	DC output offset voltage	Measured between OUTP and OUTN		1.5		mV
KCP	Click-pop performance			–60		dBV
PSRR	Power supply rejection ratio	DC, 5.5 V ≤ $V_{(PVDD)}$ ≤ 26.4 V		87		dB
		AC, $V_{(PVDD)}$= 16.5 V + 100 mV_{P-P}, $f_{(RIPPLE)}$ from 20 Hz to 10 kHz		53		
		AC, $V_{(PVDD)}$= 16.5 V + 100 mV_{P-P}, $f_{(RIPPLE)}$ from 10 Hz to 20 kHz		50		
$R_{DS(on)FET}$	Power stage FET on-resistance	T_A = 25°C		120		mΩ
$R_{DS(on)TOT}$	Power stage total on-resistance (FET+bond+package)	T_A = 25°C		150		mΩ
I_{PK}	Peak output current	T_A = 25°C		5		A
$f_{(HP)}$	–3 dB high-pass filter corner frequency	f = 44.1 kHz		3.675		Hz
		f = 48 kHz		4		
		f = 88.2 kHz		7.35		
		f = 96 kHz		8		
$f_{(PWM)}$	PWM switching frequency	Values: 6, 8, 10, 12, 14, 16, 20, and 24	6		24	f_S

(1) When PVDD is less than 5.5 V, the voltage regulator that operates the analog circuitry does not have enough headroom to maintain the nominal 5.4-V internal voltage. The lack of headroom causes a direct reduction in gain (approximately –0.8 dB at 5 V and –1.74 dB at 4.5 V), but the device functions properly down to V_{PVDD} = 4.5 V.

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
t_{ACTIVE}	Shutdown to Active Time	From deassertion of SDZ (both pin and I^2C register bit) until the Class-D amplifier begins switching.		25		ms
t_{WAKE}	Wake Time	From the deassertion of SLEEP until the Class-D amplifier starts switching.		1		
t_{SLEEP}	Sleep Time	From the assertion of SLEEP until the Class-D amplifier stops switching.		t_{vrmp} + 1		
t_{MUTE}	Play to Mute Time	From the assertion of MUTE mode until the volume has ramped to the minimum.		t_{vrmp}		
t_{PLAY}	Un-Mute to Play Time	From the deassertion of MUTE until the volume has returned to its current setting.		t_{vrmp}		
t_{SD}	Active to Shutdown Time	From the assertion of SDZ (pin or I^2C register bit) until the Class-D amplifier stops switching.		t_{vrmp} + 1		
SERIAL AUDIO PORT						
t_{H_L}	Time high and low, BCLK, LRCLK, SDIN inputs		10			ns
t_{SU} t_{HLD}	Setup and hold time. LRCLK, SDIN input to BCLK edge.	Input t_{RISE} ≤ 1 ns, input t_{FALL} ≤ 1 ns			5	ns
		Input t_{RISE} ≤ 4 ns, input t_{FALL} ≤ 4 ns	8			
		Input t_{RISE} ≤ 8 ns, input t_{FALL} ≤ 8 ns	12			
t_{RISE}	Rise-time BCLK, LRCLK, SDIN inputs				8	ns
t_{FALL}	Fall-time BCLK, LRCLK, SDIN inputs				8	
I^2C CONTROL PORT						
t_{BUS}	Bus free time between start and stop conditions		1.3			µs
$t_{HOLD1(I2C)}$	Hold Time, SCL to SDA		80			ns
$t_{HOLD2(I2C)}$	Hold Time, start condition to SCL		0.6			µs
$t_{START(I2C)}$	I2C Startup Time after DVDD Power On Reset				12	ms
$t_{RISE(I2C)}$	Rise Time, SCL and SDA				300	ns
$t_{FALL(I2C)}$	Fall Time, SCL and SDA				300	ns
$t_{SU1(I2C)}$	Setup, SDA to SCL		100			ns
$t_{SU2(I2C)}$	Setup, SCL to start condition		0.6			µs
$t_{SU3(I2C)}$	Setup, SCL to stop condition		0.6			µs
$t_{W(H)}$	Required pulse duration, SCL "HIGH"		0.6			µs
$t_{W(L)}$	Required pulse duration, SCL "LOW"		1.3			µs
PROTECTION						
t_{FAULTZ}	Amplifier fault time-out period	DC detect error		650		ms
		OTE or OCE fault		1.3		s

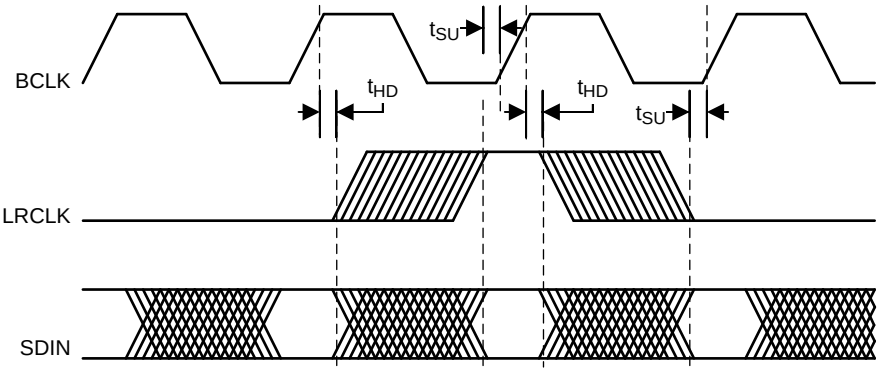


Figure 1. SAIF Timing

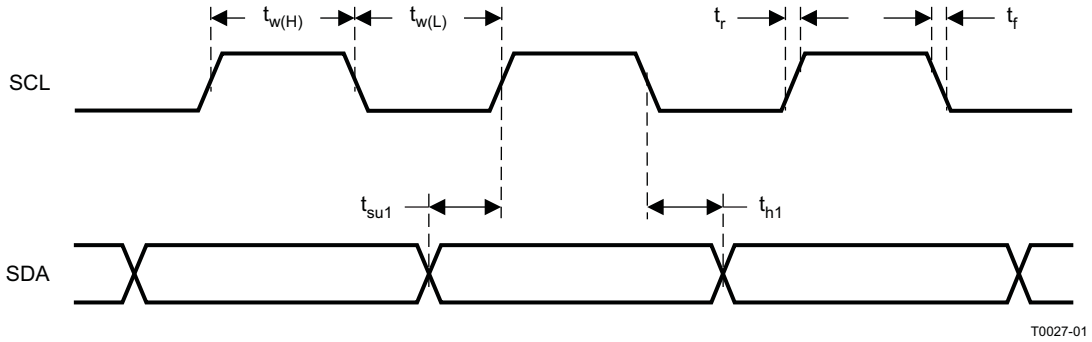


Figure 2. SCL and SDA Timing

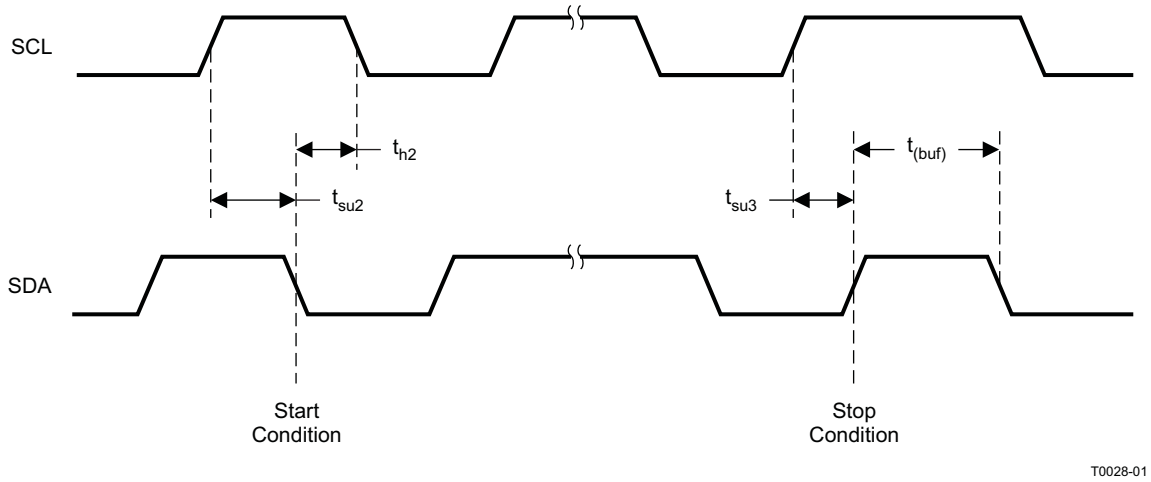


Figure 3. Start and Stop Conditions Timing

When SDZ is deasserted (and the device is not in sleep mode), the amplifier begins to switch after a period of t_{ACTIVE}. At this point, the volume ramps from –100 dB to the programmed digital volume control (DVC) setting at a rate of 0.5 dB every eight sample periods. Ramping the volume prevents audible artifacts that can occur if discontinuous volume changes are applied while audio is being played back. This period, t_{VRMP}, depends on the DVC setting and sample rate. Typical values for t_{VRMP} for a DVC of 0 dB are shown in *Timing Requirements*. Figure 4 illustrates mode timing.

The time to enter or exit sleep or mute and the time to enter shudown are dominated by t_{VRMP}. Table 1 lists the timing parameters based on t_{VRMP}.

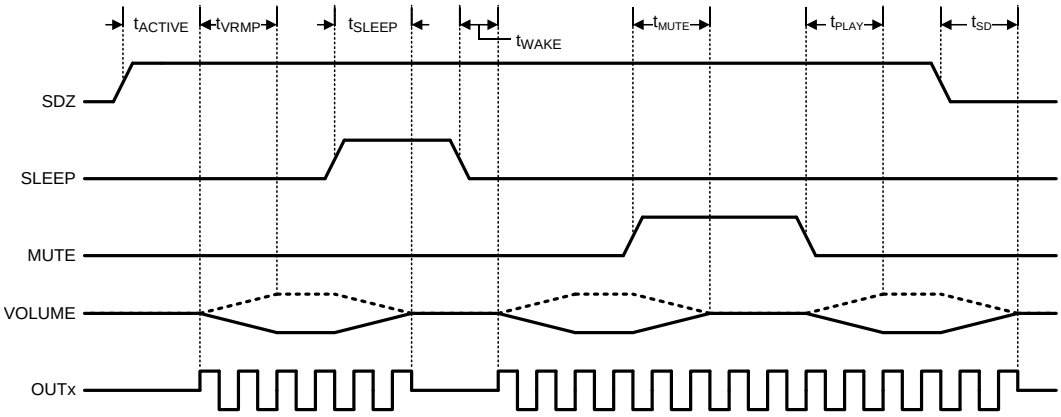


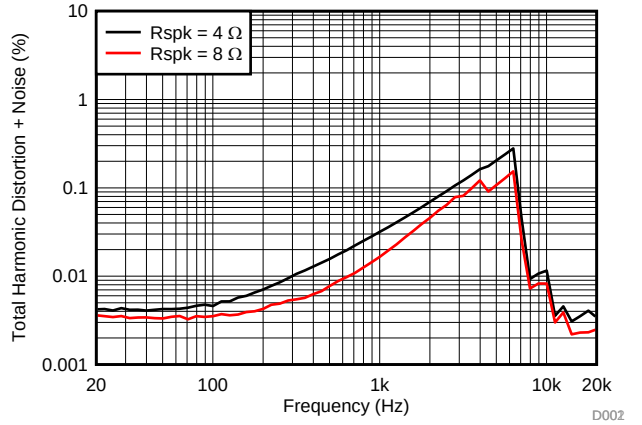
Figure 4. Mode Timing

Table 1. Typical DVC Ramp Times

SAMPLE RATE (kHZ)	RAMP TIMES (t_{VRAMP}) FROM –100 dB to 0 dB (ms)
44.1	36.3
48	33.3
88.2	18.1
96	16.7

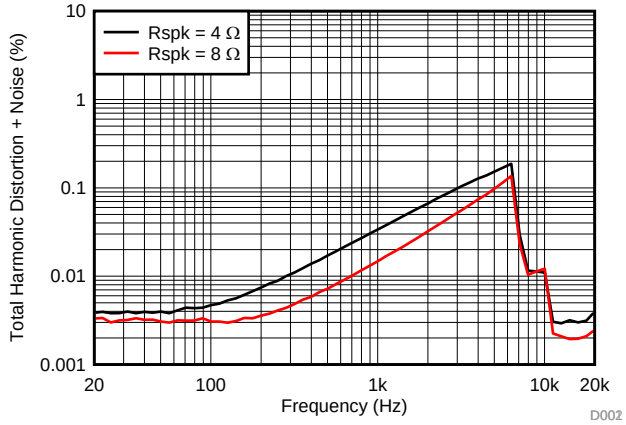
6.7 Typical Characteristics

T_A = 25ºC, $V_{(PVDD)}$ = 15 V, $V_{(DVDD)}$ = 3.3 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_s = 48 kHz, $f_{(PWM)}$ = 768 kHz, Gain = 20.7 dBV, SDZ = 1, Measured with an Audio Precision SYS-2722 High-Performance Audio Analyzer and using a 15-µH, 0.68-µF reconstruction filter at the device output.



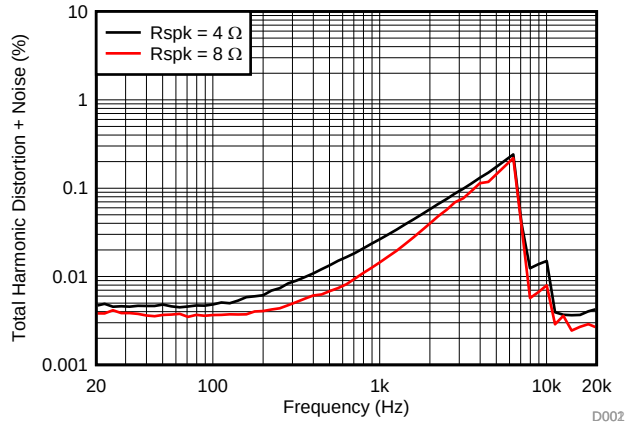
$V_{(PVDD)}$ = 7.2 V P_{OUT} = 1 W $f_{(PWM)}$ = 384 kHz

Figure 5. THD+N vs Frequency



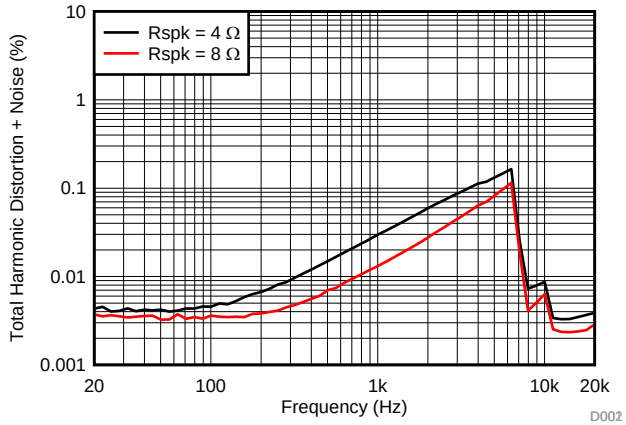
$V_{(PVDD)}$ = 7.2 V P_{OUT} = 1 W

Figure 6. THD+N vs Frequency



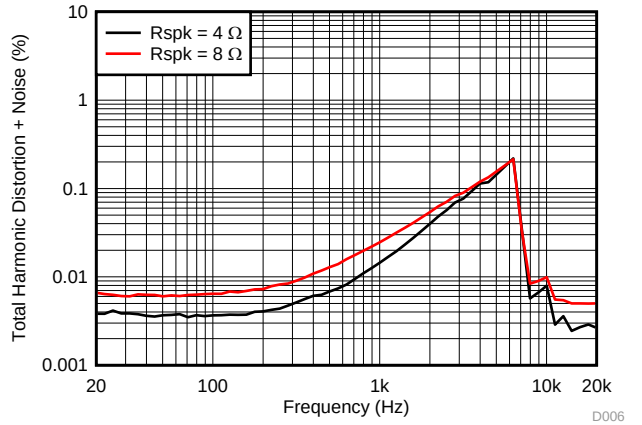
$V_{(PVDD)}$ = 12 V P_{OUT} = 1 W $f_{(PWM)}$ = 384 kHz

Figure 7. THD+N vs Frequency



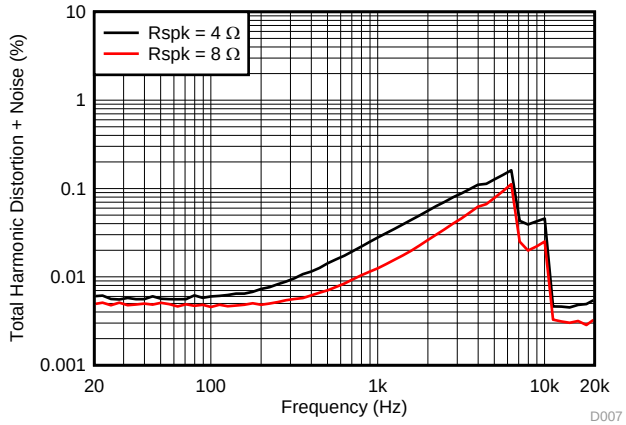
$V_{(PVDD)}$ = 12 V P_{OUT} = 1 W

Figure 8. THD+N vs Frequency



$V_{(PVDD)}$ = 15 V P_{OUT} = 1 W $f_{(PWM)}$ = 384 kHz

Figure 9. THD+N vs Frequency

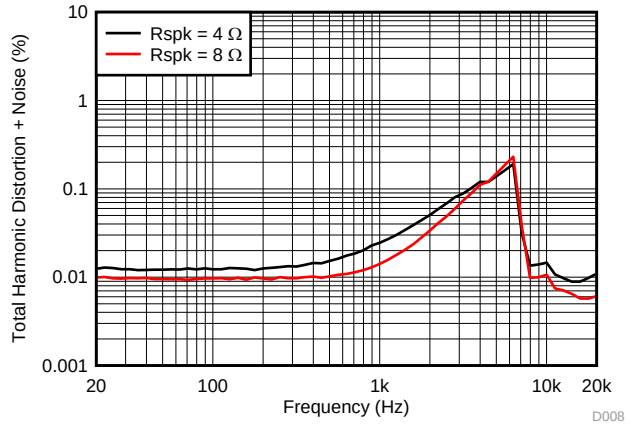


$V_{(PVDD)}$ = 15 V P_{OUT} = 1 W

Figure 10. THD+N vs Frequency

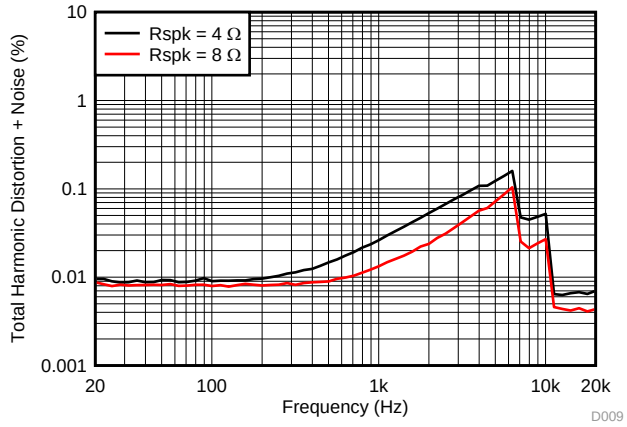
Typical Characteristics (continued)

T_A = 25ºC, $V_{(PVDD)}$ = 15 V, $V_{(DVDD)}$ = 3.3 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_s = 48 kHz, $f_{(PWM)}$ = 768 kHz, Gain = 20.7 dBV, SDZ = 1, Measured with an Audio Precision SYS-2722 High-Performance Audio Analyzer and using a 15-µH, 0.68-µF reconstruction filter at the device output.



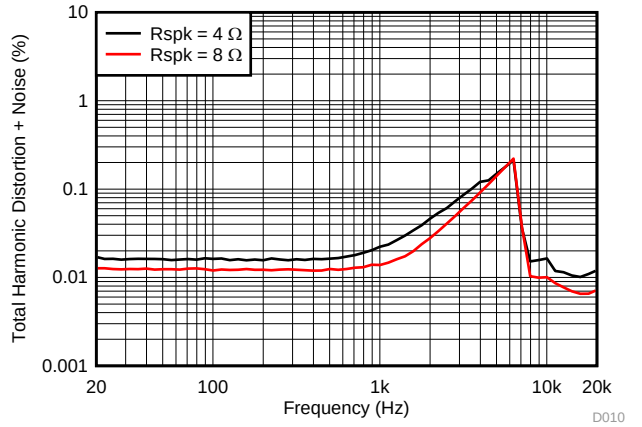
$V_{(PVDD)}$ = 19 V P_{OUT} = 1 W $f_{(PWM)}$ = 384 kHz

Figure 11. THD+N vs Frequency



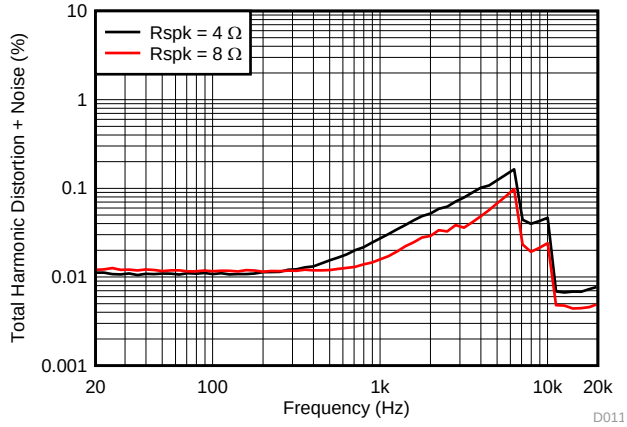
$V_{(PVDD)}$ = 19 V P_{OUT} = 1 W

Figure 12. THD+N vs Frequency



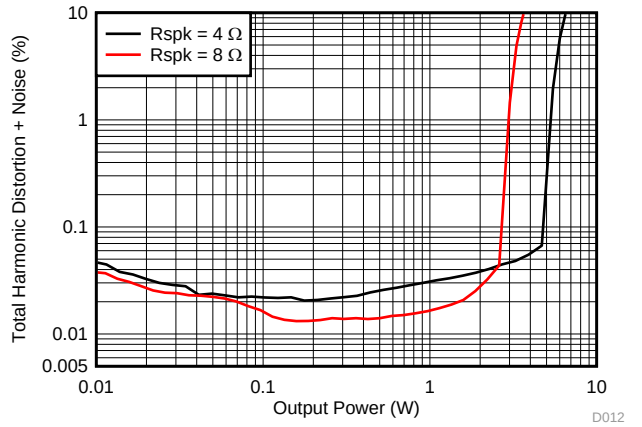
$V_{(PVDD)}$ = 24 V P_{OUT} = 1 W $f_{(PWM)}$ = 384 kHz

Figure 13. THD+N vs Frequency



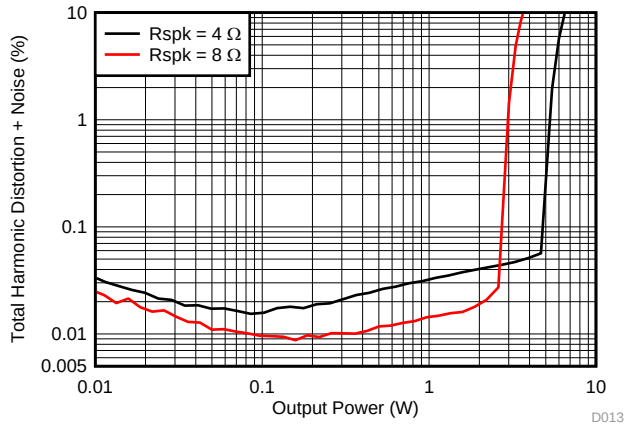
$V_{(PVDD)}$ = 24 V P_{OUT} = 1 W

Figure 14. THD+N vs Frequency



$V_{(PVDD)}$ = 7.2 V $f_{(PWM)}$ = 384 kHz

Figure 15. THD+N vs Output Power

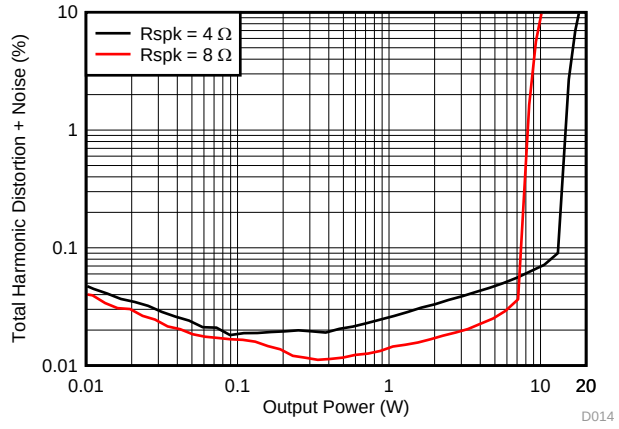


$V_{(PVDD)}$ = 7.2 V

Figure 16. THD+N vs Output Power

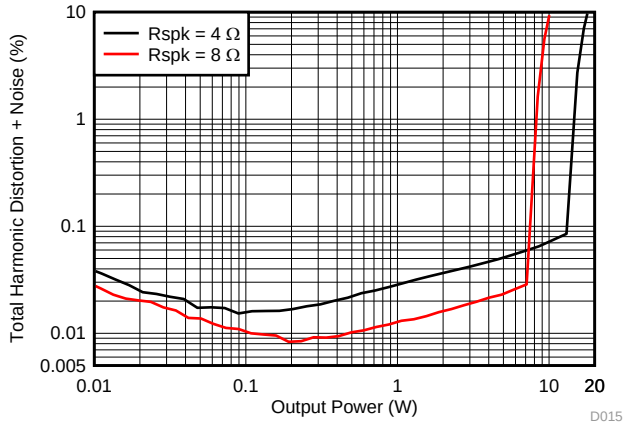
Typical Characteristics (continued)

T_A = 25ºC, $V_{(PVDD)}$ = 15 V, $V_{(DVDD)}$ = 3.3 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_s = 48 kHz, $f_{(PWM)}$ = 768 kHz, Gain = 20.7 dBV, SDZ = 1, Measured with an Audio Precision SYS-2722 High-Performance Audio Analyzer and using a 15-µH, 0.68-µF reconstruction filter at the device output.



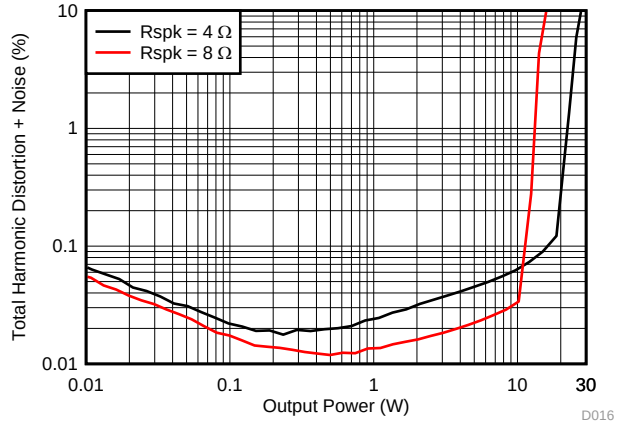
$V_{(PVDD)}$ = 12 V $f_{(PWM)}$ = 384 kHz

Figure 17. THD+N vs Output Power



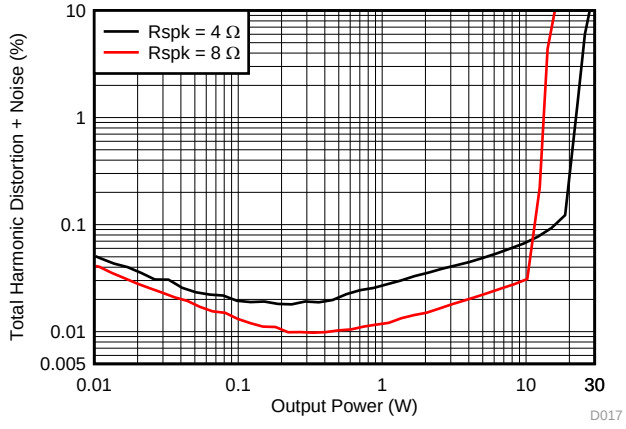
$V_{(PVDD)}$ = 12 V

Figure 18. THD+N vs Output Power



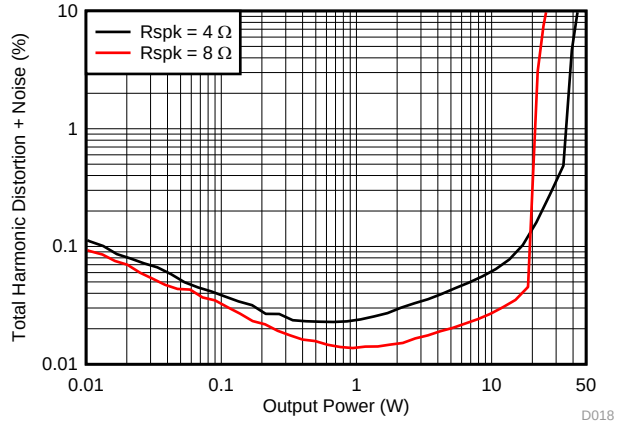
$V_{(PVDD)}$ = 15 V $f_{(PWM)}$ = 384 kHz

Figure 19. THD+N vs Output Power



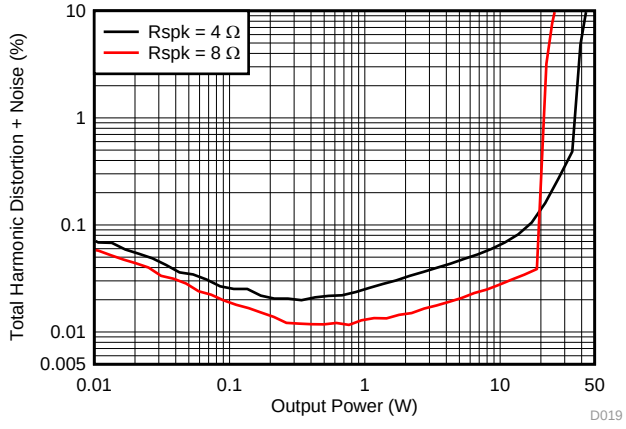
$V_{(PVDD)}$ = 15 V

Figure 20. THD+N vs Output Power



$V_{(PVDD)}$ = 19 V $f_{(PWM)}$ = 384 kHz

Figure 21. THD+N vs Output Power

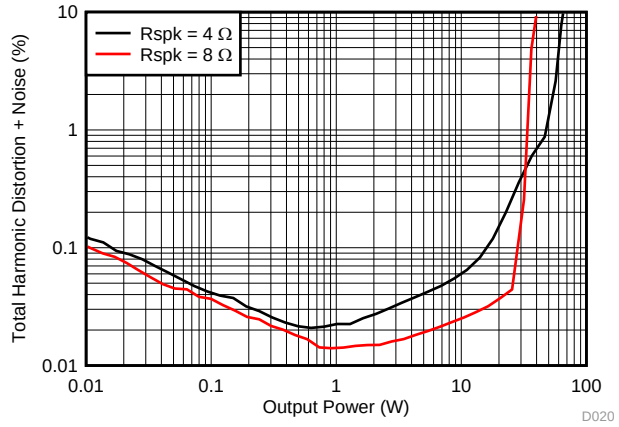


$V_{(PVDD)}$ = 19 V

Figure 22. THD+N vs Output Power

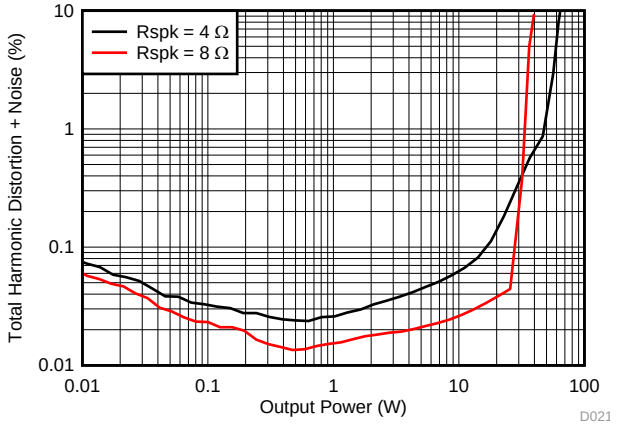
Typical Characteristics (continued)

T_A = 25ºC, $V_{(PVDD)}$ = 15 V, $V_{(DVDD)}$ = 3.3 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_s = 48 kHz, $f_{(PWM)}$ = 768 kHz, Gain = 20.7 dBV, SDZ = 1, Measured with an Audio Precision SYS-2722 High-Performance Audio Analyzer and using a 15-µH, 0.68-µF reconstruction filter at the device output.



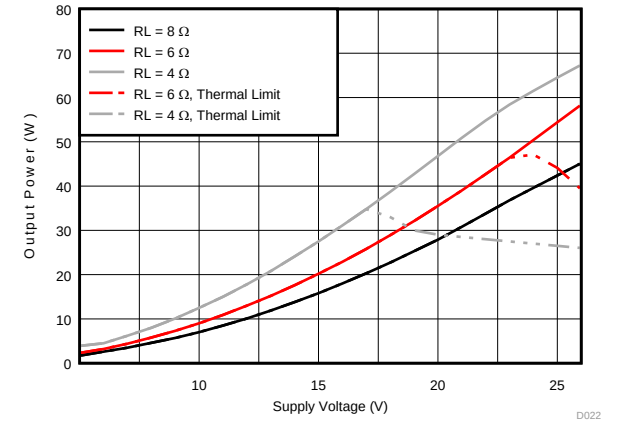
$V_{(PVDD)}$ = 24 V $f_{(PWM)}$ = 384 kHz

Figure 23. THD+N vs Output Power



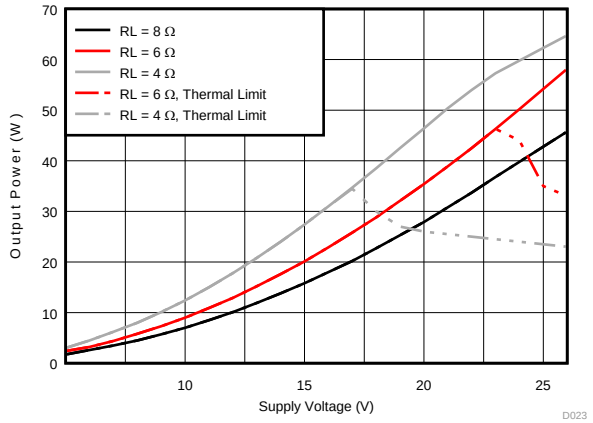
$V_{(PVDD)}$ = 24 V Gain = 20.7 dBV

Figure 24. THD+N vs Output Power



Analog Gain = Setting 11 $f_{(PWM)}$ = 384 kHz

Figure 25. Output Power vs Supply Voltage

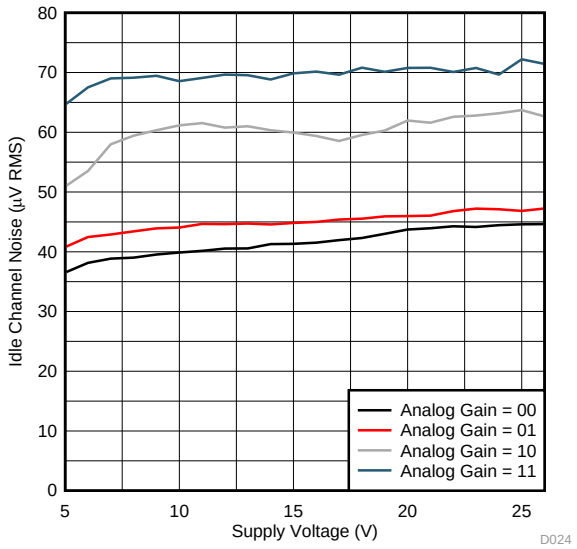


Analog Gain = Setting 11

Figure 26. Output Power vs Supply Voltage

Typical Characteristics (continued)

T_A = 25ºC, $V_{(PVDD)}$ = 15 V, $V_{(DVDD)}$ = 3.3 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_s = 48 kHz, $f_{(PWM)}$ = 768 kHz, Gain = 20.7 dBV, SDZ = 1, Measured with an Audio Precision SYS-2722 High-Performance Audio Analyzer and using a 15-µH, 0.68-µF reconstruction filter at the device output.



$f_{(PWM)}$ = 384 kHz

Figure 27. A-Weighted Idle Channel Noise vs Supply Voltage

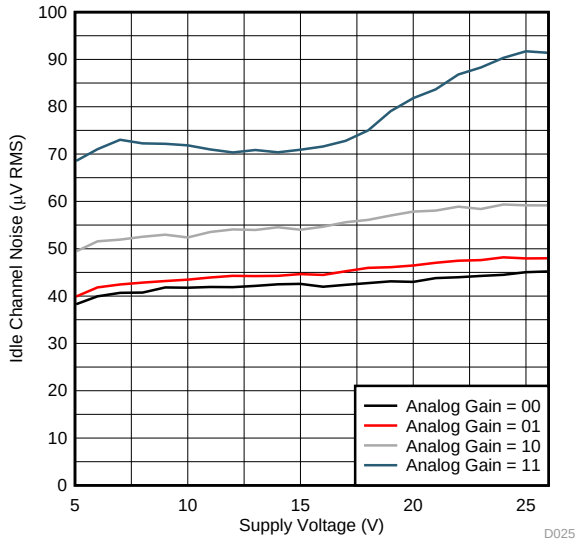
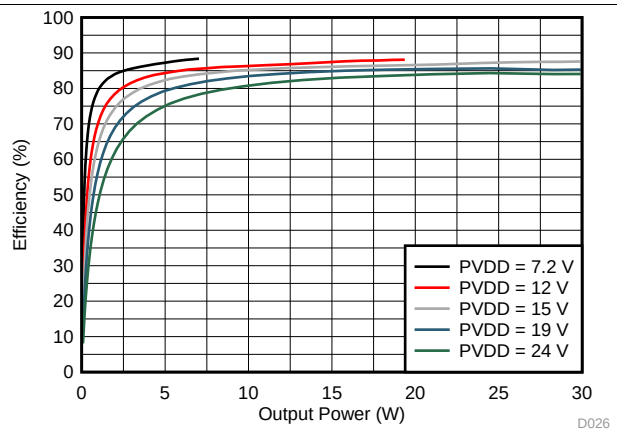
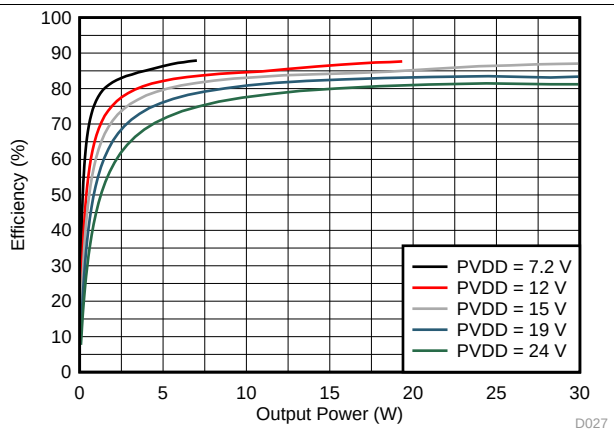


Figure 28. Efficiency vs Output Power



R_L = 4 Ω $f_{(PWM)}$ = 384 kHz

Figure 29. Efficiency vs Output Power

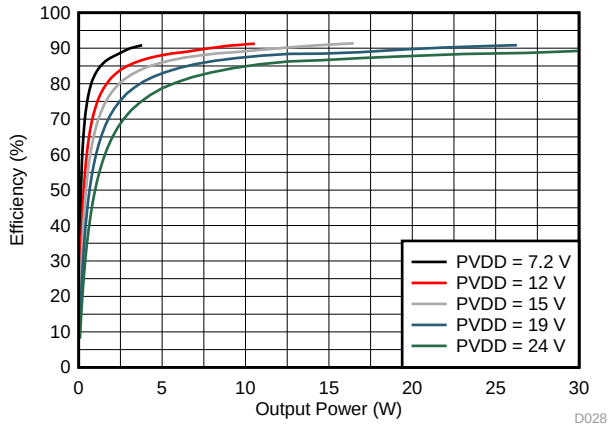


R_L = 4 Ω

Figure 30. Efficiency vs Output Power

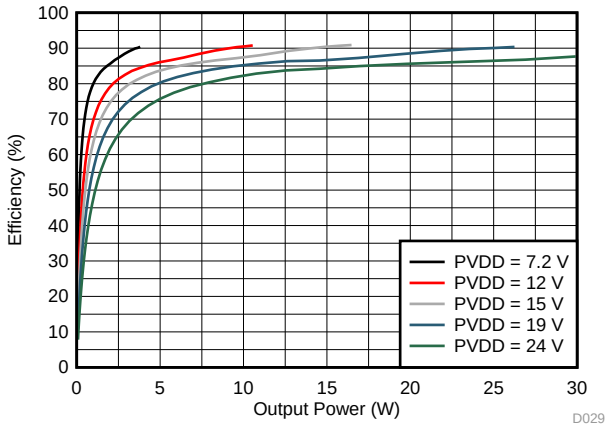
Typical Characteristics (continued)

T_A = 25ºC, $V_{(PVDD)}$ = 15 V, $V_{(DVDD)}$ = 3.3 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_s = 48 kHz, $f_{(PWM)}$ = 768 kHz, Gain = 20.7 dBV, SDZ = 1, Measured with an Audio Precision SYS-2722 High-Performance Audio Analyzer and using a 15-µH, 0.68-µF reconstruction filter at the device output.



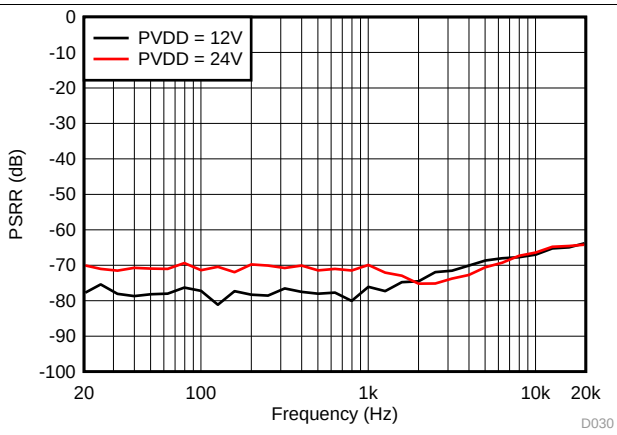
R_L = 8 Ω $f_{(PWM)}$ = 384 kHz

Figure 31. Efficiency vs Output Power



R_L = 8 Ω

Figure 32. Efficiency vs Output Power



$f_{(PWM)}$ = 384 kHz

Figure 33. PVDD PSRR vs Frequency

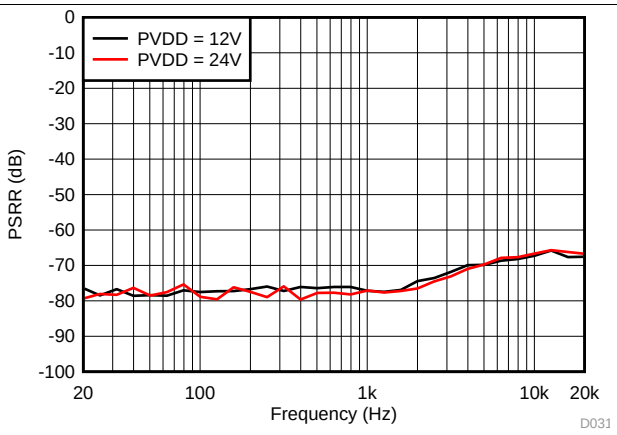
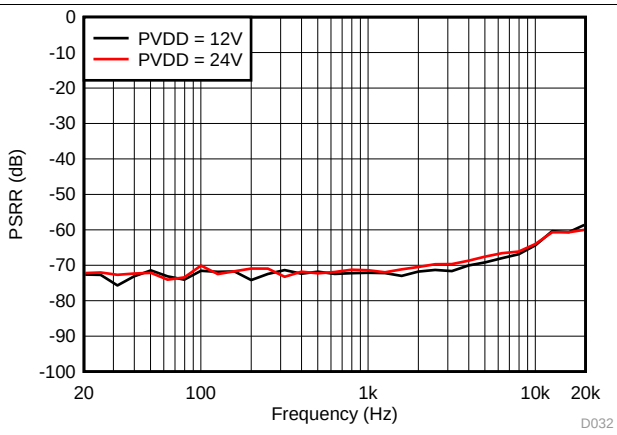


Figure 34. PVDD PSRR vs Frequency



$f_{(PWM)}$ = 384 kHz

Figure 35. DVDD PSRR vs Frequency

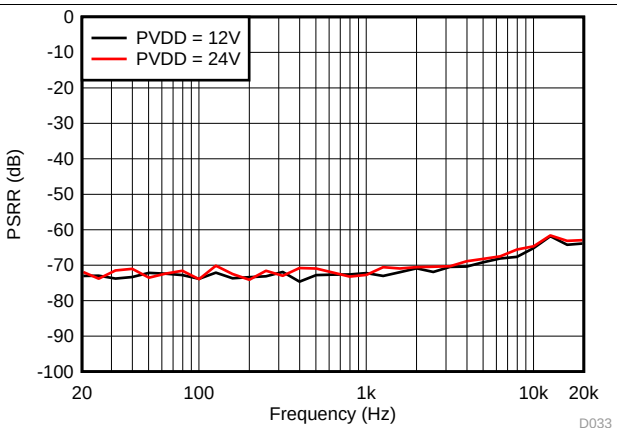


Figure 36. DVDD PSRR vs Frequency

Typical Characteristics (continued)

T_A = 25ºC, $V_{(PVDD)}$ = 15 V, $V_{(DVDD)}$ = 3.3 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_s = 48 kHz, $f_{(PWM)}$ = 768 kHz, Gain = 20.7 dBV, SDZ = 1, Measured with an Audio Precision SYS-2722 High-Performance Audio Analyzer and using a 15-µH, 0.68-µF reconstruction filter at the device output.

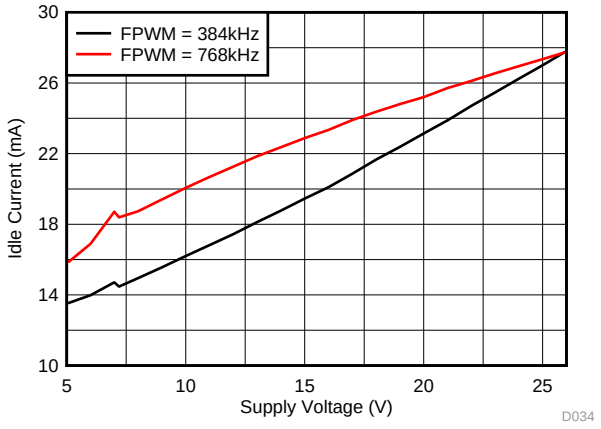


Figure 37. Supply Idle Current vs PVDD

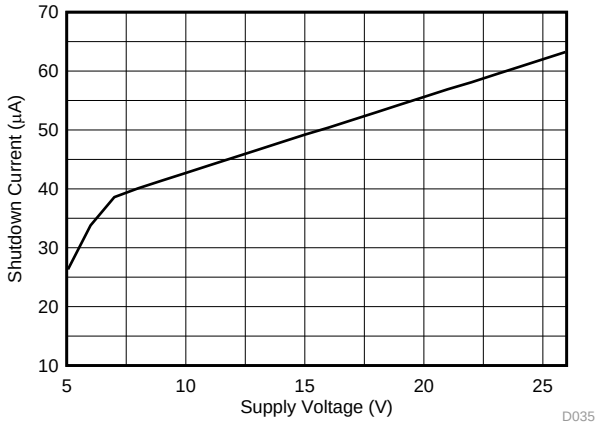


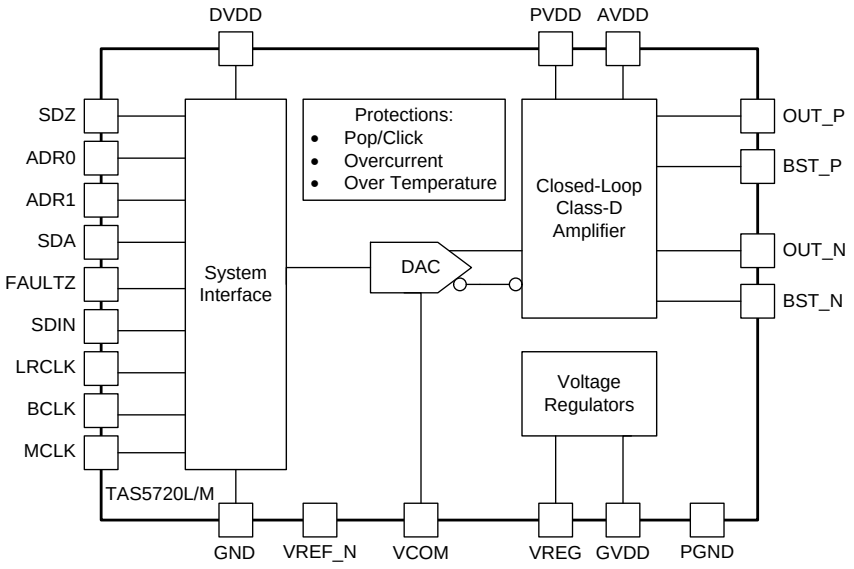
Figure 38. Shutdown Current vs PVDD

7 Detailed Description

7.1 Overview

The TAS5720L/M device is a high-efficiency mono Class-D audio power amplifier optimized for high-transient power capability to utilize the dynamic power headroom of small loudspeakers. It's capable of delivering more than 15-W continuously into a 4-Ω speaker.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adjustable I²C Address

The TAS5720L/M device has two address pins, which allow up to 8 I²C addressable devices to share a common TDM bus. Table 2 lists each I²C *Device ID* setting.

NOTE

The I²C Device ID is the 7 most significant bits of the 8-bit address transaction on the bus (with the read/write bit being the least significant bit). For example, a Device ID of 0x6C would be read as 0xD8 when the read/write bit is 0.

Table 2. I²C Device Identifier (ID) Generation

ADR1	ADR0	I2C_DEV_ID	DEFAULT TDM SLOT
Short to GND	Short to GND	0x6C	0
	22-kΩ to GND	0x6D	1
	22-kΩ to DVDD	0x6E	2
	Short to DVDD	0x6F	3
22-kΩ to GND	Short to GND	0x70	4
	22-kΩ to GND	0x71	5
	22-kΩ to DVDD	0x72	6
	Short to DVDD	0x73	7

Use a 22-kΩ resistor with a 5% (or better) tolerance to operate as a pull-up or pull-down resistor. By default, the device uses the TDM time slot equal to the offset from the base I²C Device ID (see Table 2). The TDM slot can also be manually configured by setting the TDM_CFG_SRC bit high (bit 6, reg 0x02) and programming the TDM_SLOT_SELECT[2:0] bits to the desired slot (bits 0-2, reg 0x03).

For 2-channel, I²S operation, TDM slots 0 and 1 correspond to right and left channels respectively. For left and right justified formats, TDM slots 0 and 1 correspond to left and right channels respectively.

7.3.2 I²C Interface

The TAS5720L/M device has a bidirectional I²C interface that is compatible with the Inter-Integrated Circuit (I²C) bus protocol and supports both 100-kHz and 400-kHz data transfer rates. This slave-only device does not support a multimaster bus environment or wait-state insertion. The control interface is used to program the registers of the device and to read device status.

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most-significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock (SCL) is "HIGH" to indicate start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. The conditions are shown in Figure 39. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The TAS5720L/M device holds SDA "LOW" during the acknowledge clock period to indicate an acknowledgment. When this hold occurs, the master transmits the next byte of the sequence. All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pull-up resistor must be used for the SDA and SCL signals to set the "HIGH" level for the bus.

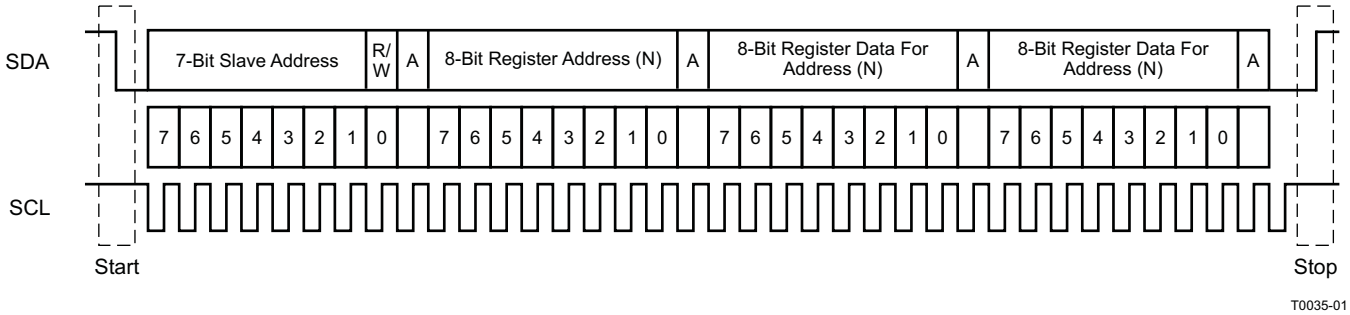


Figure 39. Typical I²C Timing Sequence

Any number of bytes can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 39.

7.3.2.1 Writing to the I²C Interface

As shown Figure 40, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C bit and the read/write bit. The read/write bit determines the direction of the data transfer. For a data-write transfer, the read/write bit is a 0. After receiving the correct I²C bit and the read/write bit, the TAS5720L/M device responds with an acknowledge bit. Next, the master transmits the address byte corresponding to the TAS5720L/M device register being accessed. After receiving the address byte, the TAS5720L/M device again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5720L/M device again responds with an acknowledge bit. Lastly, the master device transmits a stop condition to complete the single-byte data-write transfer.

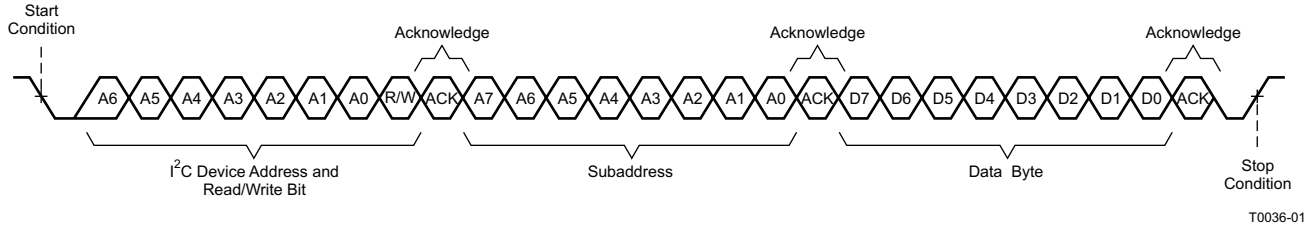


Figure 40. Single Byte Write Transfer Timing

A multi-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted as shown in Figure 41. After receiving each data byte, the TAS5720L/M device responds with an acknowledge bit. Sequential data bytes are written to sequential addresses.

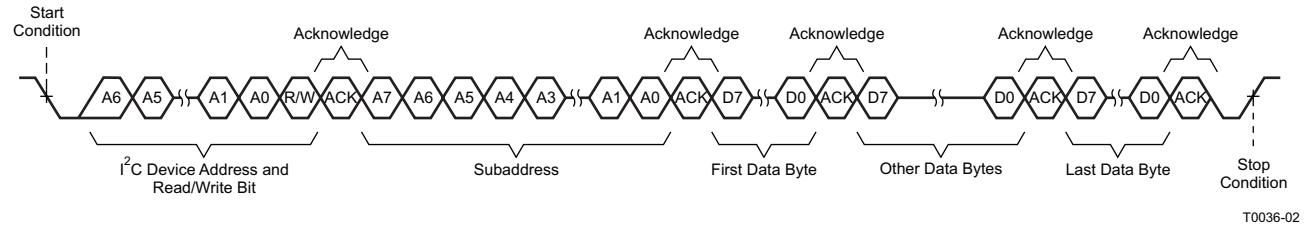


Figure 41. Multi-Byte Write Transfer Timing

7.3.2.2 Reading from the I²C Interface

As shown in Figure 41, a data-read transfer begins with the master device transmitting a start condition, followed by the I² device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal register to be read. As a result, the read/write bit becomes a 0. After receiving the TAS5720L/M device address and the read/write bit, TAS5720L/M device responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the TAS5720L/M device address and the read/write bit again. This time, the read/write bit becomes a 1, indicating a read transfer. After receiving the address and the read/write bit, the TAS5720L/M device again responds with an acknowledge bit. Next, the TAS5720L/M device transmits the data byte from the register being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the data-read transfer.

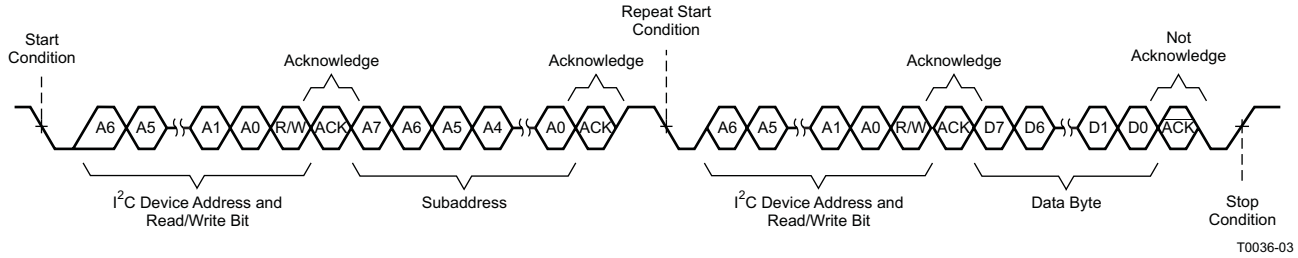


Figure 42. Single Byte Read Transfer Timing

A multiple-byte data read transfer is identical to a single-byte data read transfer except that multiple data bytes are transmitted by the TAS5720L/M to the master device as shown Figure 43. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

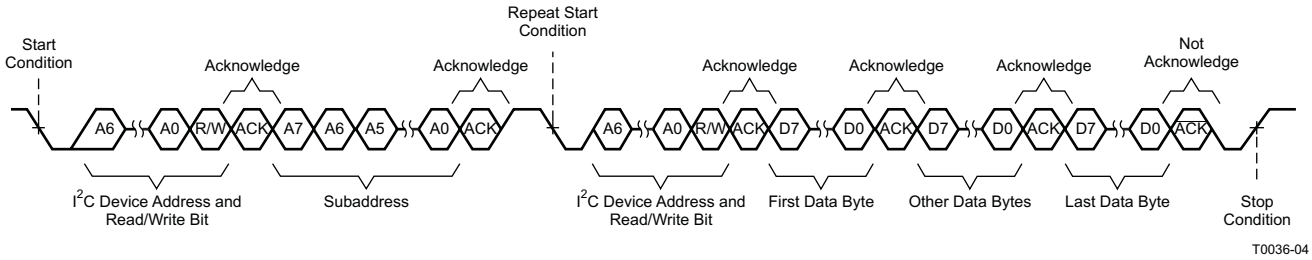


Figure 43. Multi-Byte Read Transfer Timing

7.3.3 Serial Audio Interface (SAIF)

The TAS5720L/M device SAIF supports a variety of standard stereo serial audio formats including I²S, left-justifiedand Right Justified. The device also supports a time division multiplexed (TDM) format that is capable of transporting up to 8 channels of audio data on a single bus. LRCLK and SDIN are sampled on the rising edge of BCLK.

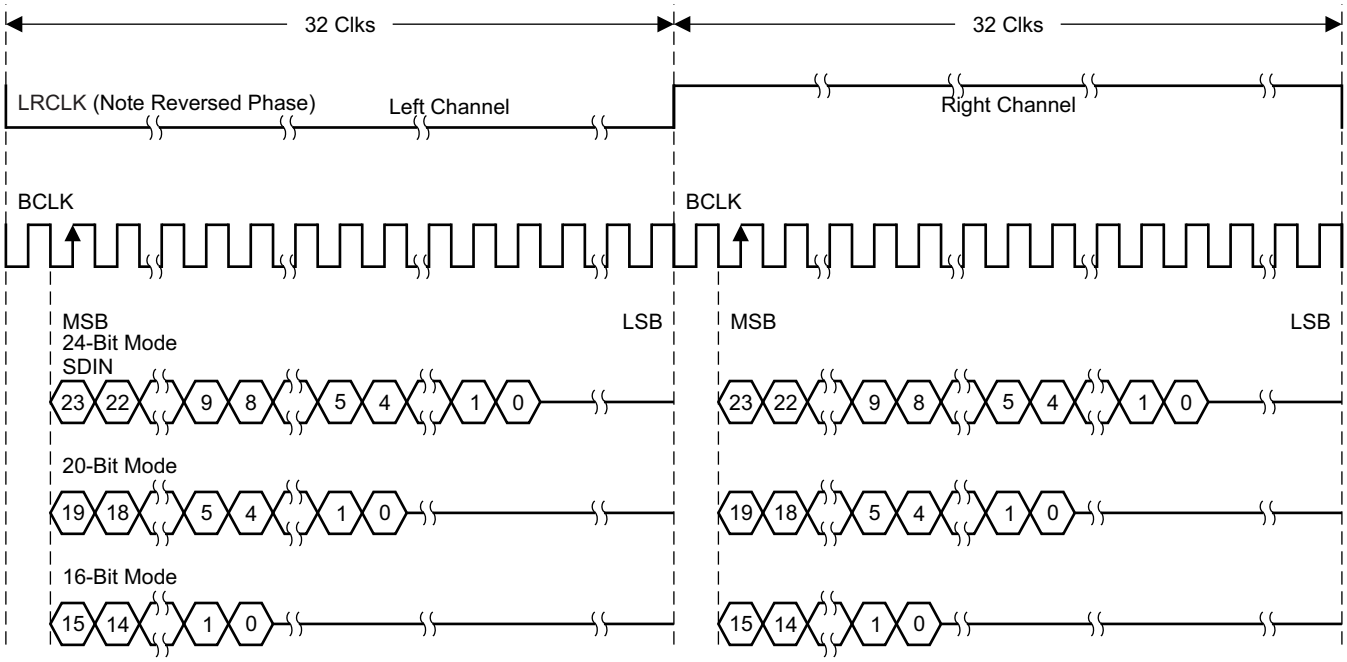
For the stereo formats (I²S, left-justified and right-justified), the TAS5720L/M device supports BCLK to LRCLK ratios of 32, 48 and 64. If the BCLK to LRCLK ratio is 64, MCLK can be tied directly to BCLK. Otherwise MCLK must be driven externally. The valid MCLK to LRCLK ratios are 64, 128, 256 and 512 as long as the frequency of MCLK is 25MHz or less.

For TDM operation, the TAS5720L/M device supports 4 or 8 channels for single speed (44.1/48 kHz) and double speed (88.2/96 kHz) sample rates. Each channel occupies a 32-bit time slot, therefore valid BCLK to LRCLK ratios are 128 and 256. MCLK can be tied to BCLK for all TDM modes or driven externally. If MCLK is driven externally, the MCLK to LRCLK ratio should be 64, 128, 256 or 512 and MCLK should be no faster than 25MHz.

The TAS5720L/M device selects the channel for playback based on either the I²C base address offset or based on a dedicated time slot selection register. See the *Adjustable I²C Address* section for more information.

7.3.3.1 Stereo I²S Format Timing

Figure 44 illustrates the timing of the stereo I²S format with 64 BCLKs per LRCLK. Two's complement data is transmitted MSB to LSB with the left channel word beginning one BCLK after the falling edge of LRCLK and the right channel beginning one BCLK after the rising edge of LRCLK. Because data is MSB aligned to the beginning of word transmission, data precision does not be configured. Set the SAIF_FORMAT[2:0] register bits to I²S (register 0x02, bits 2:0=3'b100).

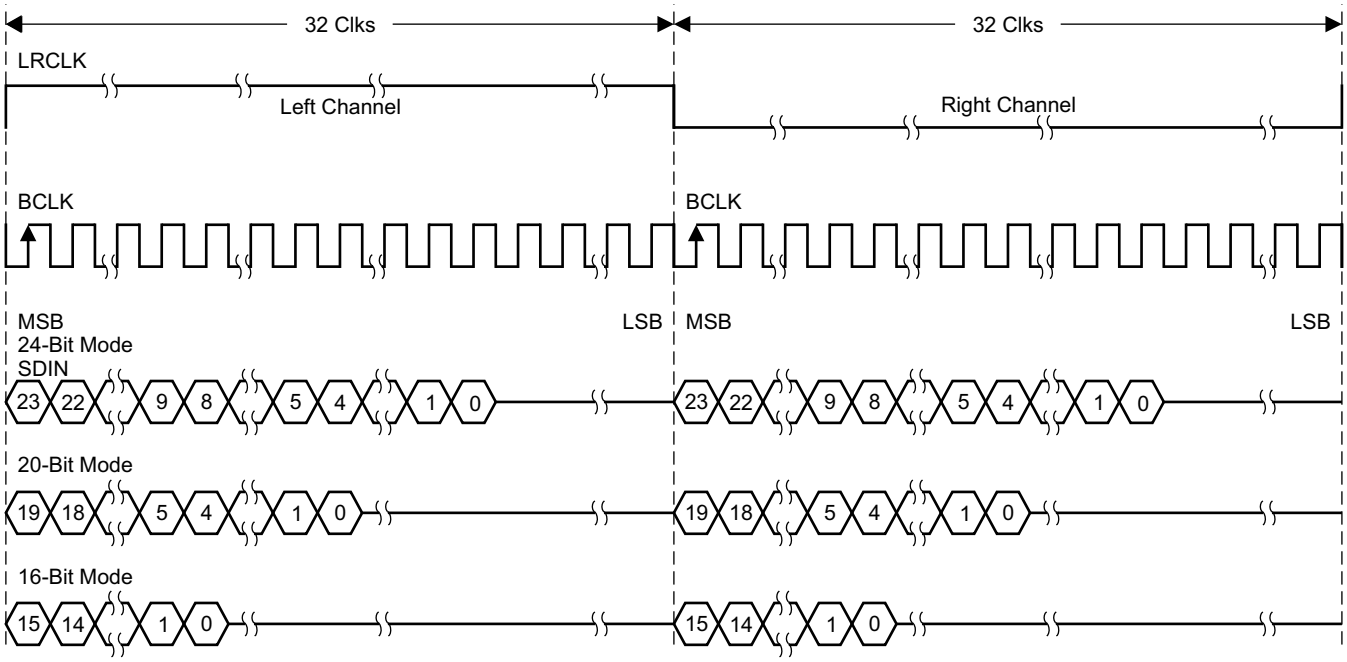


A. Data presented in two's-complement form with most significant bit (MSB) first.

Figure 44. I²S 64-f_{SW} Format

7.3.3.2 Stereo Left-Justified Format Timing

The stereo left justified format is very similar to the I^2S format timing, except the data word begins transmission at the same cycle that LRCLK toggles (when it is shifted by one bit from I^2S). The phase of LRCLK is also opposite of I^2S. The left channel begins transmission when LRCLK transitions from low to high and the right channel begins transmission when LRCLK transitions from high-to-low. Set the SAIF_FORMAT[2:0] register bits to left-justified (register 0x02, bits 2:0=3'b101).The timing is illustrated in Figure 45.



A. Data presented in two's-complement form with most significant bit (MSB) first.

Figure 45. Left-Justified 64-f_{SW} Format

7.3.3.3 Stereo Right-Justified Format Timing

The stereo right justified format aligns the LSB of left channel data to the high to low transition of LRCLK and the LSB of the right channel data to the low to high transition of LRCLK. To insure data is received correctly, the SAIF must be configured for the proper data precision. The TAS5720L/M supports 16, 18, 20 and 24-bit data precision in right justified format. Set the SAIF_FORMAT[2:0] register bits (register 0x02, bits 2:0) to the appropriate right-justifiedsetting based on bit precision (value=3'b000 for 24-bit, 3'b001 for 20-bit, 3'b010 for 18-bit and 3'b011 for 16-bit). The timing is illustrated in Figure 46.

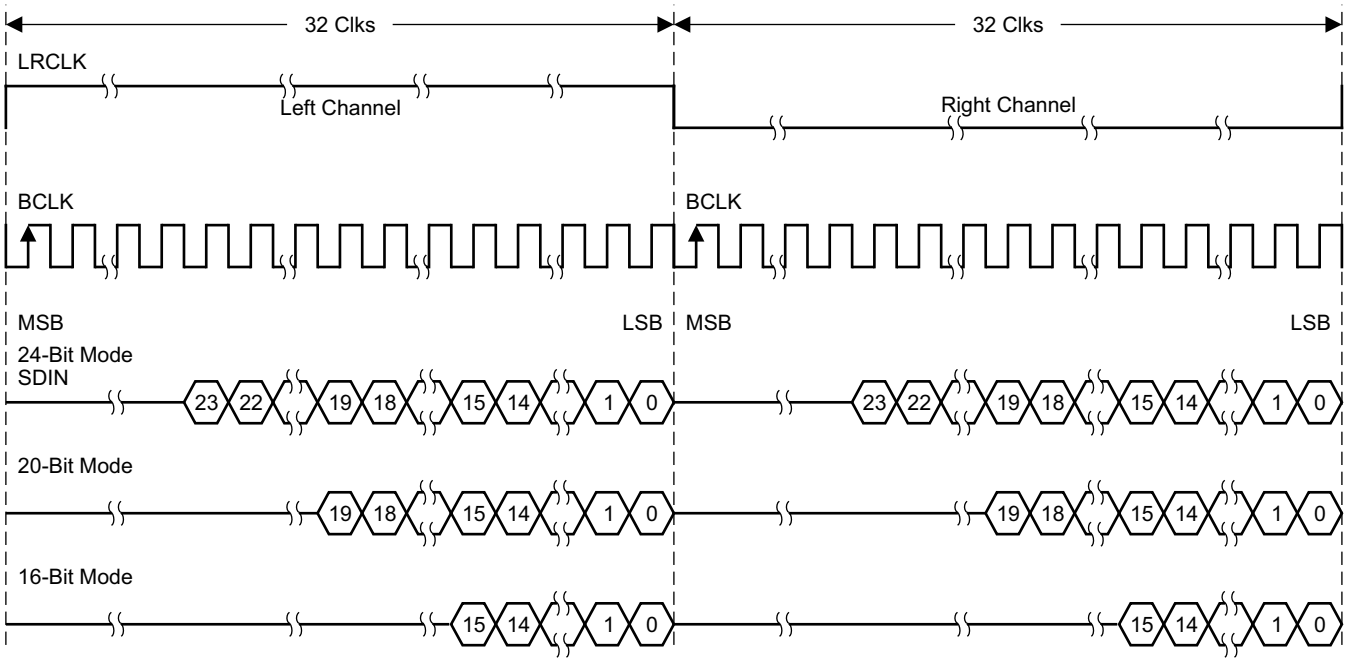


Figure 46. Right-Justified 64-f_{SW} Format

7.3.3.4 TDM Format Timing

A TDM frame begins with the low to high transition of LRCLK. As long as LRCLK is high for at least one BCLK period and low for one BCLK period, duty cycle is irrelevent. The SAIF automatically detects the number of time slots as long as valid BCLK to LRCLK ratios are utilized (see *Serial Audio Interface (SAIF)*).

For I^2S aligned TDM operation (when time slot 0 begins one clock cycle after the low to high transition of LRCLK, set SAIF_FORMAT[2:0] register bits to I2S (register 0x02, bits 2:0=3'b100). Data is MSB aligned within the 32-bit time slots, therefore data precision is not required to be configured. The TDM format timing is illustrated in Figure 47.

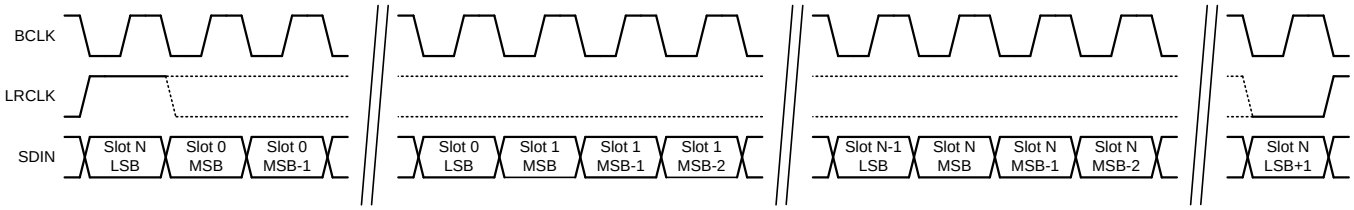


Figure 47. TDM I^2S Format

For left-justifiedTDM operation (when time slot 0 begins the cycle LRCLK transitions from low to high), SAIF_FORMAT[2:0] register bits to left-justified(register 0x02, bits 2:0=3'b101). As with I2S, data is MSB aligned. The timing is illustrated in Figure 48.

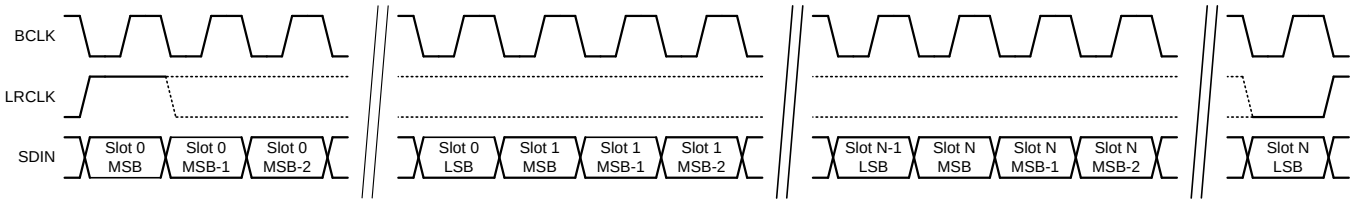


Figure 48. TDM Left- and Right-Justified Format

For right-justified TDM operation (when time slot 0 begins the cycle LRCLK transitions from low to high), data is LSB aligned to the 32-bit time slot. As with stereo right-justified formats, the TAS5720L/M must have the data precision configured. Set the SAIF_FORMAT[2:0] register bits (register 0x02, bits 2:0) to the appropriate right-justified setting based on bit precision (value=3'b000 for 24-bit, 3'b001 for 20-bit, 3'b010 for 18-bit and 3'b011 for 16-bit). The timing shown in Figure 48 is the same as left-justified TDM, with the data LSB aligned.

7.3.4 Audio Signal Path

Figure 49 illustrates the audio signal flow from the TDM SAIF to the speaker.

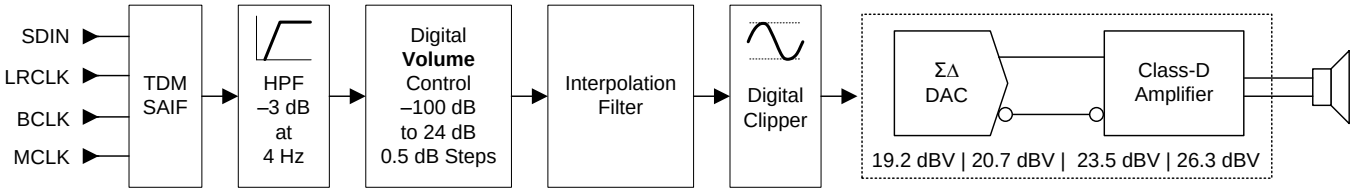


Figure 49. Audio Signal Path

7.3.4.1 High-Pass Filter (HPF)

Excessive DC in audio content can damage loudspeakers, therefore the amplifier employs a DC detect circuit that shutdowns the power stage and issue a latching fault if this condition occurs. A high-pass filter is provided in the TAS5720L/M device to remove DC from incoming audio data to prevent this from occurring. Table 3 shows the high-pass, –3 dB corner frequencies for each sample rate. The filter can be bypassed by writing a 1 into bit 7 of register 0x02.

Table 3. High-Pass Filter –3 dB Corner Frequencies by Sample Rate

SAMPLE RATE (kHZ)	-3dB CORNER FREQUENCY (Hz)
44.1	3.675
48.0	4.000
88.2	7.350
96.0	8.000

7.3.4.2 Amplifier Analog Gain and Digital Volume Control

The gain from TDM SAIF to speaker is controlled by setting the amplifier's analog gain and digital volume control. Amplifier analog gain settings are presented as the output level in dBV (dB relative to 1 Vrms) with a full scale serial audio input (0 dBFS) and the digital volume control set to 0 dB. These levels might not be achievable because of analog clipping in the amplifier, therefore they should be used to convey gain only.

Table 4 outlines each gain setting expressed in dBV and V_{PK}.

Table 4. Amplifier Gain Settings

ANALOG_GAIN {1:0} SETTING	FULL SCALE OUTPUT	
	dBV	V_{PEAK}
00	19.2	12.9
01	20.7	15.3
10	23.5	21.2
11	26.3	29.2

Equation 1 calculates the amplifiers output voltage.

$$V_{amp} = Input + A_{dvc} + A_{amp} \text{ dBV} \quad (1)$$

where

- V_{AMP} is the amplifier output voltage in dBV
- Input is the digital input amplitude in dB with respect to 0 dBFS
- A_{DVC} is the digital volume control setting, –100 dB to 24dB in 0.5-dB steps
- A_{AMP} is the amplifier analog gain setting (19.2, 20.7, 23.5, or 26.3) in dBV

Clipping in the digital domain occurs if the input level (in dB relative to 0 dBFS) plus the digital volume control setting (in dB) are greater than 0 dB. The signal path has approximately 0.5 dB of headroom, but TI does not recommend utilizing it.

The digital volume control can be adjusted from –100 dB to 24 dB in 0.5-dB steps. Equation 2 calculates the 8-bit volume control register setting at address 0x04.

$$DVC_{value} = 0xCF + \frac{A_{dvc}}{0.5} \quad (2)$$

For example, digital volume settings of 0 dB, 24 dB and –100 dB map to 0xCF, 0xFF and 0x07 respectively. Values below 0x07 are equivalent to mute (the amplifier continues to switch with no audio).When a change in digital volume control occurs, the device ramps the volume to the new setting in 0.5 dB steps after every 8 audio samples to ensure smooth transitions in volume.

The Class-D amplifier uses a closed-loop architecture, therefore the gain does not depend on the supply input (V_{PVDD}). The approximate threshold for the onset of analog clipping is calculated in Equation 3.

$$V_{PK(max,preclip)} = V_{PVDD} \left(\frac{R_L}{2 \times R_{DS(on)} + R_{interconnect} + R_L} \right) V \quad (3)$$

where

- $V_{PK(max,preclip)}$ is the maximum peak unclipped output voltage in V
- V_{PVDD} is the power supply voltage
- R_L is the speaker load in Ω
- $R_{interconnect}$ is the additional resistance in the PCB (such as cabling and filters) in Ω
- $R_{DS(on)}$ is the power stage total on resistance (FET+bonding+packaging) in Ω

The effective on-resistance for this device (including FETs, bonding and packaging leads) is approximately 150 mΩ at room temperature and increasex by approximately 1.6 times over 100°C rise in temperature.Table 5 shows approximate maximum unclipped peak output voltages at room temperature (excluding interconnect resistances).

Table 5. Approximate Maximum Unclipped Peak Output Voltage at Room Temperature

SUPPLY VOLTAGE V_{PVDD} (V)	MAXIMUM UNCLIPPED PEAK VOLTAGE V_{PK} (V)	
	R_L = 4 Ω	R_L = 8 Ω
12	11.16	11.57
17	15.81	16.39

7.3.4.3 Digital Clipper

The digital clipper hard limits the maximum DAC sample value, which provides a simple hardware mechanism to control the largest signal applied to the speaker. Because this block resides in the digital domain, the actual maximum output voltage also depends on the amplifier gain setting and the supply voltage (V_{PVDD}) limited amplifier voltage swing (For example, analog clipping can occur before digital clipping).

The maximum amplifier output voltage (excluding limitation due to swing) is calculated in Equation 4.

$$V_{AMP(max,dc)} = 20 \times \log_{10} \left(\frac{DC_{level}}{0xFFFFF} \right) + 0.5 + A_{AMP} \quad (4)$$

where

- $V_{AMP(max,dc)}$ is the amplifier maximum output voltage in dBV
- DC_{level} is the digital clipper level
- A_{AMP} is the amplifier analog gain setting (19.2, 20.7, 23.5, or 26.3) in dBV

Configure the digital clipper by writing the 20-bit DC_{level} to registers 0x01, 0x10 and 0x11. Set the DC_{level} to 0xFFFFF effectively bypasses the digital clipper.

7.3.4.4 Class-D Amplifier Settings

The PWM switching rate of the Class-D amplifier is a phase locked multiple of the input audio sample rate. Table 6 lists the PWM switching rate settings as programmed in bit 4 through bit 6 in register 0x06. The double-speed sample rates (for example 88.2kHz, 96kHz) have the same PWM switching frequencies as their equivalent single-speed sample rates.

Table 6. PWM Switching Rates

PWM_RATE[2:0]	SINGLE-SPEED PWM RATE (× f_{LRCLK})	DOUBLE-SPEED PWM RATE × f_{LRCLK})	44.1 kHz, 88.2 kHz f_{PWM}(kHz)	48 kHz, 96 kHz f_{PWM}(kHz)
000	6	3	264.6	288
001	8	4	352.8	384
010	10	5	441	480
011	12	6	529.2	576
100	14	7	617.4	672
101	16	8	705.6	768
110	20	10	882	960
111	24	12	1058.4	1152

The Class-D power stage Over Current detector issues a latching fault if the load current exceeds the safe limit for the device. The threshold can be proportionately adjusted if desired by programming bits 4-5 of register 0x08. Table 7 shows the relative setting for each Over Current setting.

Table 7. Over Current Threshold Settings

OC_THRESH [1:0]	OVERCURRENT THRESHOLD (%)
00	100
01	75
10	50
11	25

7.4 Device Functional Modes

This section describes the modes of operation for the TAS5720L/M device.

Table 8. Typical Current Consumption(1)

INPUT VOLTAGE V_{PVDD} (V)	MODE	PWM FREQUENCY f_{PWM} (kHz)	$I_{PVDD}+I_{AVDD}$ (mA)	INPUT CURRENT I_{DVDD} (mA)
7.2	Idle and Mute	384	14.5	4.1
		768	18.4	
	Sleep	—	9.0	1.32
	Shutdown	—	0.039	0.077
12	Idle and Mute	384	17.4	4.1
		768	21.3	
	Sleep	—	9.0	1.32
	Shutdown	—	0.045	0.077
15	Idle and Mute	384	19.4	4.1
		768	22.9	
	Sleep	—	9.1	1.32
	Shutdown	—	0.049	0.077
19	Idle and Mute	384	22.4	4.1
		768	24.8	
	Sleep	—	9.3	1.32
	Shutdown	—	0.054	0.077
24	Idle and Mute	384	26.2	4.1
		768	26.9	
	Sleep	—	9.4	1.32
	Shutdown	—	0.061	0.077

(1) T_A = 25ºC, PVDD pin tied to AVDD pin, V_{DVDD} = 3.3 V, R_{LOAD} = 4Ω, f_{IN} = Idle, f_S = 48 kHz, Gain = 20.7 dBV

7.4.1 Shutdown Mode (SDZ)

The device enters shutdown mode if either the SDZ pin is asserted low or the I^2C SDZ register bit is set low (bit 0, reg 0x01). In shutdown mode, the device consumes the minimum quiescent current with most analog and digital blocks powered down. The Class-D amplifier power stage powers down and the output pins are in a Hi-Z state. I^2C communication remains possible in shutdown mode and register bits states are retained.

If a latching fault condition has occurred (over temperature, Over Current or DC detect), the SDZ pin or I^2C bit must toggle low before the fault register can be cleared. For more information on faults and recovery, see the *Faults and Status* section.

When the device exits shutdown mode (by releasing both the SDZ pin high and setting the I^2C SDZ register bit high), the device powers up the internal analog and digital blocks required for operation. If the I^2C SLEEP bit is set low (bit 1, reg 0x01), the device powers up the Class-D amplifier and begins the switching of the power stage. If the I^2C MUTE bit is set low (bit 4, reg 0x03), the device ramps up the volume to the current setting and begins playing audio.

If shutdown mode is asserted while audio is playing, the device ramps down the volume on the audio, stops the Class-D switching, puts the Class-D power stage output pins in a Hi-Z state and powers down the analog and digital blocks.

7.4.2 Sleep Mode

Sleep mode is similar to shutdown mode, except analog and digital blocks required to begin playing audio quickly are left powered up. Sleep mode operates as a *hard mute* where the Class-D amplifier stops switching, but the device does not power down completely. Entering sleep mode does not clear latching faults.

7.4.3 Active Mode

If shutdown mode and sleep mode are not asserted, the device is in active mode. During active mode, audio playback is enabled.

7.4.4 Mute Mode

When the I^2C_MUTE bit is set high (bit 4, reg 0x03) and the device is in active mode, the volume is ramped down and the Class-D amplifier continues to operate with an idle audio input.

7.4.5 Faults and Status

During the power-up sequence, the power-on-reset circuit (POR) monitoring the DVDD pin domain releases all registers from reset (including the I^2C registers) once DVDD is valid. The device does not exit shutdown mode until the PVDD pin has a valid voltage between the undervoltage lockout (UVLO) and overvoltage lockout (OVLO) thresholds. If DVDD drops below the POR threshold the device transitions into shutdown mode with all registers held in reset. If UVLO or OVLO thresholds are violated by the PVDD pin thresholds, the device transitions into shutdown mode, but registers are not be forced into reset. Both of the conditions are non-latching and the device operates normally once supply voltages are valid again. The device can be reset only by reducing DVDD below the POR threshold.

The device transitions into sleep mode if it detects any faults with the SAIF clocks such as

- Invalid MCLK to LRCLK and BCLK to LRCLK ratios
- Invalid MCLK and LRCLK switching rates
- Halting of MCLK, BCLK or LRCLK switching

Upon detection of a SAIF clock error, the device transitions into sleep mode as quickly as possible to limit the possibility of audio artifacts. Once all SAIF clock errors are resolved, the device will volume ramp back to the previous playback state. During a SAIF clock error, the FAULTZ pin will be asserted low and the CLKE bit will be asserted high (register 0x08, bit 3).

While operating in shutdown mode, the SAIF clock error detect circuitry powers down and the CLKE bit reads high. This reading is not an indication of a SAIF clock error. If the device has not entered active mode after a power-up sequence or after transitioning out of shutdown mode, the FAULTZ pin pulses low for only approximately 10 µs every 350 µs. This action prevents a possible locking condition if the FAULTZ is connected to the SDZ pin to accomplish automatic recovery. Once the device has entered active mode one time (after power up or deassertion of shutdown mode), the SAIF clock errors pull the FAULTZ pin low continuously until the fault has cleared.

The device also monitors die temperature, power stage load current and amplifier output DC content and issues latching faults if any of the conditions occur. A die temperature of approximately 150°C causes the device to enter sleep mode and issue an Over-temperature error (OTE) readable via I^2C (bit 0, reg 0x08).

Sustained excessive DC content at the output of the Class-D amplifier can damage loudspeakers via voice coil heating. The amplifier has an internal circuit to detect significant DC content that forces the device into sleep mode. The device issues a DC detect error (DCE) readable via I^2C (bit 1, reg 0x08).

If the Class-D amplifier load current exceeds the threshold set by the OC_THRESH register bits (bits 5-4, reg 0x08), the device enters sleep mode and issues an Over Current Error (OCE) that is readable via I^2C (bit 2, reg 0x08).

During OTE, DCE and OCE, the FAULTZ pin asserts low until the latched fault is cleared. FAULTZ is an open drain pin and requires a pull-up resistor to the DVDD pin.

Latched faults can be cleared only by toggling the SDZ pin or SDZ I^2C bit (bit 0, reg 0x01). This toggle does not clear I^2C registers (except the fault status of OTE, OCE and DCE). If the device is intended to attempt automatic recovery after latching faults, implement a circuit like the one shown in Figure 50. The device waits approximately 650 ms after a DCE fault has cleared and 1.3 s after an OTE or OCE fault has cleared before releasing FAULTZ high and allowing the device to enter active mode.

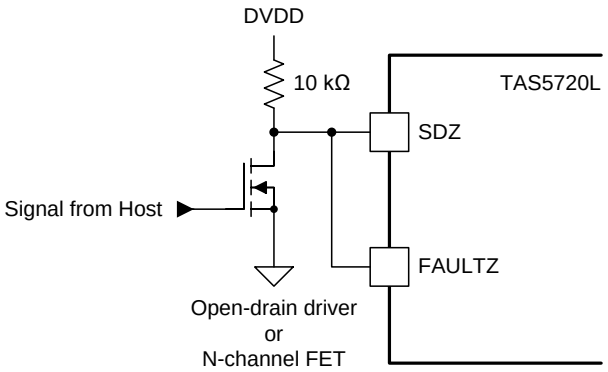


Figure 50. Auto Recovery Circuit

7.5 Register Maps

When writing to registers with reserved bits, maintain the values shown in Table 9 to ensure proper device operation. Default register values are loaded during the power-up sequence or any time the DVDD voltage falls below the power-on-reset (POR) threshold and then returns to valid operation.

Table 9. I²C Register Map Summary

ADDR (Dec)	ADDR (Hex)	REGISTER NAME	REGISTER BITS								DEFAULT (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
0	0x00	Device ID	DEVICE_ID								0x01
			0	0	0	0	0	0	0	1	
1	0x01	Power Control	DIGITAL_CLIP_LEVEL [19:14]						SLEEP	SDZ	0xFD
			1	1	1	1	1	1	0	1	
2	0x02	Digital Control 1	HPF_BYPASS	TDM_CFG_SRC	RSV		SSZ/DS	SAIF_FORMAT			0x04
			0	0	0	0	0	1	0	0	
3	0x03	Digital Control 2	RSV			MUTE	RSV	TDM_SLOT_SELECT			0x80
			1	0	0	0	0	0	0	0	
4	0x04	Volume Control	VOLUME_CONTROL								0xCF
			1	1	0	0	1	1	1	1	
6	0x06	Analog Control	RSV	PWM_RATE			ANALOG_GAIN		RSV		0x55
			0	1	0	1	0	1	0	1	
8	0x08	Fault Config and Error Status	RSV		OC_THRESH		CLKE	OCE	DCE	OTE	0x00
			0	0	0	0	0	0	0	0	
16	0x10	Digital Clipper 2	DIGITAL_CLIP_LEVEL[13:6]								0xFF
			1	1	1	1	1	1	1	1	
17	0x11	Digital Clipper 1	DIGITAL_CLIP_LEVEL[5:0]						RSV		0xFC
			1	1	1	1	1	1	0	0	

7.5.1 Device Identification

Figure 51. Device Identification, Address: 0x000

7	6	5	4	3	2	1	0
DEVICE_ID							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. Device Identification, Address: 0x000

Bit	Field	Type	Reset	Description
7	DEVICE_ID[7:0]	R	0	This register returns a value of 0x01 when read.
6			0	
5			0	
4			0	
3			0	
2			0	
1			0	
0			1	

7.5.2 Power Control Register

Table 11. Power Control Register, Address: 0x001

7	6	5	4	3	2	1	0
DIGITAL_CLIP_LEVEL						SLEEP	SDZ
R/W						R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. Power Control Register, Address: 0x001

Bit	Field	Type	Reset	Description
7	DIGITAL_CLIP_LEVEL[19:14]	R/W	1	This register holds the top 6-bits of the 20-bit Digital Clipper level. The Digital Clipper limits the magnitude of the sample applied to the DAC. See the *Digital Clipper* section for more information.
6			1	
5			1	
4			1	
3			1	
2			1	
1	SLEEP	R/W	0	When the device enters SLEEP mode, volume ramps down and the Class-D output stage powers down to a Hi-Z state. The rest of the blocks will be kept in a state such that audio playback can be restarted as quickly as possible. This mode has lower dissipation than MUTE, but higher than SHUTDOWN. For more information see the *Device Functional Modes* section. 0: Exit Sleep (default) 1: Enter Sleep
0	SDZ	R/W	1	The device enters SHUTDOWN mode if either this bit is set to a 0 or the SDZ pin is pulled low externally. In SHUTDOWN, the device holds the lowest dissipation state. I^2C communication remains functional and all registers are retained. For more information see the *Device Functional Modes* section. 0: Enter SHUTDOWN 1: Exit SHUTDOWN (default)

7.5.3 Digital Control Register 1

Table 13. Digital Control Register 1, Address: 0x002

7	6	5	4	3	2	1	0
HPF_BYPASS	TDM_CFG_SRC	RSV		SSZ/DS	SAIF_FORMAT		
R/W	R/W	R/W		R/W	R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. Digital Control Register 1, Address: 0x002

Bit	Field	Type	Reset	Description
7	HPF_BYPASS	R/W	0	The high-pass filter removes any DC component in the audio content that could trip the DC detect protection feature in the amplifer, which is a latching fault. Setting this bit bypasses the high-pass filter. See the *High-Pass Filter (HPF)* section for more information. 0:Enable high-pass filter (default) 1: Bypass high-pass filter
6	TDM_CFG_SRC	R/W	0	This bit determines how the device selects which audio channel direct to the playback stream. See the *Serial Audio Interface (SAIF)* section for more information. 0:Set TDM Channel to I^2C Device ID (default). 1:Set TDM Channel to TDM_SLOT_SELECT in register 0x03.
5	RSV[1:0]	R/W	0	These bits are reserved and should be set to 00 when writing to this register.
4		R/W	0	
3	SSZ/DS	R/W	0	This bit sets the sample rate to single speed or double speed operation. See the Serial Audio Interface (SAIF) section for more information. 0: Single speed operation (44.1 kHz/48 kHz) - default. 1: Double speed operation (88.2 kHz/96 kHz)
2	SAIF_FORMAT[2:0]	R/W	1	These bits set the Serial Audio Interface format. See the Serial Audio Interface (SAIF) section for more information. 000: Right justified, 24-bit 001: Right justified, 20-bit
1		R/W	0	010: Right justified, 18-bit 011: Right justified, 16-bit 100: I^2S (default)
0		R/W	0	101: Left Justified, 16-24 bits 110: Reserved. Do not select this value. 111: Reserved. Do not select this value.

7.5.4 Digital Control Register 2

Table 15. Digital Control Register 2, Address: 0x003

7	6	5	4	3	2	1	0
RSV			MUTE	RSV	TDM_SLOT_SELECT		
R/W			R/W		R/W		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. Digital Control Register 2, Address: 0x003

Bit	Field	Type	Reset	Description
7	RSV[2:0]	R/W	1	These bits are reserved and should be set to 100 when this register is written to
6		R/W	0	
5		R/W	0	
4	MUTE	R/W	0	When set the device ramps down volume and play idle audio. See the Amplifier Analog Gain and Digital Volume Control section for more information. 0: Exit mute mode (default) 1: Enter mute mode
3	RSV	R/W	0	This bit is reserved and should be set to 0 when writing to this register.
2	TDM_SLOT_SELECT[2:0]	R/W	0	When the TDM_CFG_SRC bit is set to 1 in register 0x02, these bits select which TDM channel is directed to audio playback. See the *Serial Audio Interface (SAIF)* section for more information
1		R/W	0	
0		R/W	0	

7.5.5 Volume Control Register

Table 17. Volume Control Register, Address: 0x004

7	6	5	4	3	2	1	0
VOLUME_CONTROL							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. Volume Control Register, Address: 0x004

Bit	Field	Type	Reset	Description
7	VOLUME_CONTROL[7:0]	R/W	1	This register sets the Digital Volume Control, which ranges from -100 dB to +24 dB in 0.5 dB steps. Register settings of less than 0x07 are equivalent to setting the Mute bit in register 0x03. See the *Amplifier Analog Gain and Digital Volume Control* section for more information. 0xFF: +24.0 dB
6		R/W	1	0xFE: +23.5 dB
5		R/W	0	...
4		R/W	0	0xCF: 0 dB (default)
3		R/W	1	...
2		R/W	1	0x08: –99.5 dB
1		R/W	1	0x07: –100 dB
0		R/W	1	< 0x07: MUTE

7.5.6 Analog Control Register

Table 19. Analog Control Register, Address: 0x006

7	6	5	4	3	2	1	0
RSV	PWM_RATE			ANALOG_GAIN		RSV	
R/W	R/W			R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. Analog Control Register, Address: 0x006

Bit	Field	Type	Reset	Description
7	RSV	R/W	0	This bit is reserved and should be set to a 0 when this register is written to.
6	PWM_RATE[2:0]	R/W	1	These bits set the PWM switching rate, which is a locked ratio of LRCLK. For more information see the *Class-D Amplifier Settings* section. 000: 6 × LRCLK (single speed), 3 × LRCLK (double speed) 001: 8 × LRCLK (single speed), 4 × LRCLK (double speed)
5		R/W	0	010: 10 × LRCLK (single speed), 5 × LRCLK (double speed) 011: 12 × LRCLK (single speed), 6 × LRCLK (double speed) 100: 14 × LRCLK (single speed), 7 × LRCLK (double speed)
4		R/W	1	101: 16 × LRCLK (single speed), 8 × LRCLK (double speed) - default 110: 20 × LRCLK (single speed), 10 × LRCLK (double speed) 111: 24 × LRCLK (single speed), 12 × LRCLK (double speed)
3	ANALOG_GAIN[1:0]	R/W	0	Sets the analog gain of the Class-D amplifer. The values shown indicate the output level with digital volume control set to 0 dB and a full scale digital input (0 dBFS). This level might not be acheivable because of analog clipping. See the Amplifier Analog Gain and Digital Volume Control section for more information. 00: 19.2 dBV 01: 20.7 dBV (default)
2		R/W	1	10: 23.5 dBV 11: 26.3 dBV
1	RSV[1:0]	R/W	0	These bits are reserved and should be set to 01 when writing to this register
0		R/W	1	

7.5.7 Fault Configuration and Error Status Register

Table 21. Fault Configuration and Error Status Register, Address: 0x008

7	6	5	4	3	2	1	0
RSV		OC_THRESH		CLKE	OCE	DCE	OTE
R/W		R/W		R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. Fault Configuration and Error Status Register, Address: 0x008

Bit	Field	Type	Reset	Description
7	RSV[1:0]	R/W	0	This bit is reserved and should be set to a 00 when this register is written to.
6		R/W	0	
5	OC_THRESH[1:0]	R/W	0	This register sets the Over Current detector threshold. For more information see the *Class-D Amplifier Settings* section. 00: 100% of Over Current limit (default) 01: 75% of Over Current limit
4		R/W	1	10: 50% of Over Current limit 11: 25% of Over Current limit
3	CLKE	R	0	This bit indicates the status of the SAIF clock error detector. This is a self clearning value. 0: No SAIF clock errors. 1: SAIF clock errors are present.
2	OCE	R	0	This bit indicates the status of the over current error detector. This is a latching value 0: The Class-D output stage has not experienced an over current event. 1: The Class-D output stage has experienced an over current event.
1	DCE	R	0	This bit indicates the status of the DC detector. This is a latching value. 0: The Class-D output stage has not experienced a DC detect error. 1: The Class-D output stage has experienced a DC detect error.
0	OTE	R	0	This bit indicates the status of the over temperature detector. This is a latching value. 0: The Class-D output stage has not experienced an over temperature error. 1: The Class-D output stage has experienced an over temperature error.

7.5.8 Digital Clipper 2

Table 23. Digital Clipper 2, Address: 0x010

7	6	5	4	3	2	1	0
DIGITAL_CLIP_LEVEL							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. Digital Clipper 2, Address: 0x010

Bit	Field	Type	Reset	Description
7	DIGITAL_CLIP_LEVEL[13:6]	R/W	1	This register holds the bits 13 through 6 of the 20-bit Digital Clipper level. The Digital Clipper limits the magnitude of the sample applied to the DAC. See the *Digital Clipper* section for more information.
6		R/W	1	
5		R/W	1	
4		R/W	1	
3		R/W	1	
2		R/W	1	
1		R/W	1	
0		R/W	1	

7.5.9 Digital Clipper 1

Table 25. Digital Clipper 1, Address: 0x011

7	6	5	4	3	2	1	0
DIGITAL_CLIP_LEVEL							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. Digital Clipper 1, Address: 0x011

Bit	Field	Type	Reset	Description
7	DIGITAL_CLIP_LEVEL[5:0]	R/W	1	This register holds the bits 5 through 0 of the 20-bit Digital Clipper level. The Digital Clipper limits the magnitude of the sample applied to the DAC. See the *Digital Clipper* section for more information.
6		R/W	1	
5		R/W	1	
4		R/W	1	
3		R/W	1	
2		R/W	1	
1	RSV[1:0]	R/W	0	These bits are reserved and should be set to 00 when writing to this register.
0		R/W	0	

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

This section describes a filter-free,TDM application.

8.2 Typical Application

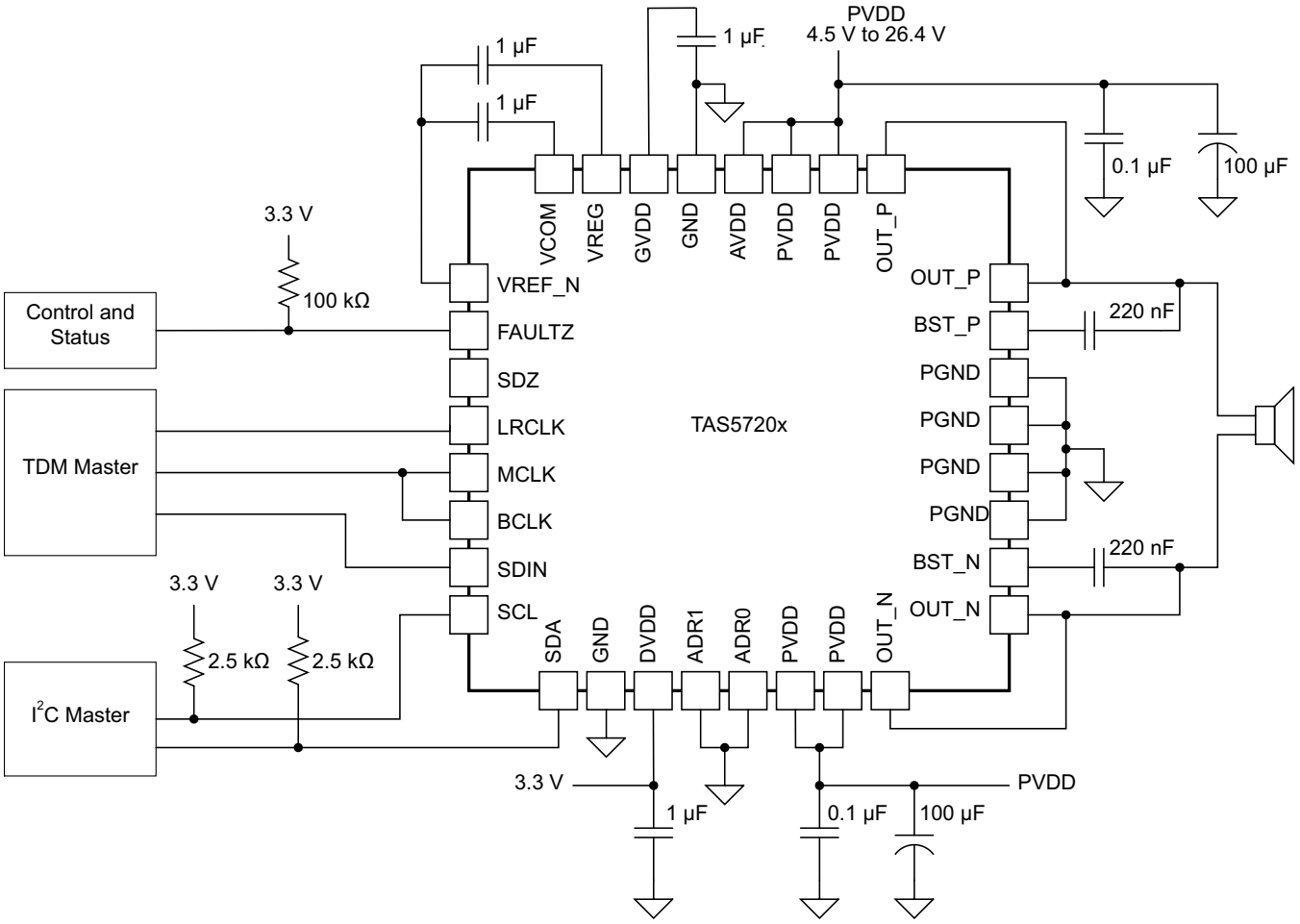


Figure 52. Filter Free 3-Wire TDM Application Circuit (I2C_DEV_ID = 0x6C)

8.2.1 Design Requirements

- Input voltage range PVDD and AVDD: 4.5 V to 26.4 V
- Input voltage range DVDD: 3.3 V to 3.6 V
- Input sample rate: 44.1 kHz to 48 kHz or 88.2 kHz to 96 kHz
- I^2C clock frequency: up tp 400 kHz

Typical Application (continued)

8.2.2 Design Procedure

8.2.2.1 Overview

The TAS5720L/M is a flexible and easy to use Class D amplifier; therefore the design process is straightforward. Before beginning the design, gather the following information regarding the audio system.

- PVDD rail planned for the design
- Speaker or load impedance
- Audio sample rate
- Maximum output power requirement
- Desired PWM frequency

8.2.2.2 Select the PWM Frequency

Set the PWM frequency by writing to the PWM_RATE bits (bits 6-4, reg 0x06). The default setting for this register is 101, which is 16 × LRCLK for single speed applications and 8 × LRCLK for double speed application. This value equates to a default PWM frequency of 768 kHz for a 48 Hz sample rate.

8.2.2.3 Select the Amplifier Gain and Digital Volume Control

To select the amplifier gain setting, the designer must determine the maximum power target and the speaker impedance. Once the parameters have been determined, calculate the required output voltage swing which delivers the maximum output power.

Choose the lowest analog gain setting that corresponds to produce an output voltage swing greater than the required output swing for maximum power. The analog gain can be set by writing to the ANALOG_GAIN bits (bits 3-2, reg 0x06). The default gain setting is 20.7 dBV referenced to 0dBFS input.

8.2.2.4 Select Input Capacitance

Select the bulk capacitors at the PVDD inputs for proper voltage margin and adequate capacitance to support the power requirements. The TAS5720L/M has very good PVDD PSRR, so the capacitor is more about limiting the ripple and droop for the rest of system than preserving good audio performance. The amount of bulk decoupling can be reduced as long as the droop and ripple is acceptable. One capacitor should be placed near the PVDD inputs at each side of the device. PVDD capacitors should be a low ESR type because they are being used in a high-speed switching application.

8.2.2.5 Select Decoupling Capacitors

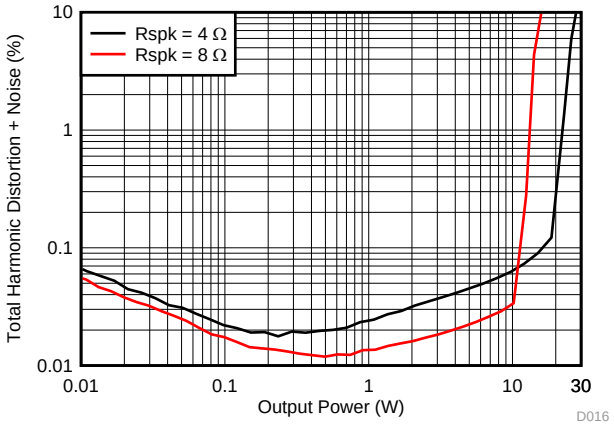
Good quality decoupling capacitors should be added at each of the PVDD inputs to provide good reliability, good audio performance, and to meet regulatory requirements. X5R or better ratings should be used in this application. Consider temperature, ripple current, and voltage overshoots when selecting decoupling capacitors. Also, the decoupling capacitors should be located near the PVDD and GND connections to the device to minimize series inductances.

8.2.2.6 Select Bootstrap Capacitors

Each of the outputs require bootstrap capacitors to provide gate drive for the high-side output FETs. For this design, use 0.22-µF, 25-V capacitors of X5R quality or better.

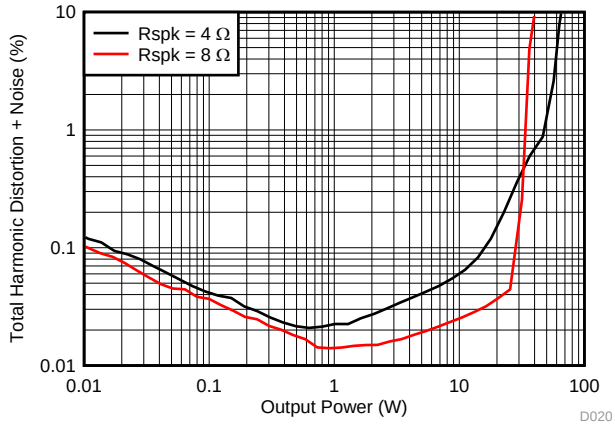
Typical Application (continued)

8.2.3 Application Curves



$V_{(PVDD)}$ = 15 V $f_{(PWM)}$ = 384 kHz

Figure 53. THD+N vs. Output Power



$V_{(PVDD)}$ = 24 V $f_{(PWM)}$ = 384 kHz

Figure 54. THD+N vs. Output Power

9 Power Supply Recommendations

The power supply requirements for the TAS5720L/M device consist of one 3.3-V supply to power the low-voltage analog and digital circuitry and one higher-voltage supply to power the output stage of the speaker amplifier. Several on-chip regulators are included on the TAS5720L/M device to generate the voltages necessary for the internal circuitry of the audio path. The voltage regulators which have been integrated are sized only to provide the current necessary to power the internal circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors to filter the supply. Connecting external circuitry to the regulator outputs can result in reduced performance and damage to the device.

The TAS5720L/M requires two power supplies. A 3.3-V supply, called DVDD, is required to power the digital section of the chip. A higher-voltage supply, between 4.5 V and 26.4 V, supplies the analog circuitry (AVDD) and the power stage (PVDD). The AVDD supply feeds several LDOs including GVDD, VREG, and VCOM. The LDO outputs are connected to external pins for filtering purposes, but should not be connected to external circuits. The LDO outputs have been sized to provide current necessary for internal functions but not for external loading.

10 Layout

10.1 Layout Guidelines

- Pay special attention to the power stage power supply layout. Each H-bridge has two PVDD input pins so that decoupling capacitors can be placed nearby. Use at least a 0.1-µF capacitor of X5R quality or better for each set of inputs.
- Keep the current circulating loops containing the supply decoupling capacitors, the H-bridges in the device and the connections to the speakers as tight as possible to reduce emissions.
- Use ground planes to provide the lowest impedance for power and signal current between the device and the decoupling capacitors. The area directly under the device should be treated as a central ground area for the device, and all device grounds must be connected directly to that area.
- Use a via pattern to connect the area directly under the device to the ground planes in copper layers below the surface. This connection helps to dissipate heat from the device.
- Avoid interrupting the ground plane with circular traces around the device. Interruption disconnects the copper and interrupt flow of heat and current. Radial copper traces are better to use if necessary.

10.2 Layout Example

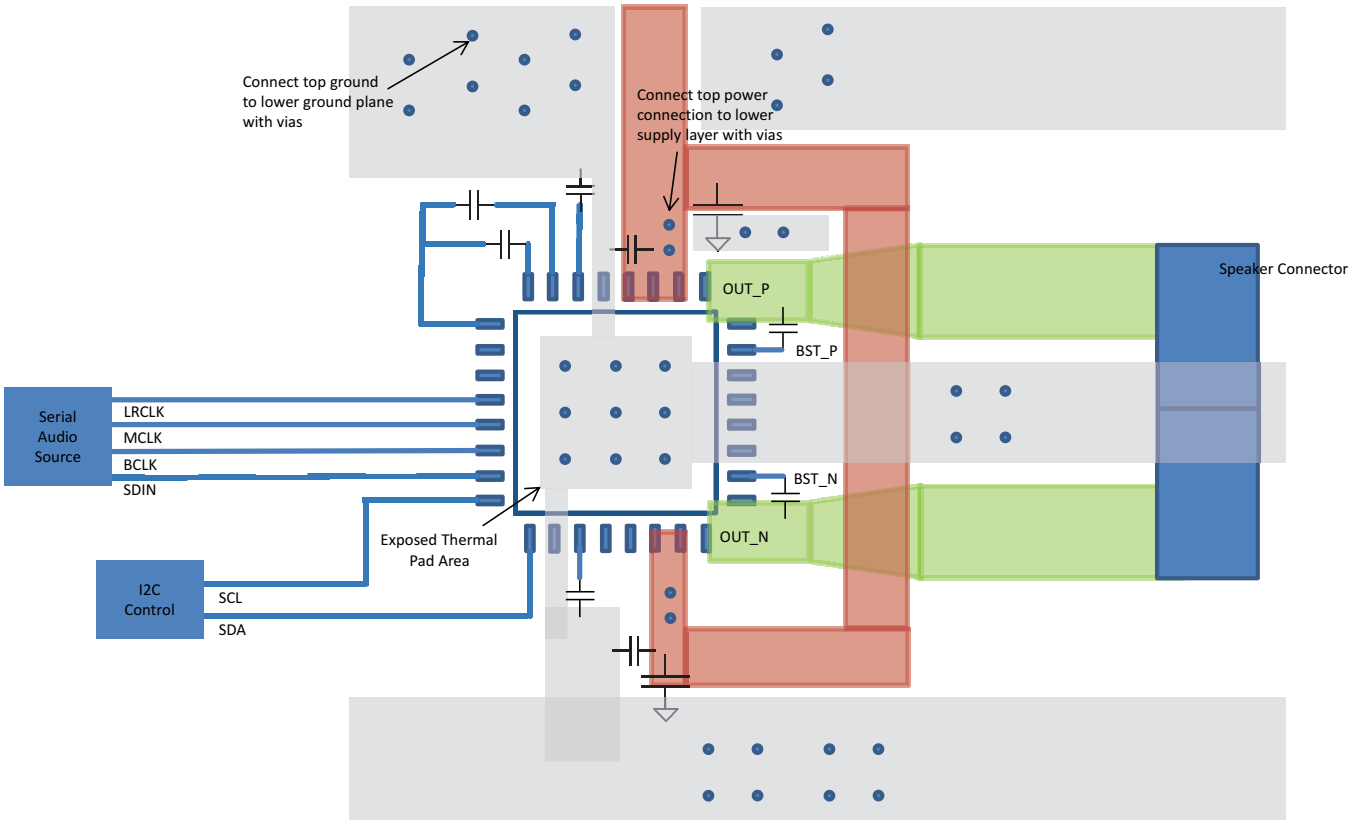


Figure 55. TAS5720L Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 27. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TAS5720L	Click here	Click here	Click here	Click here	Click here
TAS5720M	Click here	Click here	Click here	Click here	Click here

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5720LRSMR	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	TAS 5720L	Samples
TAS5720LRSMT	ACTIVE	VQFN	RSM	32	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	TAS 5720L	Samples
TAS5720MRSMR	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-25 to 85	TAS 5720M	Samples
TAS5720MRSMT	ACTIVE	VQFN	RSM	32	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	TAS 5720M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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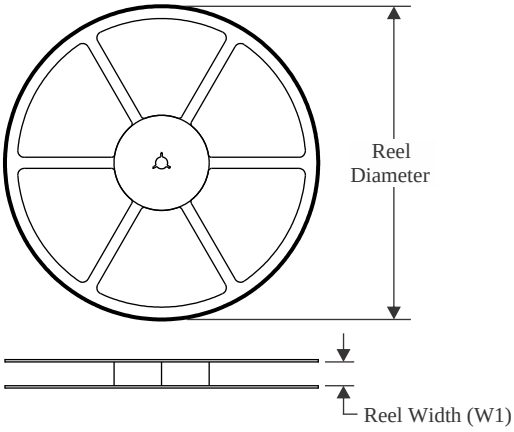
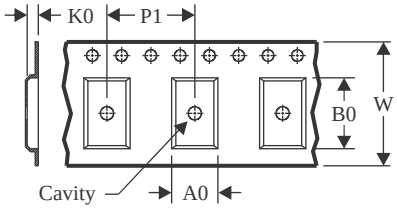
TAPE AND REEL INFORMATION

REEL DIMENSIONS

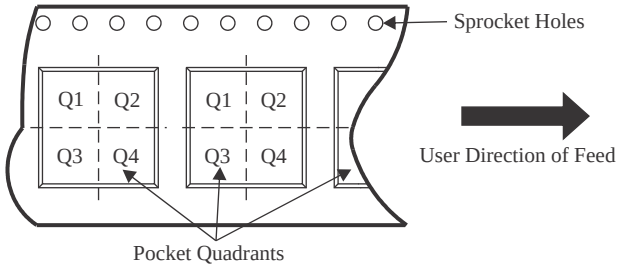


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

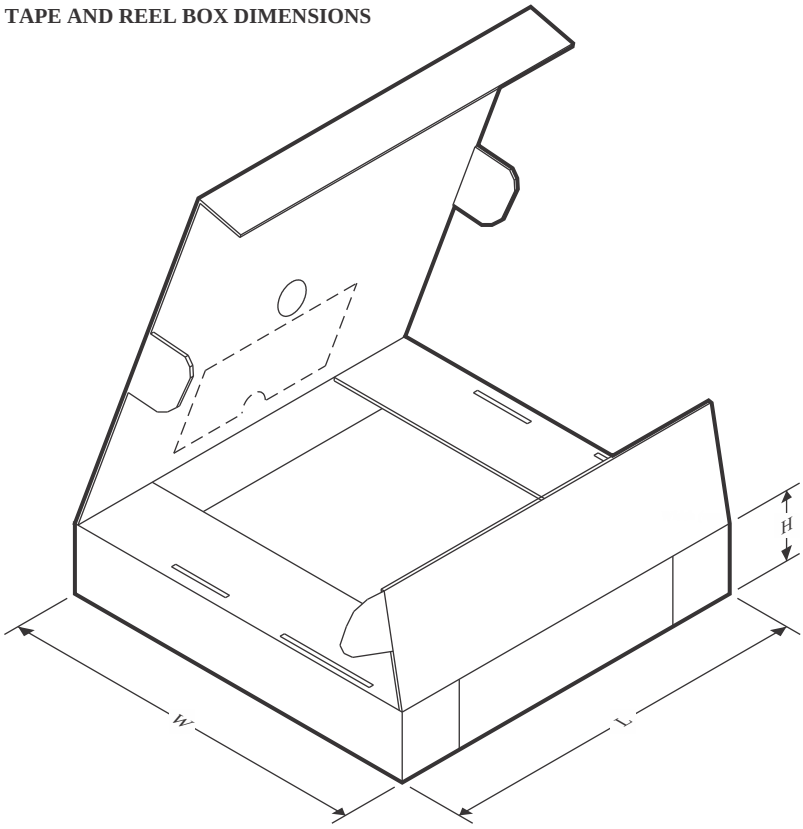
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5720LRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TAS5720LRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TAS5720MRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TAS5720MRSMT	VQFN	RSM	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5720LRSMR	VQFN	RSM	32	3000	346.0	346.0	33.0
TAS5720LRSMT	VQFN	RSM	32	250	210.0	185.0	35.0
TAS5720MRSMR	VQFN	RSM	32	3000	346.0	346.0	33.0
TAS5720MRSMT	VQFN	RSM	32	250	182.0	182.0	20.0

GENERIC PACKAGE VIEW

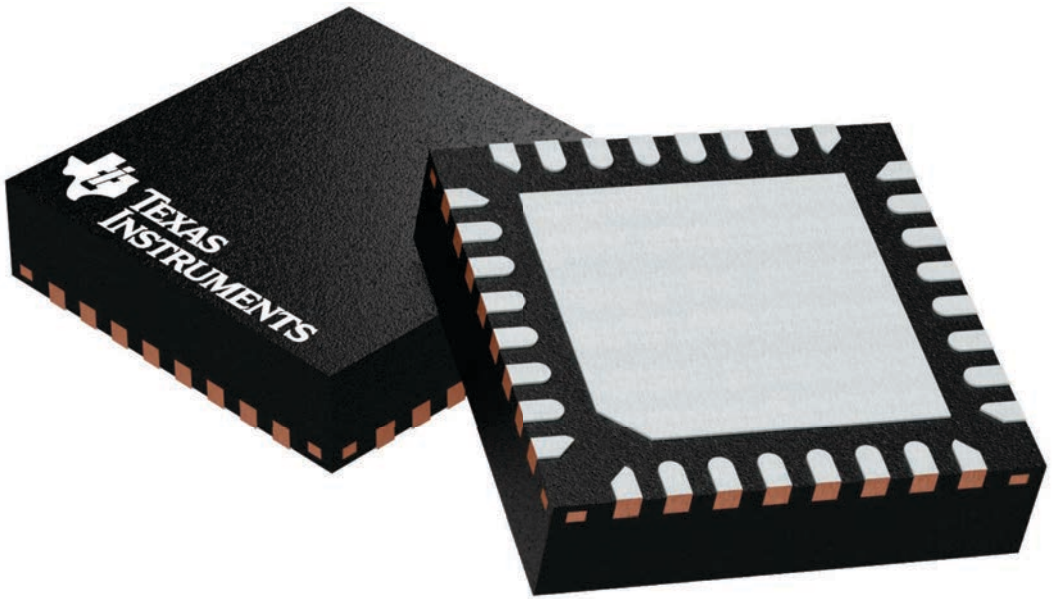
RSM 32

VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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