TCA9406 2-Bit Bidirectional 1-MHz, I²C Bus and SMBus Voltage-Level Translator With 8-kV HBM ESD

1 Features

- 2-Bit Bidirectional Translator for SDA and SCL Lines in I²C Applications
- Provides Bidirectional Voltage Translation With No Direction Pin
- High-Impedance Output SCL_A, SDA_A, SCL_B, SDA_B Pins When OE = Low or V_{CC} = 0 V
- Internal 10-kΩ Pullup Resistor on All SDA and SCL Pins
- 1.65 V to 3.6 V on A port and 2.3 V to 5.5 V on B port ($V_{CCA} \leq V_{CCB}$)
- V_{CC} Isolation Feature: If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- No Power-Supply Sequencing Required: Either V_{CCA} or V_{CCB} Can Be Ramped First
- Low I_{off} of 2 µA When Either V_{CCA} or V_{CCB} = 0 V
- OE Input Can Be Tied Directly to V_{CCA} Or Controlled By GPIO
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - A Port
    - 2500-V Human-Body Model (A114-B)
    - 250-V Machine Model (A115-A)
    - 1500-V Charged-Device Model (C101)
  - B Port
    - 8-kV Human-Body Model (A114-B)
    - 250-V Machine Model (A115-A)
    - 1500-V Charged-Device Model (C101)

2 Applications

- I²C/SMBus
- UART
- GPIO

3 Description

The TCA9406 is a 2-bit bidirectional I²C and SMBus voltage-level translator with an output enable (OE) input. It is operational from 1.65 V to 3.6 V on the A-side, referenced toV_{CCA}, and from 2.3 V to 5.5 V on the B-side, referenced to V_{CCB}. This allows the device to interface between lower and higher logic signal levels at any of the typical 1.8-V, 2.5-V, 3.3-V, and 5-V supply rails.

The OE input pin is referenced to V_{CCA}, can be tied directly to V_{CCA}, but it is also 5.5-V tolerant. The OE pin can also be controlled and set to a logic low to place all the SCL and SDA pins in a high-impedance state, which significantly reduces the quiescent current consumption.

Under normal I²C and SMBus operation or other open-drain configurations, the TCA9406 can support up to 2 Mbps; therefore, it is compatible with standard I²C speeds where the frequency of SCL is 100 kHz (Standard-mode), 400 kHz (Fast-mode), or 1 MHz (Fast-mode Plus). The device can also be used as a general purpose level translator, and when the A- and B-side ports are both driven with push-pull devices the TCA9406 can support up to 24 Mbps.

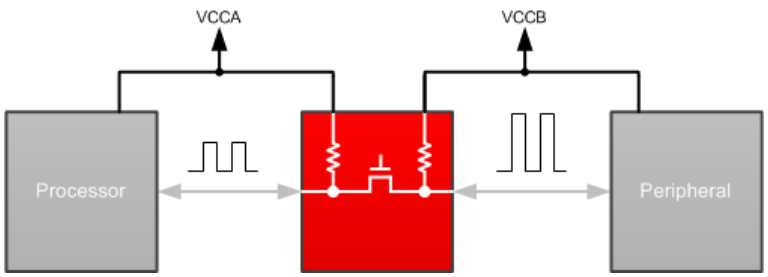
The TCA9406 features internal 10-kΩ pullup resistors on SCL_A, SDA_A, SCL_B, and SDA_B. Additional external pullup resistors can be added to the bus to reduce the total pullup resistance and speed up rising edges.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TCA9406	SM8 (8)	2.95 mm × 2.80 mm
	US8 (8)	2.30 mm × 2.00 mm
	DSBGA (8)	1.90 mm × 0.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Block Diagram for TCA9406



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (October 2018) to Revision G — **Page**

- Changed section title From: Pullup or Pulldown Resistors on I/O Lines To: Pullup Resistors on I/O Lines ... 20
- Deleted text "An external pull down..." and Equation 1 from the *Detailed Design Procedure* section ... 21
- Changed pin 1 From: To controller To: To system in Figure 13 ... 23
- Changed pin 5 From: To system To: To controller in Figure 13 ... 23

Changes from Revision E (August 2018) to Revision F — **Page**

- Changed the *Functional Block Diagram* ... 18
- Changed the *Enable and Disable* section ... 19

Changes from Revision D (July 2018) to Revision E — **Page**

- Changed the new DSBGA pinout drawing From: Bottom View to: Top View ... 5

Changes from Revision C (December 2014) to Revision D — **Page**

- Changed the updated pinout drawings ... 5
- Changed t_{dis} no external load MAX values From: 50 To: 200 ns in *Switching Characteristics (V_{CCA} = 1.8 V ± 0.15 V)* ... 10
- Changed t_{dis} no external load MAX values From: 40 To: 200 ns in *Switching Characteristics (V_{CCA} = 1.8 V ± 0.15 V)* ... 10
- Changed t_{dis} no external load MAX values From: 35 To: 200 ns in *Switching Characteristics (V_{CCA} = 1.8 V ± 0.15 V)* ... 11
- Changed t_{dis} no external load MAX values From: 50 To: 200 ns in *Switching Characteristics (V_{CCA} = 2.5 V ± 0.2 V)* ... 12
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- Changed t_{dis} no external load MAX values From: 35 To: 200 ns in *Switching Characteristics (V_{CCA} = 1.8 V ± 0.15 V)* ... 13
- Changed t_{dis} no external load MAX values From: 40 To: 200 ns in *Switching Characteristics (V_{CCA} = 1.8 V ± 0.15 V)* ... 14

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- Changed t_{dis} no external load MAX values From: 35 To: 200 ns in *Switching Characteristics (V_{CCA} = 1.8 V ± 0.15 V)*..... 14
- Changed the *Parameter Measurement Information* section..... 16

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Changes from Revision B (June 2013) to Revision C **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Revision A (Febuary 2013) to Revision B **Page**

- Removed ordering information table, information now located in POA 1

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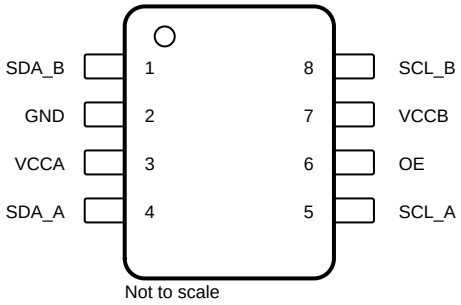
5 Pin Configuration and Functions

8-PIN SM8 OR US8
(TOP VIEW)



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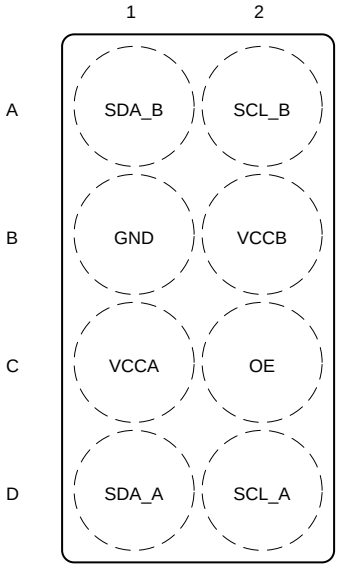
8-PIN DSBGA
(TOP VIEW)



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Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DCT, DCU	YZP		
SDA_B	1	A1	I/O	Input/output B. Referenced to V_{CCB}.
GND	2	B1	GND	Ground
VCCA	3	C1	Power	A-port supply voltage. 1.65 V ≤ V_{CCA} ≤ 3.6 V and V_{CCA} ≤ V_{CCB}
SDA_A	4	D1	I/O	Input/output A. Referenced to V_{CCA}.
SCL_A	5	D2	I/O	Input/output A. Referenced to V_{CCA}.
OE	6	C2	Input	Output enable (active High). Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
VCCB	7	B2	Power	B-port supply voltage. 2.3 V ≤ V_{CCB} ≤ 5.5 V
SCL_B	8	A2	I/O	Input/output B. Referenced to V_{CCB}.

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6 Specifications

6.1 Absolute Maximum Ratings(1)

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		–0.5	4.6	V
V_{CCB}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range(2)	A port	–0.5	4.6	V
		B port	–0.5	6.5	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	6.5	
V_O	Voltage range applied to any output in the high or low state(2)(3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	A-Port	±2500	V
			B-Port	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1500	V
		Machine model (MM), A115-A		±250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

V_{CCI} is the supply voltage associated with the input port. V_{CCO} is the supply voltage associated with the output port.

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage(1)				1.65	3.6	V
V_{CCB}	Supply voltage				2.3	5.5	V
V_{IH}	High-level input voltage	A-port I/Os	1.65 V to 1.95 V	2.3 V to 5.5 V	V_{CCI} – 0.2	V_{CCI}	V
			2.3 V to 3.6 V		V_{CCI} – 0.4	V_{CCI}	
		B-port I/Os	1.65 V to 3.6 V	2.3 V to 5.5 V	V_{CCI} – 0.4	V_{CCI}	
		OE input			V_{CCA} × 0.65	5.5	
V_{IL}(2)	Low-level input voltage	A-port I/Os	1.65 V to 3.6 V	2.3 V to 5.5 V	0	0.15	V
		B-port I/Os			0	0.15	
		OE input			0	V_{CCA} × 0.35	
Δt/Δv	Input transition rise or fall rate	A-port I/Os, push-pull driving	1.65 V to 3.6 V	2.3 V to 5.5 V		10	ns/V
		B-port I/Os, push-pull driving				10	
		Control input				10	
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCA} must be less than or equal to V_{CCB} (except during power-on transient time), and V_{CCA} must not exceed 3.6 V.
(2) The maximum V_{IL} value is provided to ensure that a valid V_{OL} is maintained. The V_{OL} value is V_{IL} plus the voltage drop across the pass-gate transistor.

6.4 Thermal Information

THERMAL METRIC(1)		TCA9406			UNIT
		DCT	DCU	YZP	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	182.6	199.1	105.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	113.3	72.4	1.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.9	77.8	10.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	39.4	6.2	3.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	93.9	77.4	10.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics[1][2][3]

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C	–40°C to 85°C		UNIT
					TYP	MIN	MAX	
V_{OHA}		I_{OH} = –20 μA, V_{IB} ≥ V_{CCB} – 0.4 V	1.65 V to 3.6 V	2.3 V to 5.5 V		V_{CCA} × 0.67		V
V_{OLA}		I_{OL} = 1 mA, V_{IB} ≤ 0.15 V	1.65 V to 3.6 V	2.3 V to 5.5 V			0.4	V
V_{OHB}		I_{OH} = –20 μA, V_{IA} ≥ V_{CCA} – 0.2 V	1.65 V to 3.6 V	2.3 V to 5.5 V		V_{CCB} × 0.67		V
V_{OLB}		I_{OL} = 1 mA, V_{IA} ≤ 0.15 V	1.65 V to 3.6 V	2.3 V to 5.5 V			0.4	V
I_I	OE	V_I = V_{CCI} or GND	1.65 V to 3.6 V	2.3 V to 5.5 V	±1		±2	μA
I_{off}	A port		0 V	0 V to 5.5 V	±1		±2	μA
	B port		0 to 3.6 V	0 V	±1		±2	μA
I_{OZ}	A or B port	OE less than V_{IL}	1.65 V to 3.6 V	2.3 V to 5.5 V	±1		±2	μA
I_{CCA}		V_I = V_O = open, I_O = 0	1.65 V to V_{CCB}	2.3 V to 5.5 V			2.4	μA
			3.6 V	0 V			2.2	
			0 V	5.5 V			–1	
I_{CCB}		V_I = V_O = open, I_O = 0	1.65 V to V_{CCB}	2.3 V to 5.5 V			12	μA
			3.6 V	0 V			–1	
			0 V	5.5 V			1	
I_{CCA} + I_{CCB}		V_I = V_O = open, I_O = 0	1.65 V to V_{CCB}	2.3 V to 5.5 V			14.4	μA
C_I	OE		3.3 V	3.3 V	2.5		3.5	pF
C_{io}	A or B port		3.3 V	3.3 V	10			pF
	A port				5	6		
	B port				6	7.5		

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6 V.

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6.6 Timing Requirements (V_{CCA} = 1.8 V ± 0.15 V)

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCB} = 2.5 V ± 0.2 V					
Data rate	Push-pull driving			21	Mbps
	Open-drain driving			2	
t_w Pulse duration	Push-pull driving	Data inputs	47		ns
	Open-drain driving		500		
V_{CC} = 3.3 V ± 0.3 V					
Data rate	Push-pull driving			22	Mbps
	Open-drain driving			2	
t_w Pulse duration	Push-pull driving	Data inputs	45		ns
	Open-drain driving		500		
V_{CC} = 5 V ± 0.5 V					
Data rate	Push-pull driving			24	Mbps
	Open-drain driving			2	
t_w Pulse duration	Push-pull driving	Data inputs	41		ns
	Open-drain driving		500		

6.7 Timing Requirements (V_{CCA} = 2.5 V ± 0.2 V)

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCB} = 2.5 V ± 0.2 V					
Data rate	Push-pull driving			20	Mbps
	Open-drain driving			2	
t_w Pulse duration	Push-pull driving	Data inputs	50		ns
	Open-drain driving		500		
V_{CC} = 3.3 V ± 0.3 V					
Data rate	Push-pull driving			22	Mbps
	Open-drain driving			2	
t_w Pulse duration	Push-pull driving	Data inputs	45		ns
	Open-drain driving		500		
V_{CC} = 5 V ± 0.5 V					
Data rate	Push-pull driving			24	Mbps
	Open-drain driving			2	
t_w Pulse duration	Push-pull driving	Data inputs	41		ns
	Open-drain driving		500		

6.8 Timing Requirements (V_{CCA} = 3.3 V ± 0.3 V)

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC} = 3.3 V ± 0.3 V					
Data rate	Push-pull driving			23	Mbps
	Open-drain driving			2	
t_w Pulse duration	Push-pull driving	Data inputs	43		ns
	Open-drain driving		500		
V_{CC} = 5 V ± 0.5 V					
Data rate	Push-pull driving			24	Mbps
	Open-drain driving			2	
t_w Pulse duration	Push-pull driving	Data inputs	41		ns
	Open-drain driving		500		

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6.9 Switching Characteristics (V_{CCA} = 1.8 V ± 0.15 V)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
V_{CCB} = 2.5 V ± 0.2 V						
t_{PHL}	A	B	Push-pull driving		5.3	ns
			Open-drain driving	2.3	8.8	
t_{PLH}			Push-pull driving		6.8	
			Open-drain driving		50	
t_{PHL}	B	A	Push-pull driving		4.4	ns
			Open-drain driving	1.9	5.3	
t_{PLH}			Push-pull driving		5.3	
			Open-drain driving		5.3	
t_{en}	OE	A or B			200	ns
t_{dis}	OE	A or B	with external load		200	ns
			no external load		200	ns
t_{rA}	A-port rise time		Push-pull driving		9.5	ns
			Open-drain driving	38	165	
t_{rB}	B-port rise time		Push-pull driving		10.8	ns
			Open-drain driving	34	145	
t_{fA}	A-port fall time		Push-pull driving		5.9	ns
			Open-drain driving		6.9	
t_{fB}	B-port fall time		Push-pull driving		13.8	
			Open-drain driving		13.8	
$t_{SK(O)}$	Channel-to-channel skew				0.7	ns
Max data rate			Push-pull driving	21		Mbps
			Open-drain driving	2		
V_{CCB} = 3.3 V ± 0.3 V						
t_{PHL}	A	B	Push-pull driving		5.4	ns
			Open-drain driving	2.4	9.6	
t_{PLH}			Push-pull driving		7.1	
			Open-drain driving		40	
t_{PHL}	B	A	Push-pull driving		4.5	ns
			Open-drain driving	1.1	4.4	
t_{PLH}			Push-pull driving		4.5	
			Open-drain driving		4.5	
t_{en}	OE	A or B			200	ns
t_{dis}	OE	A or B	with external load		200	ns
			no external load		200	ns
t_{rA}	A-port rise time		Push-pull driving		9.3	ns
			Open-drain driving	30	132	
t_{rB}	B-port rise time		Push-pull driving		9.1	ns
			Open-drain driving	23	106	
t_{fA}	A-port fall time		Push-pull driving		6	ns
			Open-drain driving		6.4	
t_{fB}	B-port fall time		Push-pull driving		16.2	ns
			Open-drain driving		16.2	
$t_{SK(O)}$	Channel-to-channel skew				0.7	ns
Max data rate			Push-pull driving	22		Mbps
			Open-drain driving	2		

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Switching Characteristics (V_{CCA} = 1.8 V ± 0.15 V) (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
V_{CCB} = 5 V ± 0.5 V						
t_{PHL}	A	B	Push-pull driving		6.8	ns
			Open-drain driving	2.6	10	
t_{PLH}			Push-pull driving		7.5	
			Open-drain driving		33	
t_{PHL}	B	A	Push-pull driving		4.7	ns
			Open-drain driving	1.2	4	
t_{PLH}			Push-pull driving		0.5	
			Open-drain driving		0.5	
t_{en}	OE	A or B			200	ns
t_{dis}	OE	A or B	with external load		200	ns
			no external load		200	ns
t_{rA}	A-port rise time		Push-pull driving		7.6	ns
			Open-drain driving	22	95	
t_{rB}	B-port rise time		Push-pull driving		7.6	ns
			Open-drain driving	10	58	
t_{fA}	A-port fall time		Push-pull driving		13.3	ns
			Open-drain driving		6.1	
t_{fB}	B-port fall time		Push-pull driving		16.2	ns
			Open-drain driving		16.2	
$t_{SK(O)}$	Channel-to-channel skew				0.7	ns
Max data rate			Push-pull driving	24		Mbps
			Open-drain driving	2		

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6.10 Switching Characteristics (V_{CCA} = 2.5 V ± 0.2 V)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
V_{CCB} = 2.5 V ± 0.2 V						
t_{PHL}	A	B	Push-pull driving		3.2	ns
			Open-drain driving	1.7	6.3	
t_{PLH}			Push-pull driving		3.5	
			Open-drain driving		3.5	
t_{PHL}	B	A	Push-pull driving		3	ns
			Open-drain driving	1.8	4.7	
t_{PLH}			Push-pull driving		2.5	
			Open-drain driving		2.5	
t_{en}	OE	A or B			200	ns
t_{dis}	OE	A or B	with external load		200	ns
			no external load		200	ns
t_{rA}	A-port rise time		Push-pull driving		7.4	ns
			Open-drain driving	34	149	
t_{rB}	B-port rise time		Push-pull driving		8.3	ns
			Open-drain driving	35	151	
t_{fA}	A-port fall time		Push-pull driving		5.7	ns
			Open-drain driving		6.9	
t_{fB}	B-port fall time		Push-pull driving		7.8	
			Open-drain driving		8.8	
$t_{SK(O)}$	Channel-to-channel skew				0.7	ns
Max data rate			Push-pull driving	20		Mbps
			Open-drain driving	2		
V_{CCB} = 3.3 V ± 0.3 V						
t_{PHL}	A	B	Push-pull driving		3.7	ns
			Open-drain driving	2	6	
t_{PLH}			Push-pull driving		4.1	
			Open-drain driving		4.1	
t_{PHL}	B	A	Push-pull driving		3.6	ns
			Open-drain driving	2.6	4.2	
t_{PLH}			Push-pull driving		1.6	
			Open-drain driving		1.6	
t_{en}	OE	A or B			200	ns
t_{dis}	OE	A or B	with external load		200	ns
			no external load		200	ns
t_{rA}	A-port rise time		Push-pull driving		6.6	ns
			Open-drain driving	28	121	
t_{rB}	B-port rise time		Push-pull driving		7.2	ns
			Open-drain driving	24	112	
t_{fA}	A-port fall time		Push-pull driving		5.5	ns
			Open-drain driving		6.2	
t_{fB}	B-port fall time		Push-pull driving		6.7	ns
			Open-drain driving		9.4	
$t_{SK(O)}$	Channel-to-channel skew				0.7	ns
Max data rate			Push-pull driving	22		Mbps
			Open-drain driving	2		

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Switching Characteristics (V_{CCA} = 2.5 V ± 0.2 V) (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
V_{CCB} = 5 V ± 0.5 V						
t_{PHL}	A	B	Push-pull driving		3.8	ns
			Open-drain driving	2.1	5.8	
t_{PLH}			Push-pull driving		4.4	
			Open-drain driving		4.4	
t_{PHL}	B	A	Push-pull driving		4.3	ns
			Open-drain driving	1.2	4	
t_{PLH}			Push-pull driving		1	
			Open-drain driving		1	
t_{en}	OE	A or B			200	ns
t_{dis}	OE	A or B	with external load		200	ns
			no external load		200	ns
t_{rA}	A-port rise time		Push-pull driving		5.6	ns
			Open-drain driving	24	89	
t_{rB}	B-port rise time		Push-pull driving		6.1	ns
			Open-drain driving	12	64	
t_{fA}	A-port fall time		Push-pull driving		5.3	ns
			Open-drain driving		5.8	
t_{fB}	B-port fall time		Push-pull driving		6.6	ns
			Open-drain driving		10.4	
$t_{SK(O)}$	Channel-to-channel skew				0.7	ns
Max data rate			Push-pull driving	24		Mbps
			Open-drain driving	2		

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6.11 Switching Characteristics (V_{CCA} = 3.3 V ± 0.3 V)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
V_{CCB} = 3.3 V ± 0.3 V						
t_{PHL}	A	B	Push-pull driving		2.4	ns
			Open-drain driving	1.3	4.2	
t_{PLH}			Push-pull driving		4.2	
			Open-drain driving		4.2	
t_{PHL}	B	A	Push-pull driving		2.5	ns
			Open-drain driving	1	124	
t_{PLH}			Push-pull driving		2.5	
			Open-drain driving		2.5	
t_{en}	OE	A or B			200	ns
t_{dis}	OE	A or B	with external load		200	ns
			no external load		200	ns
t_{rA}	A-port rise time		Push-pull driving		5.6	ns
			Open-drain driving	25	116	
t_{rB}	B-port rise time		Push-pull driving		6.4	ns
			Open-drain driving	26	116	
t_{fA}	A-port fall time		Push-pull driving		5.4	ns
			Open-drain driving		6.1	
t_{fB}	B-port fall time		Push-pull driving		7.4	ns
			Open-drain driving		7.6	
$t_{SK(O)}$	Channel-to-channel skew				0.7	ns
Max data rate			Push-pull driving	23		Mbps
			Open-drain driving	2		
V_{CCB} = 5 V ± 0.5 V						
t_{PHL}	A	B	Push-pull driving		3.1	ns
			Open-drain driving	1.4	4.6	
t_{PLH}			Push-pull driving		4.4	
			Open-drain driving		4.4	
t_{PHL}	B	A	Push-pull driving		3.3	ns
			Open-drain driving	1	97	
t_{PLH}			Push-pull driving		2.6	
			Open-drain driving		2.6	
t_{en}	OE	A or B			200	ns
t_{dis}	OE	A or B	with external load		200	ns
			no external load		200	ns
t_{rA}	A-port rise time		Push-pull driving		4.8	ns
			Open-drain driving	19	85	
t_{rB}	B-port rise time		Push-pull driving		7.4	ns
			Open-drain driving	14	72	
t_{fA}	A-port fall time		Push-pull driving		5	ns
			Open-drain driving		5.7	
t_{fB}	B-port fall time		Push-pull driving		7.6	ns
			Open-drain driving		8.3	
$t_{SK(O)}$	Channel-to-channel skew				0.7	ns
Max data rate			Push-pull driving	24		Mbps
			Open-drain driving	2		

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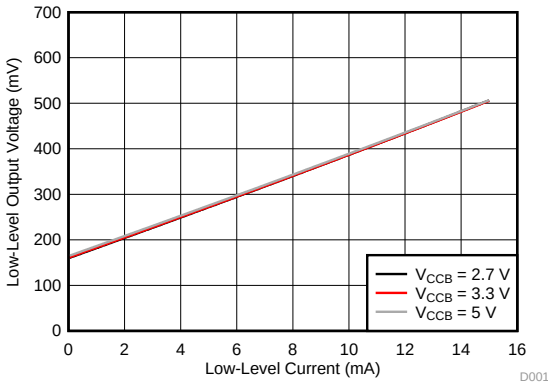
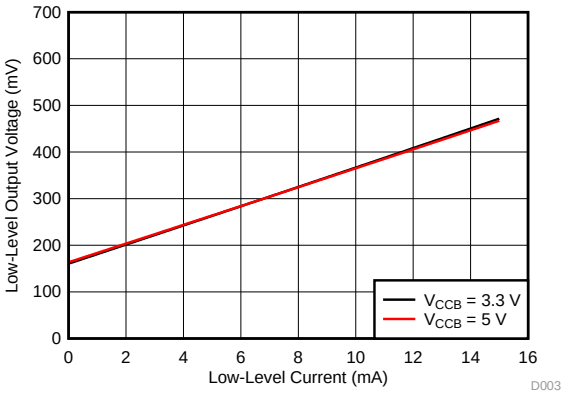
6.12 Typical Characteristics



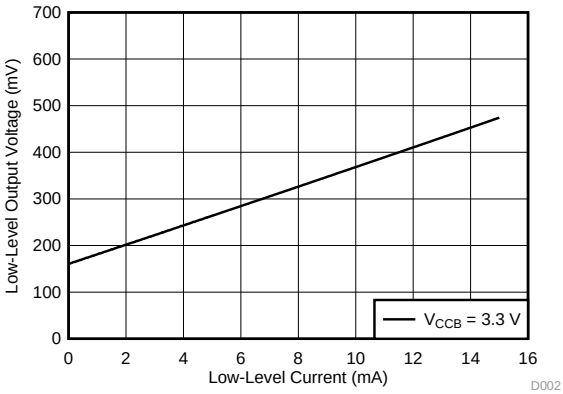
V_{CCA} = 1.8 V $V_{IL(A)}$ = 150 mV

Figure 1. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)



V_{CCA} = 2.7 V $V_{IL(A)}$ = 150 mV

Figure 2. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)



V_{CCA} = 3.3 V $V_{IL(A)}$ = 150 mV

Figure 3. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)

7 Parameter Measurement Information

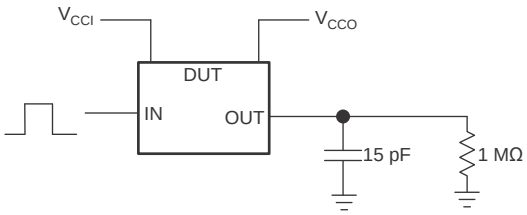


Figure 4. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using a Push-Pull Driver

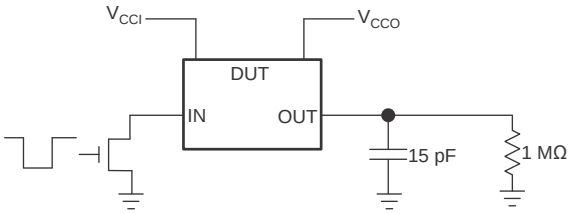
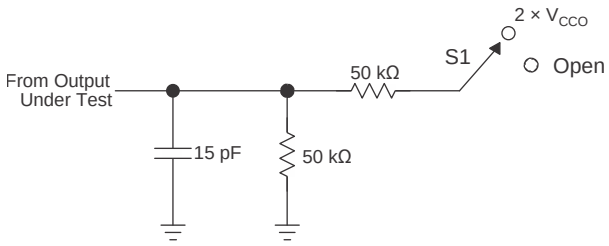


Figure 5. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time and Fall-Time Measurement Using an Open-Drain Driver



TEST	S1
t_{PZL} / t_{PLZ}	2 × V_{CCO}
t_{PHZ} / t_{PZH}	Open

Figure 6. Load Circuit for Enable-Time and Disable-Time Measurement

1. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
2. t_{PZL} and t_{PZH} are the same as t_{en}.
3. V_{CCI} is the V_{CC} associated with the input port.
4. V_{CCO} is the V_{CC} associated with the output port.

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Parameter Measurement Information (continued)

7.1 Voltage Waveforms

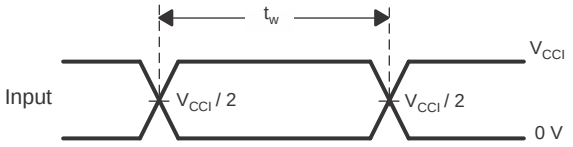


Figure 7. Pulse Duration

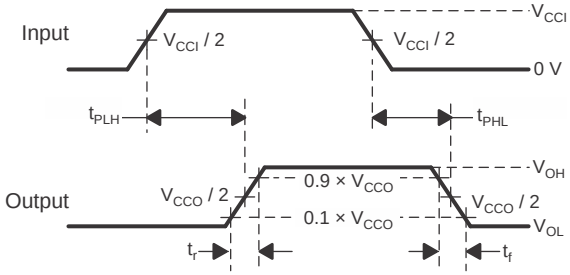


Figure 8. Propagation Delay Times

A. C_L includes probe and jig capacitance.

B. Waveform 1 in Figure 9 is for an output with internal such that the output is high, except when OE is high (see Figure 6). Waveform 2 in Figure 9 is for an output with conditions such that the output is low, except when OE is high.

C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

H. V_{CCI} is the V_{CC} associated with the input port.

I. V_{CCO} is the V_{CC} associated with the output port.

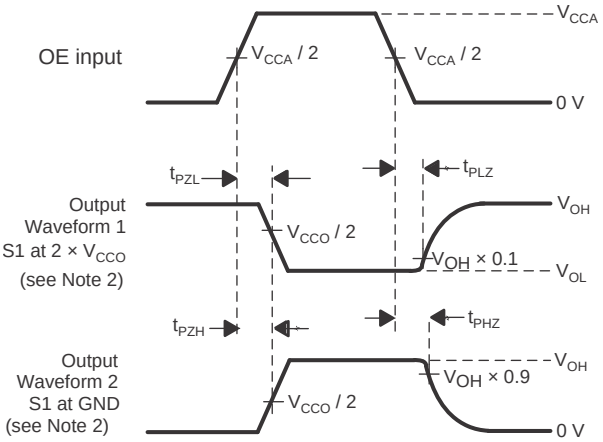


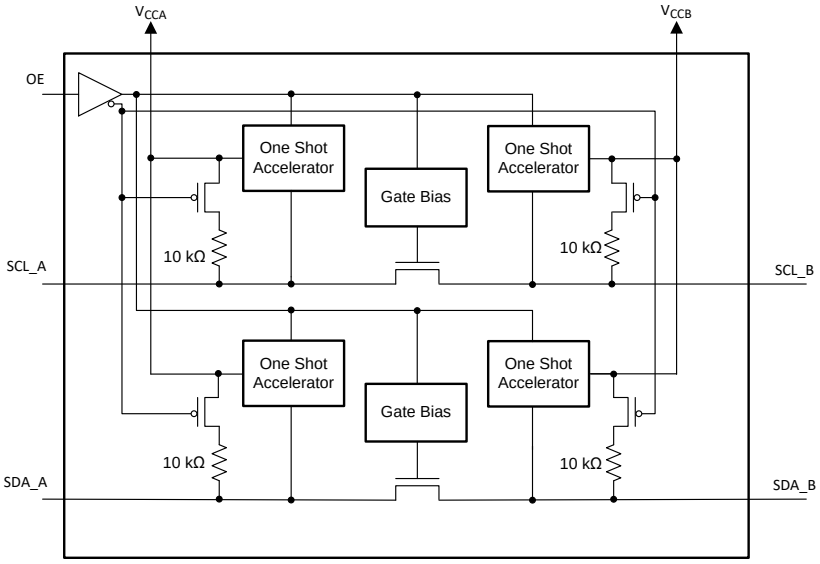
Figure 9. Enable and Disable Times

8 Detailed Description

8.1 Overview

The TCA9406 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.65 V to 3.6 V, while the B port can accept I/O voltages from 2.3 V to 5.5 V. The device is a pass-gate architecture with edge-rate accelerators (one-shots) to improve the overall data rate. 10-kΩ pullup resistors, commonly used in open-drain applications, have been conveniently integrated so that an external resistor is not needed. When TCA9406 is disabled the internal pull up resistors are also disabled. While this device is designed for open-drain applications which makes it ideal for I^2C and SMBus applications, the device can also translate push-pull CMOS logic outputs.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Architecture

The TCA9406 architecture (see Figure 5) is an auto-direction-sensing based translator that does not require a direction-control signal to control the direction of data flow from A to B or from B to A.

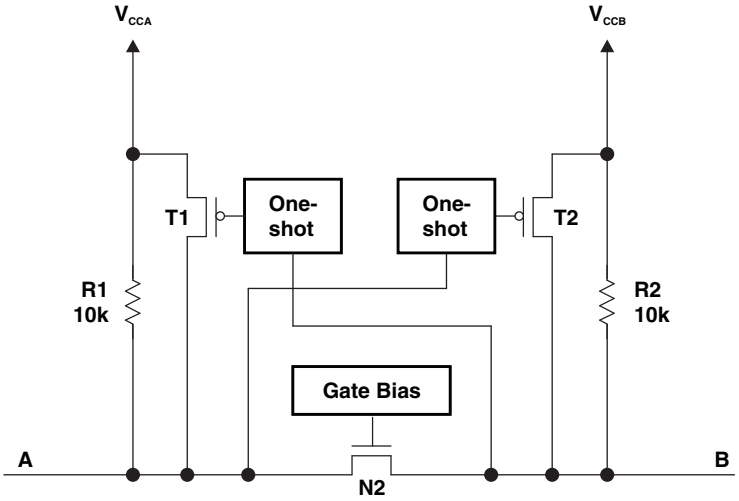


Figure 10. Architecture of a TCA9406 Cell

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Feature Description (continued)

These two bidirectional channels independently determine the direction of data flow without a direction-control signal. Each I/O pin is automatically reconfigured as either an input or an output, which is how this auto-direction feature is realized.

The TCA9406 is part of TI's "Switch" type voltage translator family and employs two key circuits to enable this voltage translation:

1) An N-channel pass-gate transistor topology that ties the A-port to the B-port

and

2) Output one-shot (O.S.) edge-rate accelerator circuitry to detect and accelerate rising edges on the A or B ports

For bidirectional voltage translation, pullup resistors are included on the device for dc current sourcing capability. The V_{GATE} gate bias of the N-channel pass transistor is set at approximately one threshold voltage (V_T) above the V_{CC} level of the low-voltage side. Data can flow in either direction without guidance from a control signal.

The O.S. rising-edge rate accelerator circuitry speeds up the output slew rate by monitoring the input edge for transitions, helping maintain the data rate through the device. During a low-to-high signal rising edge, the O.S. circuits turn on the PMOS transistors (T1, T2) to increase the current drive capability of the driver for approximately 30 ns or 95% of the input edge, whichever occurs first. This edge-rate acceleration provides high ac drive by bypassing the internal 10-kΩ pullup resistors during the low-to-high transition to speed up the signal. The output resistance of the driver is decreased to approximately 50 Ω to 70 Ω during this acceleration phase. To minimize dynamic I_{CC} and the possibility of signal contention, the user should wait for the O.S. circuit to turn off before applying a signal in the opposite direction. The worst-case duration is equal to the minimum pulse-width number provided in the *Timing Requirements* section of this data sheet.

8.3.2 Input Driver Requirements

The continuous dc-current "sinking" capability is determined by the external system-level open-drain (or push-pull) drivers that are interfaced to the TCA9406 I/O pins. Since the high bandwidth of these bidirectional I/O circuits is used to facilitate this fast change from an input to an output and an output to an input, they have a modest dc-current "sourcing" capability of hundreds of micro-Amps, as determined by the internal 10-kΩ pullup resistors.

The fall time (t_{fA}, t_{fB}) of a signal depends on the edge-rate and output impedance of the external device driving TCA9406 data I/Os, as well as the capacitive loading on the data lines.

Similarly, the t_{PHL} and max data rates also depend on the output impedance of the external driver. The values for t_{fA}, t_{fB}, t_{PHL}, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50 Ω.

8.3.3 Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper O.S. triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 30 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic ICC, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the TCA9406 output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. re-triggering, bus contention, output signal oscillations, or other adverse system-level affects.

8.3.4 Enable and Disable

The TCA9406 has an OE input that is used to disable the device by setting OE low, which places all I/Os in the Hi-Z state. When TCA9406 is disabled, the internal pull up resistors are also disabled meaning if no external pull up resistors are present then the SDA/SCL lines will be left floating. The disable time (t_{dis}) indicates the delay between the time when OE goes low and when the outputs are disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

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Feature Description (continued)

8.3.5 Pullup Resistors on I/O Lines

Each A-port I/O has an internal 10-kΩ pullup resistor to V_{CCA}, and each B-port I/O has an internal 10-kΩ pullup resistor to V_{CCB}. If a smaller value of pullup resistor is required, an external resistor must be added from the I/O to V_{CCA} or V_{CCB} (in parallel with the internal 10-kΩ resistors). Adding lower value pullup resistors will effect V_{OL} levels, however. The internal pullups of the TCA9406 are disabled when the OE pin is low.

8.4 Device Functional Modes

The TCA9406 device has two functional modes, enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high impedance state. Setting the OE input high will enable the device.

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9 Application and Implementation

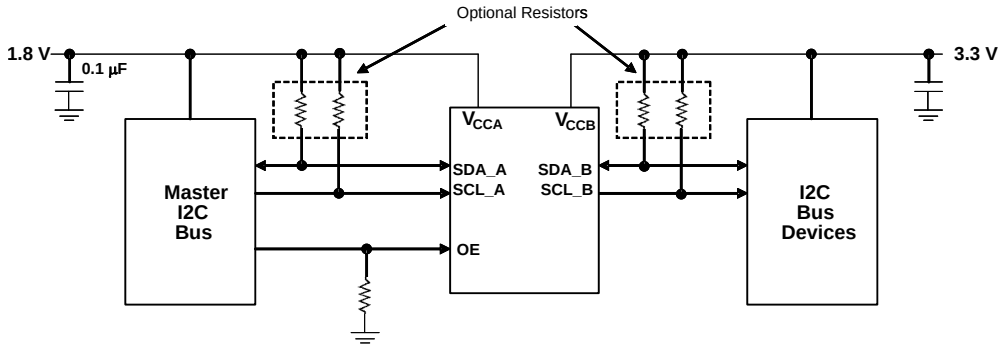
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TCA9406 can be used to bridge the digital-switching compatibility gap between two voltage nodes to successfully interface logic threshold levels found in electronic systems. It should be used in a point-to-point topology for interfacing devices or systems operating at different interface voltages with one another. Its primary target application use is for interfacing with open-drain drivers on the data I/Os such as I^2C or SMBus, where the data is bidirectional and no control signal is available.

9.2 Typical Application



Design Notes: OE can be tied directly to 1.8 V (V_{CCA}) to always be in ENABLE mode.

Figure 11. Typical Application Circuit

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1. And make sure the $V_{CCA} \leq V_{CCB}$.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.65 to 3.6 V
Output voltage range	2.3 to 5.5 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TCA9406 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the TCA9406 device is driving to determine the output voltage range
  - The TCA9406 device has 10-kΩ internal pullup resistors. External pullup resistors can be added to reduce the total RC of a signal trace if necessary.

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9.2.3 Application Curve

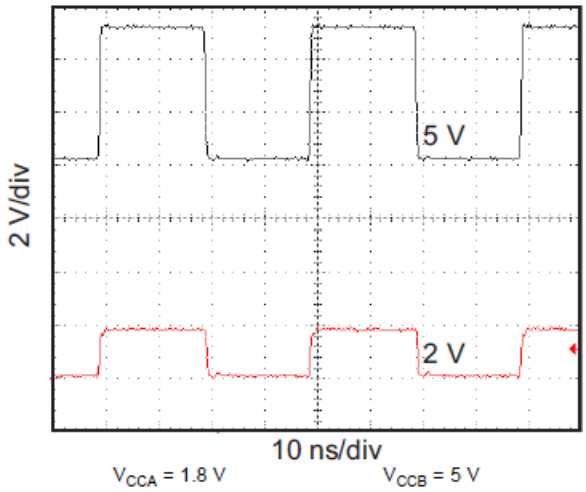

Figure 12. Level-Translation of a 2.5-MHz Signal

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10 Power Supply Recommendations

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. The sequencing of each power supply will not damage the device during the power up operation, so either power supply can be ramped up first. The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, the following common printed-circuit board layout guidelines are recommended:

- Bypass capacitors should be used on power supplies and should be placed as close as possible to the V_{CCA}, V_{CCB} pin, and G_{ND} pin.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 30 ns, ensuring that any reflection encounters low impedance at the source driver.

11.2 Layout Example

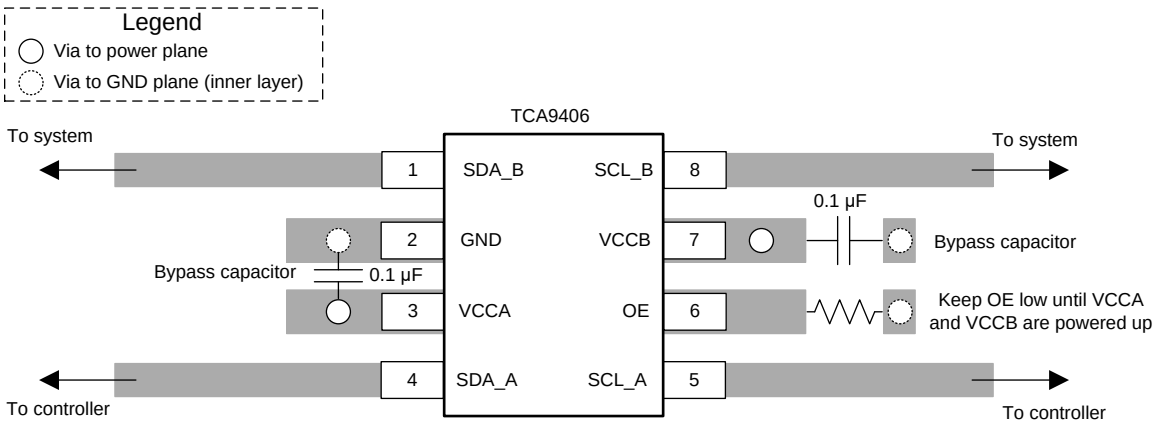

Figure 13. TCA9406 Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9406DCTR	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NF9 (R, Z)	Samples
TCA9406DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(F9, NF9R) NZ	Samples
TCA9406YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	7W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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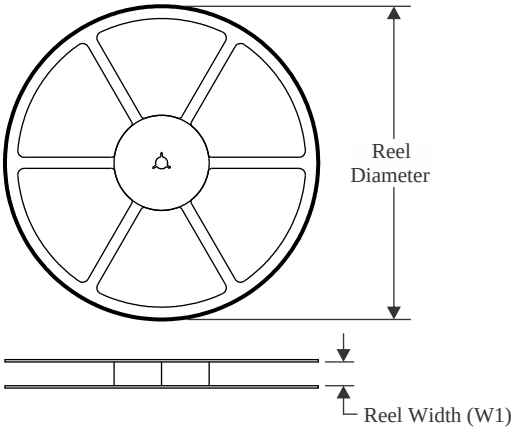
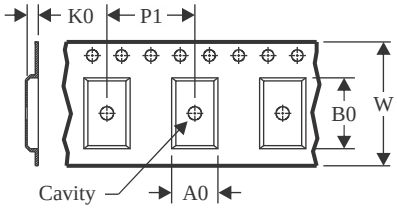
TAPE AND REEL INFORMATION

REEL DIMENSIONS

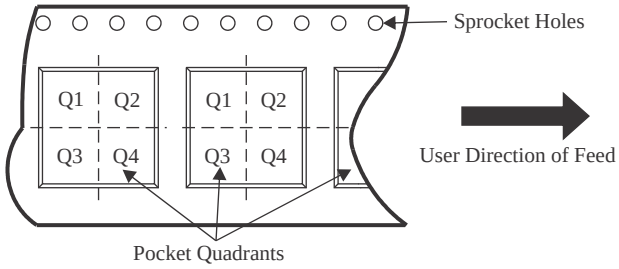


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

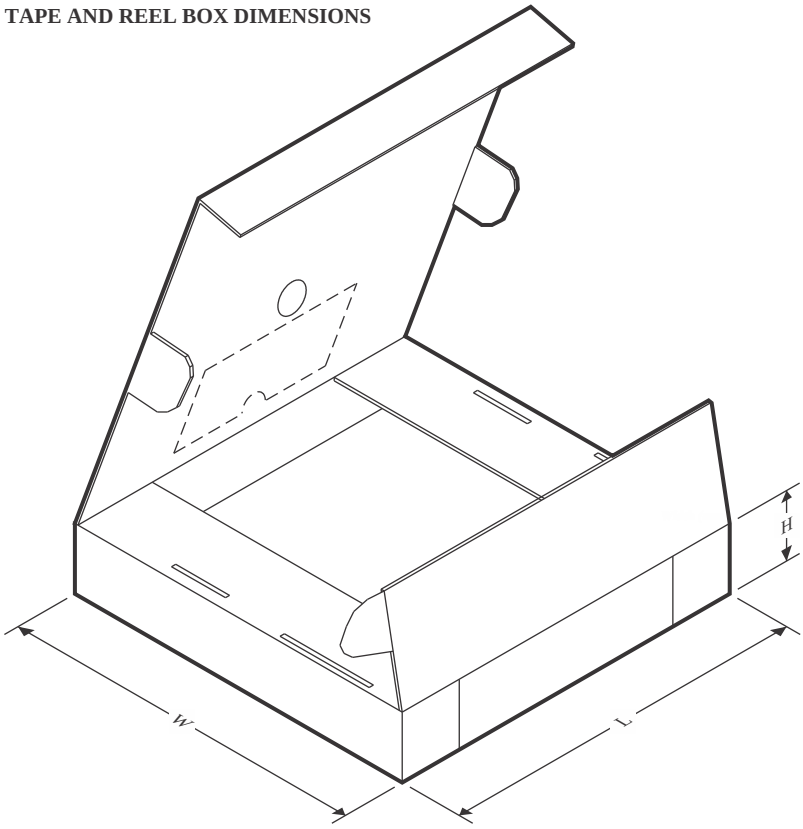
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9406DCTR	SM8	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
TCA9406DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
TCA9406DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.25	3.4	1.0	4.0	8.0	Q3
TCA9406DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TCA9406YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.11	2.1	0.56	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

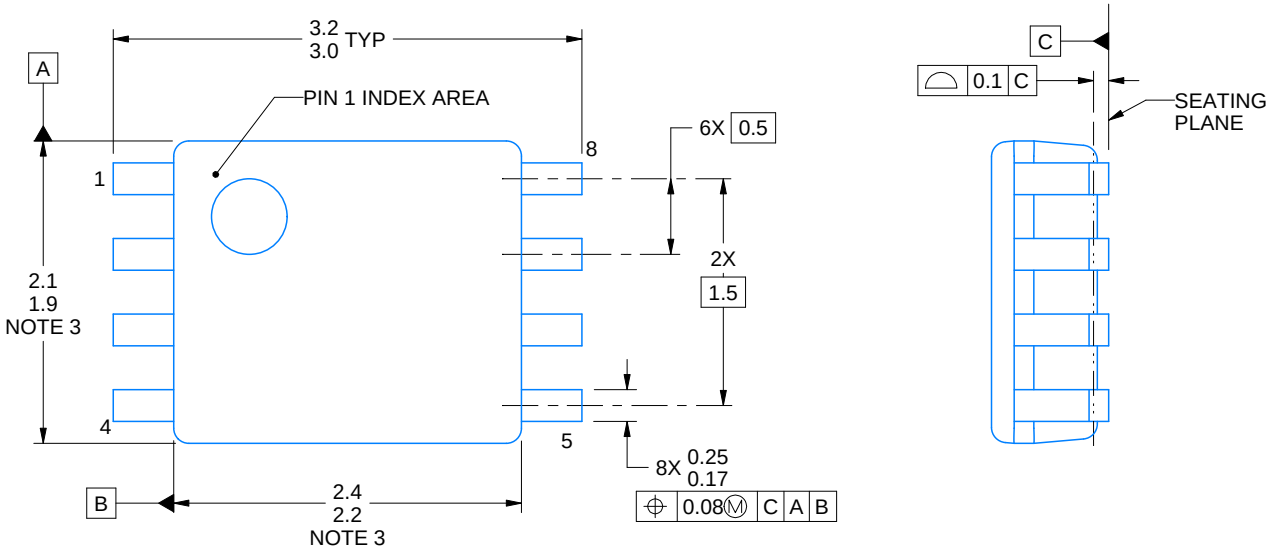
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9406DCTR	SM8	DCT	8	3000	183.0	183.0	20.0
TCA9406DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
TCA9406DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0
TCA9406DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TCA9406YZPR	DSBGA	YZP	8	3000	182.0	182.0	20.0

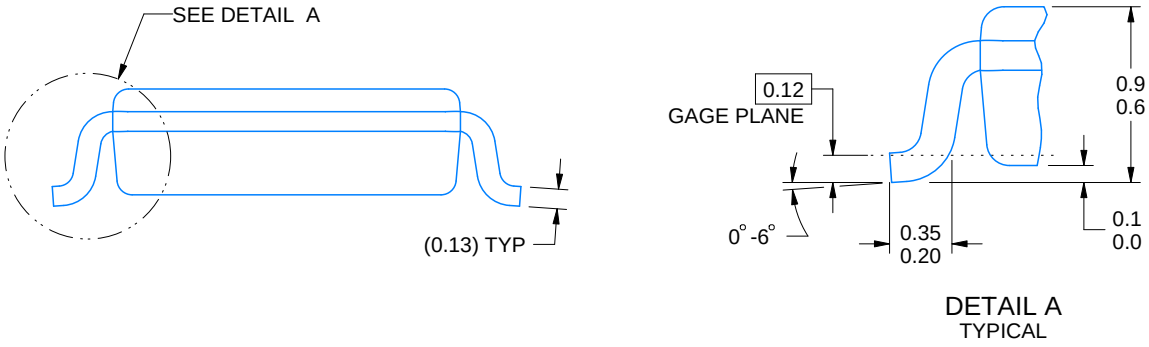
DCU0008A

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

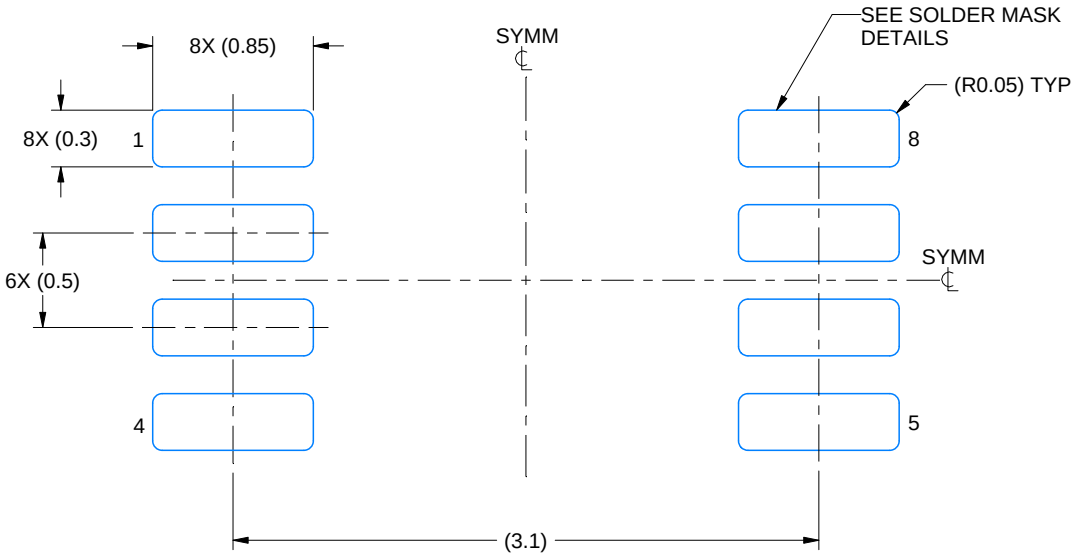




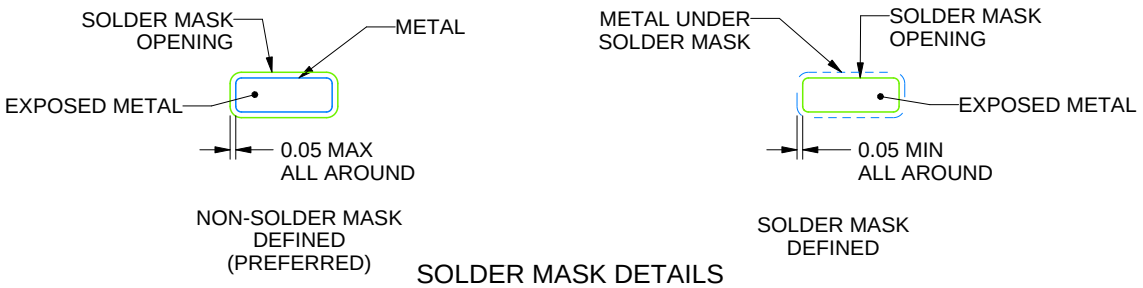
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

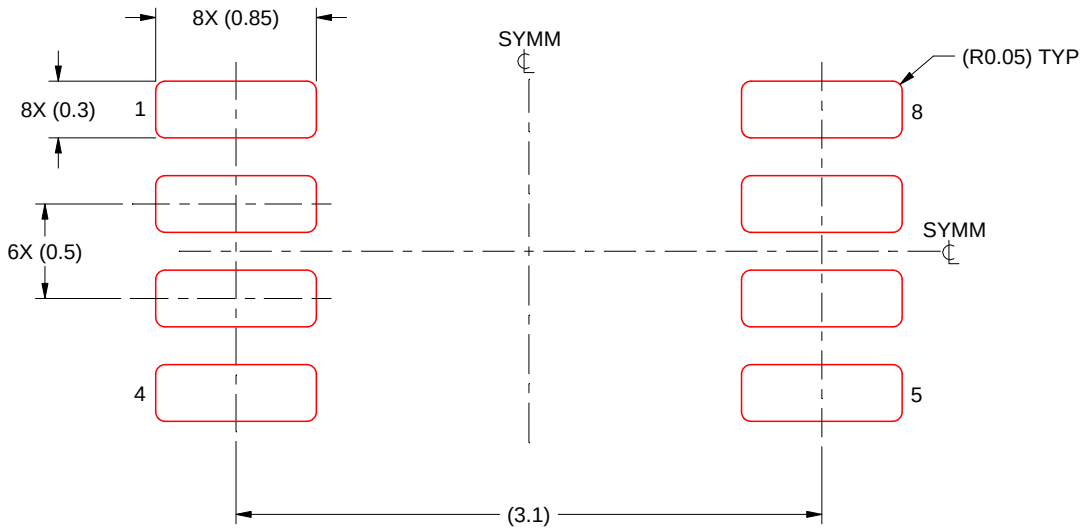


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

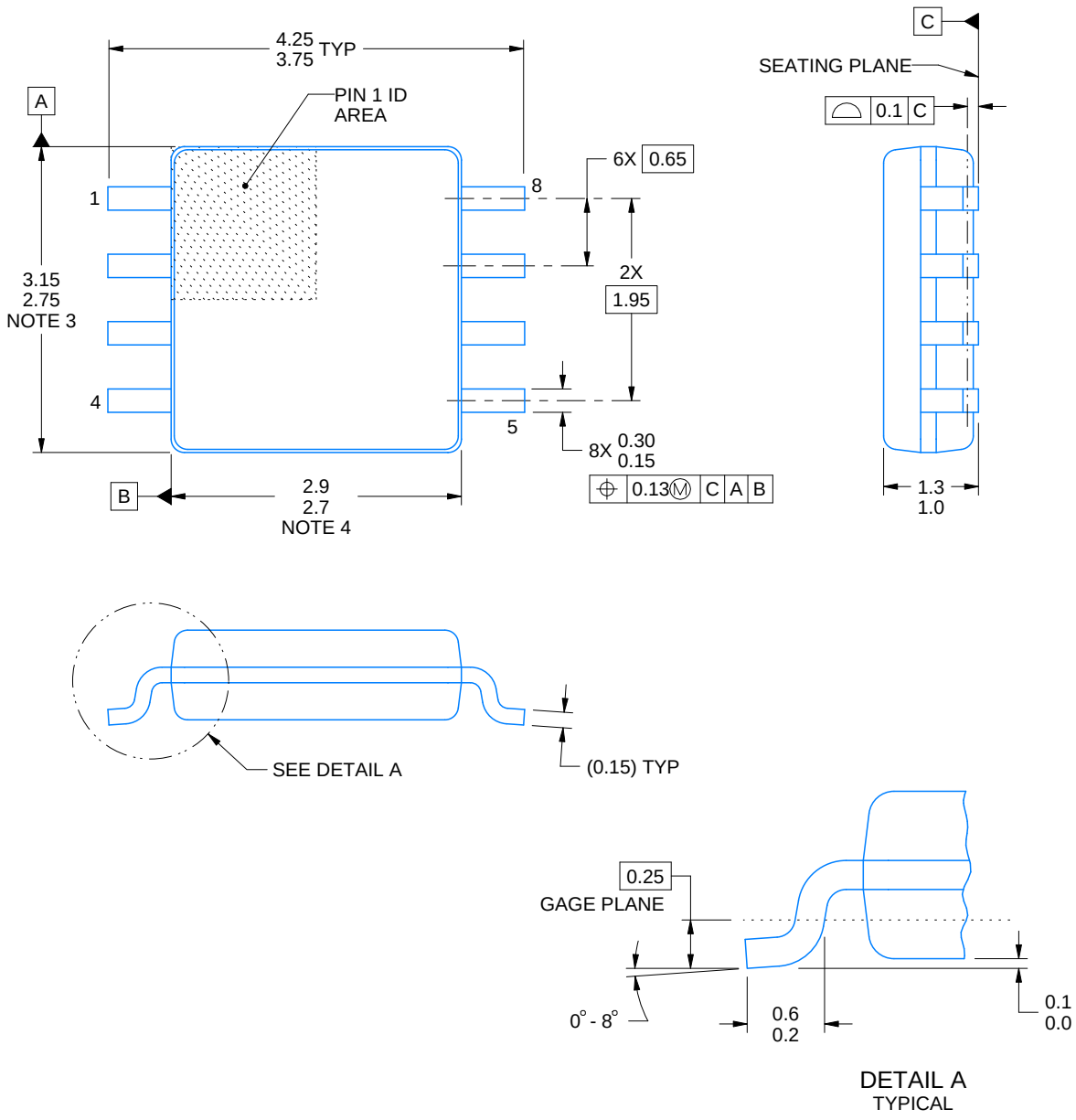
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCT0008A

SSOP - 1.3 mm max height

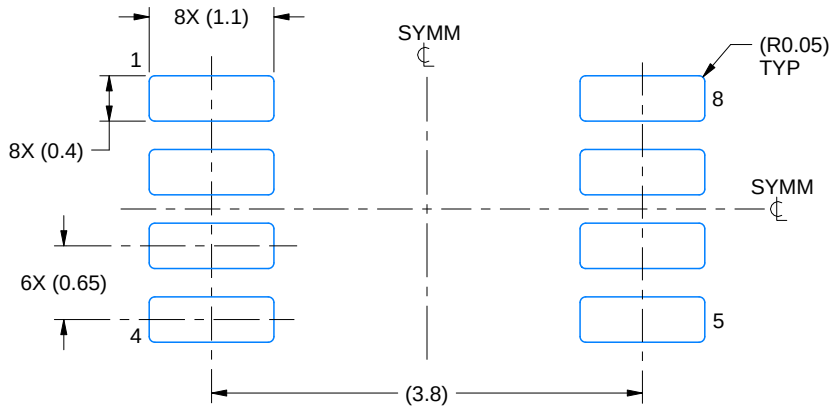
SMALL OUTLINE PACKAGE



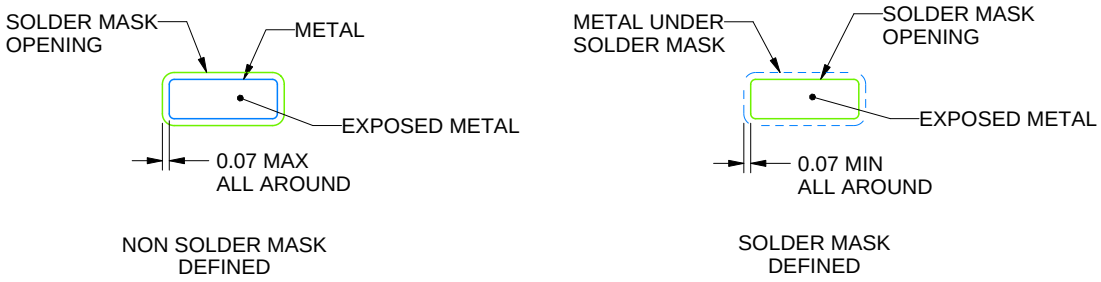
4220784/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

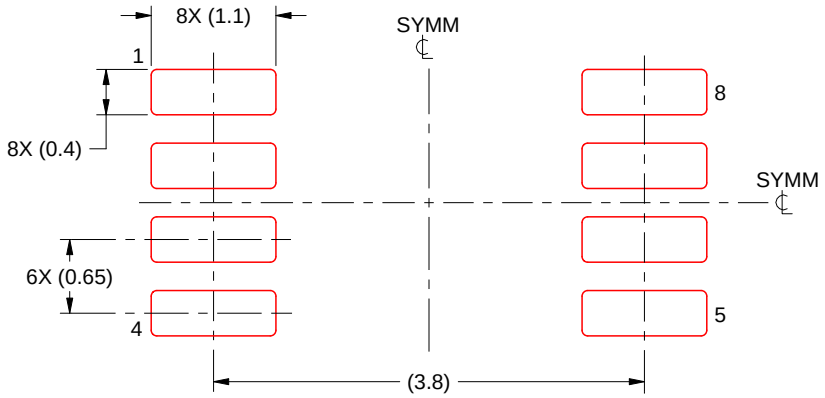


SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

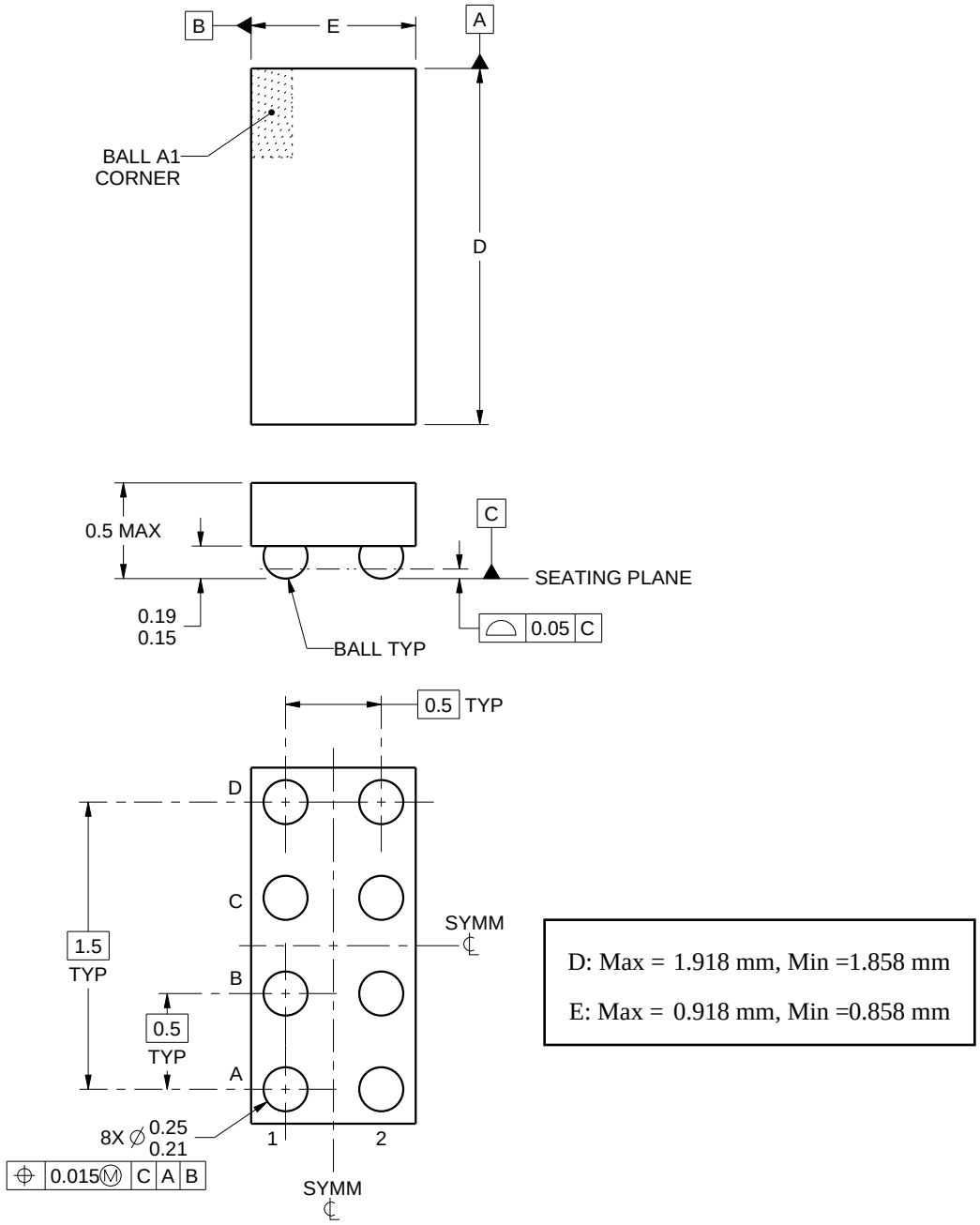
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0008

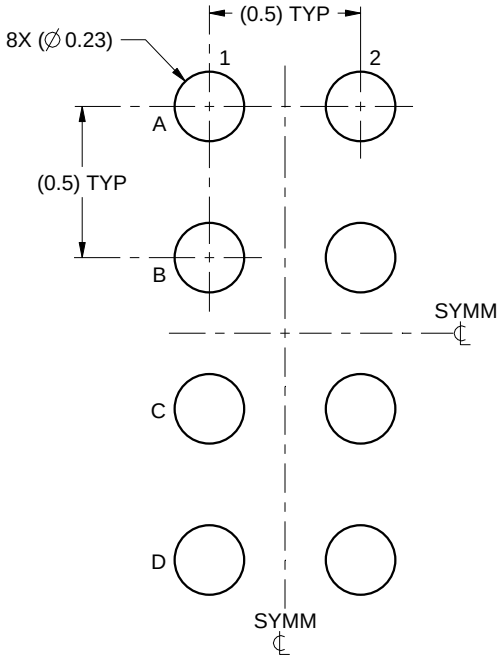
DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

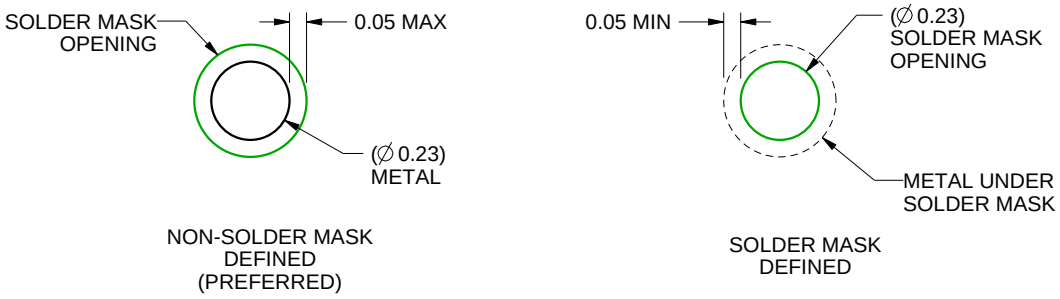


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

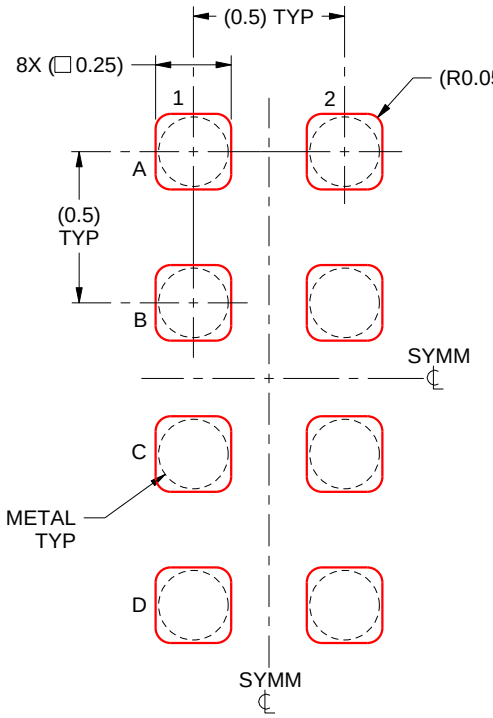


SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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