TCAN104xAV-Q1 Automotive Dual CAN FD Transceiver with 1.8-V I/O Support and Standby Mode

1 Features

- AEC-Q100 (Grade 1): Qualified for automotive applications
- Two high-speed CAN transceivers with independent mode control
- Meets the requirements of ISO 11898-2:2016 physical layer standard
- Functional Safety-Capable
  - Documentation available to aid in functional safety system design
- Support of classical CAN and optimized CAN FD performance at 2, 5, and 8 Mbps
  - Short and symmetrical propagation delays for enhanced timing margin
- I/O voltage range supports 1.7 V to 5.5 V
- Support for 12-V and 24-V battery applications
- Receiver common-mode input voltage: ±12 V
- Protection features:
  - Bus fault protection: ±58 V
  - Undervoltage protection
  - TXD-dominant time-out (DTO)
    - Data rates down to 9.2 kbps
  - Thermal-shutdown protection (TSD)
- Operating modes:
  - Normal mode
  - Low power standby mode supporting remote wake-up request
- Optimized behavior when unpowered
  - Bus and logic pins are high impedance (no load to operating bus or application)
  - Hot-plug capable: power-up and power-down glitch-free operation on bus and RXD output
- Junction temperatures from: –40°C to 150°C
- Available in space-saving SOT-23, SOIC (14) and leadless VSON (14) packages (4.5 mm x 3.0 mm) with improved automated optical inspection (AOI) capability

2 Applications

- Automotive and Transportation
  - Body control modules
  - Automotive gateway
  - Advanced driver assistance system (ADAS)
  - Infotainment

3 Description

The TCAN1046AV-Q1 and TCAN1048AV-Q1 (TCAN104xAV-Q1) are dual, high-speed controller area network (CAN) transceivers that meet the physical layer requirements of the ISO 11898-2:2016 high-speed CAN specification.

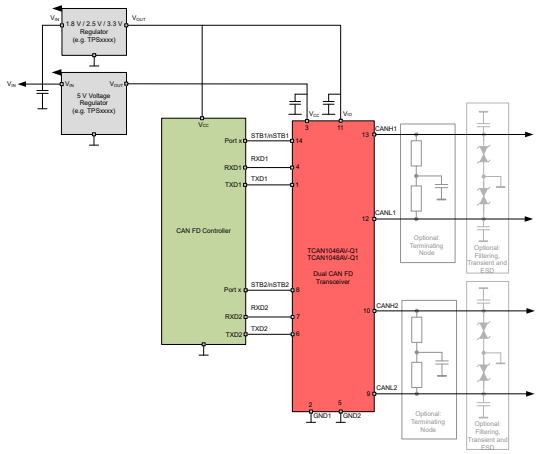
The TCAN104xAV-Q1 transceivers support both classical CAN and CAN FD networks up to 8 megabits per second (Mbps). The device includes internal logic level translation via the V_{IO} terminal to allow for interfacing the transceiver I/O's directly to 1.8-V, 2.5-V, 3.3-V, or 5-V logic levels.

The two CAN channels support independent mode control through the standby pins. Therefore, each transceiver can be placed into a low-power state, standby mode, without impacting the state of the other CAN channel. While in standby mode, the device supports remote wake-up pattern via the CAN bus which is compliant to the ISO 11898-2:2016 defined wake-up pattern (WUP).

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TCAN1046AV-Q1	VSON (14)	4.50 mm x 3.00 mm
	SOIC (14)	8.65 mm x 3.91 mm
	SOT-23 (14)	4.20 mm × 2 mm
TCAN1048AV-Q1	VSON (14)	4.50 mm x 3.00 mm
	SOIC (14)	8.95 mm x 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematics

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2021) to Revision A (December 2021)	Page
• Changed the document status from: *Advanced Information* to: *Production* data	1

5 Description Continued

The transceivers also include many protection and diagnostic features including thermal-shutdown (TSD), TXD-dominant time-out (DTO), supply undervoltage detection, and bus fault protection up to ±58 V. The devices have defined failsafe behavior in supply undervoltage or floating pin scenarios.

6 Device Comparison

Table 6-1. Device Comparison Table

Part Number	Bus Fault Protection on both CAN Channels	Low Voltage I/O Logic Support	Standby (STB) Pin Mode
TCAN1046AV-Q1	±58 V	Yes	Active-high
TCAN1048AV-Q1	±58 V	Yes	Active-low

7 Pin Configuration and Functions

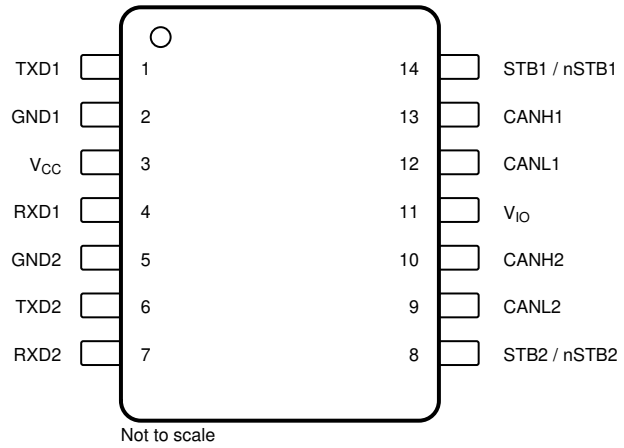


Figure 7-1. D Package, 14 Pin SOIC, Top View

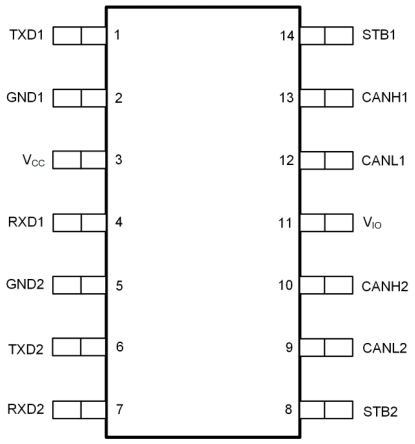


Figure 7-2. DYY Package, 14 Pin SOT-23, Top View

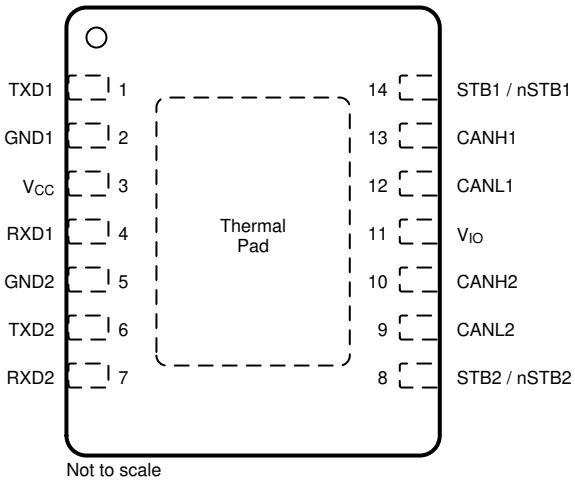


Figure 7-3. DMT Package, 14 Pin VSON, Top View

Table 7-1. Pin Functions

Pins		Type	Description
Name	No.		
TXD1	1	Digital Input	CAN transmit data input channel 1; integrated pull-up
GND1	2	GND	Ground connection
V_{CC}	3	Supply	5-V supply voltage
RXD1	4	Digital Output	CAN receive data output channel 1; tri-state when $V_{IO} < UV_{VIO}$
GND2	5	GND	Ground connection
TXD2	6	Digital Input	CAN transmit data input channel 2; integrated pull-up
RXD2	7	Digital Output	CAN receive data output channel 2; tri-state when $V_{IO} < UV_{VIO}$
STB2	8	Digital Input	Standby input of channel 2 for mode control; integrated pull-up (TCAN1046AV–Q1)
nSTB2			Standby input of channel 2 for mode control; inverse logic with integrated pull-down (TCAN1048AV–Q1)
CANL2	9	Bus IO	Low-level CAN bus channel 2 input/output line
CANH2	10	Bus IO	High-level CAN bus channel 2 input/output line
V_{IO}	11	Supply	I/O supply voltage
CANL1	12	Bus IO	Low-level CAN bus channel 1 input/output line

Table 7-1. Pin Functions (continued)

Pins		Type	Description
Name	No.		
CANH1	13	Bus IO	High-level CAN bus channel 1 input/output line
STB1	14	Digital Input	Standby input of channel 1 for mode control; integrated pull-up (TCAN1046AV–Q1)
nSTB1			Standby input of channel 1 for mode control; inverse logic with integrated pull-down (TCAN1048AV–Q1)
Thermal Pad (VSON only)		—	Connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

8 Specifications

8.1 Absolute Maximum Ratings

(1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
V_{IO}	Supply voltage I/O level shifter	–0.3	6	V
V_{BUS}	CAN Bus I/O voltage CANH1, CANL1, CANH2, CANL2	–58	58	V
V_{DIFF}	Max differential voltage between CANHx and CANLx	–45	45	V
V_{Logic_Input}	Logic input terminal voltage	–0.3	6	V
V_{RXDx}	RXDx output terminal voltage range	–0.3	6	V
$I_{O(RXDx)}$	RXDx output current	–8	8	mA
T_J	Junction temperature	–40	165	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

8.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	HBM classification level 3A for all pins	±4000	V
			HBM classification level 3B for global pins CANHx and CANLx with respect to GND	±10000	V
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C5 for all pins		±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

8.3 ESD Ratings — IEC Specifications

				VALUE	UNIT
V_{ESD}	System level Electrostatic discharge	CAN bus terminals to GND CANH1, CANL1, CANH2, CANL2	Unpowered contact discharge per ISO 10605 [1]	±8000	V
			SAE J2962-2 per ISO 10605 Powered Contact Discharge [2]	±8000	V
			SAE J2962-2 per ISO 10605 Powered Air Discharge [2]	±15000	V
V_{Tran}	Transient voltage per ISO 7637-2[3]		Pulse 1	–100	V
			Pulse 2a	75	V
			Pulse 3a	–150	V
			Pulse 3b	100	V
	Transient voltage per ISO 7637-3[4]		DCC slow transient pulse	±30	V

(1) Tested according to IEC 62228-3:2019 CAN Transceivers
(2) Results given here are specific to the SAE J2962-2 Communication Transceivers Qualification Requirements - CAN. Testing performed by OEM approved independent 3rd party, EMC report available upon request.
(3) Tested according to IEC 62228-3:2019 CAN Transceivers
(4) Tested according to SAE J2962-2

8.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IO}	Supply voltage for I/O level shifter	1.7		5.5	V
$I_{OH(RXDx)}$	RXDx terminal high-level output current	–1.5			mA
$I_{OL(RXDx)}$	RXDx terminal low-level output current			1.5	mA
T_J	Operating junction temperature	-40		150	℃

8.5 Thermal Characteristics

THERMAL METRIC(1)		TCAN1046AV-Q1 / TCAN1048AV-Q1			UNIT
		D (SOIC)	DYY (SOT)	DMT (VSON)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75.8	87.2	38.1	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.8	35.2	38.7	℃/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.4	31.6	15.0	℃/W
Ψ_{JT}	Junction-to-top characterization parameter	6.6	11.2	2.0	℃/W
Ψ_{JB}	Junction-to-board characterization parameter	37.0	31.5	15.0	℃/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	5.9	℃/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8.6 Supply Characteristics

Over recommended operating conditions with T_J = -40°C to 150°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current Normal mode	Dominant One Channel(1)	TCAN1046AV: STB1 = STB2 = 0 V TCAN1048AV: nSTB1 = nSTB2 = V_{IO} TXDx = 0 V, TXDy = V_{IO} R_{L1} = R_{L2} = 60 Ω, C_L = open; See Figure 9-1		50	77.5	mA
			TCAN1046AV: STB1 = STB2 = 0 V TCAN1048AV: nSTB1 = nSTB2 = V_{IO} TXDx = 0 V, TXDy = V_{IO} R_{L1} = R_{L2} = 50 Ω, C_L = open; See Figure 9-1		55	87.5	mA
		Dominant Two channels(1)	TCAN1046AV: STB1 = STB2 = 0 V TCAN1048AV: nSTB1 = nSTB2 = V_{IO} TXDx = TXDy = 0 V R_{L1} = R_{L2} = 60 Ω, C_L = open; See Figure 9-1		95	140	mA
		Dominant Two channels(1)	TCAN1046AV: STB1 = STB2 = 0 V TCAN1048AV: nSTB1 = nSTB2 = V_{IO} TXDx = TXDy = 0 V R_{L1} = R_{L2} = 50 Ω, C_L = open; See Figure 9-1		100	160	mA
		Recessive Two channels	TCAN1046AV: STB1 = STB2 = 0 V TCAN1048AV: nSTB1 = nSTB2 = V_{IO} TXDx = TXDy = V_{IO} R_{L1} = R_{L2} = 50 Ω, C_L = open; See Figure 9-1		10	15	mA
		CANx dominant with bus fault CANy recessive(1) (2)	TCAN1046AV: STB1 = STB2 = 0 V TCAN1048AV: nSTB1 = nSTB2 = V_{IO} TXDx = TXDy = V_{IO} CANHx = CANLx = ±25 V R_{Lx} = open, R_{Ly} = 50 Ω, C_L = open; See Figure 9-1		90	137.5	mA
		CANx dominant with bus fault CANy dominant(1) (2)	TCAN1046AV: STB1 = STB2 = 0 V TCAN1048AV: nSTB1 = nSTB2 = V_{IO} TXDx = TXDy = 0 V CANHx = CANLx = ±25 V R_{Lx} = open, R_{Ly} = 50 Ω, C_L = open; See Figure 9-1		135	210	mA
		CANx and CANy dominant with bus fault(1) (2)	TCAN1046AV: STB1 = STB2 = 0 V TCAN1048AV: nSTB1 = nSTB2 = V_{IO} TXDx = TXDy = 0 V CANH1 = CANL1 = ±25 V CANH2 = CANL2 = ±25 V R_{Lx} = R_{Ly} = open, C_L = open; See Figure 9-1		170	260	mA
	Supply current Standby mode		TCAN1046AV: STB1 = STB2 = V_{IO} TCAN1048AV: nSTB1 = nSTB2 = 0 V TXDx = TXDy = V_{IO} R_{Lx} = R_{Ly} = 60 Ω, C_L = open See Figure 9-1		0.4	3	µA

8.6 Supply Characteristics (continued)

Over recommended operating conditions with T_J = -40°C to 150°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IO}	I/O supply current Normal mode	Dominant One channel(1)	TCAN1046AV: STB1 = STB2 = 0 V TCAN1048AV: nSTB1 = nSTB2 = V_{IO} TXDx = 0 V, TXDy = V_{IO} R_{Lx} = R_{Ly} = 60 Ω, C_L = open RXD1 and RXD2 floating		150	350	µA
		Dominant Two channels(1)	TCAN1046AV: STB1 = STB2 = 0 V TCAN1048AV: nSTB1 = nSTB2 = V_{IO} TXDx = TXDy = 0 V R_{Lx} = R_{Ly} = 60 Ω, C_L = open RXD1 and RXD2 floating		255	600	µA
		Recessive Two channels(1)	TCAN1046AV: STB1 = STB2 = 0 V TCAN1048AV: nSTB1 = nSTB2 = V_{IO} TXDx = TXDy = V_{IO} R_{Lx} = R_{Ly} = 60 Ω, C_L = open RXD1 and RXD2 floating		50	100	µA
	I/O supply current Standby mode		TCAN1046AV: STB1 = STB2 = V_{IO} TCAN1048AV: nSTB1 = nSTB2 = 0 V TXDx = TXDy = V_{IO} R_{Lx} = R_{Ly} = 60 Ω, C_L = open RXD1 and RXD2 floating		17	30	µA
UV_{CC}	Rising undervoltage detection on V_{CC}				4.2	4.4	V
	Falling undervoltage detection on V_{CC}			3.5	4	4.25	V
$V_{HYS(UVCC)}$	Hysteresis voltage on UV_{CC}				200		mV
UV_{VIO}	Rising undervoltage detection on V_{IO}				1.56	1.65	V
	Falling undervoltage detection on V_{IO}			1.4	1.51	1.59	V
$V_{HYS(UVIO)}$	Hysteresis voltage on UV_{IO}				40		mV

(1) TXD1 and TXD2 are interchangeable for TXDx and TXDy
(2) CAN1 and CAN2 are interchangeable for CANx and CANy

8.7 Dissipation Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	One channel average power dissipation Normal mode	V_{CC} = 5 V, V_{IO} = 1.8 V, T_J= 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		95		mW
		V_{CC} = 5 V, V_{IO} = 3.3 V, T_J= 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		95		mW
		V_{CC} = 5 V, V_{IO} = 5 V, T_J= 27°C, R_L = 60Ω, TXD input = 250 kHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		95		mW
		V_{CC} = 5.5 V, V_{IO} = 1.8 V, T_J= 150°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		120		mW
		V_{CC} = 5.5 V, V_{IO} = 3.3 V, T_J= 150°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		120		mW
		V_{CC} = 5.5 V, V_{IO} = 5 V, T_J= 150°C, R_L = 60Ω, TXD input = 2.5 MHz 50% duty cycle square wave, C_{L_RXD} = 15 pF		120		mW
T_{TSD}	Thermal shutdown temperature		175	195	210	°C
$T_{TSD(HYS)}$	Thermal shutdown hysteresis			12		

8.8 Electrical Characteristics

Over recommended operating conditions with T_J = -40°C to 150°C (unless otherwise noted), CAN electrical parameters apply to both channels

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Electrical Characteristics							
$V_{O(DOM)}$	Dominant output voltage Normal mode	CANH	STB = 0 V / nSTB = V_{IO} TXD = 0 V 50 Ω ≤ R_L ≤ 65 Ω, C_L = open; See Figure 9-2 and Figure 10-3	2.75		4.5	V
		CANL		0.5		2.25	V
$V_{O(REC)}$	Recessive output voltage Normal mode	CANH and CANL	STB = 0 V / nSTB = V_{IO} TXD = V_{IO} R_L = open (no load); See Figure 9-2 and Figure 10-3	2	0.5 V_{CC}	3	V
V_{SYM}	Driver symmetry ($V_{O(CANH)}$ + $V_{O(CANL)}$)/V_{CC}		STB = 0 V / nSTB = V_{IO} TXD = 250 kHz, 1 MHz, 2.5 MHz R_L = 60 Ω, C_{SPLIT} = 4.7 nF, C_L = open; See Figure 9-2 and Figure 10-3	0.9		1.1	V/V
V_{SYM_DC}	DC output symmetry (V_{CC} - $V_{O(CANH)}$ - $V_{O(CANL)}$)		STB = 0 V / nSTB = V_{IO} R_L = 60 Ω, C_L = open; See Figure 9-2 and Figure 10-3	–400		400	mV
$V_{OD(DOM)}$	Differential output voltage Normal mode Dominant	CANH - CANL	STB = 0 V / nSTB = V_{IO} TXD = 0 V 50 Ω ≤ R_L ≤ 65 Ω, C_L = open; See Figure 9-2 and Figure 10-3	1.5		3	V
			STB = 0 V / nSTB = V_{IO} TXD = 0 V 45 Ω ≤ R_L ≤ 70 Ω, C_L = open; See Figure 9-2 and Figure 10-3	1.4		3.3	V
			STB = 0 V / nSTB = V_{IO} TXD = 0 V R_L = 2240 Ω, C_L = open; See Figure 9-2 and Figure 10-3	1.5		5	V
$V_{OD(REC)}$	Differential output voltage Normal mode Recessive	CANH - CANL	STB = 0 V / nSTB = V_{IO} TXD = V_{IO} R_L = 60 Ω, C_L = open; See Figure 9-2 and Figure 10-3	–120		12	mV
			STB = 0 V / nSTB = V_{IO} TXD = V_{IO} R_L = open, C_L = open; See Figure 9-2 and Figure 10-3	–50		50	mV
$V_{O(STB)}$	Bus output voltage Standby mode	CANH	STB = V_{IO} / nSTB = 0 V R_L = open; See Figure 9-2 and Figure 10-3	-0.1		0.1	V
		CANL		-0.1		0.1	V
		CANH - CANL		-0.2		0.2	V
$I_{OS(SS\_DOM)}$	Short-circuit steady-state output current, dominant Normal mode		STB = 0 V / nSTB = V_{IO} TXD = 0 V $V_{(CANH)}$ = -15 V to 40 V, CANL = open; See Figure 9-8 and Figure 10-3	–115			mA
			STB = 0 V / nSTB = V_{IO} TXD = 0 V $V_{(CAN\_L)}$ = -15 V to 40 V, CANH = open; See Figure 9-8 and Figure 10-3			115	mA
$I_{OS(SS\_REC)}$	Short-circuit steady-state output current, recessive Normal mode		STB = 0 V / nSTB = V_{IO} TXD = V_{IO} –27 V ≤ V_{BUS} ≤ 32 V, where V_{BUS} = CANH = CANL; See Figure 9-8 and Figure 10-3	–5		5	mA
Receiver Electrical Characteristics							
V_{IT}	Input threshold voltage Normal mode		STB = 0 V / nSTB = V_{IO} -12 V ≤ V_{CM} ≤ 12 V; See Figure 9-3 and Table 10-5	500		900	mV
$V_{IT(STB)}$	Input threshold Standby mode		STB = V_{IO} / nSTB = 0 V -12 V ≤ V_{CM} ≤ 12 V; See Figure 9-3 and Table 10-5	400		1150	mV

8.8 Electrical Characteristics (continued)

Over recommended operating conditions with T_J = -40℃ to 150℃ (unless otherwise noted), CAN electrical parameters apply to both channels

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DOM}	Dominant state differential input voltage range Normal mode	STB = 0 V / nSTB = V_{IO} -12 V ≤ V_{CM} ≤ 12 V; See Figure 9-3 and Table 10-5	0.9		9	V
V_{REC}	Recessive state differential input voltage range Normal mode	STB = 0 V / nSTB = V_{IO} -12 V ≤ V_{CM} ≤ 12 V; See Figure 9-3 and Table 10-5	-4		0.5	V
$V_{DOM(STB)}$	Dominant state differential input voltage range Standby mode	STB = V_{IO} / nSTB = 0 V -12 V ≤ V_{CM} ≤ 12 V; See Figure 9-3 and Table 10-5	1.15		9	V
$V_{REC(STB)}$	Recessive state differential input voltage range Standby mode	STB = V_{IO} / nSTB = 0 V -12 V ≤ V_{CM} ≤ 12 V; See Figure 9-3 and Table 10-5	-4		0.4	V
V_{HYS}	Hysteresis voltage for input threshold Normal mode	STB = 0 V / nSTB = V_{IO} -12 V ≤ V_{CM} ≤ 12 V; See Figure 9-3 and Table 10-5		115		mV
V_{CM}	Common mode range Normal and standby modes	See Figure 9-3 and Table 10-5	–12		12	V
$I_{LKG(IOFF)}$	Unpowered bus input leakage current (measured individually for each channel)	CANH = CANL = 5 V, V_{CC} = V_{IO} = GND			5	µA
C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{IO}			20	pF
C_{ID}	Differential input capacitance				10	pF
R_{ID}	Differential input resistance	STB = 0 V / nSTB = V_{IO} TXD = V_{IO} -12 V ≤ V_{CM} ≤ 12 V	40		90	kΩ
R_{IN}	Single ended input resistance (CANH or CANL)		20		45	kΩ
$R_{IN(M)}$	Input resistance matching [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100 %	$V_{(CAN\_H)}$ = $V_{(CAN\_L)}$ = 5 V	–1		1	%
TXD Terminal (CAN Transmit Data Input)						
V_{IH}	High-level input voltage		0.7 V_{IO}			V
V_{IL}	Low-level input voltage				0.3 V_{IO}	V
I_{IH}	High-level input leakage current	TXD = V_{CC} = V_{IO} = 5.5 V	–2.5	0	1	µA
I_{IL}	Low-level input leakage current	TXD = 0 V V_{CC}= V_{IO} = 5.5 V	–200	-100	–20	µA
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.5 V V_{CC}= V_{IO} = 0 V	–1	0	1	µA
C_I	Input capacitance	V_{IN} = 0.4×sin(2×π×2×10^6×t)+2.5 V		5		pF
RXD Terminal (CAN Receive Data Output)						
V_{OH}	High-level output voltage	I_O = –1.5 mA See Figure 9-3	0.8 V_{IO}			V
V_{OL}	Low-level output voltage	I_O = 1.5mA See Figure 9-3			0.2 V_{IO}	V
$I_{LKG(OFF)}$	Unpowered leakage current	RXD = 5.5 V V_{CC} = V_{IO} = 0 V	–1	0	1	µA
STB / nSTB Terminal (Standby Mode Input)						
V_{IH}	High-level input voltage		0.7 V_{IO}			V
V_{IL}	Low-level input voltage				0.3 V_{IO}	V
I_{IH}	TCAN1046AV high-level input leakage current STB	STB = V_{CC} = V_{IO} = 5.5 V	–2		2	µA
I_{IL}	TCAN1046AV low-level input leakage current STB	STB = 0 V V_{CC} = V_{IO} = 5.5 V,	–20		–2	µA
I_{IH}	TCAN1048AV high-level input leakage current nSTB	nSTB = V_{CC} = V_{IO} = 5.5 V	2		25	µA
I_{IL}	TCAN1048AV low-level input leakage current nSTB	nSTB = 0 V V_{CC} = V_{IO} = 5.5 V,	-2		2	µA

8.8 Electrical Characteristics (continued)

Over recommended operating conditions with T_J = -40℃ to 150℃ (unless otherwise noted), CAN electrical parameters apply to both channels

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LKG(OFF)}$	TCAN1046AV unpowered leakage current	STB = 5.5V V_{CC} = V_{IO} = 0 V	–1		1	µA
	TCAN1048AV unpowered leakage current	nSTB = 0 V V_{CC} = V_{IO} = 0 V	–1		1	µA

8.9 Switching Characteristics

Over recommended operating conditions with T_J = -40℃ to 150℃ (unless otherwise noted); Parameters apply to both CAN channels

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay Driver input (TXD) to receiver output (RXD), recessive to dominant	STB = 0 V / nSTB = V_{IO} V_{IO} = 2.8 V to 5.5 V R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; See Figure 9-4		125	210	ns
$t_{PROP(LOOP1)}$	Total loop delay Driver input (TXD) to receiver output (RXD), recessive to dominant	STB = 0 V / nSTB = V_{IO} V_{IO} = 1.7 V R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; See Figure 9-4		165	255	ns
$t_{PROP(LOOP2)}$	Total loop delay Driver input (TXD) to receiver output (RXD), dominant to recessive	STB = 0 V / nSTB = V_{IO} V_{IO} = 2.8 V to 5.5 V R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; See Figure 9-4		150	210	ns
$t_{PROP(LOOP2)}$	Total loop delay Driver input (TXD) to receiver output (RXD), dominant to recessive	STB = 0 V / nSTB = V_{IO} V_{IO} = 1.7 V R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF; See Figure 9-4		180	255	ns
t_{MODE}	Mode change time, from normal to standby or from standby to normal	See Figure 9-5 and Figure 9-6			20	µs
t_{WK_FILTER}	Filter time for a valid wake-up pattern	See Figure 10-5	0.5		1.8	µs
$t_{WK\_TIMEOUT}$	Bus wake-up timeout		0.8		6	ms
Driver Switching Characteristics						
t_{pHR}	Propagation delay time, high TXD to driver recessive (dominant to recessive)	STB = 0 V / nSTB = V_{IO} R_L = 60 Ω, C_L = 100 pF; See Figure 9-2		80		ns
t_{pLD}	Propagation delay time, low TXD to driver dominant (recessive to dominant)			70		ns
$t_{sk(p)}$	Pulse skew (|tpHR - tpLD|)			14		ns
t_R	Differential output signal rise time			28		ns
t_F	Differential output signal fall time			50		ns
t_{TXD_DTO}	Dominant timeout	STB = 0 V / nSTB = V_{IO} R_L = 60 Ω, C_L = 100 pF; See Figure 9-7	1.2		4.0	ms
Receiver Switching Characteristics						
t_{pRH}	Propagation delay time, bus recessive input to high output (dominant to recessive)	STB = 0 V / nSTB = V_{IO} $C_{L(RXD)}$ = 15 pF See Figure 9-3		81		ns
t_{pDL}	Propagation delay time, bus dominant input to low output (recessive to dominant)			66		ns
t_R	RXD output signal rise time			10		ns
t_F	RXD output signal fall time			10		ns

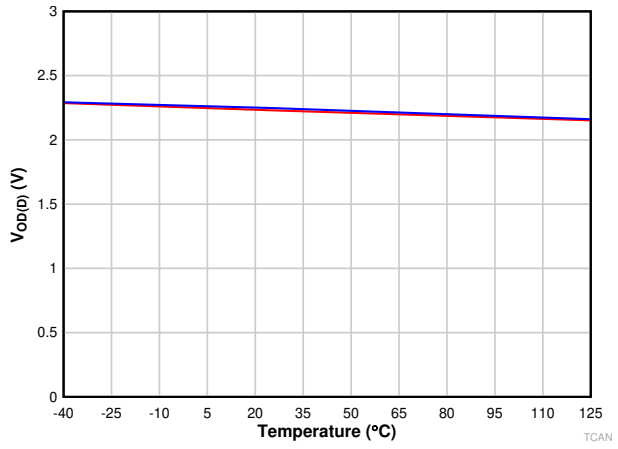
8.9 Switching Characteristics (continued)

Over recommended operating conditions with T_J = -40℃ to 150℃ (unless otherwise noted); Parameters apply to both CAN channels

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FD Timing Characteristics						
$t_{BIT(BUS)}$	Bit time on CAN bus output pins $t_{BIT(TXD)}$ = 500 ns	STB = 0 V / nSTB = V_{IO} R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF $\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$; See Figure 9-4	450		525	ns
	Bit time on CAN bus output pins $t_{BIT(TXD)}$ = 200 ns		160		205	ns
	Bit time on CAN bus output pins $t_{BIT(TXD)}$ = 125 ns(1)		85		130	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins $t_{BIT(TXD)}$ = 500 ns		410		540	ns
	Bit time on RXD output pins $t_{BIT(TXD)}$ = 200 ns		130		210	ns
	Bit time on RXD output pins $t_{BIT(TXD)}$ = 125 ns(1)		75		135	ns
t_{REC}	Receiver timing symmetry $t_{BIT(TXD)}$ = 500 ns		-50		20	ns
	Receiver timing symmetry $t_{BIT(TXD)}$ = 200 ns		-40		10	ns
	Receiver timing symmetry $t_{BIT(TXD)}$ = 125 ns(1)		-40		10	ns

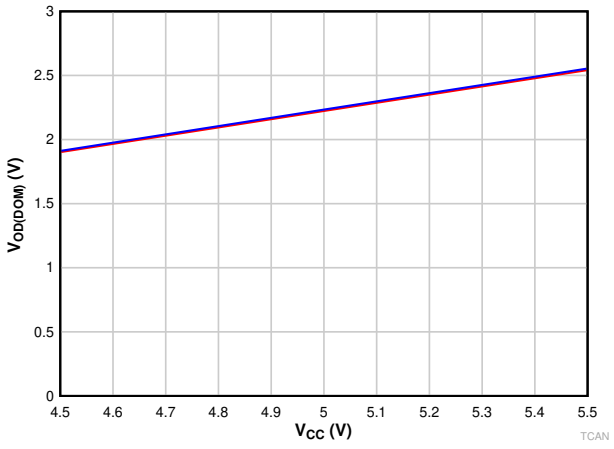
(1) Measured during characterization and not an ISO 11898-2:2016 parameter.

8.10 Typical Characteristics



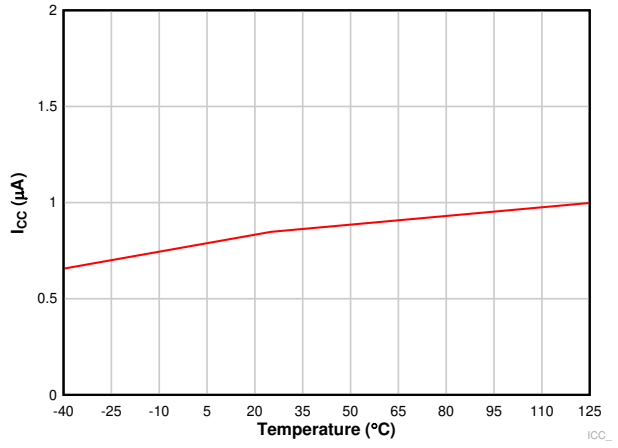
V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω

Figure 8-1. $V_{OD(DOM)}$ Over Temperature $V_{OD(DOM)}$ vs V_{CC} Channel 1 & Channel 2



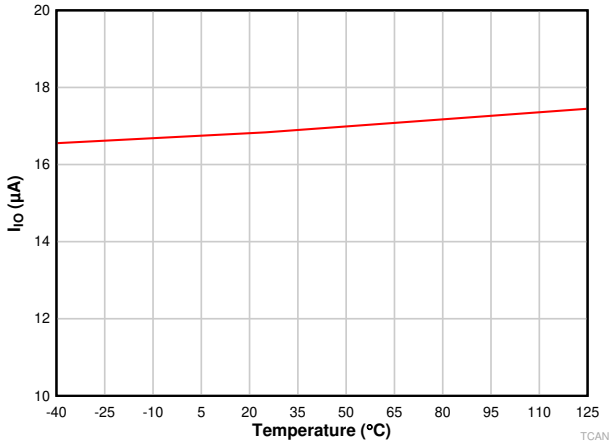
A. Temp = 25 °C R_L = 60 Ω

Figure 8-2. $V_{OD(DOM)}$ Over V_{CC} $V_{OD(DOM)}$ vs V_{CC} Channel 1 & Channel 2



V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω

Figure 8-3. I_{CC} Standby vs Temperature



V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω

Figure 8-4. I_{IO} Standby vs Temperature

9 Parameter Measurement Information

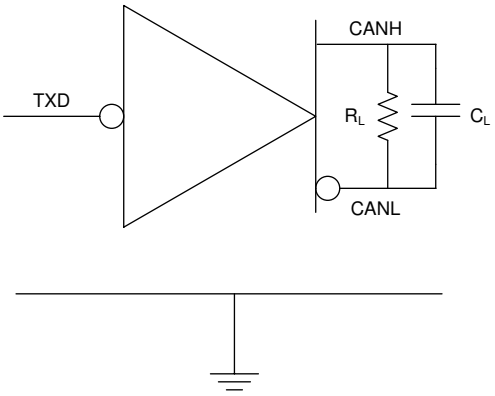


Figure 9-1. I_{CC} Test Circuit

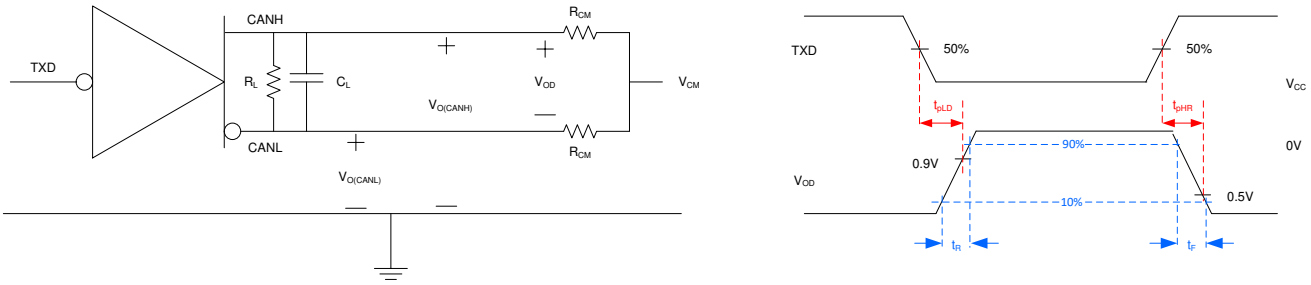


Figure 9-2. Driver Test Circuit and Measurement

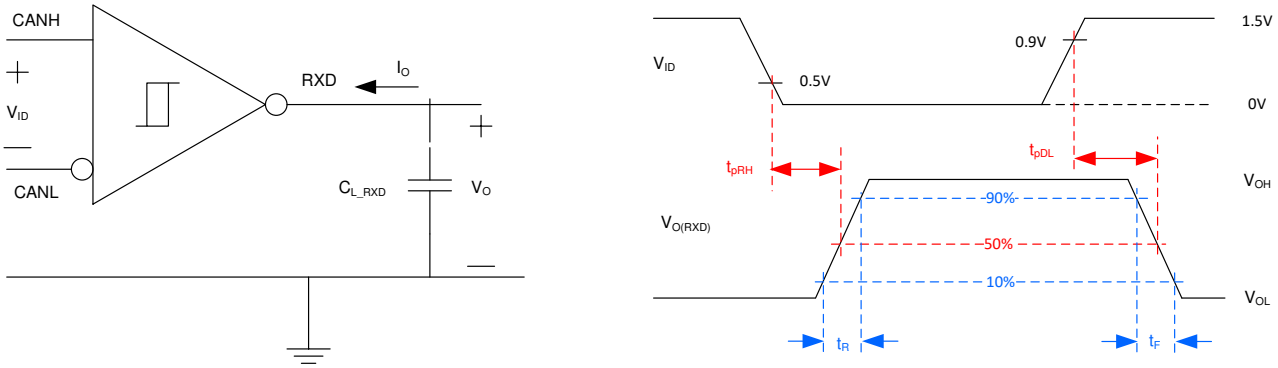


Figure 9-3. Receiver Test Circuit and Measurement

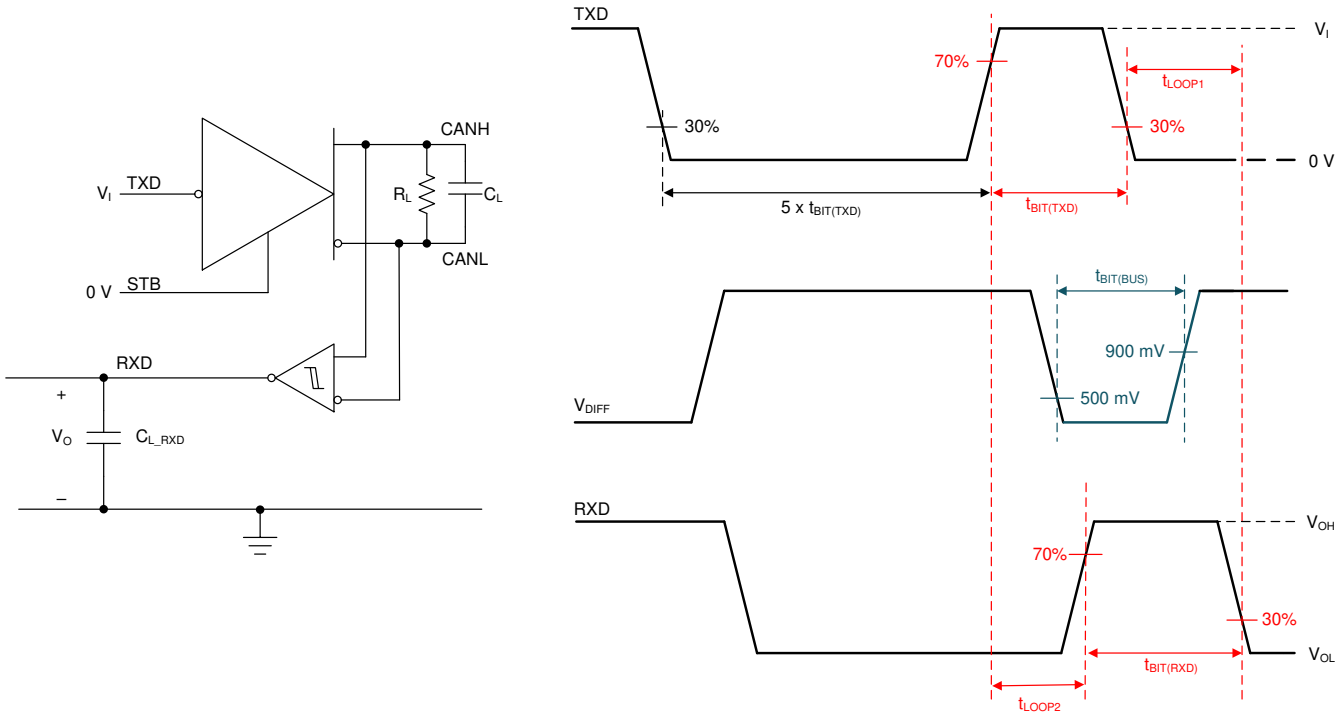


Figure 9-4. Transmitter and Receiver Timing Test Circuit and Measurement

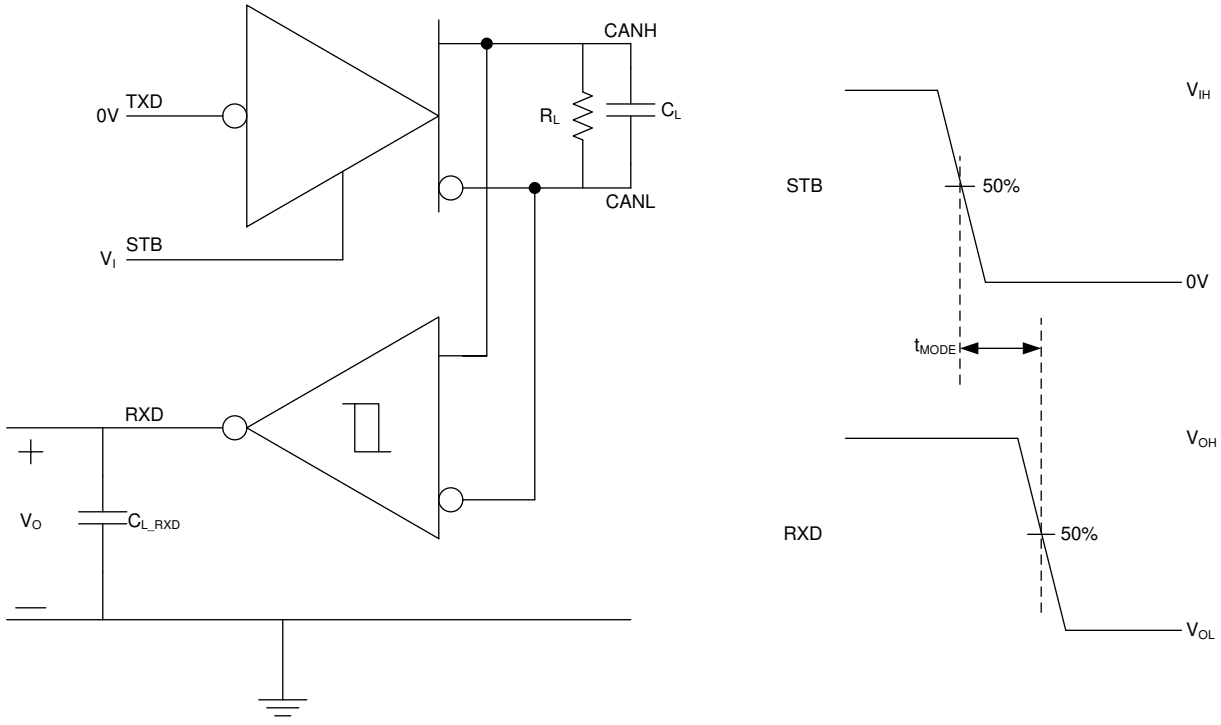


Figure 9-5. TCAN1046AV t_{MODE} Test Circuit and Measurement

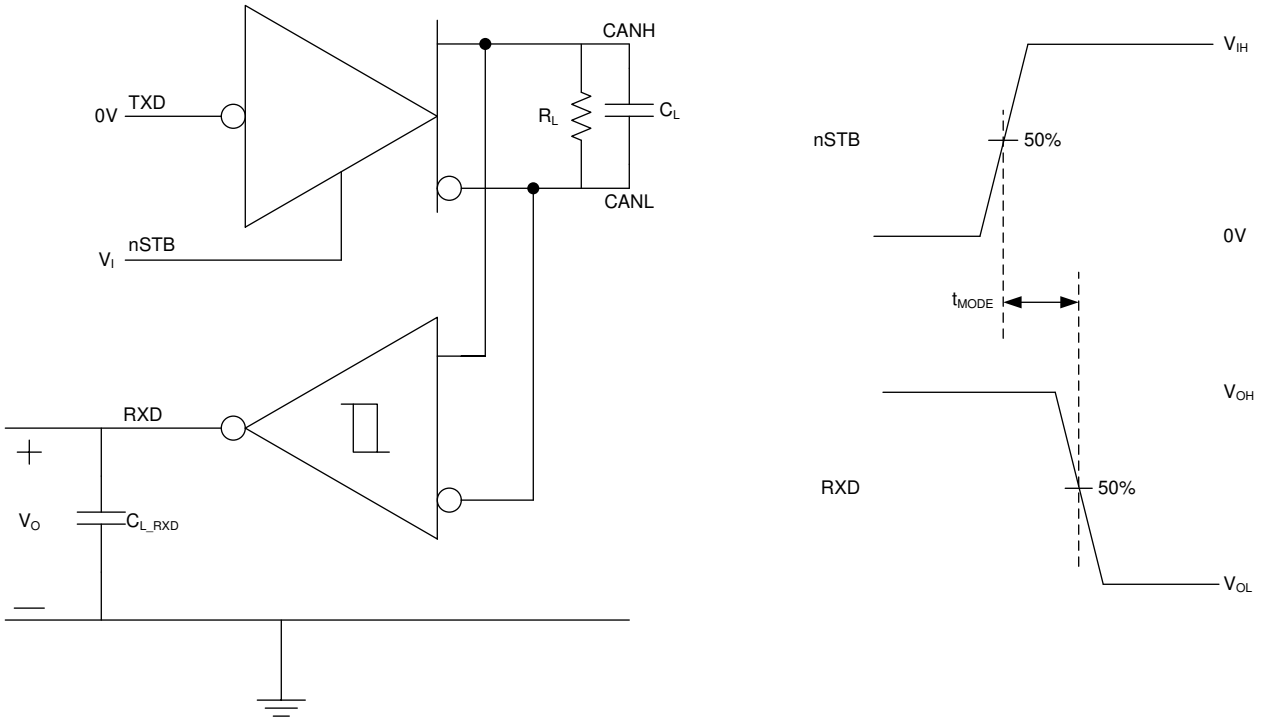


Figure 9-6. TCAN1048AV t_{MODE} Test Circuit and Measurement

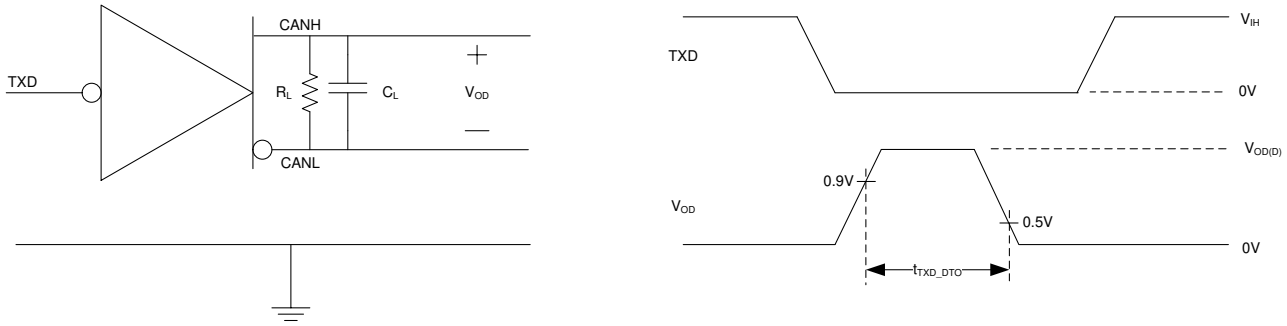


Figure 9-7. TXD Dominant Timeout Test Circuit and Measurement

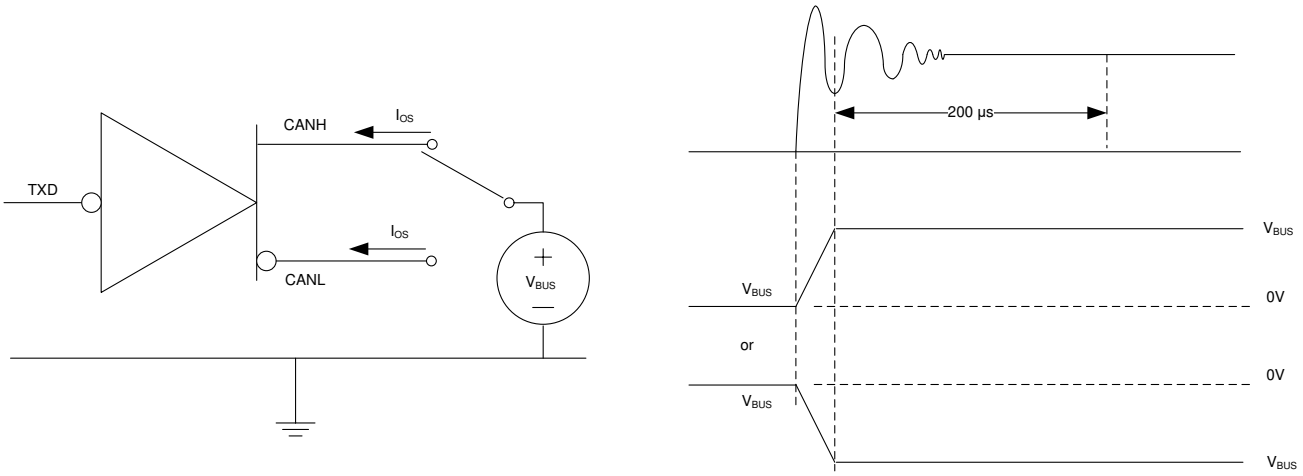


Figure 9-8. Driver Short-Circuit Current Test and Measurement

10 Detailed Description

10.1 Overview

The TCAN104xAV-Q1 devices meet or exceed the specifications of the ISO 11898-2:2016 high speed CAN (Controller Area Network) physical layer standard. The devices have been certified to the requirements of ISO 11898-2:2016 physical layer requirements according to the GIFT/ICT high speed CAN test specification. The transceivers provide a number of different protection features making them ideal for the stringent automotive system requirements while also supporting CAN FD data rates up to 8 Mbps.

The TCAN104xAV-Q1 support the following CAN standards:

- CAN transceiver physical layer standards:
  - ISO 11898-2:2016 High speed medium access unit
  - ISO 11898-5:2007 High speed medium access unit with low-power mode
  - SAE J2284-1: High Speed CAN (HSC) for Vehicle Applications at 125 kbps
  - SAE J2284-2: High Speed CAN (HSC) for Vehicle Applications at 250 kbps
  - SAE J2284-3: High Speed CAN (HSC) for Vehicle Applications at 500 kbps
  - SAE J2284-4: High-Speed CAN (HSC) for Vehicle Applications at 500 kbps with CAN FD Data at 2 Mbps
  - SAE J2284-5: High-Speed CAN (HSC) for Vehicle Applications at 500 kbps with CAN FD Data at 5 Mbps
- EMC requirements:
  - IEC 62228-3 EMC evaluation of transceivers - CAN transceivers
  - VeLIO (Vehicle LAN Interoperability and Optimization) CAN and CAN-FD Transceiver Requirements
  - SAE J2962-2 Communication Transceivers Qualification Requirements – CAN
- Conformance test requirements:
  - ISO 16845-2 Road vehicles – Controller area network (CAN) conformance test plan Part 2: High-speed medium access unit conformance test plan

10.2 Functional Block Diagram

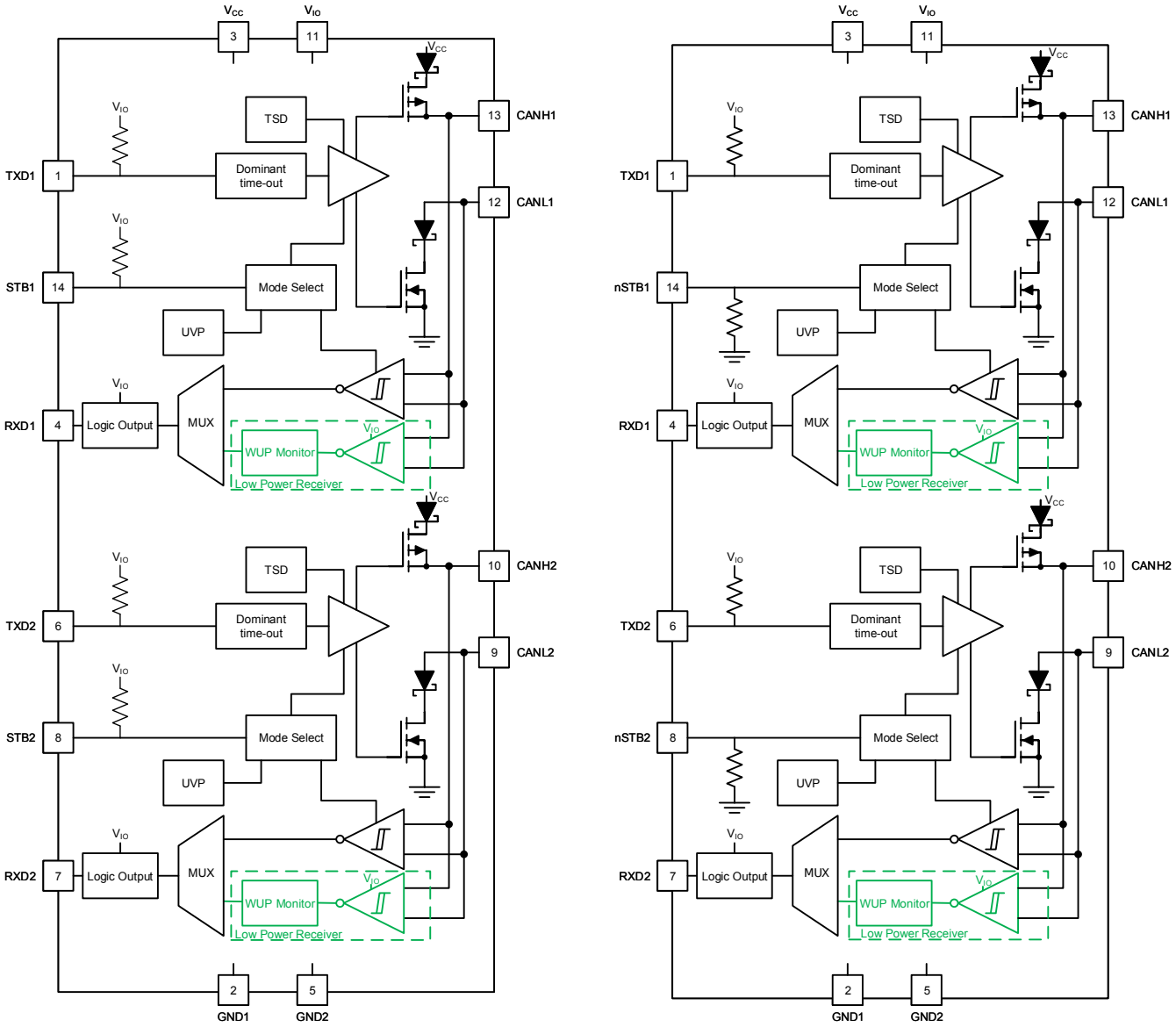


Figure 10-1. TCAN1046AV-Q1 (left image with pull-up on STB) and TCAN1048AV-Q1 (right image with pull-down on nSTB) Block Diagrams

10.3 Feature Description

10.3.1 Pin Description

10.3.1.1 TXD1 and TXD2

TXD1 and TXD2 are the logic-level signals, referenced to V_{IO}, from a CAN controller to the device.

10.3.1.2 GND1 and GND2

GND1 and GND2 are ground pins of the transceiver, both must be connected to the PCB ground.

10.3.1.3 V_{CC}

V_{CC} provides the 5-V power supply to both the CAN channels.

10.3.1.4 RXD1 and RXD2

RXD1 and RXD2 are the logic-level signals, referenced to V_{IO}, from the TCAN104xAV-Q1 to a CAN controller. These pins are only driven once V_{IO} is present.

10.3.1.5 V_{IO}

The V_{IO} pin provides the digital I/O voltage to match the CAN controller voltage thus avoiding the requirement for a level shifter. The V_{IO} pin supports voltages from 1.7 V to 5.5 V providing the widest range of controller support.

10.3.1.6 CANH and CANL

The CAN high and CAN low are differential bus pins of the two integrated CAN channels. The CANH and CANL pins are connected to the CAN transceiver and the low-voltage WUP CAN receiver.

10.3.1.7 STB1, STB2, nSTB1, and nSTB2 (Standby)

The STB1, STB2, nSTB1, and nSTB2 pins are input pins used for mode control of the transceiver.

The TCAN1046AV-Q1 implements STB1 and STB2 which can be supplied from either the system processor or from a static system voltage source. If normal mode is the only intended mode of operation than the STB pins can be tied directly to GND.

The TCAN1048AV-Q1 implements nSTB1 and nSTB2 which can be supplied from either the system processor or from a static system voltage source. If normal mode is the only intended mode of operation, the nSTB pins can be tied directly to the V_{IO} voltage source.

10.3.2 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See Figure 10-2 and Figure 10-3.

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD1, TXD2, RXD1 and RXD2 pins. A recessive bus state occurs when the bus is biased to $V_{CC}/2$ via the high-resistance internal input resistors (R_{IN}) of the receiver and corresponds to a logic high on the TXD1, TXD2, RXD1 and RXD2 pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

The TCAN104xAV-Q1 transceiver implements a low-power standby (STB or nSTB) mode which enables a third bus state where the bus pins are weakly biased to ground via the high resistance internal resistors of the receiver. See Figure 10-2 and Figure 10-3.

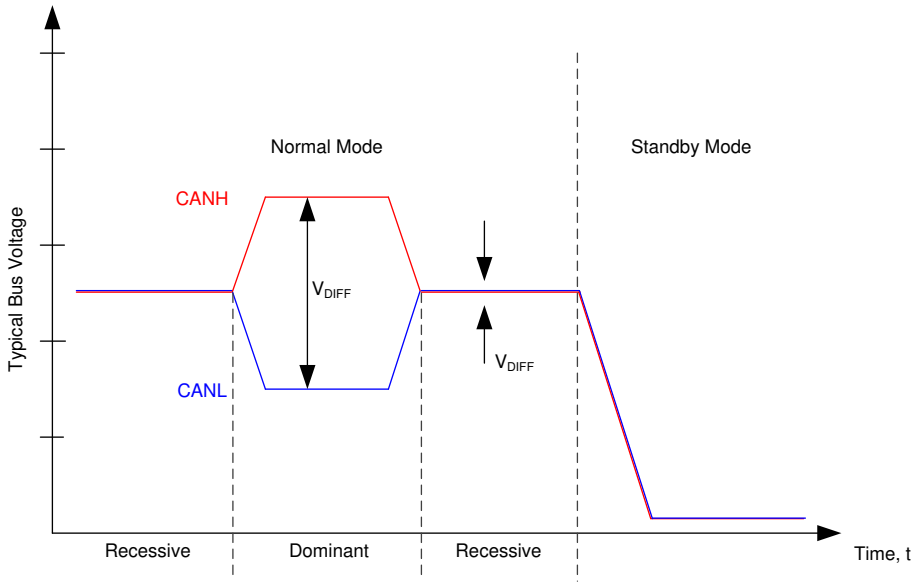
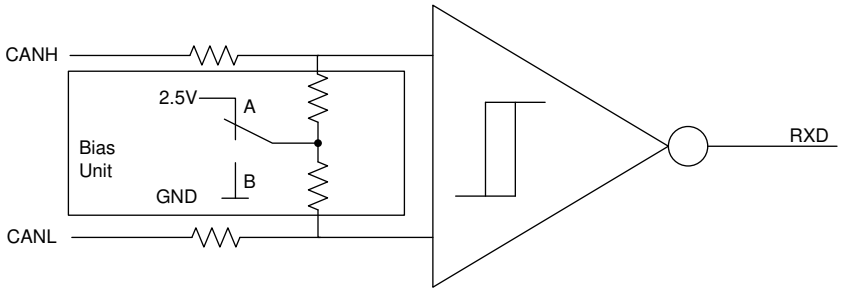


Figure 10-2. Bus States



A. Normal Mode
B. Standby Mode

Figure 10-3. Simplified Recessive Common Mode Bias Unit and Receiver

10.3.3 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit, t_{TXD_DTO}, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin which clears the dominant time out. The receiver remains active and biased to $V_{CC}/2$. The RXD output reflects the activity on the CAN bus during the TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using Equation 1.

$$\text{Minimum Data Rate} = 11 \text{ bits} / t_{TXD\_DTO} = 11 \text{ bits} / 1.2 \text{ ms} = 9.2 \text{ kbps} \quad (1)$$

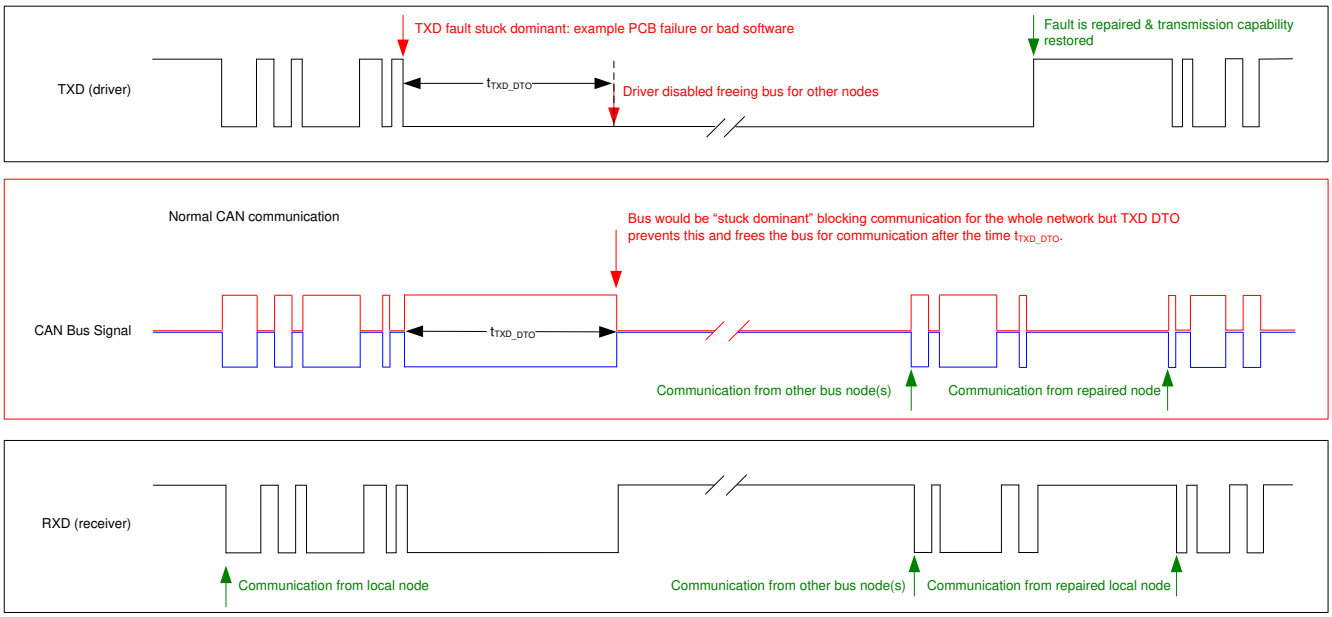


Figure 10-4. Example Timing Diagram for TXD Dominant Timeout

10.3.4 CAN Bus Short Circuit Current Limiting

The TCAN104xAV-Q1 has several protection features that limit the short circuit current when a CAN bus line is shorted. The features include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout which prevents permanently having the higher short-circuit current of a dominant state in case of a system fault. During CAN communication, the bus switches between the dominant and recessive states, thus the short-circuit current may be viewed as either the current during each bus state or as a DC average current. When selecting termination resistors or a common-mode choke for the CAN design the average power rating, $I_{OS(AVG)}$, should be used. The percentage dominant is limited by the TXD DTO and the CAN protocol which has forced state changes and recessive bits due to bit stuffing, control fields, and interframe space. These provides for a minimum amount of recessive time on the bus even if the data field contains a high percentage of dominant bits.

The average short-circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short-circuit currents. The average short-circuit current may be calculated using Equation 2.

$$I_{OS(AVG)} = \%\ \text{Transmit} \times [(\%\ \text{REC\_Bits} \times I_{OS(SS)\_REC}) + (\%\ \text{DOM\_Bits} \times I_{OS(SS)\_DOM})] + [\%\ \text{Receive} \times I_{OS(SS)\_REC}] \quad (2)$$

Where:

- $I_{OS(AVG)}$ is the average short-circuit current
- % Transmit is the percentage the node is transmitting CAN messages
- % Receive is the percentage the node is receiving CAN messages
- % REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- % DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short-circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short- circuit current

The short-circuit current and the possible fault cases of the network should be considered when sizing the power supply used to generate the transceivers V_{CC} supply.

10.3.5 Thermal Shutdown (TSD)

If the junction temperature of the TCAN104xAV-Q1 exceeds the thermal shutdown threshold, T_{TSD}, the device turns off the CAN driver circuitry and blocks the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below T_{TSD}. The CAN bus pins are biased to V_{CC}/2

during a TSD fault and the receiver to RXD path remains operational. The TCAN104xAV-Q1 TSD circuit includes hysteresis which prevents the CAN driver output from oscillating during a TSD fault.

10.3.6 Undervoltage Lockout

The supply pins, V_{CC} and V_{IO}, have undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

Table 10-1. Undervoltage Lockout - TCAN104xAV-Q1

V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	> UV_{VIO}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	> UV_{VIO}	STB = V_{IO}: Standby mode; TCAN1046AV-Q1	High impedance Weak pull-down to ground	V_{IO}: Remote wake request(1)
		STB = GND: Protected mode; TCAN1046AV-Q1	High impedance	Recessive
		nSTB = V_{IO}: Protected mode; TCAN1048AV-Q1	High impedance	Recessive
		nSTB = GND: Standby mode; TCAN1048AV-Q1	High impedance Weak pull-down to ground	V_{IO}: Remote wake request(1)
> UV_{VCC}	< UV_{VIO}	Protected	High impedance	High impedance
< UV_{VCC}	< UV_{VIO}	Protected	High impedance	High impedance

(1) See Section 10.4.3.1

Once the undervoltage condition is cleared and t_{MODE} has expired, the TCAN104xAV-Q1 transitions to normal mode and the host controller can send and receive CAN traffic.

10.3.7 Unpowered Device

The TCAN104xAV-Q1 is designed to be an ideal passive or no load to the CAN bus if the device is unpowered. The bus pins were designed to have low leakage currents when the device is unpowered, and do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational.

The logic pins also have low leakage currents when the device is unpowered, and do not load other circuits which may remain powered.

10.3.8 Floating pins

The TCAN104xAV-Q1 has internal pull-ups or pull-downs on critical pins which place the device into known states if the pin floats. This internal bias should not be relied upon by design though, especially in noisy environments, but instead should be considered a failsafe protection feature.

When a CAN controller supporting open-drain outputs is used an adequate external pull-up resistor must be chosen. This specifies that the TXD output of the CAN controller maintains acceptable bit time to the input of the CAN transceiver. See Table 10-2 for details on pin bias conditions.

Table 10-2. Pin Bias

Pin	Pull-up or Pull-down	Comment
TXD1 and TXD2	Pull-up	Weakly biases TXD1 and TXD2 towards recessive to prevent bus blockage or TXD DTO triggering
STB1 and STB2	Pull-up	Weakly biases STB1 and STB2 towards low-power standby mode to prevent excessive system power; TCAN1046AV-Q1 only
nSTB1 and nSTB2	Pull-down	Weakly biases nSTB1 and nSTB2 towards low-power standby mode to prevent excessive system power; TCAN1048AV-Q1 only

10.4 Device Functional Modes

10.4.1 Operating Modes

The TCAN104xAV-Q1 has two main operating modes; normal mode and standby mode. Operating mode selection is made by applying a high or low level to the STB or nSTB pins on the TCAN1046A or TCAN1048A device respectively.

Table 10-3. Operating Modes

STB	nSTB	Device Mode	Driver	Receiver	RXD Pin
High	Low	Standby mode	Disabled	Low-power receiver with bus monitor enable	High (recessive) until valid WUP is received See section Section 10.4.3.1
Low	High	Normal Mode	Enabled	Enabled	Mirrors bus state

10.4.2 Normal Mode

This is the normal operating mode of the TCAN104xAV-Q1. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD1 and TXD2 inputs to a differential output on the CANH1, CANL1 and CANH2, CANL2 bus pins. The receiver is translating the differential signal from CANH1, CANL1 and CANH2, CANL2 to a digital output on the RXD1 and RXD2 outputs.

10.4.3 Standby Mode

This is the low-power mode of the TCAN104xAV-Q1. The CAN driver and main receiver are switched off and bi-directional CAN communication is not possible. The low-power receiver and bus monitor circuits are enabled to allow for RXD wake-up requests via the CAN bus. A wake-up request is output to RXD1 or RXD2 depending on the channel which receives the WUP as shown in Figure 10-5. The local CAN protocol controller should monitor RXD1 and RXD2 for transitions (high-to-low) and reactivate the device to normal mode by pulling the STB1 and STB2 pins low or the nSTB1 and nSTB2 pins high. The CAN bus pins are weakly pulled to GND in this mode; see Figure 10-2 and Figure 10-3.

In standby mode, only the V_{IO} supply is required; therefore. the V_{CC} may be switched off for additional system level current savings.

10.4.3.1 Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

The TCAN104xAV-Q1 supports a remote wake-up request that is used to indicate to the host controller that the bus is active and the node should return to normal operation.

The device uses the multiple filtered dominant wake-up pattern (WUP) from the ISO 11898-2:2016 standard to qualify bus activity. Once a valid WUP has been received, the wake request is indicated to the controller by a falling edge and low period corresponding to a filtered dominant on the RXD output of the TCAN104xAV-Q1.

The WUP consists of a filtered dominant pulse, followed by a filtered recessive pulse, and finally by a second filtered dominant pulse. The first filtered dominant initiates the WUP, and the bus monitor then waits on a filtered recessive; other bus traffic does not reset the bus monitor. Once a filtered recessive is received the bus monitor is waiting for a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon reception of the second filtered dominant the bus monitor recognizes the WUP and drives the RXD output low every time an additional filtered dominant signal is received from the bus.

For a dominant or recessive to be considered filtered, the bus must be in that state for more than the t_{WK_FILTER} time. Due to variability in t_{WK_FILTER} the following scenarios are applicable. Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP and thus no wake request is generated. Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ may be detected as part of a WUP and a wake-up request may be generated. Bus state times greater than $t_{WK\_FILTER(MAX)}$ are always detected as part of a WUP, and thus a wake request is always generated. See Figure 10-5 for the timing diagram of the wake-up pattern.

The pattern and t_{WK_FILTER} time used for the WUP prevents noise and bus stuck dominant faults from causing false wake-up requests while allowing any valid message to initiate a wake-up request.

The ISO 11898-2:2016 standard has defined times for a short and long wake-up filter time. The t_{WK_FILTER} timing for the device has been picked to be within the minimum and maximum values of both filter ranges. This timing has been chosen such that a single bit time at 500 kbps, or two back-to-back bit times at 1 Mbps triggers the filter in either bus state. Any CAN frame at 500 kbps or less would contain a valid WUP.

For an additional layer of robustness and to prevent false wake-ups, the device implements a wake-up timeout feature. For a remote wake-up event to successfully occur, the entire WUP must be received within the timeout value $t \leq t_{WK\_TIMEOUT}$. If not, the internal logic is reset and the transceiver remains in its current state without waking up. The full pattern must then be transmitted again, conforming to the constraints mentioned in this section. See Figure 10-5 for the timing diagram of the wake-up pattern with wake timeout feature.

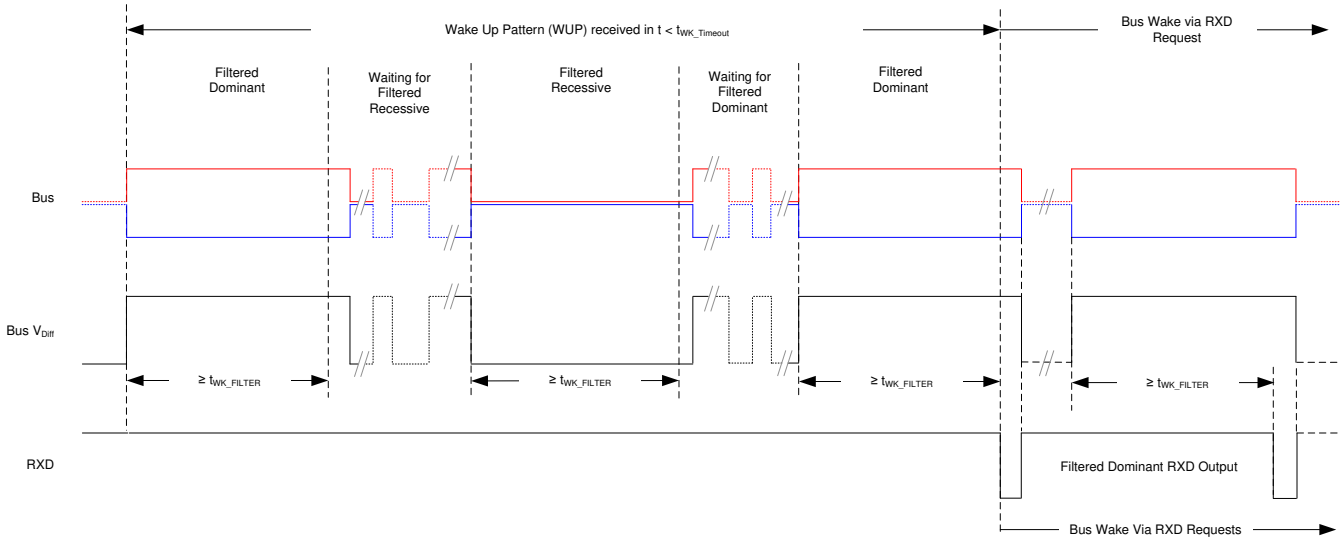


Figure 10-5. Wake-Up Pattern (WUP) with $t_{WK\_TIMEOUT}$

10.4.4 Driver and Receiver Function

Table 10-4. Driver Function Table

Device Mode	TXD Input	Bus Outputs		Driven Bus State(2)
		CANH	CANL	
Normal	Low	High	Low	Dominant
	High or open	High impedance	High impedance	Biased recessive
Standby	X(1)	High impedance	High impedance	Biased to ground

(1) X = irrelevant
(2) For bus state and bias see Figure 10-2 and Figure 10-3

Table 10-5. Receiver Function Table Normal and Standby Mode

Device Mode	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus State	RXD Pin
Normal	$V_{ID} \geq 0.9$ V	Dominant	Low
	0.5 V < V_{ID} < 0.9 V	Undefined	Undefined
	$V_{ID} \leq 0.5$ V	Recessive	High
Standby	$V_{ID} \geq 1.15$ V	Dominant	High Low if a remote wake event occurred See Figure 10-5
	0.4 V < V_{ID} < 1.15 V	Undefined	
	$V_{ID} \leq 0.4$ V	Recessive	
Any	Open ($V_{ID} \approx 0$ V)	Open	High

11 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

11.1 Application Information

11.2 Typical Application

Figure 11-1 shows a typical configuration for 5 V system using the TCAN104xAV-Q1. The bus termination is shown for illustrative purposes.

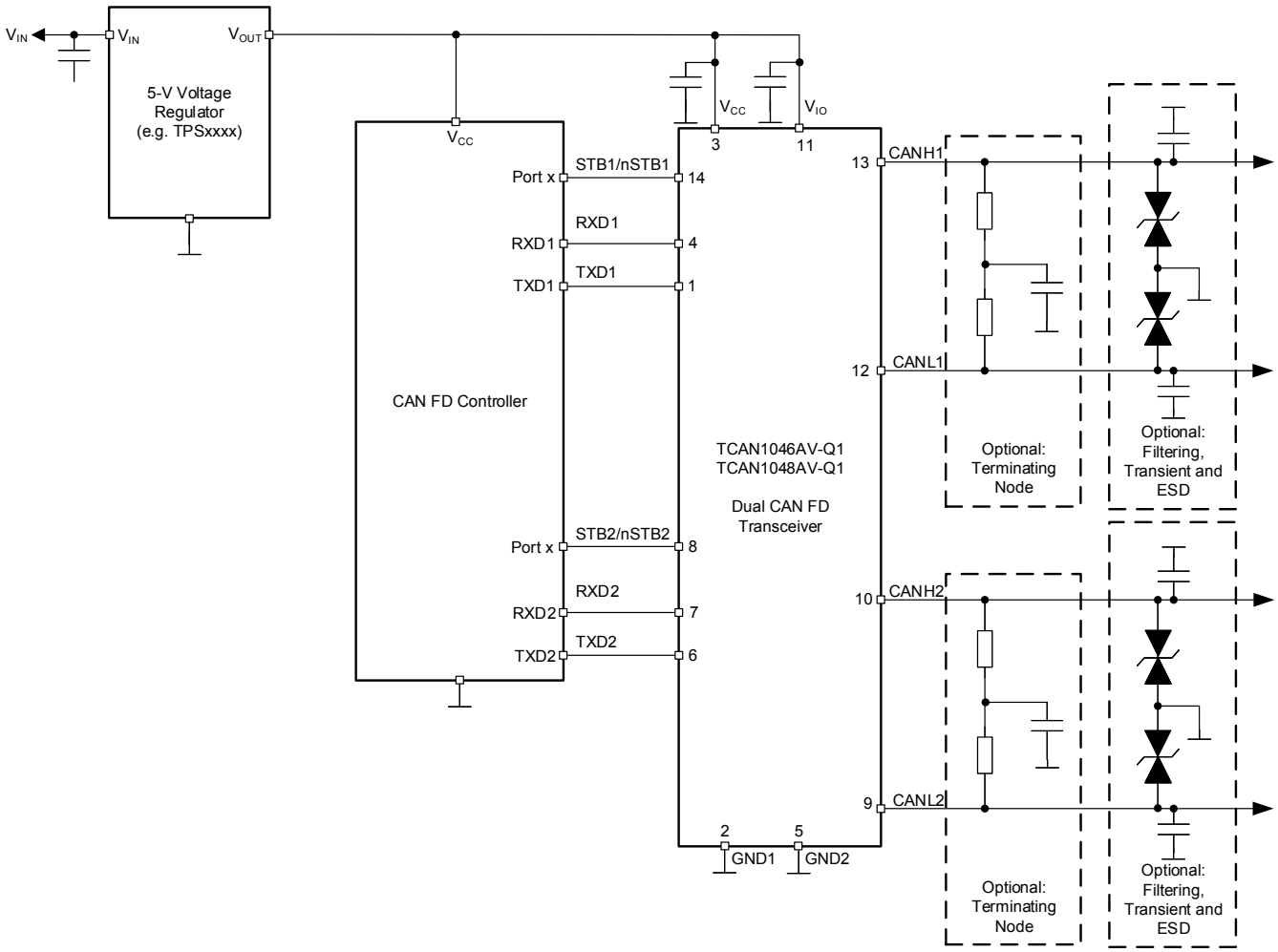


Figure 11-1. Transceiver Application Using 5 V I/O Connections

11.2.1 Design Requirements

11.2.1.1 CAN Termination

Termination may be a single 120-Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired, then split termination may be used, see Figure 11-2. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

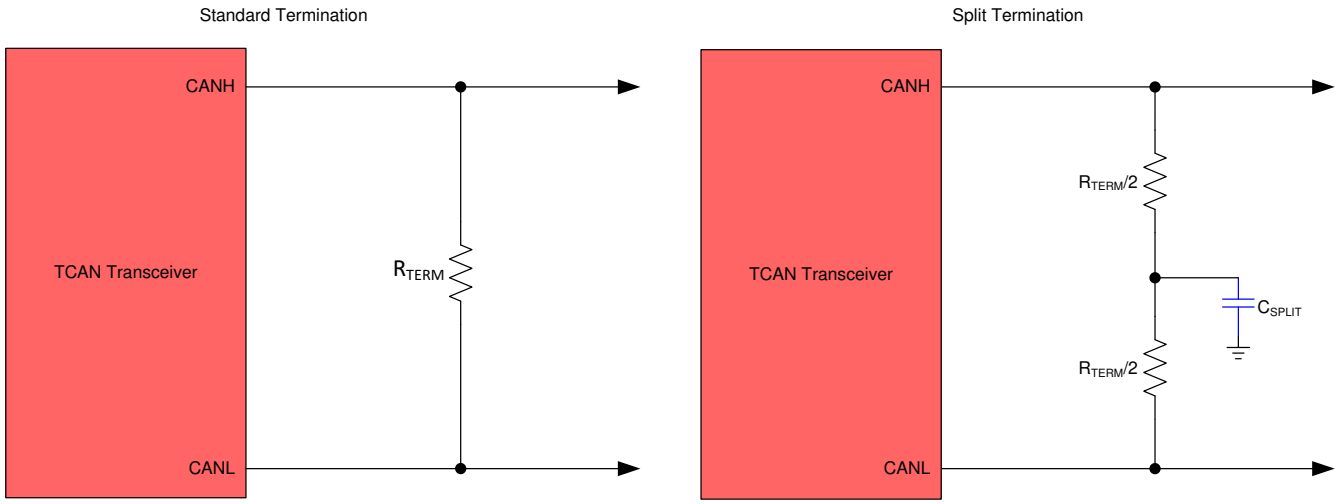


Figure 11-2. CAN Bus Termination Concepts

11.2.2 Detailed Design Procedures

11.2.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN104xAV-Q1.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2016 specification, the driver differential output is specified with a bus load that can range from 50 Ω to 65 Ω where the differential output must be greater than 1.5 V. The TCAN104xAV-Q1 family is specified to meet the 1.5-V requirement down to 50 Ω and is specified to meet 1.4-V differential output at 45-Ω bus load. The differential input resistance of the TCAN104xAV-Q1 is a minimum of 40 kΩ. If 100 TCAN104xAV-Q1 transceivers are in parallel on a bus, this is equivalent to a 400-Ω differential load in parallel with the nominal 60-Ω bus termination which gives a total bus load of approximately 52 Ω. Therefore, the TCAN104xAV-Q1family theoretically supports over 100 transceivers on a single bus segment. However, for a CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility, the CAN network system, a good network design is required for robust network operation.

Please refer to the application report SLLA270: Controller Area Network Physical layer requirements. This document discusses in detail all system design physical layer parameters.

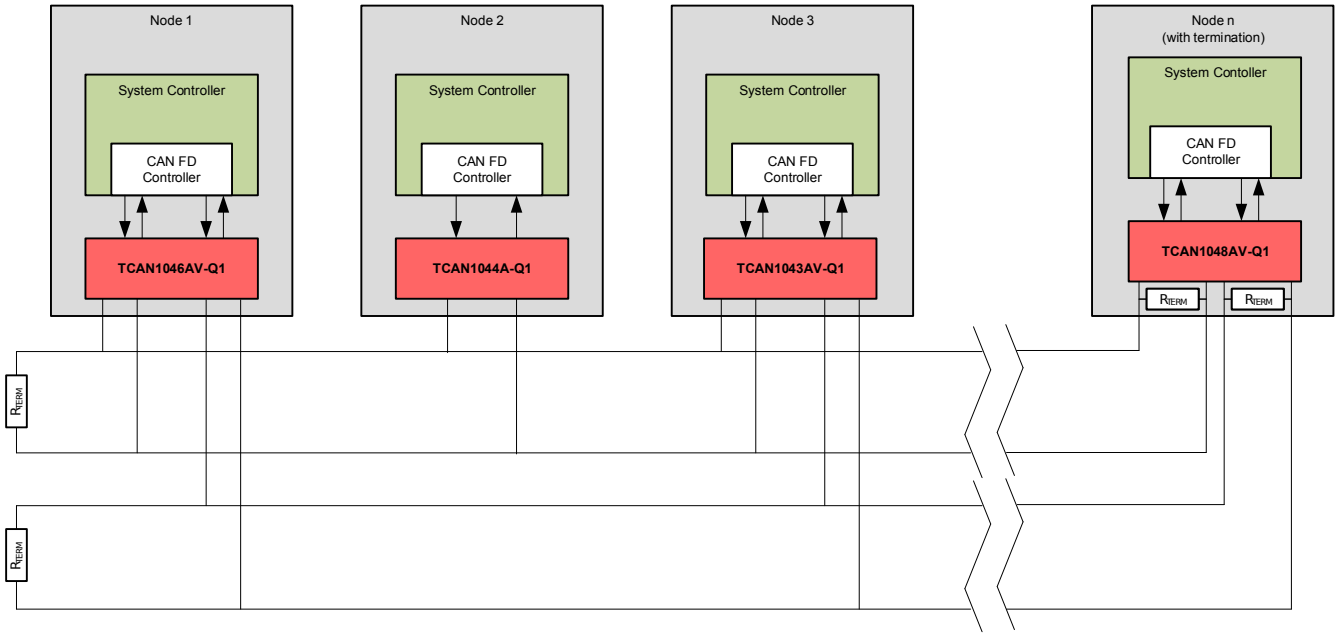
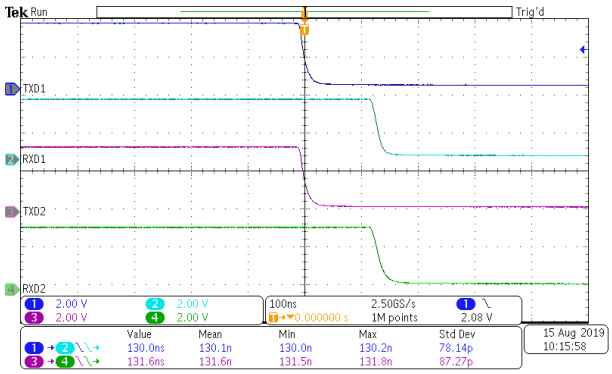


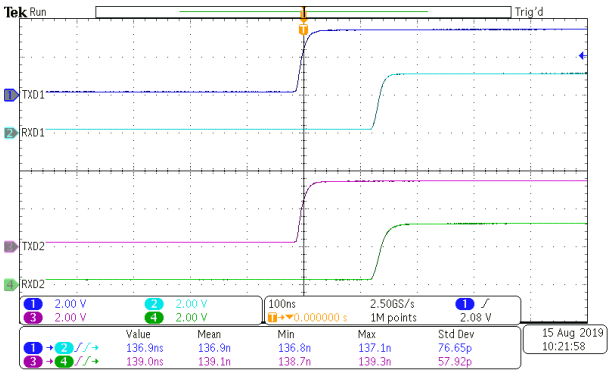
Figure 11-3. Typical CAN Bus

11.2.3 Application Curves



V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω

Figure 11-4. $t_{PROP(LOOP1)}$ TRX1 & TRX2



A. V_{CC} = 5 V V_{IO} = 3.3 V R_L = 60 Ω

Figure 11-5. $t_{PROP(LOOP2)}$ TRX1 & TRX2

11.3 System Examples

The CAN transceiver is typically used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. A 1.8 V, 2.5 V, or 3.3 V application is shown in Figure 11-6. The bus termination is shown for illustrative purposes.

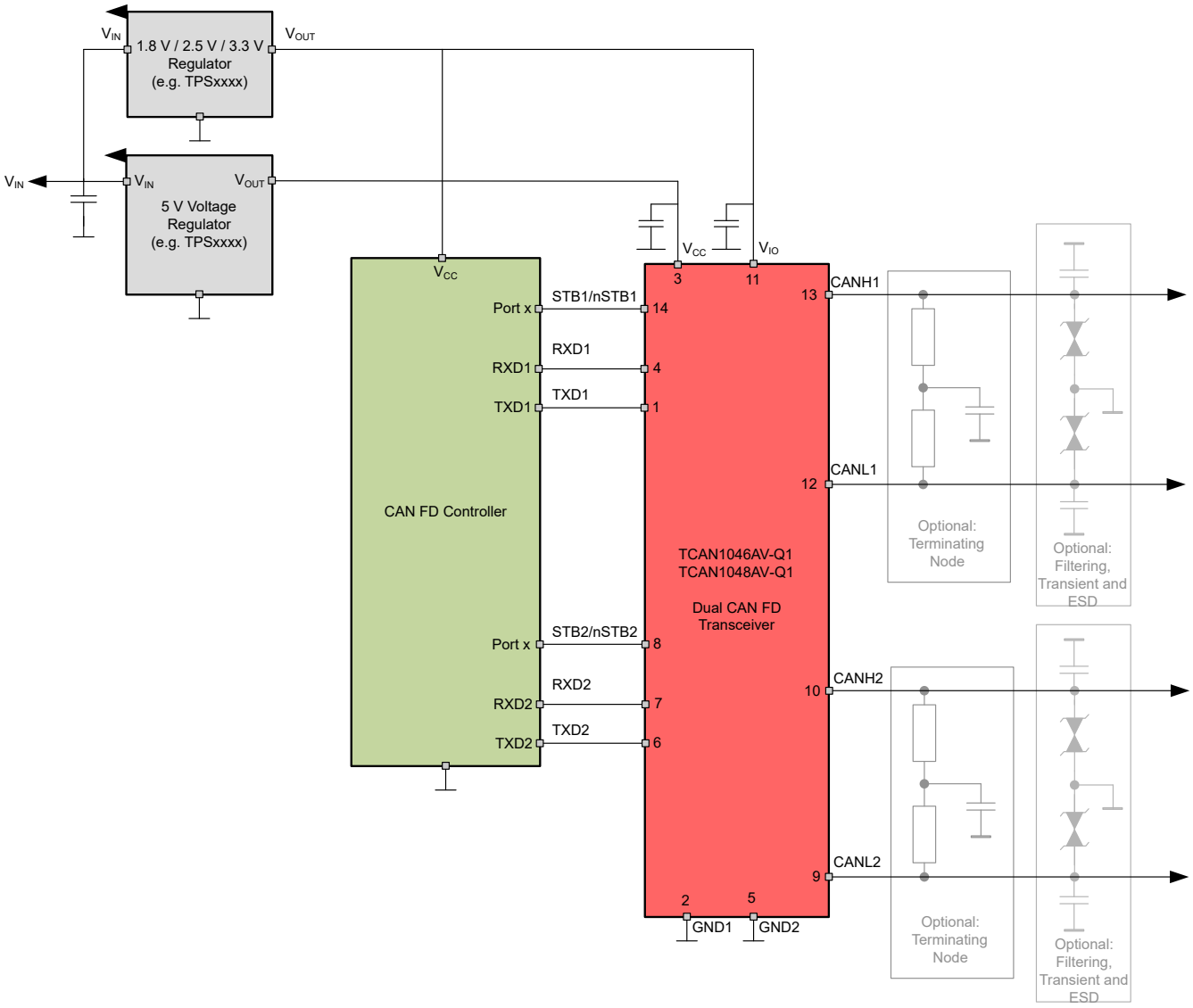


Figure 11-6. Transceiver Application Using 1.8 V, 2.5 V, 3.3 V I/O Connections

12 Power Supply Recommendations

The TCAN104xAV-Q1 device is designed to operate with a main V_{CC} input voltage supply range between 4.5 V and 5.5 V. The device has an I/O level shifting supply input, V_{IO}, designed for a range between 1.8 V and 5.5 V. Both supply inputs must be well regulated. A decoupling capacitor, typically 100 nF, should be placed near the CAN transceiver's main V_{CC} and V_{IO} supply pins in addition to bypass capacitors.

13 Layout

Robust and reliable CAN node design may require special layout techniques depending on the application and automotive design requirements. Since transient disturbances have high frequency content and a wide bandwidth, high-frequency layout techniques should be applied during PCB design.

13.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD, and noise from propagating onto the board. This layout example shows optional transient voltage suppression (TVS) diodes, D1 and D2, which may be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows optional bus filter capacitors C6, C8, C9 and C11.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Decoupling capacitors should be placed as close as possible to the supply pins V_{CC} and V_{IO} of transceiver.
- Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

Note

High frequency current follows the path of least impedance and not the path of least resistance.

- This layout example shows how split termination could be implemented on the CAN node. The termination is split into two resistors, R8 and R9 for channel 1, R10 and R11 for channel 2 with the center or split tap of the termination connected to ground via capacitor C7 or C10. Split termination provides common-mode filtering for the bus. See CAN Termination, CAN Bus Short Circuit Current Limiting, and Equation 2 for information on termination concepts and power ratings needed for the termination resistor(s).

13.2 Layout Example

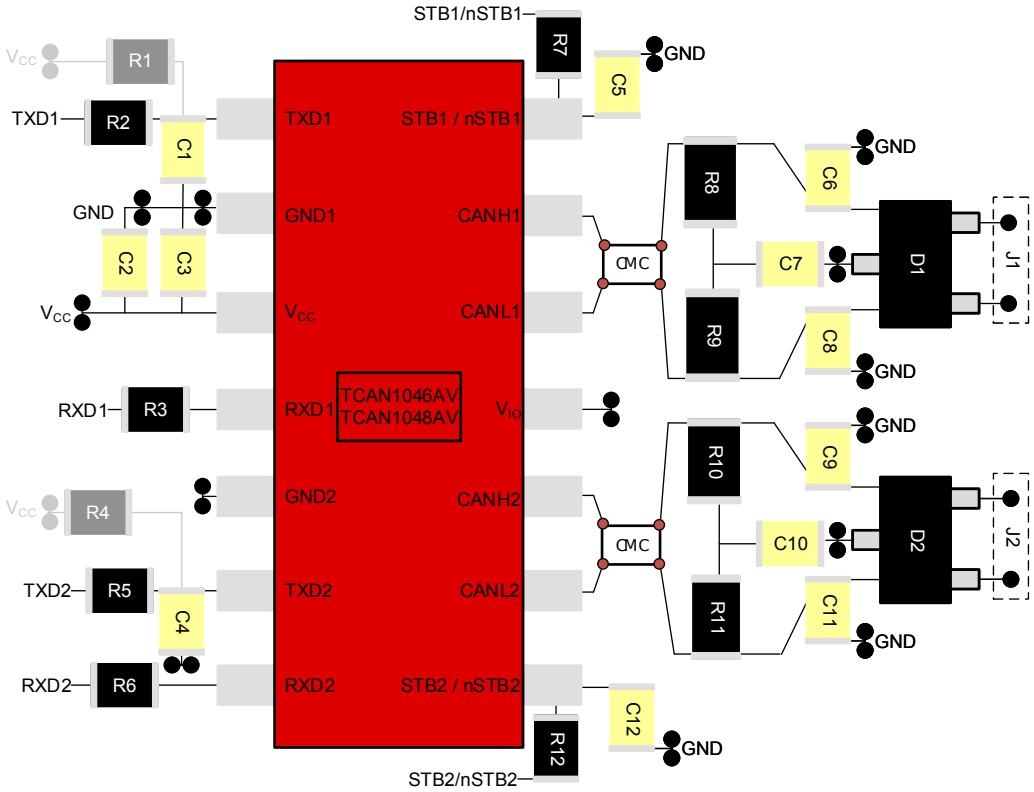


Figure 13-1. Layout Example

14 Device and Documentation Support

14.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

14.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

14.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

14.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCAN1046AVDMTRQ1	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	46AV
TCAN1046AVDMTRQ1.A	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	46AV
TCAN1046AVDRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1046AV
TCAN1046AVDRQ1.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1046AV
TCAN1046AVDYYRQ1	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1046AV
TCAN1046AVDYYRQ1.A	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1046AV
TCAN1048AVDMTRQ1	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	48AV
TCAN1048AVDMTRQ1.A	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	48AV
TCAN1048AVDRQ1	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1048AV
TCAN1048AVDRQ1.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 150	1048AV

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

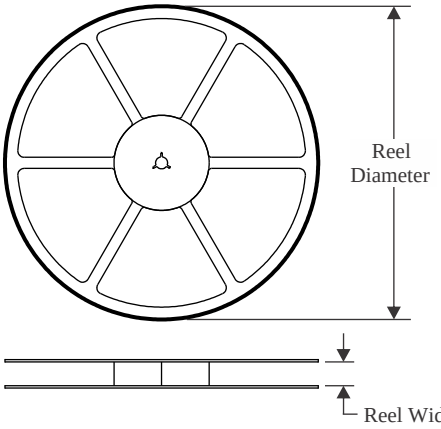
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

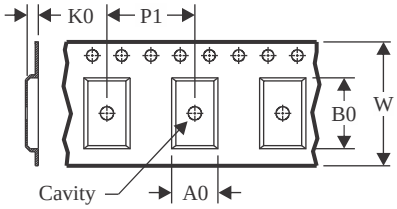
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

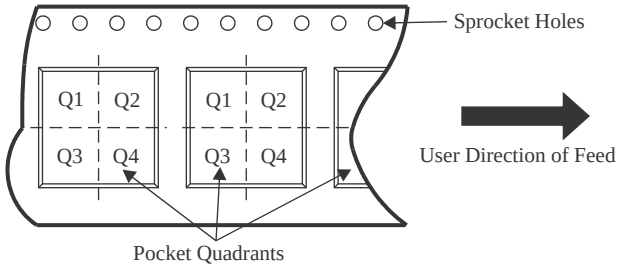


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

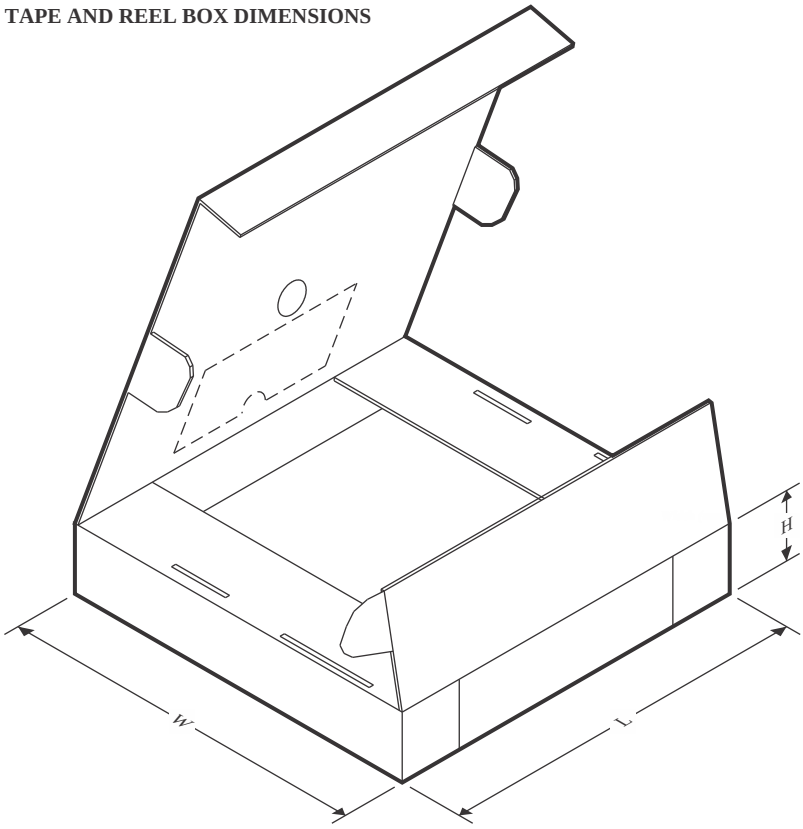
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1046AVDMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TCAN1046AVDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TCAN1046AVDYYRQ1	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TCAN1048AVDMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TCAN1048AVDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

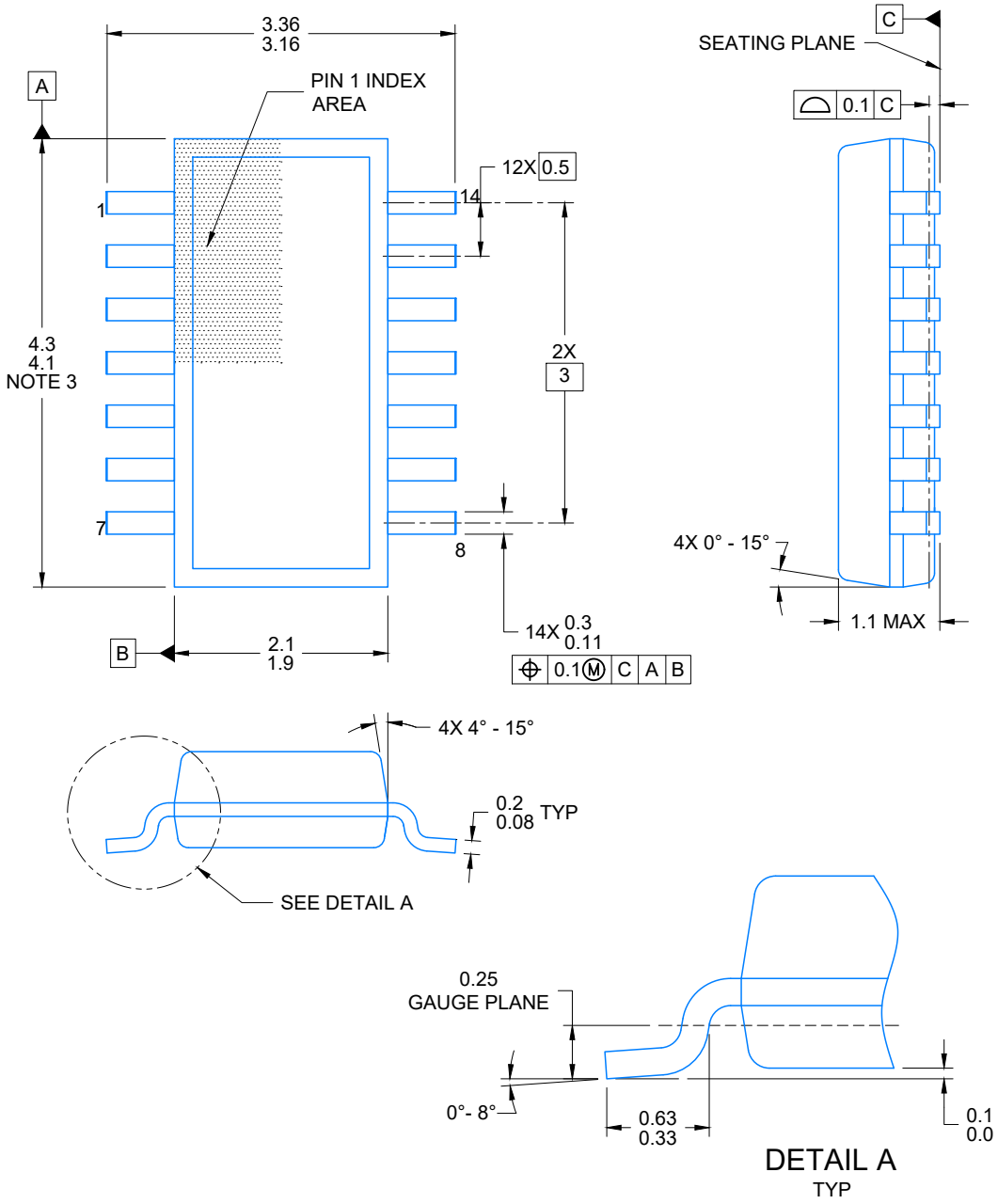
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1046AVDMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0
TCAN1046AVDRQ1	SOIC	D	14	2500	353.0	353.0	32.0
TCAN1046AVDYYRQ1	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TCAN1048AVDMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0
TCAN1048AVDRQ1	SOIC	D	14	2500	353.0	353.0	32.0

PACKAGE OUTLINE

DYY0014A

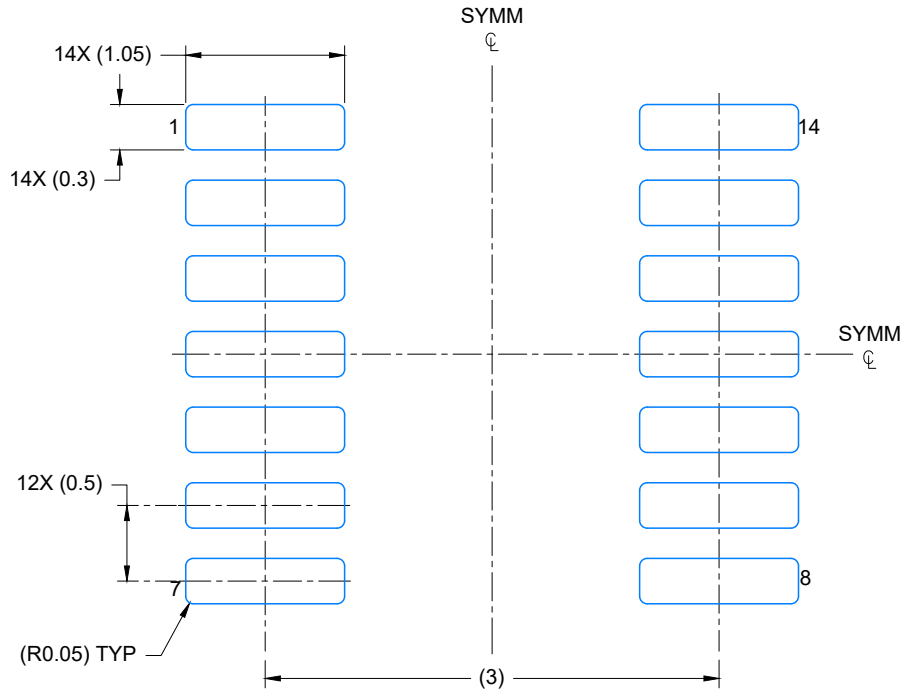
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

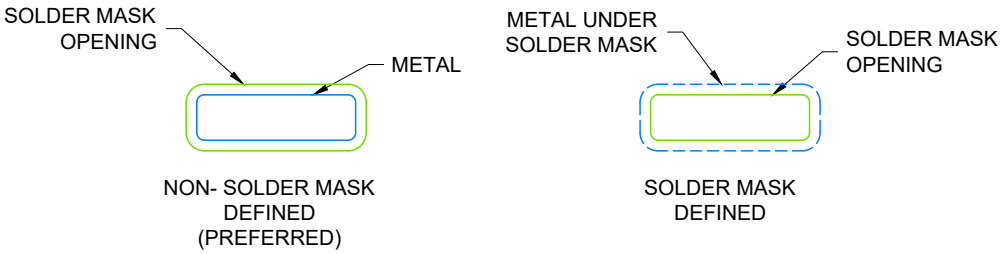


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

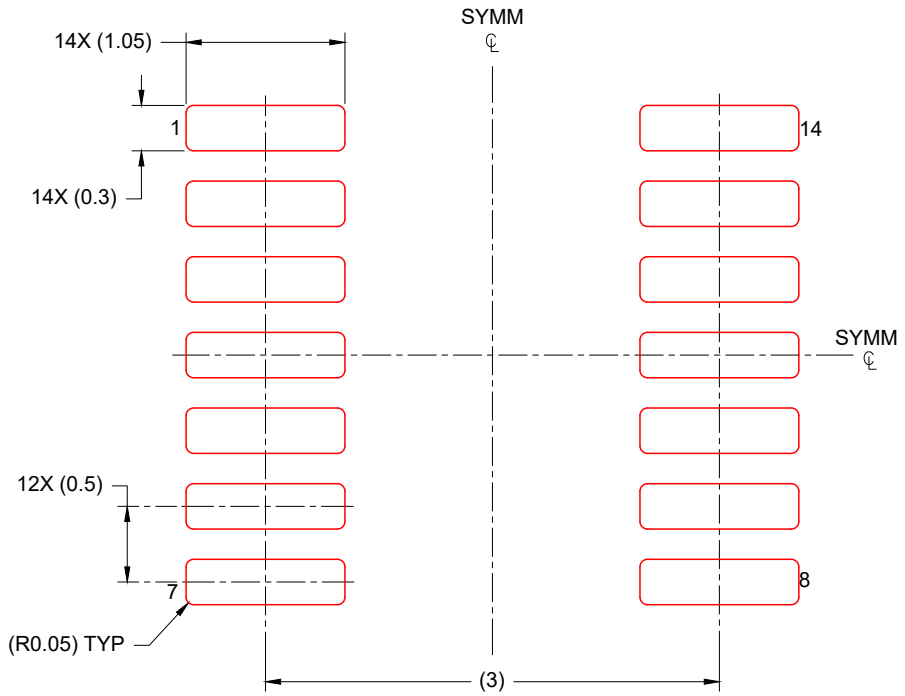


SOLDER MASK DETAILS

4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

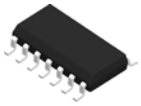


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

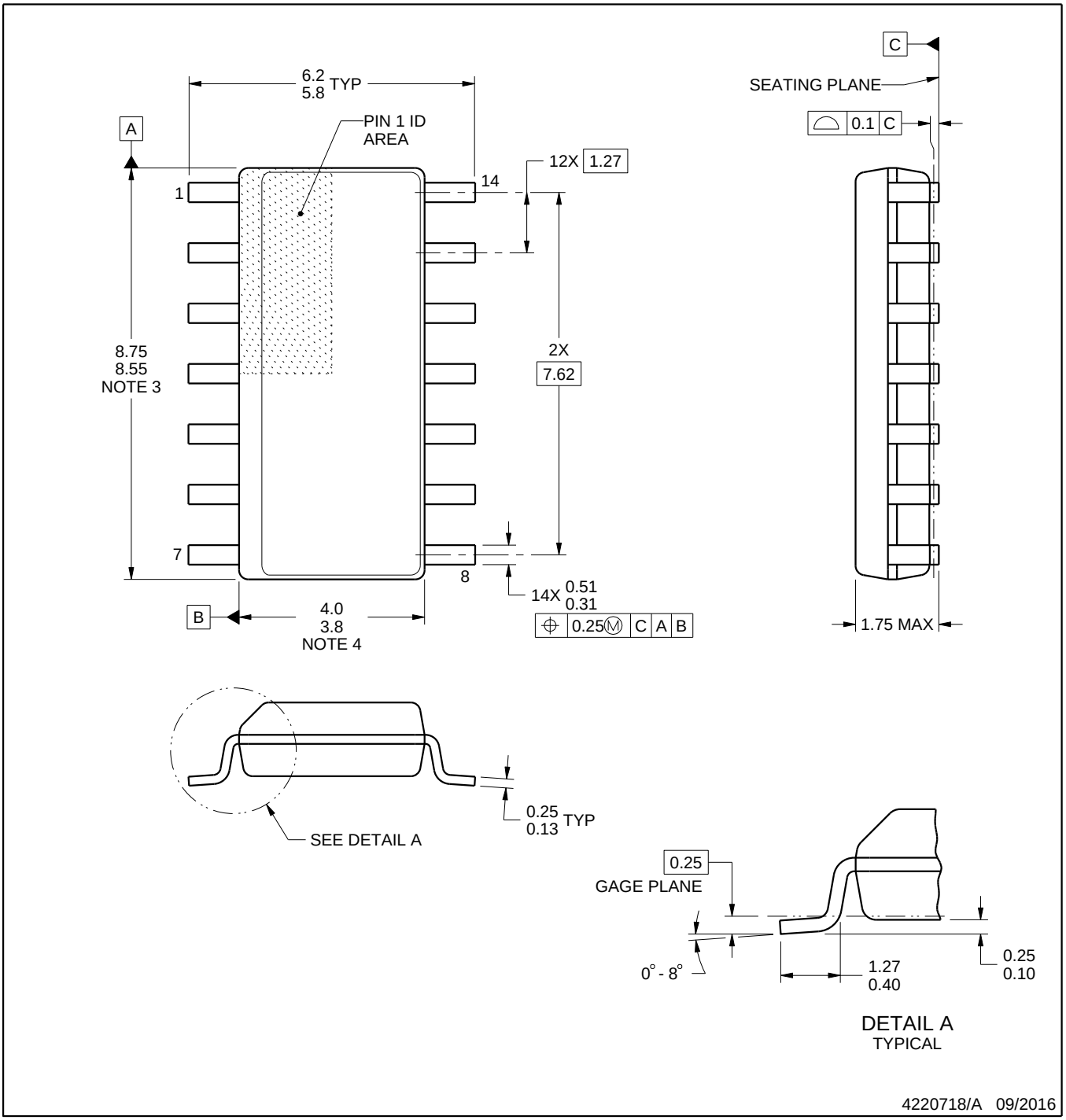


PACKAGE OUTLINE

D0014A

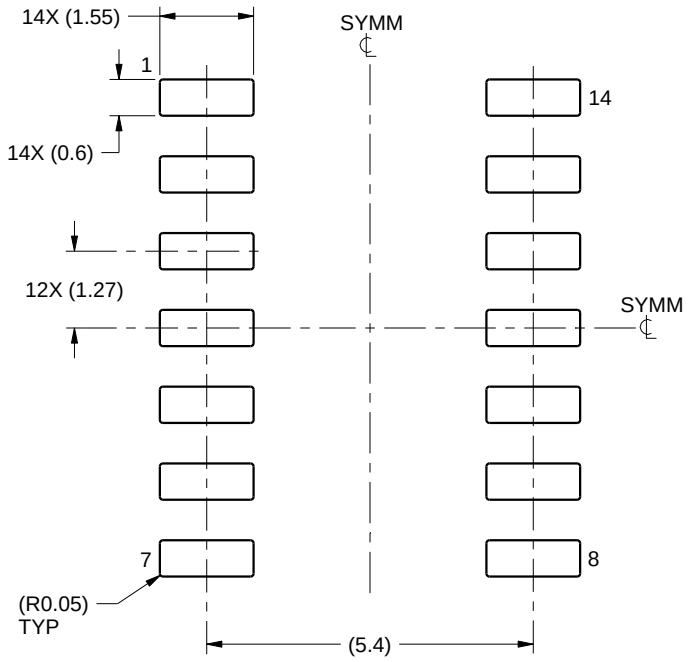
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

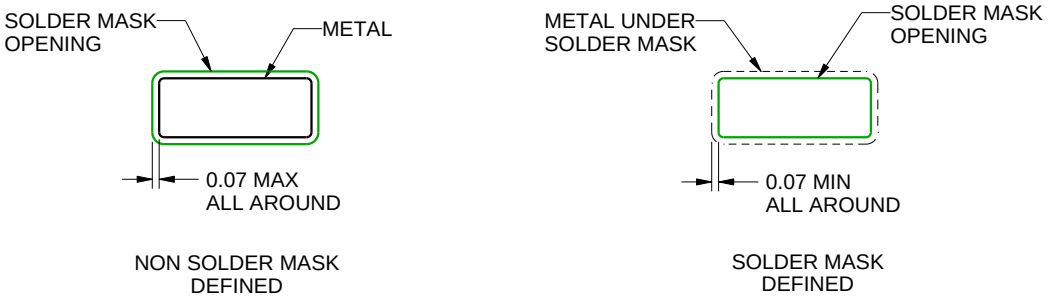


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

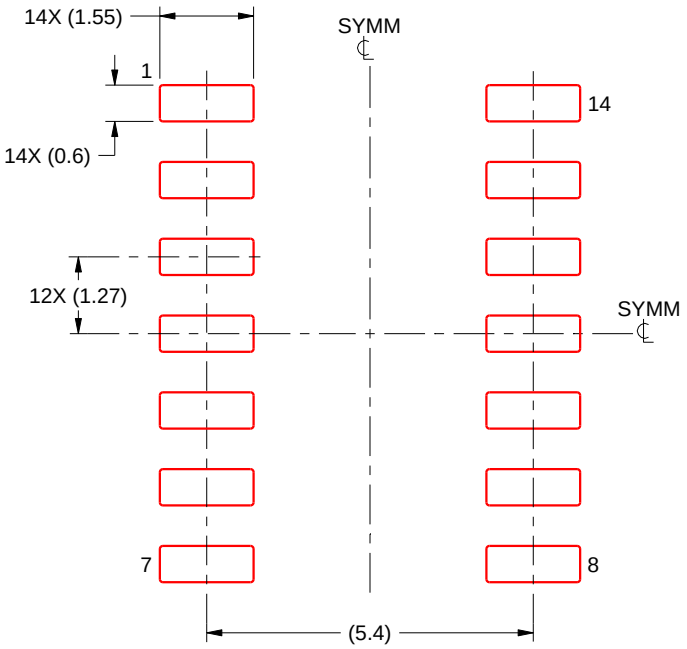
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

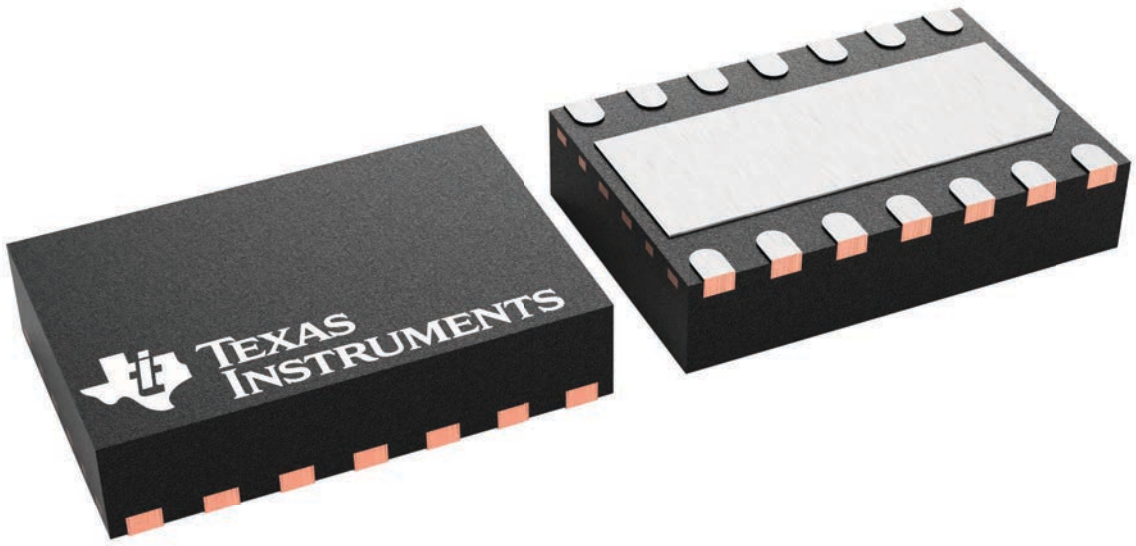
DMT 14

VSON - 0.9 mm max height

3 x 4.5, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



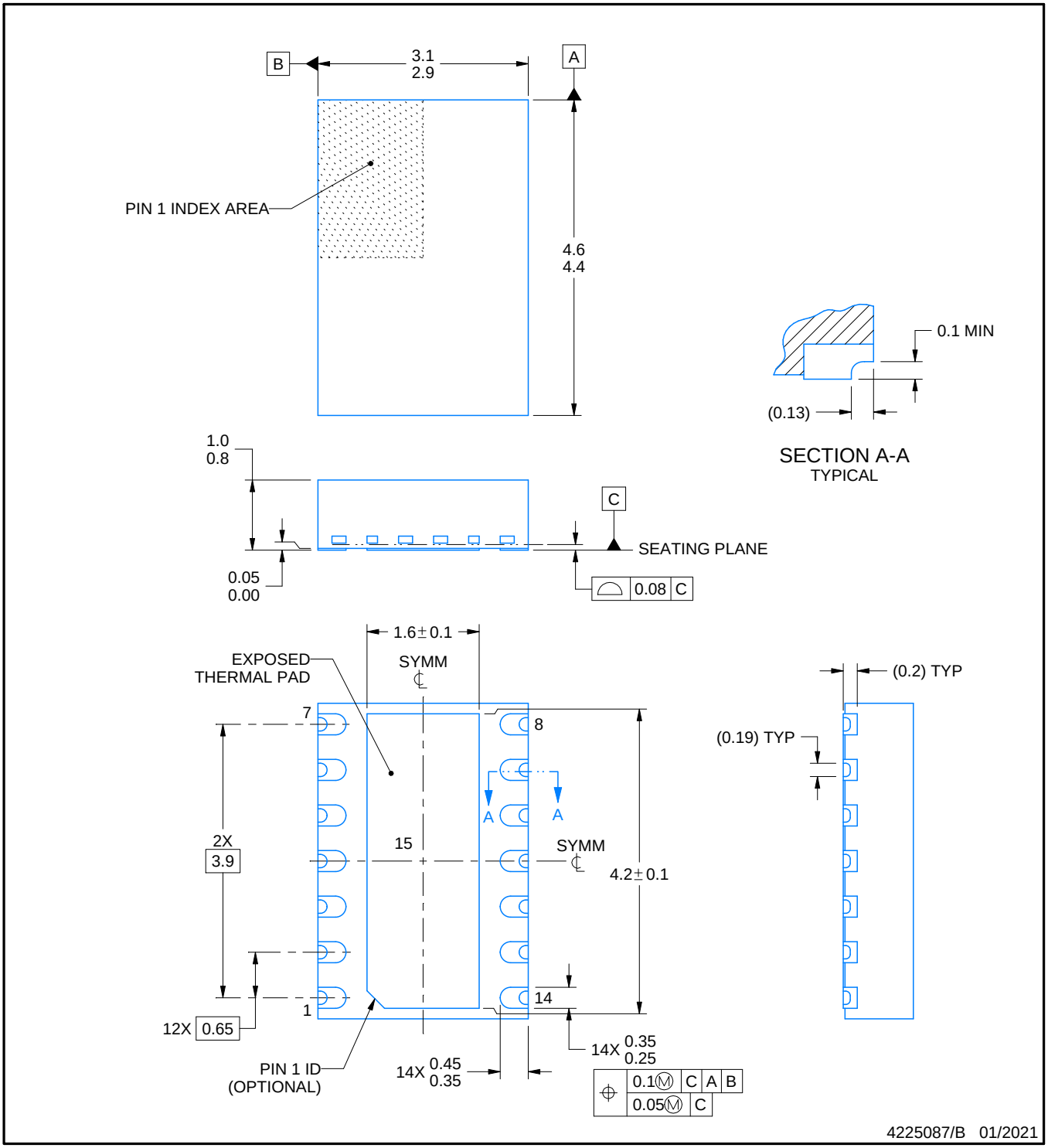
4225088/A

DMT0014B

PACKAGE OUTLINE

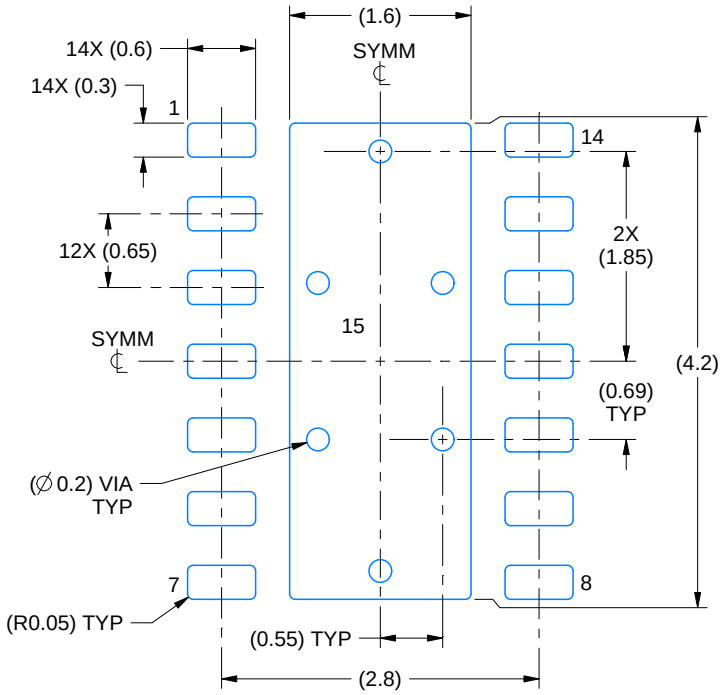
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

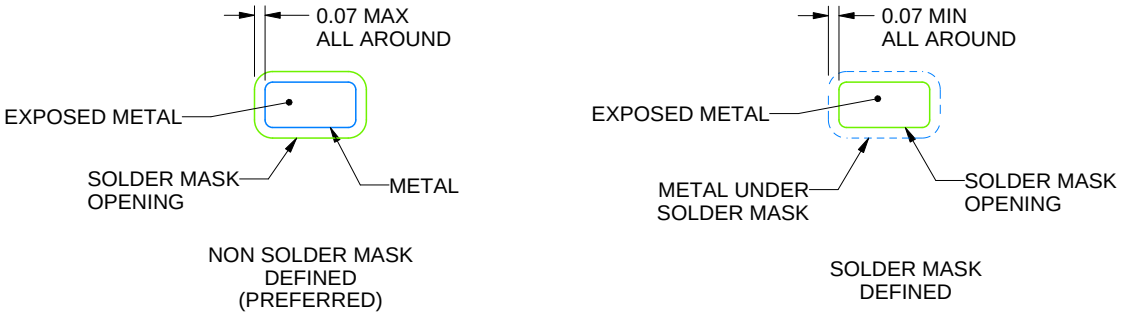


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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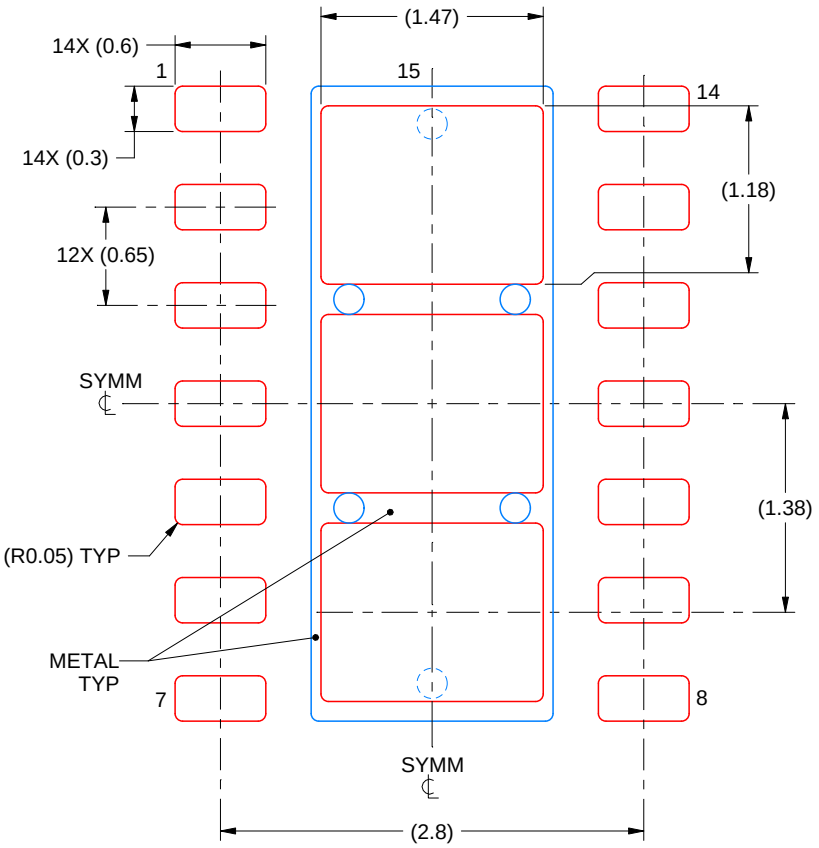
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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