TCAN1476-Q1 Automotive Fault-Protected Dual CAN FD Transceiver With Signal Improvement Capability (SIC) and Standby Mode

1 Features

- AEC Q100 qualified for automotive applications
- Functional Safety-Capable
  – Documentation available to aid functional safety system design
- Two high-speed CAN SIC transceivers with independent mode control in one device
- Meets the requirements of ISO 11898-2:2024 including CAN SIC specifications of Annex A
- Supports CAN FD up to 8Mbps
  – Actively improves the bus signal by reducing ringing effects in complex topologies
  – Backward compatible for use in classic CAN networks
- V_{IO} level shifting supports: 1.7V to 5.5V
- Operating Modes
  – Normal mode
  – Low-power standby mode supporting remote wake-up request
- Passive behavior when unpowered
  – Bus and logic terminals are high impedance (no load to operating bus or application)
  – Hot plug capable: power up/down glitch free operation on bus and RXD output
  – Defined device behavior with floating logic pins and in undervoltage supply conditions
- Protection features
  – IEC ESD protection on bus pins
  – ±58 V CAN bus fault tolerant
  – Undervoltage protection on V_{CC} and V_{IO} (V variants only) supply terminals
  – TXD dominant state timeout (TXD DTO)
  – Thermal shutdown protection (TSD)
- Available in leadless VSON (14) package with wettable flanks for improved automated optical inspection (AOI) capability

2 Applications

- Automotive gateway
- Advanced driver assistance system (ADAS)
- Body electronics and lighting
- Hybrid, electric & powertrain systems
- Automotive infotainment & cluster

3 Description

The TCAN1476-Q1 is a dual, high speed Controller Area Network (CAN) SIC transceiver that meets the physical layer requirements of the ISO 11898-2:2024 Annex A Signal Improvement (SIC) specification. The device reduces signal ringing at dominant-to-recessive edge and enables higher throughput in complex network topologies. Signal improvement capability allows the applications to extract real benefit of CAN FD (flexible data rate) by being able to operate at 2Mbps, 5Mbps or even beyond in large networks with multiple unterminated stubs.

The device meets the timing specifications mandated by ISO 11898-2:2024 Annex A SIC mode specifications; thus, has much tighter bit timing symmetry compared to regular CAN FD transceivers. This provides larger timing window to sample the correct bit and enables error-free communication in large complex star networks where ringing and bit distortion are inherent.

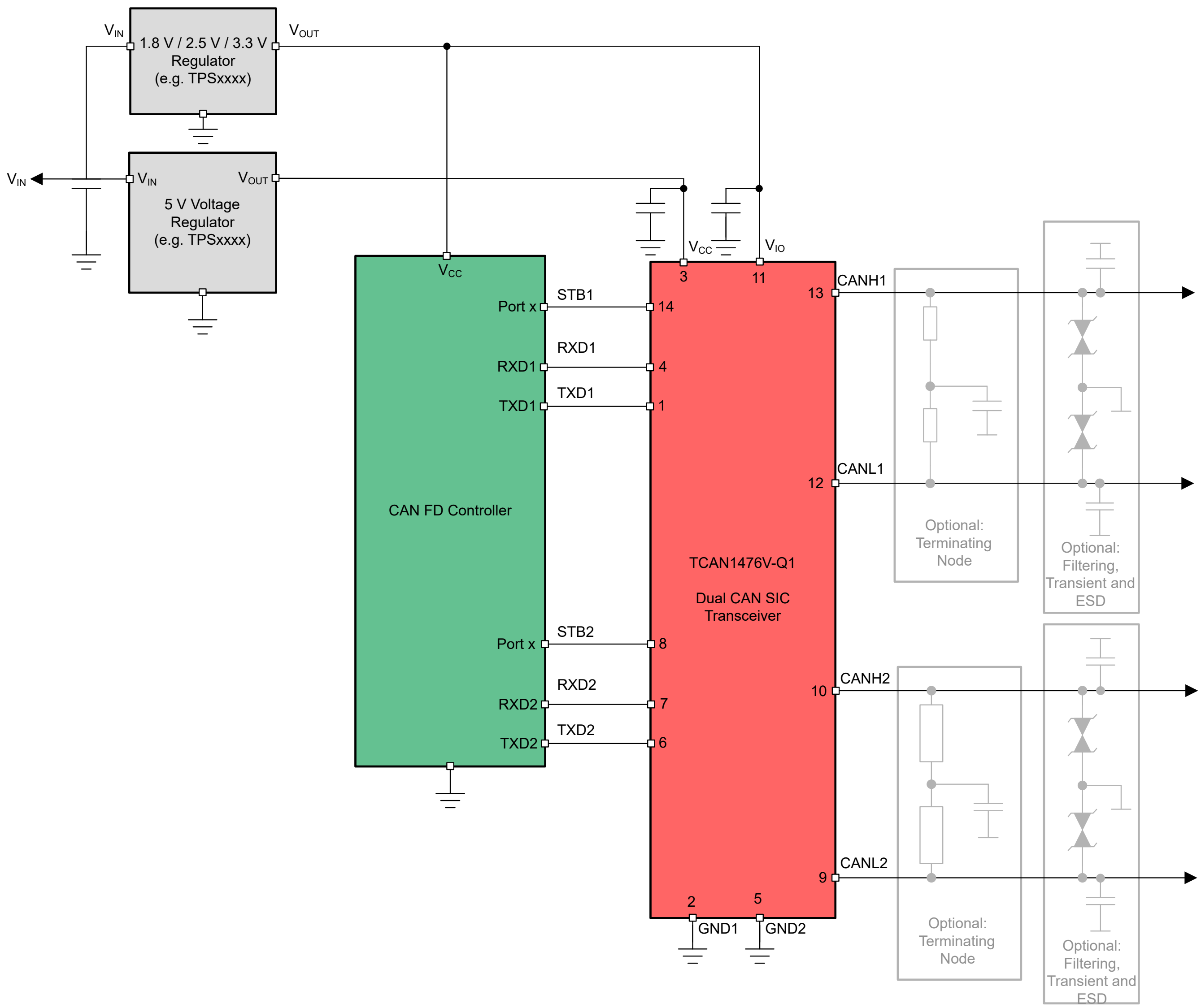
This device is pin-compatible to 14-pin dual CAN FD transceivers, such as TCAN1046A-Q1 or TCAN1046AV-Q1.

The TCAN1476-Q1 devices with suffix "V" include internal logic level translation via the V_{IO} logic supply terminal to allow for interfacing directly to 1.8V, 2.5V, or 3.3V controllers. The two CAN channels support independent mode control through the standby pins. Therefore, each transceiver can be placed into a low-power state, standby mode, without impacting the state of the other CAN channel. The low power standby mode allows remote wake-up via CAN bus compliant with ISO 11898-2:2024 defined wake-up pattern (WUP). The device also includes many protection features such as undervoltage detection, thermal shutdown (TSD), driver dominant timeout (TXD DTO), and ±58V bus fault protection.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TCAN1476-Q1 TCAN1476V-Q1	VSON(14, DMT)	4.5mm x 3mm

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Block Diagram

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4 Device Comparison

Table 4-1. Device Comparison Table

Part Number	Bus Fault Protection on both CAN Channels	Low Voltage I/O Logic Support	SIC per ISO 11898-2:2024 Annex A
TCAN1476-Q1	±58V	No	Yes
TCAN1476V-Q1	±58V	Yes	Yes

5 Pin Configuration and Functions

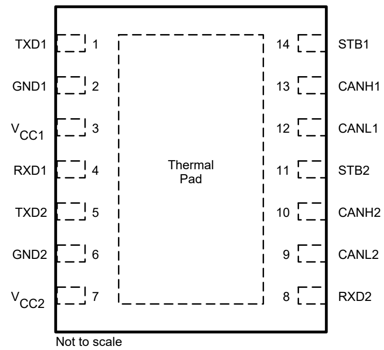


Figure 5-1. TCAN1476-Q1, DMT (VSON) Package, 14 Pin (Top View)

Table 5-1. Pin Functions (TCAN1476-Q1)

Pins		Type	Description
Name	No.		
TXD1	1	Digital Input	CAN transmit data input channel 1; integrated pull-up
GND1	2	GND1	Ground connection, channel 1
V_{CC1}	3	Supply	5V supply voltage, channel 1
RXD1	4	Digital Output	CAN receive data output channel 1; tri-state when V_{CC} < UV_{VCC}
TXD2	5	Digital Input	CAN transmit data input channel 2; integrated pull-up
GND2	6	GND2	Ground connection, channel 2
V_{CC2}	7	Supply	5V supply voltage, channel 2
RXD2	8	Digital Output	CAN receive data output channel 2; tri-state when V_{CC} < UV_{VCC}
CANL2	9	Bus IO	Low-level CAN bus channel 2 input/output line
CANH2	10	Bus IO	High-level CAN bus 2 input/output line
STB2	11	Digital Input	Standby input of channel 2 for mode control; integrated pull-up
CANL1	12	Bus IO	Low-level CAN bus channel 1 input/output line
CANH1	13	Bus IO	High-level CAN bus channel 1 input/output line
STB1	14	Digital Input	Standby input of channel 1 for mode control; integrated pull-up
Thermal Pad (VSON only)		—	Connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

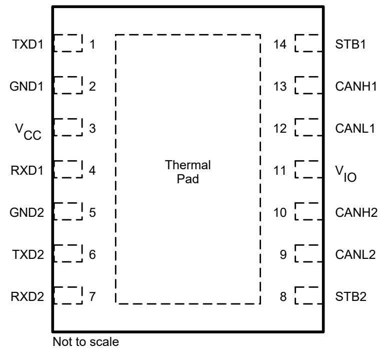


Figure 5-2. TCAN1476V-Q1, DMT (VSON) Package, 14 Pin (Top View)

Table 5-2. Pin Functions (TCAN1476V-Q1)

Pins		Type	Description
Name	No.		
TXD1	1	Digital Input	CAN transmit data input channel 1; integrated pull-up
GND1	2	GND	Ground connection
V_{CC}	3	Supply	5-V supply voltage
RXD1	4	Digital Output	CAN receive data output channel 1; tri-state when $V_{IO} < UV_{VIO}$
GND2	5	GND	Ground connection
TXD2	6	Digital Input	CAN transmit data input channel 2; integrated pull-up
RXD2	7	Digital Output	CAN receive data output channel 2; tri-state when $V_{IO} < UV_{VIO}$
STB2	8	Digital Input	Standby input of channel 2 for mode control; integrated pull-up
CANL2	9	Bus IO	Low-level CAN bus channel 2 input/output line
CANH2	10	Bus IO	High-level CAN bus channel 2 input/output line
V_{IO}	11	Supply	I/O supply voltage
CANL1	12	Bus IO	Low-level CAN bus channel 1 input/output line
CANH1	13	Bus IO	High-level CAN bus channel 1 input/output line
STB1	14	Digital Input	Standby input of channel 1 for mode control; integrated pull-up
Thermal Pad (VSON only)		—	Connect the thermal pad to the printed circuit board (PCB) ground plane for thermal relief

6 Specifications

6.1 Absolute Maximum Ratings

(1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
V_{IO}	Supply voltage I/O level shifter (Devices with the "V" suffix)	–0.3	6	V
V_{BUS}	CAN bus I/O voltage range on CANH1/CANH2 and CANL1/CANL2	–58	58	V
V_{DIFF}	Max differential voltage between CANHx and CANLx V_{DIFF} = (CANH - CANL)	–45	45	V
V_{Logic_Input}	Logic pin input voltage (TXD1/TXD2, STB1/STB2)	–0.3	6	V
V_{RXD}	Logic output voltage range (RXD1/RXD2)	–0.3	6	V
$I_{O(RXD)}$	RXD1/RXD2 output current	–8	8	mA
T_J	Junction temperature	–40	165	°C
T_{STG}	Storage temperature	–65	165	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	HBM classification level 3A for all pins	±4000	V
			HBM classifitation level 3B for global pins CANHx and CANLx with respect to GND	±10000	V
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C5 for all pins		±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings, IEC Transients

				VALUE	UNIT
V_{ESD}	System level electrostatic discharge	CAN bus terminals to GND CANH1, CANH2, CANL1, CANL2	SAE J2962-2 per ISO 10605 Powered contact discharge	±8000	V
			SAE J2962-2 per ISO 10605 Powered air discharge	±15000	V
			IEC 62228-3 per ISO 10605	±8000	V
V_{Tran}	ISO 7637-2 Transient immunity[1]		Pulse 1	–100	V
			Pulse 2a	75	V
			Pulse 3a	–150	V
			Pulse 3b	100	V
	Direct capacitor coupling, SAE J2962-2 per ISO 7637-3[2]		DCC slow transient pulse	±30	V

(1) Tested according to IEC 62228-3:2019 CAN Transcievers, Section 6.3; standard pulses parameters defined in ISO 7637-2 (2011)
(2) Tested according to SAE J2962-2

6.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IO}	Supply voltage for IO level shifter (Devices with V_{IO})	1.7		5.5	V
$I_{OH(RXDx)}$	RXDx terminal high-level output current	–1.5			mA
$I_{OL(RXDx)}$	RXDx terminal low-level output current			1.5	mA
T_J	Junction temperature	–40		150	°C

6.5 Thermal Characteristics

THERMAL METRIC(1)		TCAN1476-Q1	UNIT
		DMT (VSON)	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance		℃/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance		℃/W
$R_{\Theta JB}$	Junction-to-board thermal resistance		℃/W
Ψ_{JT}	Junction-to-top characterization parameter		℃/W
Ψ_{JB}	Junction-to-board characterization parameter		℃/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		℃/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Supply Characteristics

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 5V, V_{IO} = 3.3V (for devices with V_{IO}), Device ambient maintained at 27℃) unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC} [1]	Supply current Normal mode	Dominant One channel[2]	STB1 = STB2 = 0V TXDx = 0V, TXDy = V_{IO} R_{L1} = R_{L2} = 60Ω, C_L = open		50	77.5	mA
			STB1 = STB2 = 0V TXDx = 0V, TXDy = V_{IO} R_{L1} = R_{L2} = 50Ω, C_L = open		55	87.5	mA
		Dominant Two channels[2]	STB1 = STB2 = 0V TXDx = TXDy = 0V R_{L1} = R_{L2} = 60Ω, C_L = open		95	140	mA
			STB1 = STB2 = 0V TXDx = TXDy = 0V R_{L1} = R_{L2} = 50Ω, C_L = open		100	160	mA
		Recessive Two channels[2]	STB1 = STB2 = 0V TXDx = TXDy = V_{IO} R_{L1} = R_{L2} = 50Ω, C_L = open		14	22	mA
		CANx dominant with bus fault CANy recessive[2] [3]	STB1 = STB2 = 0V TXDx = 0V, TXDy = V_{IO} CANHx = CANLx = ±25V R_{Lx} = open, R_{Ly} = 50Ω, C_L = open		90	137.5	mA
		CANx dominant with bus fault CANy dominant[2] [3]	STB1 = STB2 = 0V TXDx = TXDy = 0V CANHx = CANLx = ±25V R_{Lx} = open, R_{Ly} = 50Ω, C_L = open		135	210	mA
		CANx and CANy dominant with bus fault[2] [3]	STB1 = STB2 = 0V TXDx = TXDy = 0V CANHx = CANLx = ±25V CANHy = CANLy = ±25V R_{Lx} = open, R_{Ly} = open, C_L = open		170	260	mA
	Supply current Standby mode (Devices with V_{IO})[2]		TXDx = TXDy = STB1 = STB2 = V_{IO} R_{L1} = R_{L2} = 50Ω, C_L = open, T_J ≤ 85°C			2	µA
			TXDx = TXDy = STB1 = STB2 = V_{IO} R_{L1} = R_{L2} = 50Ω, C_L = open, T_J ≤ 125°C			4	µA
			TXDx = TXDy = STB1 = STB2 = V_{IO} R_{L1} = R_{L2} = 50Ω, C_L = open, T_J ≤ 150°C			10	µA
	Supply current Standby mode (Devices without V_{IO})[2]		TXDx = TXDy = STB1 = STB2 = V_{CC} R_{L1} = R_{L2} = 50Ω, C_L = open, T_J ≤ 85°C			30	µA
			TXDx = TXDy = STB1 = STB2 = V_{CC} R_{L1} = R_{L2} = 50Ω, C_L = open, T_J ≤ 125°C			32	µA
			TXDx = TXDy = STB1 = STB2 = V_{CC} R_{L1} = R_{L2} = 50Ω, C_L = open, T_J ≤ 150°C			42	µA
I_{IO}	I/O supply current Normal mode	Dominant One channel[2]	STB1 = STB2 = 0V TXDx = 0V, TXDy = V_{IO} R_{Lx} = R_{Ly} = 60Ω, C_L = open RXD1 and RXD2 floating		150	350	µA
		Dominant Two channels[2]	STB1 = STB2 = 0V TXDx = TXDy = 0V R_{Lx} = R_{Ly} = 60Ω, C_L = open RXD1 and RXD2 floating		255	600	µA
		Recessive Two channels[2]	STB1 = STB2 = 0V TXDx = TXDy = V_{IO} R_{Lx} = R_{Ly} = 60Ω, C_L = open RXD1 and RXD2 floating		50	100	µA
	I/O supply current Standby mode[2]		STB1 = STB2 = V_{IO} TXDx = TXDy = V_{IO} R_{Lx} = R_{Ly} = 60Ω, C_L = open RXD1 and RXD2 floating			36	µA
$UV_{CC(R)}$	Undervoltage detection V_{CC} rising		Ramp up		4.2	4.4	V
$UV_{CC(F)}$	Undervoltage detection on V_{CC} falling		Ramp down	3.5	4		V
$UV_{IO(R)}$	Undervoltage detection V_{IO} rising		Ramp up		1.6	1.65	V

6.6 Supply Characteristics (continued)

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 5V, V_{IO} = 3.3V (for devices with V_{IO}), Device ambient maintained at 27℃) unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$UV_{IO(F)}$	Undervoltage detection on V_{IO} falling	Ramp down	1.4	1.5		V

(1) For devices without V_{IO}, parameter I_{CC} represents the sum of currents into V_{CC1} and V_{CC2}.
(2) TXD1 and TXD2 are interchangeable for TXDx and TXDy
(3) CAN1 and CAN2 are interchangeable for CANx and CANy

6.7 Dissipation Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	One channel Average power dissipation Normal mode	V_{CC} = 5V, V_{IO} = 3.3V, T_J = 27°C, R_L = 60Ω, C_{L_RXD} = 15pF TXD input = 250kHz 50% duty cycle square wave		60		mW
		V_{CC} = 5.5V, V_{IO} = 5.5V, T_J = 150°C, R_L = 50Ω, C_{L_RXD} = 15pF TXD input = 2.5MHz 50% duty cycle square wave		120		mW
T_{TSD}	Thermal shutdown temperature			192		°C
T_{TSD_HYS}	Thermal shutdown hysteresis			10		°C

6.8 Electrical Characteristics

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 5V, V_{IO} = 3.3V, Device ambient maintained at 27℃) unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver Electrical Characteristics							
$V_{CANH(D)}$	Dominant output voltage normal mode	CANH	V_{CC} = 4.5V to 5.5V, TXD = 0V, STB = 0V 50Ω ≤ R_L ≤ 65Ω, C_L = open, See Figure 7-2 and Figure 8-6	2.75	3.5	4.5	V
$V_{CANL(D)}$		CANL		0.5	1.5	2.25	V
$V_{CANH(D)}$	Dominant output voltage normal mode	CANH	V_{CC} = 4.75V to 5.25V, TXD = 0V, STB = 0V 45Ω ≤ R_L ≤ 65Ω, C_L = open	3	3.5	4.26	V
$V_{CANL(D)}$		CANL		0.75	1.5	2.01	V
$V_{CANH(R)}$, $V_{CANL(R)}$	Recessive output voltage normal mode	CANH and CANL	V_{CC} = 4.5V to 5.5V, TXD = V_{IO}, STB = 0V R_L = open (no load), C_L = open, See Figure 7-2 and Figure 8-6	2	2.5	3	V
$V_{CANH(R)}$, $V_{CANL(R)}$	Recessive output voltage normal mode	CANH and CANL	V_{CC} = 4.75V to 5.25V, TXD = V_{IO}, STB = 0V 45Ω ≤ R_L ≤ 65Ω , C_L = 4.7nF	2.256		2.756	V
V_{SYM}	Driver symmetry ($V_{O(CANH)}$ + $V_{O(CANL)}$)/($V_{CANH(R)}$ + $V_{CANL(R)}$)		V_{CC} = 4.75 V to 5.25 V, TXD = 250 kHz, 1 MHz, 2.5 MHz, STB = 0 V 45 Ω ≤ R_L ≤ 65 Ω, C_{SPLIT} = 4.7 nF, C_L = open, See Figure 7-2 and Figure 9-3	0.95		1.05	V/V
			V_{CC} = 4.5V to 5.5V, TXD = 250kHz, 1MHz, 2.5MHz, STB = 0V 45Ω ≤ R_L ≤ 65Ω, C_{SPLIT} = 4.7nF, C_L = open, See Figure 7-2 and Figure 9-3	0.9		1.1	V/V

6.8 Electrical Characteristics (continued)

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 5V, V_{IO} = 3.3V, Device ambient maintained at 27℃) unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DIFF(D)}$	Differential output voltage normal mode Dominant	CANH - CANL	V_{CC} = 4.75V to 5.25V, TXD = 0V, STB = 0 V 45Ω ≤ R_L ≤ 65Ω, C_L = open, See Figure 7-2 and Figure 8-6	1.5		3	V
			V_{CC} = 4.75V to 5.25V, TXD = 0V, STB = 0V 45Ω ≤ R_L ≤ 70Ω, C_L = open, See Figure 7-2 and Figure 8-6	1.5		3.3	V
			V_{CC} = 4.5V to 5.5V, TXD = 0V, STB = 0V 50Ω ≤ R_L ≤ 65Ω, C_L = open, See Figure 7-2 and Figure 8-6	1.5		3	V
			V_{CC} = 4.5V to 5.5V, TXD = 0V, STB = 0V 45Ω ≤ R_L ≤ 70Ω, C_L = open, See Figure 7-2 and Figure 8-6	1.4		3.3	V
			V_{CC} = 4.5V to 5.5V, TXD = 0V, STB = 0 V R_L = 2240Ω, C_L = open, See Figure 7-2 and Figure 8-6	1.5		5	V
$V_{DIFF(R)}$	Differential output voltage normal mode Recessive	CANH - CANL	TXD = V_{IO}, STB = 0V 45Ω ≤ R_L ≤ 65Ω, C_{SPLIT} = 4.7nF, C_L = open, See Figure 7-2 and Figure 8-6	–50		50	mV
			TXD = V_{IO}, STB = 0V R_L = open, C_L = open, See Figure 7-2 and Figure 8-6	–50		50	mV
$V_{CANH(INACT)}$	Bus output voltage standby mode	CANH	TXD = STB = V_{IO} R_L = open , C_L = open, See Figure 7-2 and Figure 8-6	-0.1		0.1	V
$V_{CANL(INACT)}$		CANL		-0.1		0.1	V
$V_{DIFF(INACT)}$		CANH - CANL		-0.2		0.2	V
$R_{DIFF(DOM)}$	Differential input resistance in dominant phase		TXD = 0V, STB = 0V, See Figure 8-2		40		Ω
$R_{SE\_SIC\_ACT\_REC}$	Single ended resistance CANH/CANL in active recessive phase		V_{CC} = 4.75V to 5.25V, 2V ≤ $V_{CANH/L}$ ≤ V_{CC} - 2V	37.5	50	66.5	Ω
$R_{DIFF\_SIC\_ACT\_REC}$	Differential input resistance in active recessive drive phase		V_{CC} = 4.75V to 5.25V, 2V ≤ $V_{CANH/L}$ ≤ V_{CC} - 2V	75	100	133	Ω
$I_{CANH(OS)}$	Short-circuit bus output current, TXD is dominant or recessive or toggling, normal mode		$V_{(CANH)}$ = -15V to 40V, CANL = open, TXD = 0V or V_{IO} or 250kHz, 2.5MHz square wave, See Figure 7-7 and Figure 8-6	–115		115	mA
$I_{CANL(OS)}$			$V_{(CAN\_L)}$ = -15V to 40V, CANH = open, TXD = 0V or V_{IO} or 250kHz, 2.5MHz square wave, See Figure 7-7 and Figure 8-6	–115		115	mA
Receiver Electrical Characteristics							
V_{IT}	Input threshold voltage normal mode		-12V ≤ V_{CM} ≤ 12V, STB = 0V, See Figure 7-3 and Table 8-6	500		900	mV
$V_{IT(STB)}$	Input threshold standby mode		-12V ≤ V_{CM} ≤ 12V, STB = V_{IO} , See Figure 7-3 and Table 8-6	400		1150	mV
$V_{DIFF\_RX(D)}$	Normal mode dominant state differential input voltage range		-12V ≤ V_{CM} ≤ 12V, STB= 0V, See Figure 7-3 and Table 8-6	0.9		9	V
$V_{DIFF\_RX(R)}$	Normal mode recessive state differential input voltage range		-12V ≤ V_{CM} ≤ 12V , STB = 0V, See Figure 7-3 and Table 8-6	-4		0.5	V
$V_{DIFF\_RX(D\_INACT)}$	Standby mode dominant state differential input voltage range		STB = V_{IO}, -12V ≤ V_{CM} ≤ 12V, See Figure 7-3 and Table 8-6	1.15		9	V
$V_{DIFF\_RX(R\_INACT)}$	Standby mode recessive state differential input voltage range		STB = V_{IO}, -12V ≤ V_{CM} ≤ 12V, See Figure 7-3 and Table 8-6	-4		0.4	V
V_{HYS}	Hysteresis voltage for input threshold normal mode		-12V ≤ V_{CM} ≤ 12V, STB = 0V, See Figure 7-3 and Table 8-6		100		mV
V_{CM}	Common mode range normal and standby modes		See Figure 7-3 and Table 8-6	–12		12	V
$I_{LKG(OFF)}$	Unpowered bus input leakage current		CANH = CANL = 5V, V_{CC} = V_{IO} = GND			5	µA

6.8 Electrical Characteristics (continued)

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 5V, V_{IO} = 3.3V, Device ambient maintained at 27℃) unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{IO}			20	pF
C_{ID}	Differential input capacitance across bus terminals				10	pF
$R_{DIFF\_PAS\_REC}$	Differential input resistance in passive recessive phase	TXD = $V_{IO,}$ STB = 0V -12V ≤ V_{CM} ≤ 12V, Delta V/Delta I	40		90	kΩ
$R_{SE\_PAS\_REC}$	Single ended input resistance in passive recessive phase (CANH or CANL)		20		45	kΩ
m_R	Input resistance matching [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100 %	$V_{(CAN\_H)}$ = $V_{(CAN\_L)}$ = 5V	–1		1	%
TXD Terminal (CAN Transmit Data Input)						
V_{IH}	High-level input voltage	Devices without V_{IO}	0.7 V_{CC}			V
V_{IH}	High-level input voltage	Devices with V_{IO}	0.7 V_{IO}			V
V_{IL}	Low-level input voltage	Devices without V_{IO}			0.3 V_{CC}	V
V_{IL}	Low-level input voltage	Devices with V_{IO}			0.3 V_{IO}	V
I_{IH}	High-level input leakage current	TXD = V_{CC} = V_{IO} = 5.5V	–2.5	0	1	μA
I_{IL}	Low-level input leakage current	TXD = 0V, V_{CC} = V_{IO} = 5.5V	–200	-100	–20	μA
$I_{LKG\_TXD(OFF)}$	Unpowered leakage current	TXD = 5.5V, V_{CC} = V_{IO} = 0V	–1	0	1	μA
C_{I_TXD}	Input capacitance	V_{IN} = 0.4×sin(2×π×2×10^6×t)+2.5V		6		pF
RXD Terminal (CAN Receive Data Output)						
V_{OH}	High-level output voltage	Devices without V_{IO} I_O = –1.5mA, See Figure 7-3	0.8 V_{CC}			V
V_{OH}	High-level output voltage	I_O = –1.5mA, Devices with V_{IO} See Figure 7-3	0.8 V_{IO}			V
V_{OL}	Low-level output voltage	Devices without V_{IO} I_O = 1.5mA, See Figure 7-3			0.2 V_{CC}	V
V_{OL}	Low-level output voltage	Devices with V_{IO} I_O = 1.5mA, Devices with V_{IO} See Figure 7-3			0.2 V_{IO}	V
$I_{LKG\_RXD(OFF)}$	Unpowered leakage current	RXD = 5.5V, V_{CC} = V_{IO} = 0V	–1	0	1	μA
STB Terminal (Standby Mode Input)						
V_{IH}	High-level input voltage	Devices without V_{IO}	0.7 V_{CC}			V
V_{IH}	High-level input voltage	Devices with V_{IO}	0.7 V_{IO}			V
V_{IL}	Low-level input voltage	Devices without V_{IO}			0.3 V_{CC}	V
V_{IL}	Low-level input voltage	Devices with V_{IO}			0.3 V_{IO}	V
I_{IH}	High-level input leakage current	V_{CC} = V_{IO} = STB = 5.5V	–2		2	μA
I_{IL}	Low-level input leakage current	V_{CC} = V_{IO} = 5.5V, STB = 0V	–20		–2	μA
$I_{LKG\_STB(OFF)}$	Unpowered leakage current	STB = 5.5V, V_{CC}= V_{IO} = 0V	–1	0	1	μA

6.9 Switching Characteristics

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 5V, V_{IO} = 3.3V, Device ambient maintained at 27℃) unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device Switching Characteristics						
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	See Figure 7-4 , normal mode, V_{IO} = 4.5V to 5.5V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%)		90	145	ns
		See Figure 7-4 , normal mode, V_{IO} = 3V to 3.6V, 4Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%)		95	155	ns
		See Figure 7-4 , normal mode, V_{IO} = 2.25V to 2.75V, 45Ω ≤ R_L ≤ 65Ω, C_L = 10pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%)		110	170	ns
		See Figure 7-4 , normal mode, V_{IO} = 1.71V to 1.89V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%)		125	190	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive	See Figure 7-4 , normal mode, V_{IO} = 4.5V to 5.5V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%)		95	150	ns
		See Figure 7-4 , normal mode, V_{IO} = 3V to 3.6V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%)		100	160	ns
		See Figure 7-4 , normal mode, V_{IO} = 2.25V to 2.75V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%)		110	175	ns
		See Figure 7-4 , normal mode, V_{IO} = 1.71V to 1.89V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%)		125	190	ns
t_{MODE}	Mode change time, from normal to standby or from standby to normal	See Figure 7-5			30	μs
t_{WK_FILTER}	Filter time for a valid wake-up pattern	See Figure 8-8	0.5		0.95	μs
$t_{WK\_TIMEOUT}$	Bus wake-up timeout value	See Figure 8-8	0.8		6	ms
Tstartup	Time duration after V_{CC} or V_{IO} hass cleared rising undervoltage threshold, and device can resume normal operation				1.5	ms
$T_{filter(STB)}$	Filter on STB pin to filter out any glitches		0.5	1	2	μs
Driver Switching Characteristics						
$t_{prop(TxD\text{-}busrec)}$	Propagation delay time, low-to-high TXD edge to driver recessive (dominant to recessive)	See Figure 7-2 , STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), V_{IO} = 4.5V to 5.5V		35	70	ns
		See Figure 7-2 STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), V_{IO} = 3V to 3.6V		40	70	ns
		See Figure 7-2 STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), V_{IO} = 2.25V to 2.75V		40	75	ns
		See Figure 7-2 STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), V_{IO} = 1.71V to 1.89V		42	80	ns
$t_{prop(TxD\text{-}busdom)}$	Propagation delay time, high-to-low TXD edge to driver dominant (recessive to dominant)	See Figure 7-2 , STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), V_{IO} = 4.5V to 5.5V		35	75	ns
		See Figure 7-2 STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), V_{IO} = 3V to 3.6V		35	75	ns
		See Figure 7-2 STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), V_{IO} = 2.25V to 2.75V		40	80	ns
		See Figure 7-2 STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), V_{IO} = 1.71V to 1.89V		42	80	ns

6.9 Switching Characteristics (continued)

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 5V, V_{IO} = 3.3V, Device ambient maintained at 27℃) unless otherwise noted

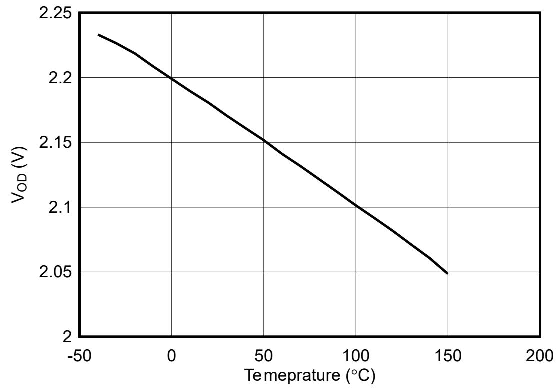
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{sk(p)}$	Pulse skew (|$t_{prop(TxD-busrec)}$ - $t_{prop(TxD-busdom)}$|)	STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), See Figure 7-2		1	10	ns
t_{BUS_R}	Differential output signal rise time	See Figure 7-2 , STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%)		15	30	ns
t_{BUS_F}	Differential output signal fall time	See Figure 7-2 , STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%)		15	40	ns
t_{TXD_DTO}	Dominant timeout	See Figure 7-6 , 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), STB = 0V	1.2		4.0	ms
Receiver Switching Characteristics						
$t_{prop(busrec-RXD)}$	Propagation delay time, bus recessive input to RXD high output (dominant to recessive)	See Figure 7-3 , STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%), V_{IO} = 4.5V to 5.5V		60	85	ns
		See Figure 7-3 STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%), V_{IO} = 3V to 3.6V		65	95	ns
		See Figure 7-3 STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%), V_{IO} = 2.25V to 2.75V		70	105	ns
		See Figure 7-3 STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%), V_{IO} = 1.71V to 1.89V		80	110	ns
$t_{prop(busdom-RXD)}$	Propagation delay time, bus dominant input to RXD low output (recessive to dominant)	See Figure 7-3 , STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%), V_{IO} = 4.5V to 5.5V		50	75	ns
		See Figure 7-3 STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%), V_{IO} = 3V to 3.6V		60	80	ns
		See Figure 7-3 STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%), V_{IO} = 2.25V to 2.75V		65	90	ns
		See Figure 7-3 STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%), V_{IO} = 1.71V to 1.89V		80	110	ns
t_{RXD_R}	RXD output signal rise time	See Figure 7-3 , STB = 0V, $C_{L(RXD)}$ = 15pF(≤ ±1%)		8	25	ns
t_{RXD_F}	RXD output signal fall time			7	30	ns
FD Timing Characteristics						
$t_{BIT(BUS)}$	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 500 ns	V_{CC} = 4.5V to 5.5V, STB = 0V, 4 Ω ≤ R_L ≤ 65Ω , C_L = 100pF, $C_{L(RXD)}$ = 15pF	490		510	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 200 ns	V_{CC} = 4.5V to 5.5V, STB = 0 V, 45Ω ≤ R_L ≤ 65Ω , C_L = 100pF, $C_{L(RXD)}$ = 15pF	190		210	ns
	Bit time on CAN bus output pins with $t_{BIT(TXD)}$ = 125 ns	V_{CC} = 4.5V to 5.5V, STB = 0 V, 45Ω ≤ R_L ≤ 65Ω , C_L = 100pF, $C_{L(RXD)}$ = 15pF	115		135	ns
$t_{BIT(RXD)}$	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 500 ns	V_{CC} = 4.75V to 5.25V, STB = 0V, 45 Ω ≤ R_L ≤ 65Ω , C_L = 100pF, $C_{L(RXD)}$ = 15pF	470		520	ns
		V_{CC} = 4.5V to 5.5V, STB = 0V, 45Ω ≤ R_L ≤ 65Ω , C_L = 100pF, $C_{L(RXD)}$ = 15pF	470		525	ns
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 200 ns	V_{CC} = 4.75V to 5.25V, STB = 0V, 45Ω ≤ R_L ≤ 65Ω , C_L = 100pF, $C_{L(RXD)}$ = 15pF	170		220	ns
		V_{CC} = 4.5V to 5.5V, STB = 0 V, 45Ω ≤ R_L ≤ 65Ω , C_L = 100pF, $C_{L(RXD)}$ = 15pF	170		225	ns
	Bit time on RXD output pins with $t_{BIT(TXD)}$ = 125 ns	V_{CC} = 4.75V to 5.25V, STB = 0V, 45Ω ≤ R_L ≤ 65Ω , C_L = 100pF, $C_{L(RXD)}$ = 15pF	95		145	ns
		V_{CC} = 4.5V to 5.5V, STB = 0 V, 45Ω ≤ R_L ≤ 65Ω , C_L = 100pF, $C_{L(RXD)}$ = 15pF	95		150	ns
Signal Improvement Timing Characteristics						

6.9 Switching Characteristics (continued)

parameters valid over recommended operating conditions with -40℃ ≤ T_J ≤ 150℃ (Typical values are at V_{CC} = 5V, V_{IO} = 3.3V, Device ambient maintained at 27℃) unless otherwise noted

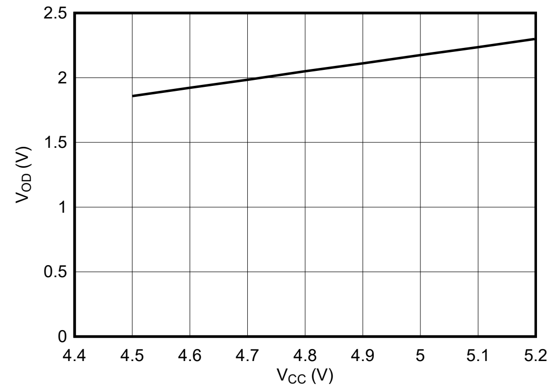
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PAS\_REC\_START}$	Start time of passive recessive phase	Time duration from TXD rising 50% edge (<5ns slope) to start of passive recessive phase	420		530	ns
$t_{ACT\_REC\_START}$	Start time of active signal improvement phase	Time duration from TXD rising 50% edge (<5ns slope) to start of passive recessive phase			120	ns
$t_{ACT\_REC\_END}$	End time of active signal improvement phase		355			ns
$t_{\Delta\ Bit(Bus)}$	Transmitted bit width variation	V_{CC} = 4.75V to 5.25V, TXD <= 8Mbps, $t_{\Delta\ Bit(Bus)} = t_{Bit(Bus)} - t_{Bit(TxD)}$ STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100 pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%), See Figure 7-4	–10		10	ns
		V_{CC} = 4.5V to 5.5V, TXD <= 8Mbps, $t_{\Delta\ Bit(Bus)} = t_{Bit(Bus)} - t_{Bit(TxD)}$ STB = 0V, R_L = 60Ω, C_L = 100pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%), See Figure 7-4	–10		10	ns
$t_{\Delta\ BIT(RxD)}$	Received bit width variation	V_{CC} = 4.75V to 5.25V, TXD <= 8Mbps, $t_{\Delta\ BIT(RxD)} = t_{Bit(RxD)} - t_{Bit(TxD)}$ STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%), $C_{L(RXD)}$ = 15pF, See Figure 7-4	–30		20	ns
		V_{CC} = 4.5V to 5.5V, TXD <= 8Mbps, $t_{\Delta\ BIT(RxD)} = t_{Bit(RxD)} - t_{Bit(TxD)}$ STB = 0V, R_L = 60Ω, C_L = 100pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%), $C_{L(RXD)}$ = 15 pF, See Figure 7-4	–30		20	ns
$t_{\Delta\ REC}$	Receiver timing symmetry	V_{CC} = 4.75V to 5.25V, TXD <= 8Mbps, $t_{\Delta\ REC} = t_{Bit(RxD)} - t_{Bit(Bus)}$ STB = 0V, 45Ω ≤ R_L ≤ 65Ω, C_L = 100pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%), See Figure 7-4	–20		15	ns
		V_{CC} = 4.5V to 5.5V, TXD <= 8Mbps, $t_{\Delta\ REC} = t_{Bit(RxD)} - t_{Bit(Bus)}$ STB = 0V, R_L = 60Ω, C_L = 100pF (≤ ±1%), $C_{L(RXD)}$ = 15pF (≤ ±1%), See Figure 7-4	–20		15	ns

6.10 Typical Characteristics



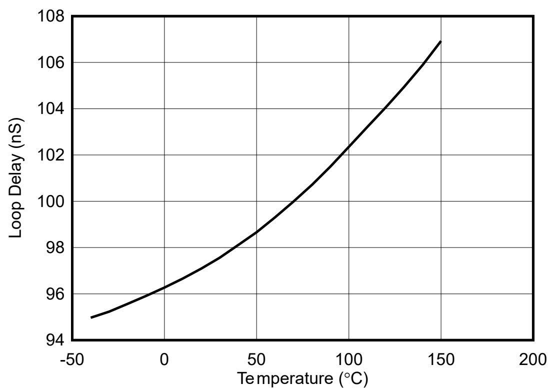
STB = GND Temp = Sweep R_L = 60Ω

Figure 6-1. $V_{OD(DOM)}$ Over temperature



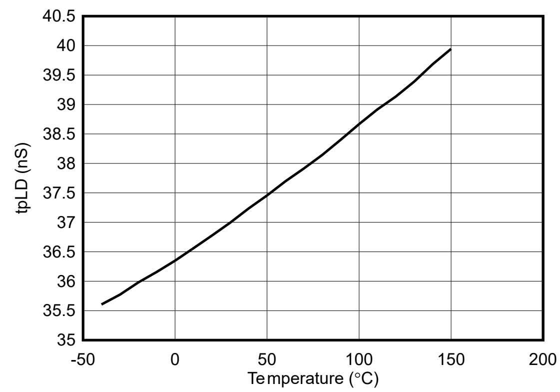
T_A = 25°C R_L = 60Ω STB = GND

Figure 6-2. $V_{OD(DOM)}$ over V_{CC}



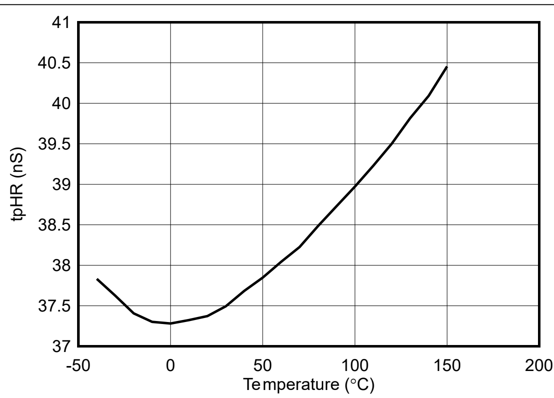
V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

Figure 6-3. Loop delay vs Temperature



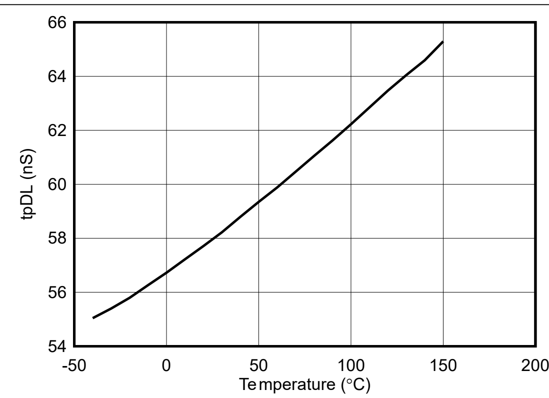
V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

Figure 6-4. Driver propagation delay - High to Low



V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

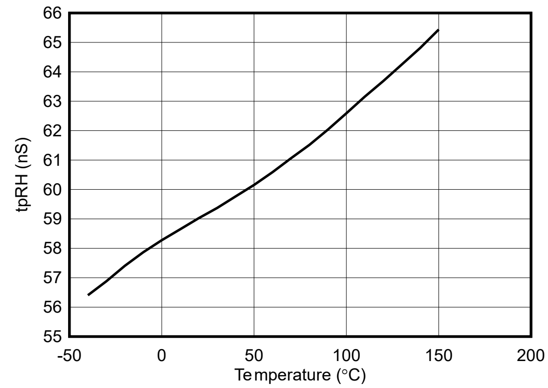
Figure 6-5. Driver propagation delay - Low to High



V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

Figure 6-6. Receiver propagation delay - Bus dominant to RXD low

6.10 Typical Characteristics (continued)



V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

Figure 6-7. Receiver propagation delay - Bus recessive to RXD high

7 Parameter Measurement Information

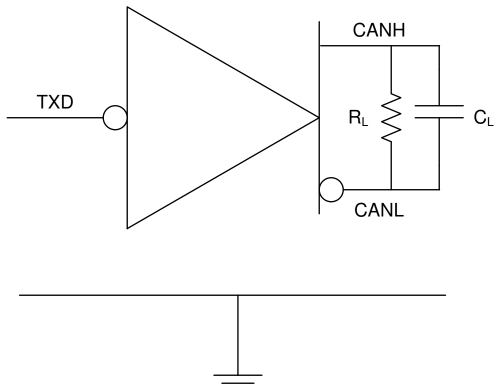


Figure 7-1. I_{CC} Test Circuit

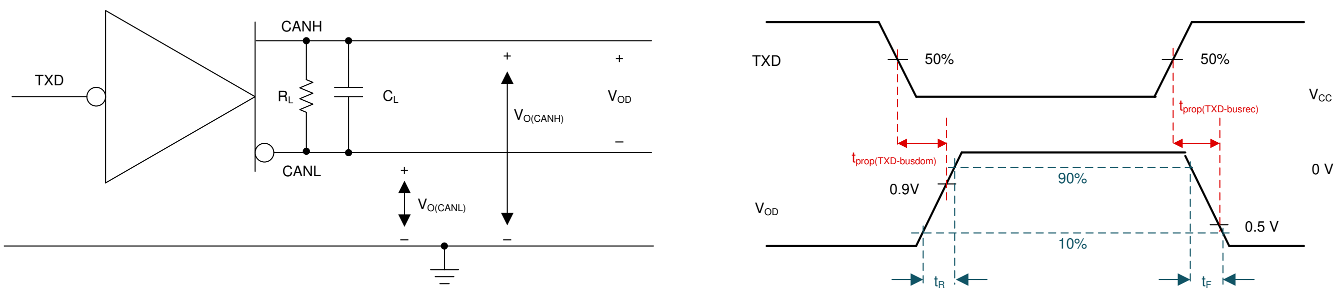


Figure 7-2. Driver Test Circuit and Measurement

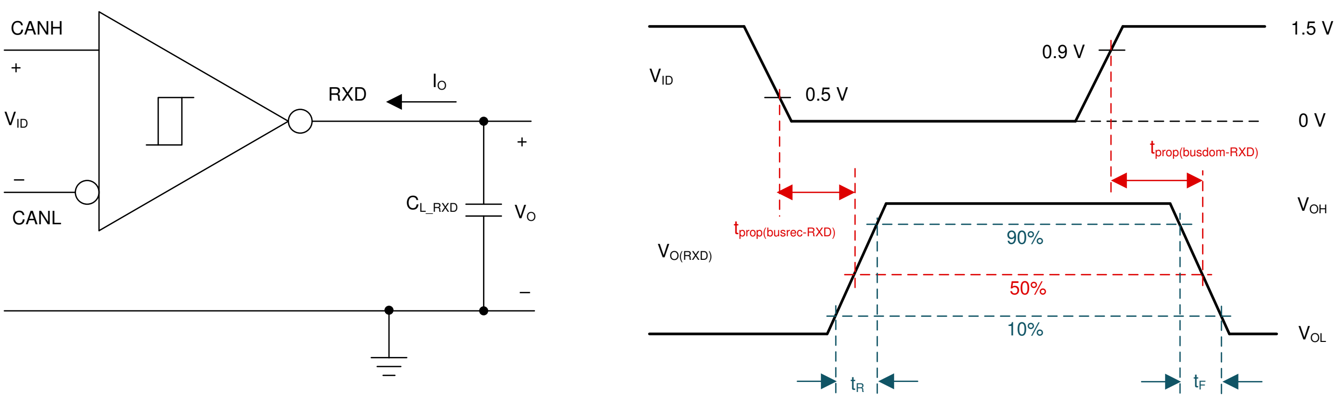
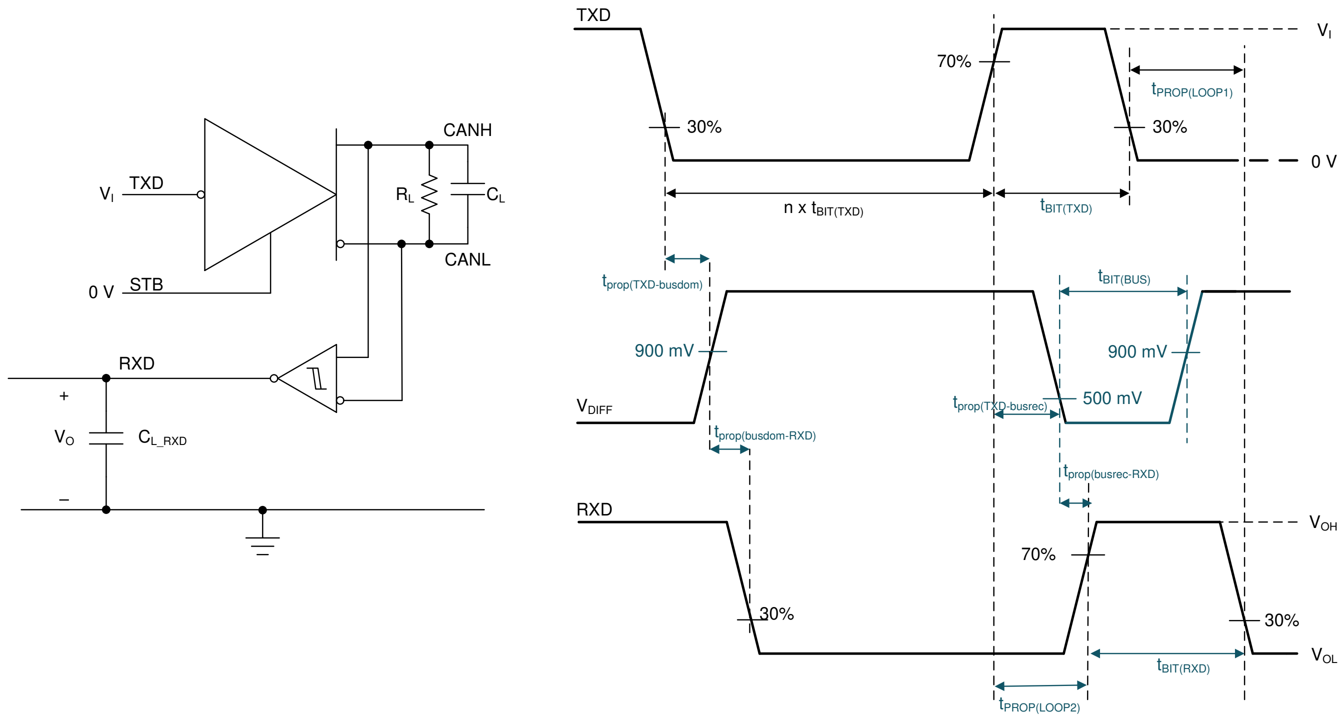


Figure 7-3. Receiver Test Circuit and Measurement



n = 1 to 5;
TXD rise/fall time < 10 ns

Figure 7-4. Transmitter and Receiver Timing Behavior Test Circuit and Measurement

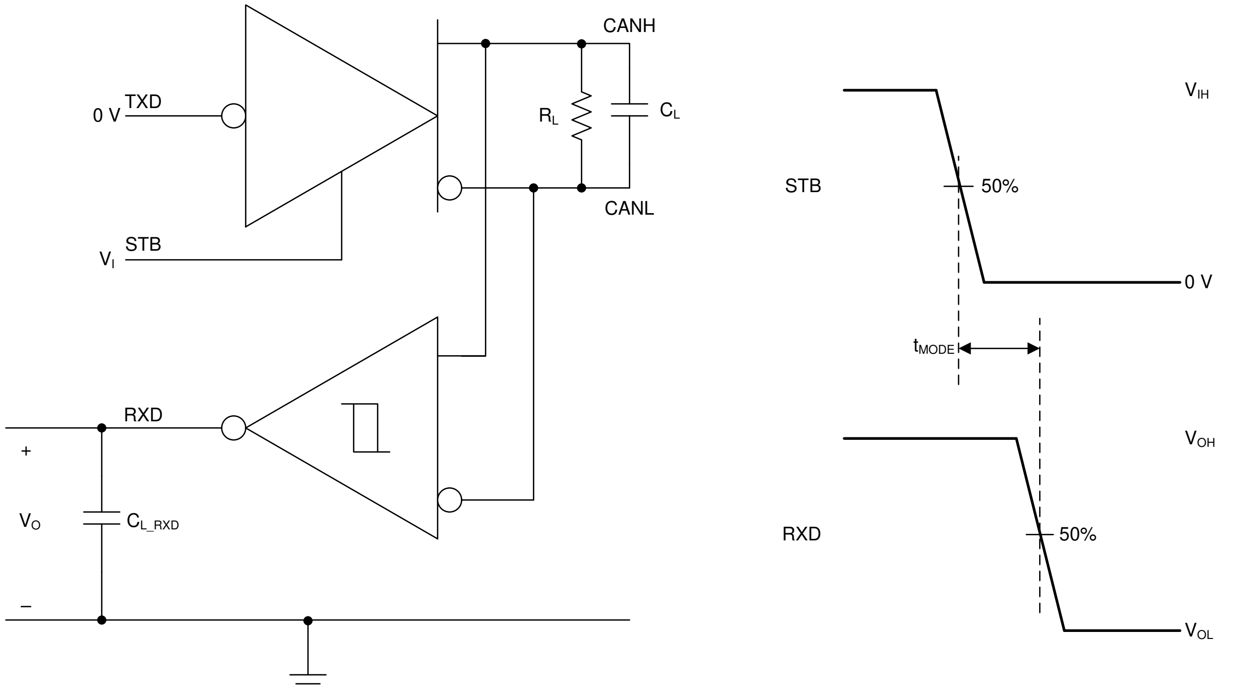


Figure 7-5. t_{MODE} Test Circuit and Measurement

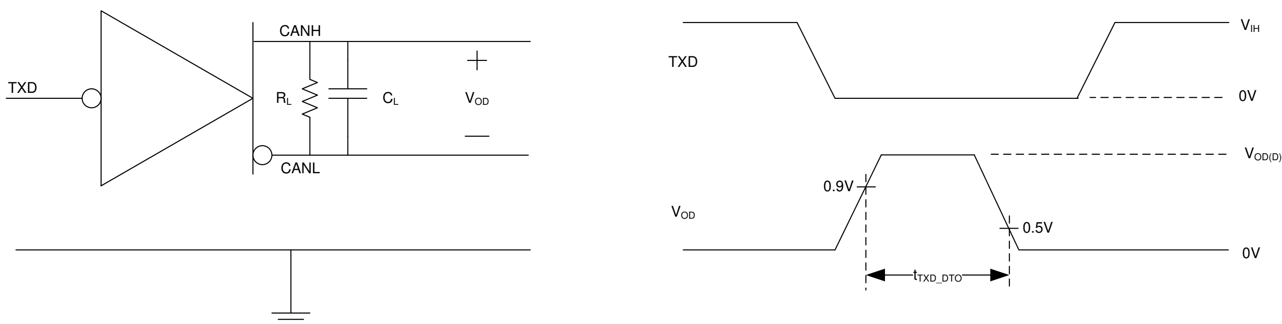


Figure 7-6. TXD Dominant Timeout Test Circuit and Measurement

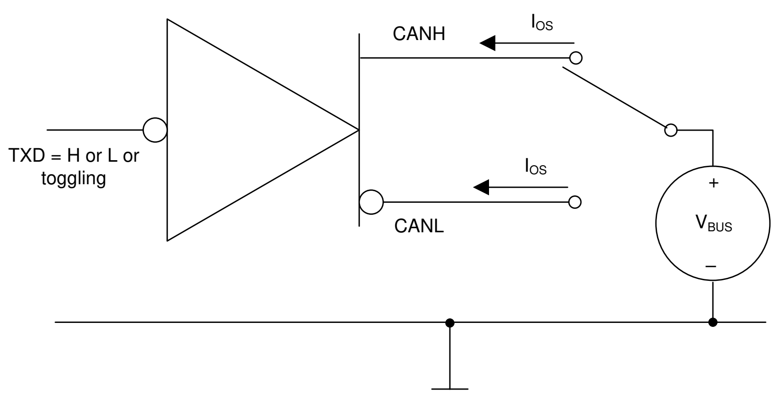


Figure 7-7. Driver Short-Circuit Current Test and Measurement

8 Detailed Description

8.1 Overview

The TCAN1476-Q1 devices meets or exceed the specifications of the Annex A Signal Improvement Capability (SIC) specification of ISO 11898-2:2024 Controller Area Network physical layer standard. The devices are data rate agnostic making them backward compatible for supporting classic CAN (CAN CC) applications while also supporting CAN FD networks up to 8Mbps. These devices have standby mode support which puts the CAN channel in ultra-low current consumption mode. Upon receiving valid wake-up pattern (WUP) on the CAN bus, the device signals to the microcontroller through the RXD pin. The MCU can then put the channel into normal mode using the STB pin.

The TCAN1476-Q1 has two separate bus-side supply rails, V_{CC1} and V_{CC2}. The TCAN1476V-Q1 has two separate supply rails, V_{CC} bus-side supply and V_{IO} logic supply for logic-level translation for interfacing directly to 1.8V, 2.5V, 3.3V, or 5V controllers.

8.1.1 Signal Improvement

Signal improvement is an additional capability added to CAN FD transceiver that enhances the maximum data rate achievable in complex star topologies by minimizing signal ringing. Signal ringing is the result of reflections caused by impedance mismatch at various points in a CAN network due to the nodes that act as stubs.

An example of a complex network is shown in Figure 8-1.

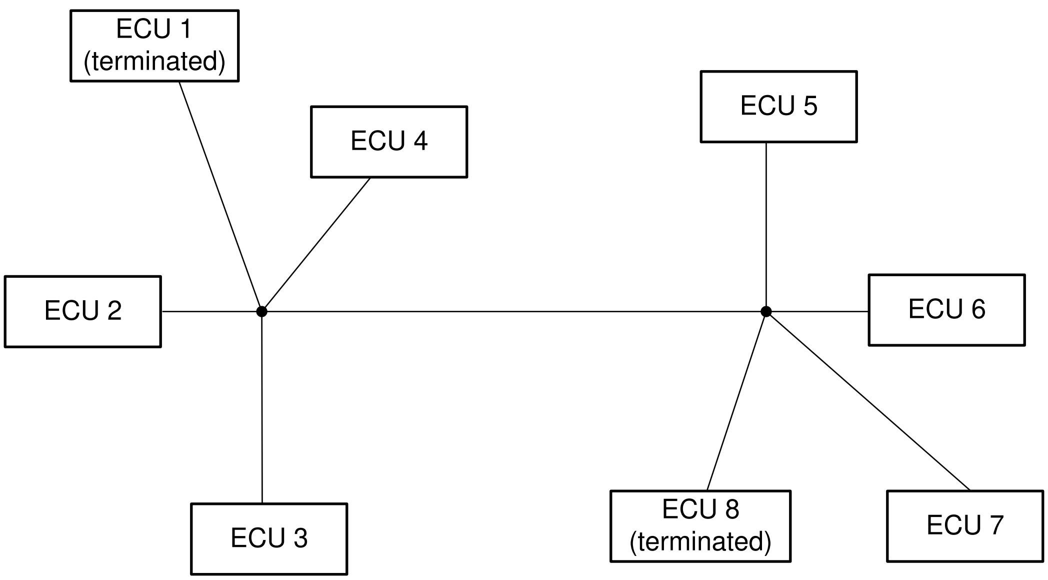


Figure 8-1. CAN Network: Star topology

Recessive-to-dominant signal edge is usually clean and driven by the transmitter. For a regular CAN FD transceiver, dominant-to-recessive edge is when the driver output impedance goes to approximately 60kΩ and signal reflected back experiences impedance mismatch which causes ringing. TCAN1476-Q1 resolves this issue by TX-based Signal improvement capability (SIC). The device continues to drive the bus recessive until $t_{SIC\_TX\_base}$, so the reflections die down and the recessive bit is clean at sampling point. In the active recessive phase, transmitter output impedance is low (approximately 100Ω). After this phase is over and device goes to passive recessive phase, driver output impedance goes to high-Z. This phenomenon is explained with Figure 8-2.

For more information on the TI signal improvement technology and the compares with similar devices in market, please refer to the white paper *How Signal Improvement Capability Unlocks the Real Potential of CAN-FD Transceivers*.

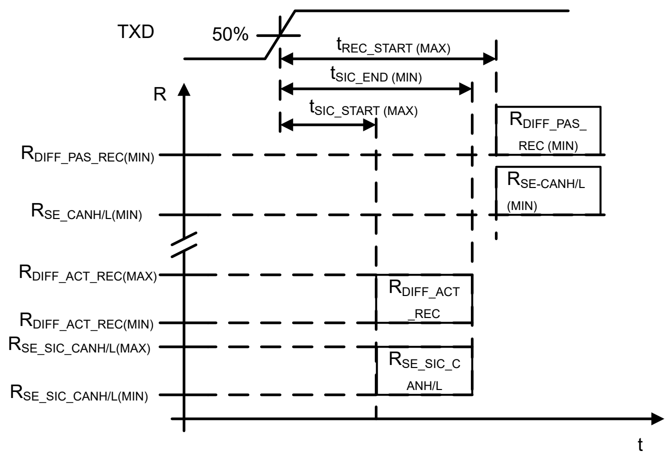


Figure 8-2. TX based SIC

8.2 Functional Block Diagrams

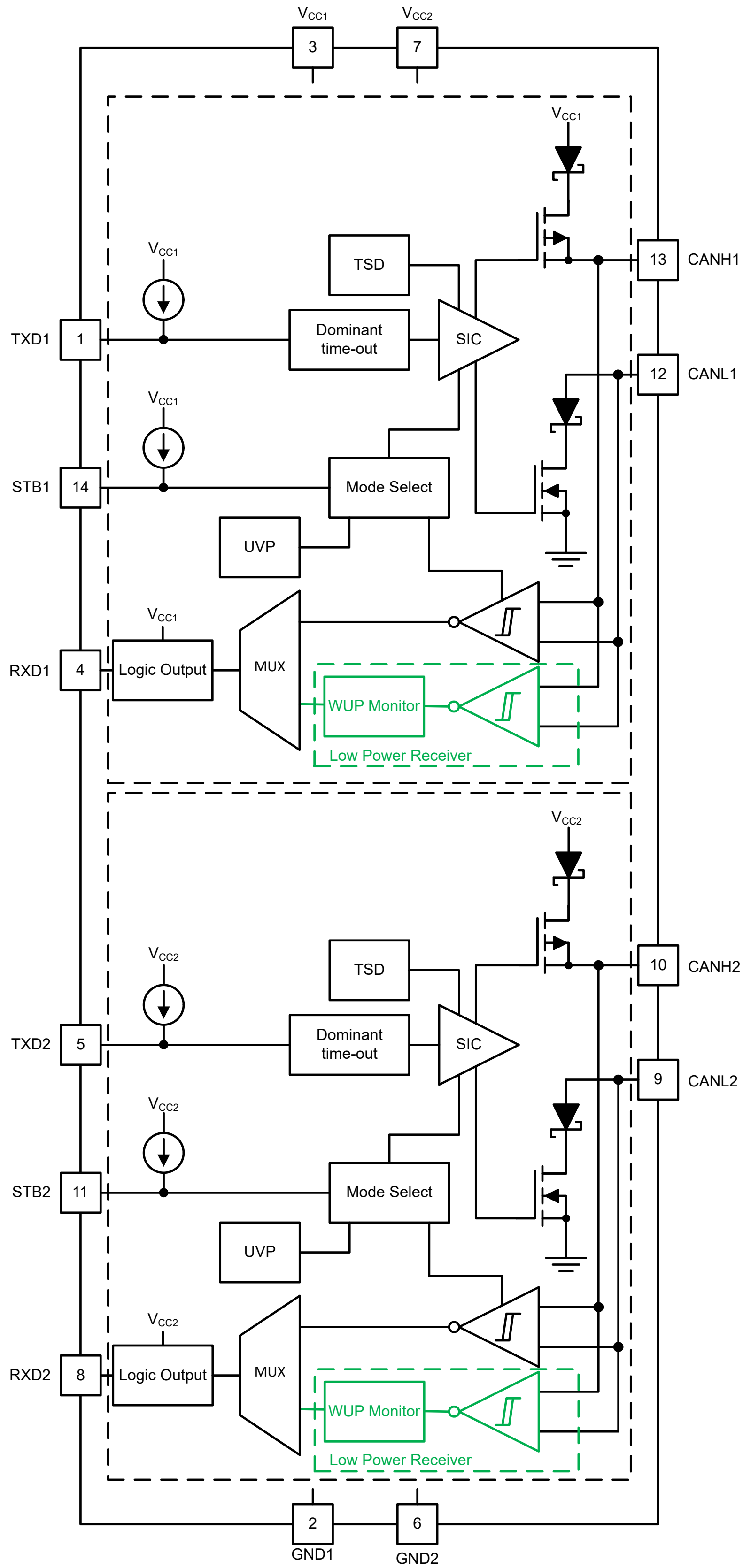


Figure 8-3. TCAN1476-Q1 Block Diagram

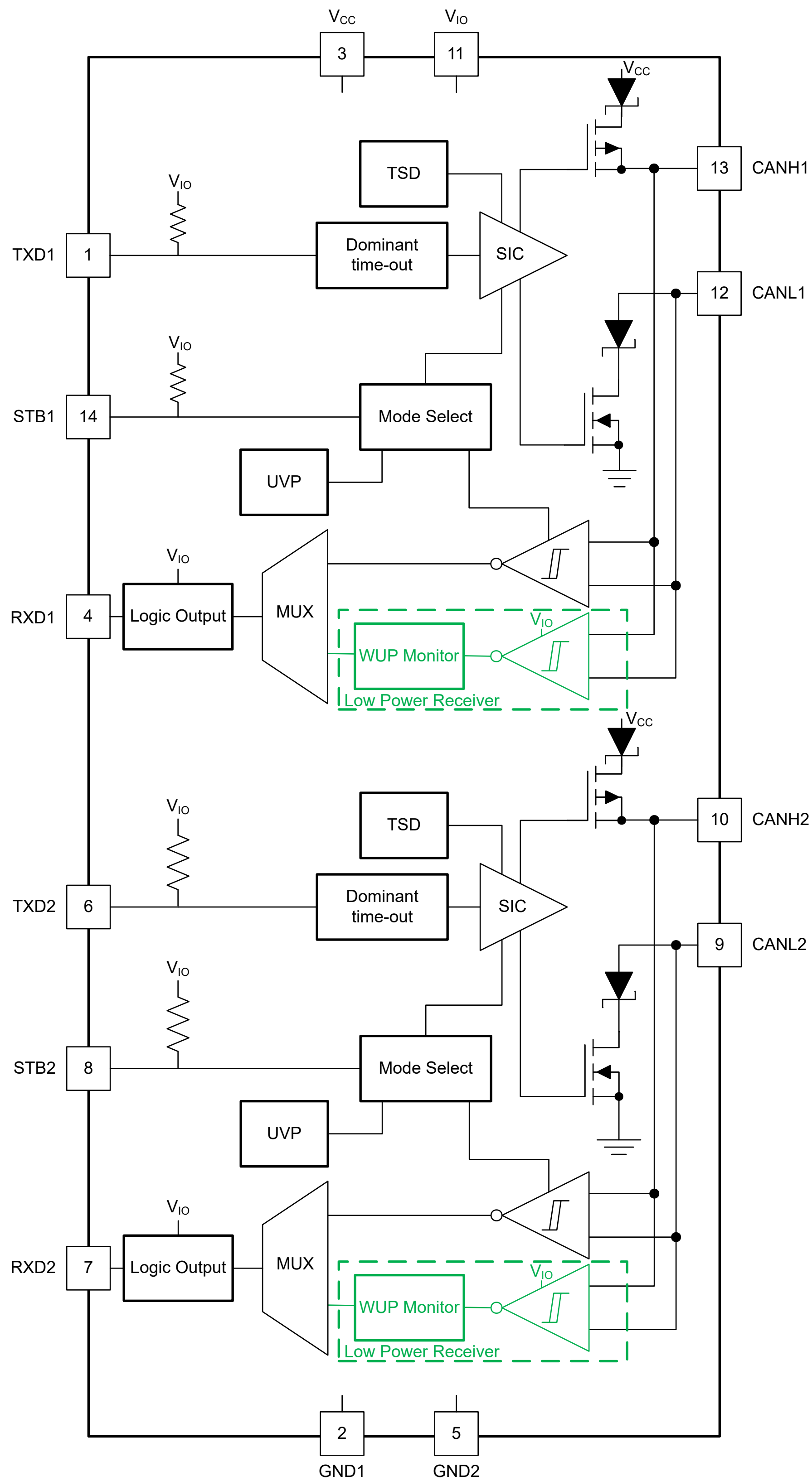


Figure 8-4. TCAN1476V-Q1 Block Diagram

8.3 Feature Description

8.3.1 Pin Description

8.3.1.1 TXD1 and TXD2

TXD1 and TXD2 are logic-level signals from CAN controllers to the transceivers. The inputs are referenced to V_{CC} for TCAN1476-Q1 or to V_{IO} for TCAN1476V-Q1.

8.3.1.2 GND1 and GND2

GND1 and GND2 are ground pins of the transceiver, both must be connected to the PCB ground.

8.3.1.3 V_{CC}

For TCAN1476-Q1, V_{CC1} and V_{CC2} provide the 5V nominal power supply input to their respective CAN transceiver. For TCAN1476V-Q1, V_{CC} provides the 5V power supply to both the CAN channels.

8.3.1.4 RXD1 and RXD2

RXD1 and RXD2 are the logic-level signals, referenced to V_{IO}, from the TCAN1476-Q1 to a CAN controller. These pins are only driven once V_{IO} is present, if applicable.

When a wake event takes place RXD is driven low.

8.3.1.5 V_{IO} (TCAN1476V-Q1 only)

The V_{IO} pin provides the digital I/O voltage to match the CAN controller voltage thus avoiding the requirement for a level shifter. The V_{IO} pin supports voltages from 1.7V to 5.5V providing the widest range of controller support.

8.3.1.6 CANH1, CANL1, CANH2, and CANL2

The CAN high and CAN low are differential bus pins of the two integrated CAN channels. The CANH and CANL pins are connected to the CAN transceiver and the low-voltage WUP CAN receiver.

8.3.1.7 STB1 and STB2 (Standby)

The STB1 and STB2 pins are input pins used for mode control of the transceiver. STB1 and STB2 can be supplied from either the system processor or from a static system voltage source. If normal mode is the only intended mode of operation, the STB pins can be tied directly to GND.

8.3.2 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See Figure 8-5 and Figure 8-6.

A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD1, TXD2, RXD1 and RXD2 pins. A recessive bus state occurs when the bus is biased to $V_{CC}/2$ via the high-resistance internal input resistors (R_{IN}) of the receiver and corresponds to a logic high on the TXD1, TXD2, RXD1 and RXD2 pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

The TCAN1476-Q1 transceiver implements a low-power standby (STB or nSTB) mode which enables a third bus state where the bus pins are weakly biased to ground via the high resistance internal resistors of the receiver. See Figure 8-5 and Figure 8-6.

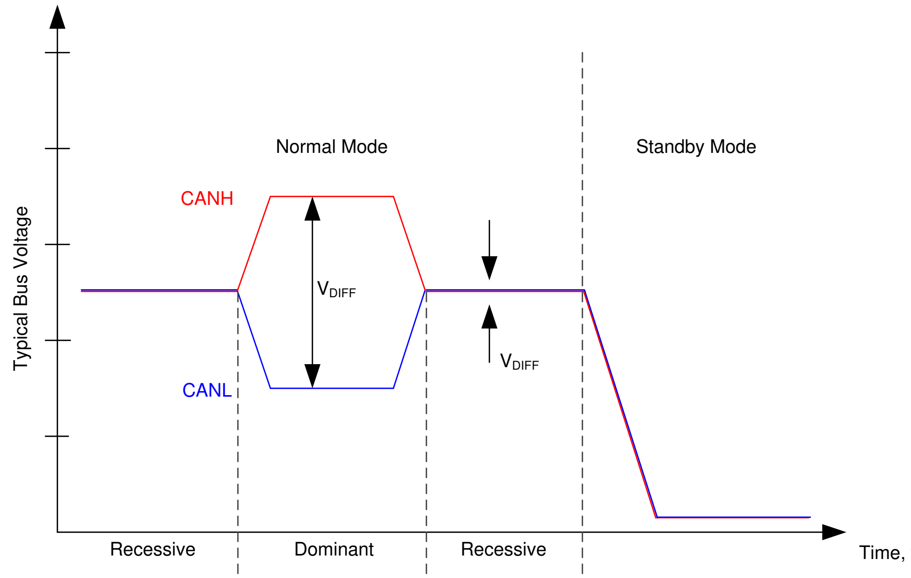
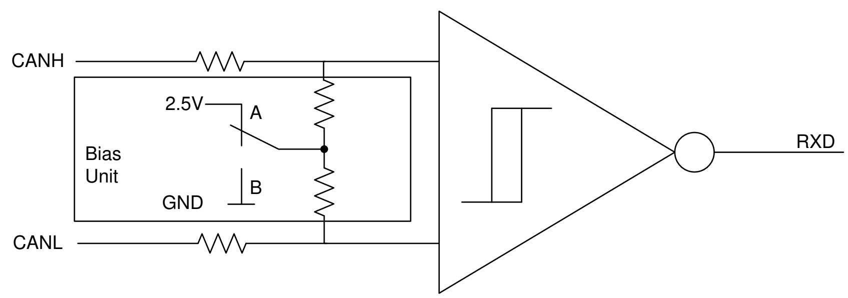


Figure 8-5. Bus States



A. Normal Mode
B. Standby Mode

Figure 8-6. Simplified Recessive Common Mode Bias Unit and Receiver

8.3.3 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit, t_{TXD_DTO}, the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin which clears the dominant time out. The receiver remains active and biased to $V_{CC}/2$. The RXD output reflects the activity on the CAN bus during the TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using Equation 1.

$$\text{Minimum Data Rate} = 11\text{ bits} / t_{TXD\_DTO} = 11\text{ bits} / 1.2\text{ ms} = 9.2\text{ kbps} \quad (1)$$

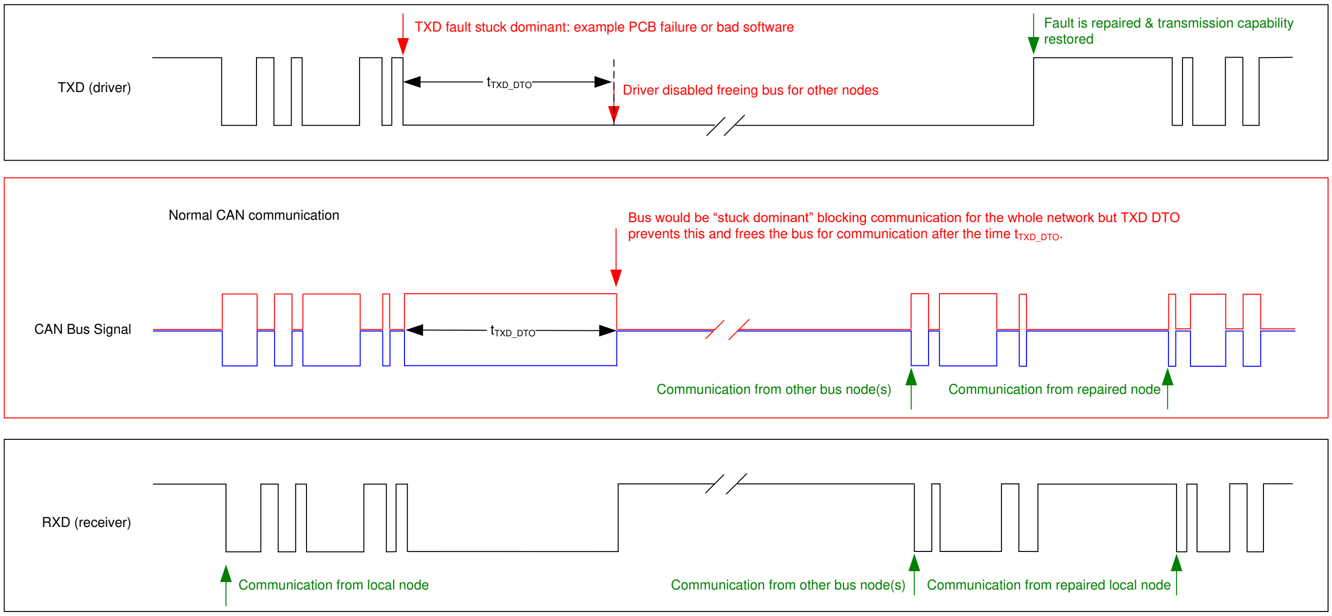


Figure 8-7. Example Timing Diagram for TXD Dominant Timeout

8.3.4 CAN Bus Short Circuit Current Limiting

The TCAN1476-Q1 has several protection features that limit the short circuit current when a CAN bus line is shorted. The features include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout which prevents permanently having the higher short-circuit current of a dominant state in case of a system fault. During CAN communication, the bus switches between the dominant and recessive states; thus, the short-circuit current may be viewed as either the current during each bus state or as a DC average current. When selecting termination resistors or a common-mode choke for the CAN design the average power rating, $I_{OS(AVG)}$, should be used. The percentage dominant is limited by the TXD DTO and the CAN protocol which has forced state changes and recessive bits due to bit stuffing, control fields, and interframe space. These provides for a minimum amount of recessive time on the bus even if the data field contains a high percentage of dominant bits.

The average short-circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short-circuit currents. The average short-circuit current may be calculated using Equation 2.

$$I_{OS(AVG)} = \%\ \text{Transmit}\ \text{x}\ [(\%\ \text{REC\_Bits}\ \text{x}\ I_{OS(SS)\_REC}) + (\%\ \text{DOM\_Bits}\ \text{x}\ I_{OS(SS)\_DOM})] + [\%\ \text{Receive}\ \text{x}\ I_{OS(SS)\_REC}] \quad (2)$$

Where:

- $I_{OS(AVG)}$ is the average short-circuit current
- % Transmit is the percentage the node is transmitting CAN messages
- % Receive is the percentage the node is receiving CAN messages
- % REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- % DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short-circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short- circuit current

The short-circuit current and the possible fault cases of the network should be considered when sizing the power supply used to generate the transceivers V_{CC} supply.

8.3.5 Thermal Shutdown (TSD)

If the junction temperature of the TCAN1476-Q1 exceeds the thermal shutdown threshold, T_{TSD}, the device turns off the CAN driver circuitry and blocks the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below T_{TSD}. The CAN bus pins are biased to $V_{CC}/2$ during a

TSD fault and the receiver to RXD path remains operational. The TCAN1476-Q1 TSD circuit includes hysteresis which prevents the CAN driver output from oscillating during a TSD fault.

8.3.6 Undervoltage Lockout

The supply pins, V_{CC} and V_{IO}, have undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

Table 8-1. Undervoltage Lockout - TCAN1476-Q1

V_{CC}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	Protected	High impedance (1)	High impedance

(1) V_{CC} = GND, see $I_{LKG(OFF)}$

Table 8-2. Undervoltage Lockout - TCAN1476V-Q1

V_{CC}	V_{IO}	DEVICE STATE	BUS	RXD PIN
> UV_{VCC}	> UV_{VIO}	Normal	Per TXD	Mirrors bus
< UV_{VCC}	> UV_{VIO}	STB = V_{IO}: Standby mode	High impedance Weak pull-down to ground	V_{IO}: Remote wake request(1)
		STB = GND: Protected mode	High impedance	Recessive
> UV_{VCC}	< UV_{VIO}	Protected	High impedance	High impedance
< UV_{VCC}	< UV_{VIO}	Protected	High impedance	High impedance

(1) See Section 8.4.3.1

Once the undervoltage condition is cleared and t_{MODE} has expired, the TCAN1476-Q1 transitions to normal mode and the host controller can send and receive CAN traffic.

8.3.7 Unpowered Device

The TCAN1476-Q1 is designed to be a passive or no load to the CAN bus if the device is unpowered. The bus pins were designed to have low leakage currents when the device is unpowered, and do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational.

The logic pins also have low leakage currents when the device is unpowered, and do not load other circuits which may remain powered.

8.3.8 Floating pins

The TCAN1476-Q1 has internal pull-ups or pull-downs on critical pins which place the device into known states if the pin floats. This internal bias should not be relied upon by design though, especially in noisy environments, but instead should be considered a failsafe protection feature.

When a CAN controller supporting open-drain outputs is used an adequate external pull-up resistor must be chosen. This specifies that the TXD output of the CAN controller maintains acceptable bit time to the input of the CAN transceiver. See Table 8-3 for details on pin bias conditions.

Table 8-3. Pin Bias

Pin	Pull-up or Pull-down	Comment
TXD1 and TXD2	Pull-up	Weakly biases TXD1 and TXD2 towards recessive to prevent bus blockage or TXD DTO triggering
STB1 and STB2	Pull-up	Weakly biases STB1 and STB2 towards low-power standby mode to prevent excessive system power

8.4 Device Functional Modes

8.4.1 Operating Modes

The TCAN1476-Q1 has two main operating modes; normal mode and standby mode. Operating mode selection is made by applying a high or low level to the STB pins on the device.

Table 8-4. Operating Modes

STB	Device Mode	Driver	Receiver	RXD Pin
High	Standby mode	Disabled	Low-power receiver with bus monitor enable	High (recessive) until valid WUP is received See section Section 8.4.3.1
Low	Normal Mode	Enabled	Enabled	Mirrors bus state

8.4.2 Normal Mode

This is the normal operating mode of the TCAN1476-Q1. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on the TXD1 and TXD2 inputs to a differential output on the CANH1, CANL1 and CANH2, CANL2 bus pins. The receiver is translating the differential signal from CANH1, CANL1 and CANH2, CANL2 to a digital output on the RXD1 and RXD2 outputs.

8.4.3 Standby Mode

This is the low-power mode of the TCAN1476-Q1. The CAN driver and main receiver are switched off and bi-directional CAN communication is not possible. The low-power receiver and bus monitor circuits are enabled to allow for RXD wake-up requests via the CAN bus. A wake-up request is output to RXD1 or RXD2 depending on the channel which receives the WUP as shown in Figure 8-8. The local CAN protocol controller should monitor RXD1 and RXD2 for transitions (high-to-low) and reactivate the device to normal mode by pulling the STB1 and STB2 pins low. The CAN bus pins are weakly pulled to GND in this mode (see Figure 8-5 and Figure 8-6).

When the TCAN1476V-Q1 is in standby mode, only the V_{IO} supply is required; therefore, the V_{CC} may be switched off for additional system level current savings.

8.4.3.1 Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

The TCAN1476-Q1 supports a remote wake-up request that is used to indicate to the host controller that the bus is active and the node should return to normal operation.

The device uses the multiple filtered dominant wake-up pattern (WUP) from the ISO 11898-2:2024 standard to qualify bus activity. Once a valid WUP has been received, the wake request is indicated to the controller by a falling edge and low period corresponding to a filtered dominant on the RXD output of the TCAN1476-Q1.

The Wake-Up Pattern (WUP) comprises four pulses: a filtered dominant, followed by a filtered recessive, then another filtered dominant, and finally another filtered recessive. After the first filtered dominant pulse, the bus monitor waits for a filtered recessive without being reset by other bus traffic and does the same until second filtered recessive pulse. Upon receiving the second filtered recessive pulse, WUP is recognized. RXD is set permanently low upon subsequent dominant pulses.

For a dominant or recessive to be considered filtered, the bus must be in that state for more than the t_{WK_FILTER} time. Due to variability in t_{WK_FILTER} the following scenarios are applicable. Bus state times less than $t_{WK\_FILTER(MIN)}$ are never detected as part of a WUP, and therefore, no wake request is generated. Bus state times between $t_{WK\_FILTER(MIN)}$ and $t_{WK\_FILTER(MAX)}$ may be detected as part of a WUP and a wake-up request may be generated. Bus state times greater than $t_{WK\_FILTER(MAX)}$ are always detected as part of a WUP, and thus a wake request is always generated. See Figure 8-8 for the timing diagram of the wake-up pattern.

The pattern and t_{WK_FILTER} time used for the WUP prevents noise and bus stuck dominant faults from causing false wake-up requests while allowing any valid message to initiate a wake-up request.

The ISO 11898-2:2024 standard has defined wakeup filter time to enable 1Mbps arbitration.

For an additional layer of robustness and to prevent false wake-ups, the device implements a wake-up timeout feature. For a remote wake-up event to successfully occur, the entire WUP must be received within the timeout value $t \le t_{WK\_TIMEOUT}$. If not, the internal logic is reset and the transceiver remains in the current state without waking up. The full pattern must then be transmitted again, conforming to the constraints mentioned in this section. See Figure 8-8 for the timing diagram of the wake-up pattern with wake timeout feature.

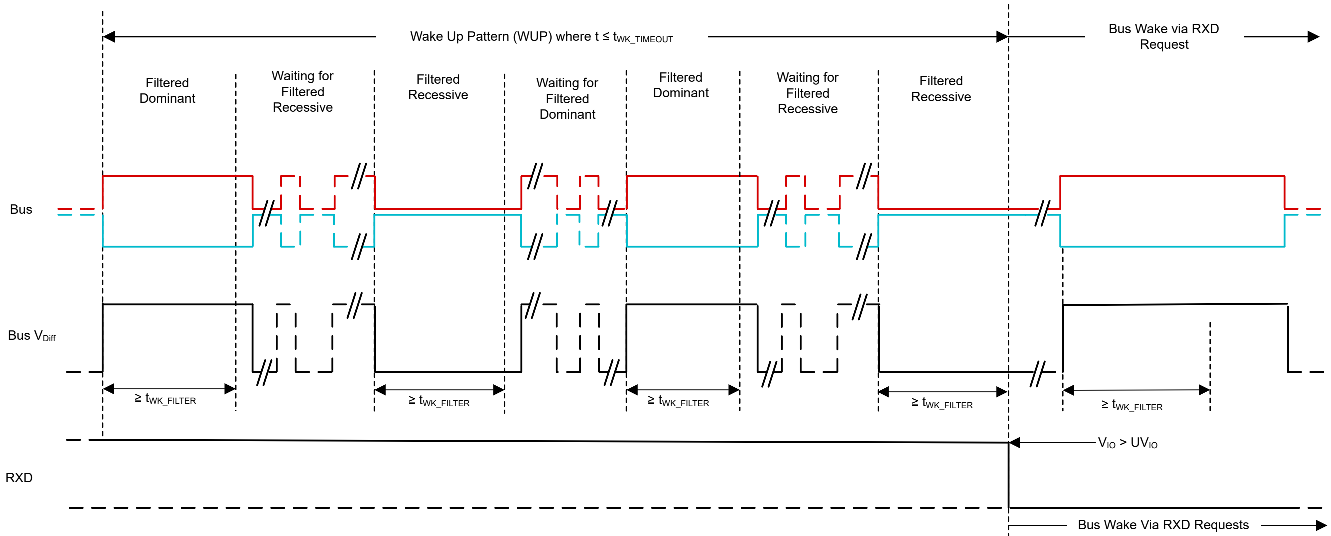


Figure 8-8. Wake-Up Pattern (WUP) with $t_{WK\_TIMEOUT}$

8.4.4 Driver and Receiver Function

Table 8-5. Driver Function Table

Device Mode	TXD Input	Bus Outputs		Driven Bus State[(2)]
		CANH	CANL	
Normal	Low	High	Low	Dominant
	High or open	High impedance	High impedance	Biased recessive
Standby	X[(1)]	High impedance	High impedance	Biased to ground

(1) X = irrelevant
(2) For bus state and bias see Figure 8-5 and Figure 8-6

Table 8-6. Receiver Function Table Normal and Standby Mode

Device Mode	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus State	RXD Pin
Normal	$V_{ID} \ge 0.9V$	Dominant	Low
	$0.5\ V < V_{ID} < 0.9V$	Undefined	Undefined
	$V_{ID} \le 0.5V$	Recessive	High
Standby	$V_{ID} \ge 1.15V$	Dominant	High Low if a remote wake event occurred, See Figure 8-8
	$0.4V < V_{ID} < 1.15V$	Undefined	
	$V_{ID} \le 0.4V$	Recessive	
Any	Open ($V_{ID} \approx 0V$)	Open	High

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Figure 9-2 shows a typical configuration for 5V system using the TCAN1476-Q1. The bus termination is shown for illustrative purposes.

9.2 Typical Application

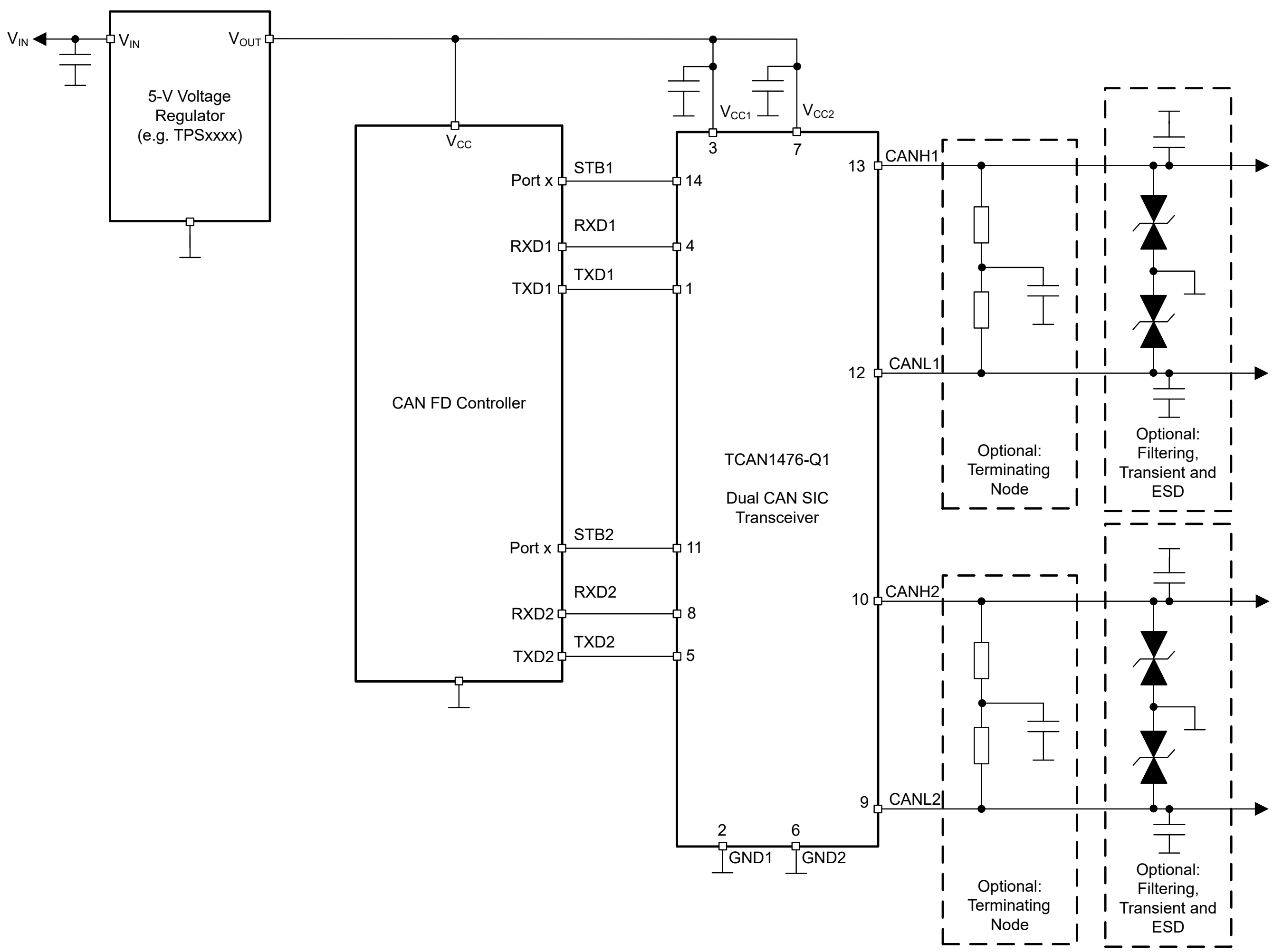


Figure 9-1. TCAN1476-Q1 Application Using 5V V_{CC}

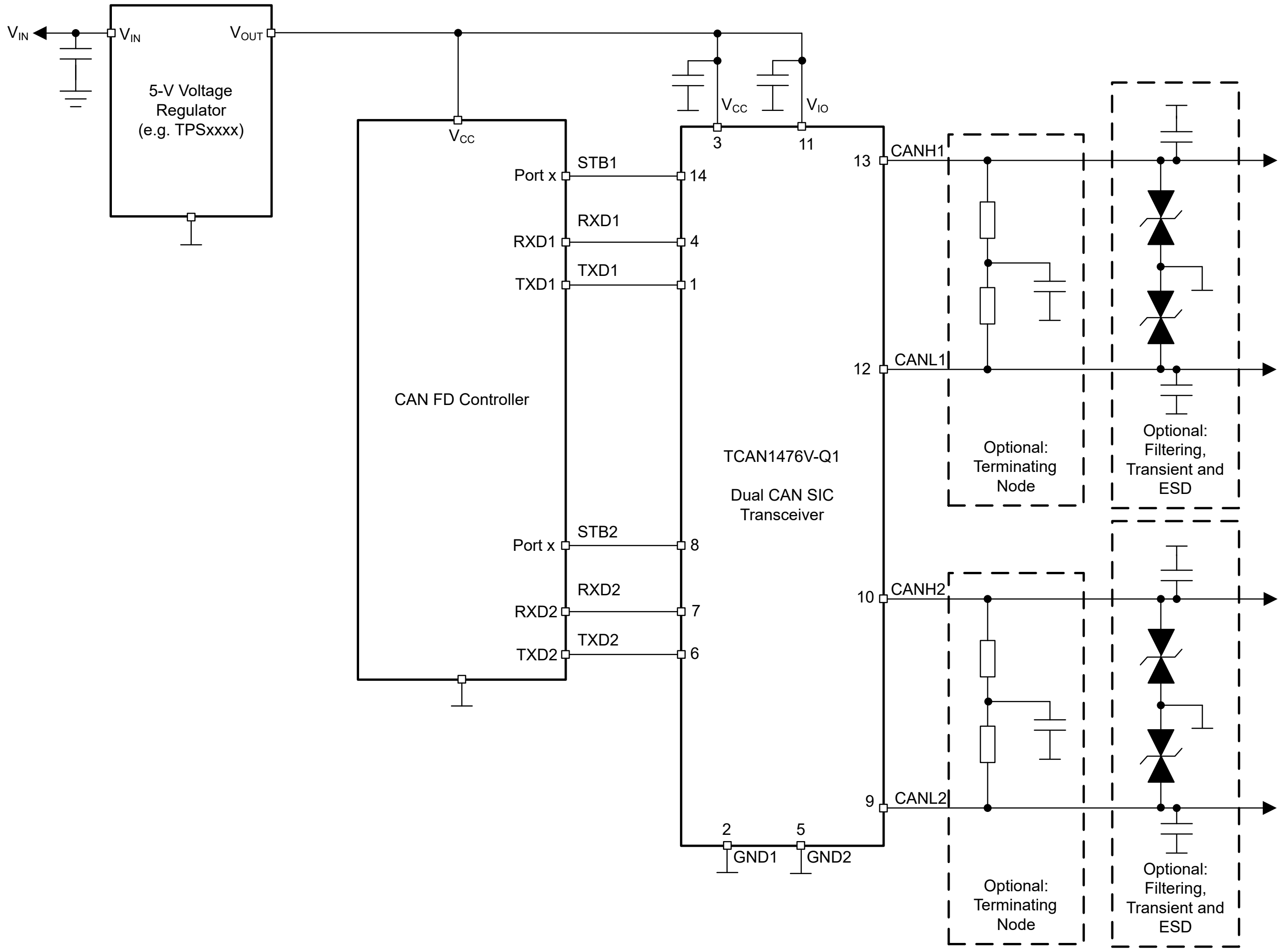


Figure 9-2. TCAN1476V-Q1 Application Using 5V I/O Connections

9.2.1 Design Requirements

9.2.1.1 CAN Termination

Termination may be a single 120Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired, then split termination may be used, see Figure 9-3. Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.

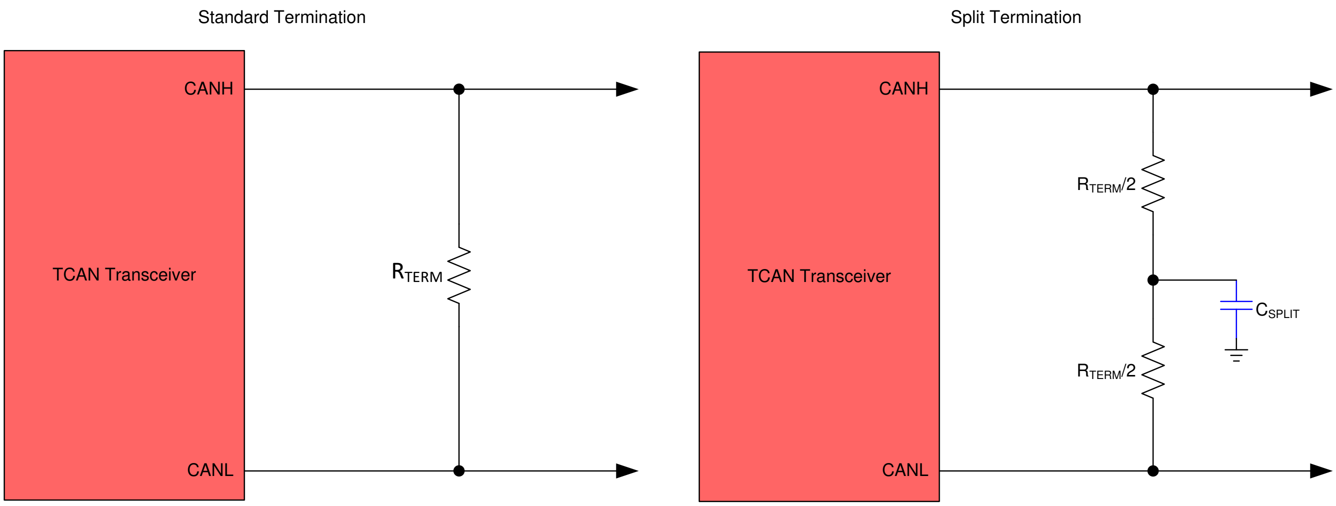


Figure 9-3. CAN Bus Termination Concepts

9.2.2 Detailed Design Procedures

9.2.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN1476-Q1. Additionally, since TCAN1476-Q1 has SIC, in a given network size, higher data rate can be achieved because signal ringing is attenuated.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2024 specification, the driver differential output is specified with a bus load that can range from 45Ω to 65Ω where the differential output must be greater than 1.5V. The TCAN1476-Q1 family is specified to meet the 1.5V requirement down to 45Ω bus load. The differential input resistance of the TCAN1476-Q1 is a minimum of 40kΩ. If 100 TCAN1476-Q1 transceivers are in parallel on a bus, this is equivalent to a 400Ω differential load in parallel with the nominal 60Ω bus termination which gives a total bus load of approximately 52Ω. Therefore, the TCAN1476-Q1 family theoretically supports over 100 transceivers on a single bus segment. However, for a CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility, the CAN network system, a good network design is required for robust network operation.

Please refer to the application report SLLA270: Controller Area Network Physical layer requirements. This document discusses in detail all system design physical layer parameters.

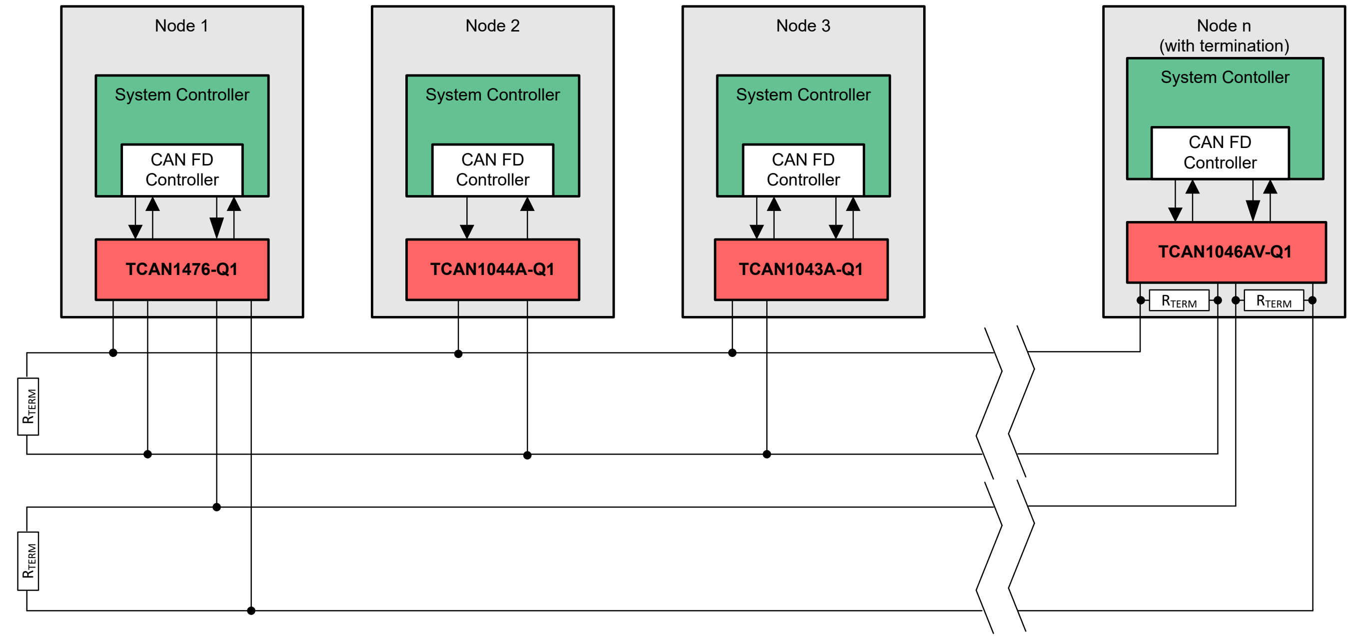
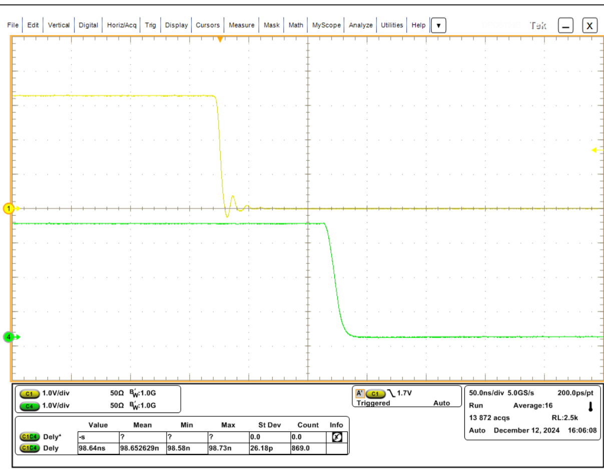


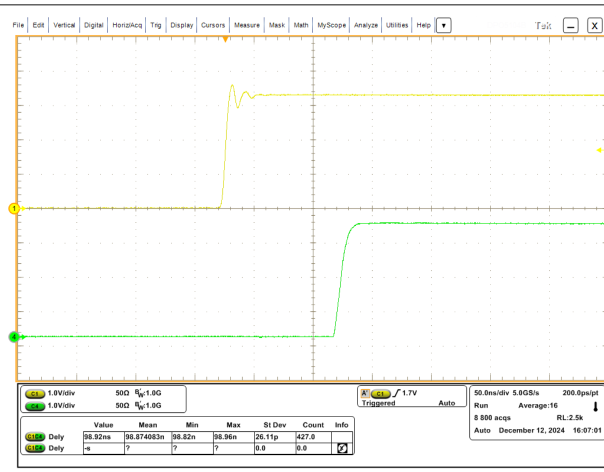
Figure 9-4. Typical CAN Bus

9.2.3 Application Curves



V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

Figure 9-5. $t_{PROP(LOOP1)}$



V_{CC} = 5V V_{IO} = 3.3V R_L = 60Ω

Figure 9-6. $t_{PROP(LOOP2)}$

9.3 System Examples

The CAN transceiver is typically used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. A 1.8V, 2.5V, or 3.3V application is shown in Figure 9-7. The bus termination is shown for illustrative purposes.

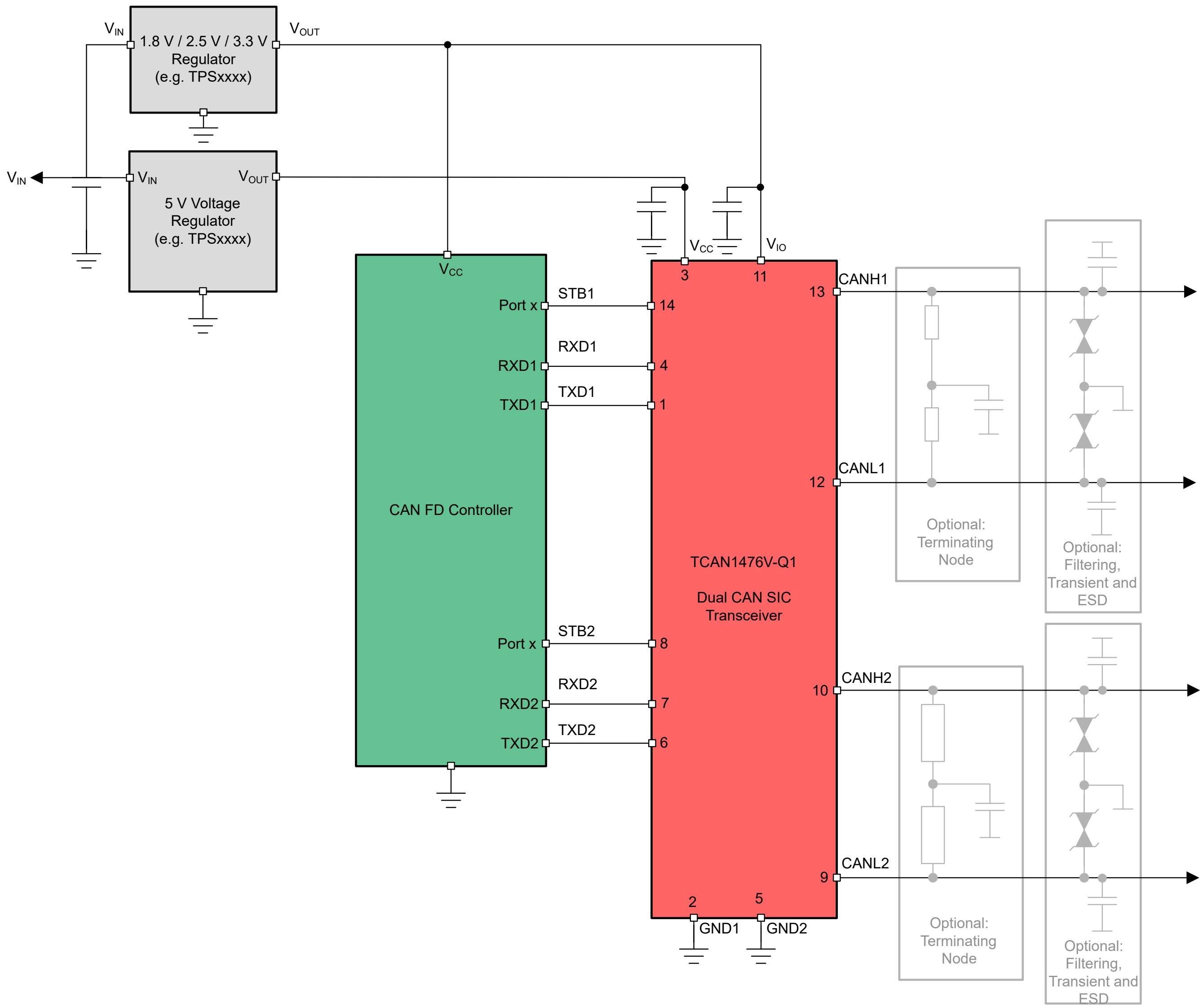


Figure 9-7. TCAN1476V-Q1 Application Using 1.8V, 2.5V, 3.3V I/O Connections

9.4 Power Supply Recommendations

The TCAN1476-Q1 family is designed to operate with a main V_{CC} input voltage supply range between 4.5V and 5.5V. The TCAN1476V-Q1 has an I/O level shifting supply input, V_{IO}, designed for a range between 1.8V and 5.5V. Both supply inputs must be well regulated. A decoupling capacitor, typically 100nF, should be placed near the CAN transceiver main V_{CC} and V_{IO} supply pins in addition to bypass capacitors.

9.5 Layout

Robust and reliable CAN node design may require special layout techniques depending on the application and automotive design requirements. Since transient disturbances have high frequency content and a wide bandwidth, high-frequency layout techniques should be applied during PCB design.

9.5.1 Layout Guidelines

- Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD, and noise from propagating onto the board. This layout example shows optional transient voltage suppression (TVS) diodes, D1 and D2, which may be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows optional bus filter capacitors C6, C8, C9 and C11.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Decoupling capacitors should be placed as close as possible to the supply pins V_{CC} and V_{IO} of transceiver.
- Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

Note

High frequency current follows the path of least impedance and not the path of least resistance.

- This layout example shows how split termination could be implemented on the CAN node. The termination is split into two resistors, R8 and R9 for channel 1, R10 and R11 for channel 2 with the center or split tap of the termination connected to ground via capacitor C7 or C10. Split termination provides common-mode filtering for the bus. See CAN Termination, CAN Bus Short Circuit Current Limiting, and Equation 2 for information on termination concepts and power ratings needed for the termination resistor(s).

9.5.2 Layout Example

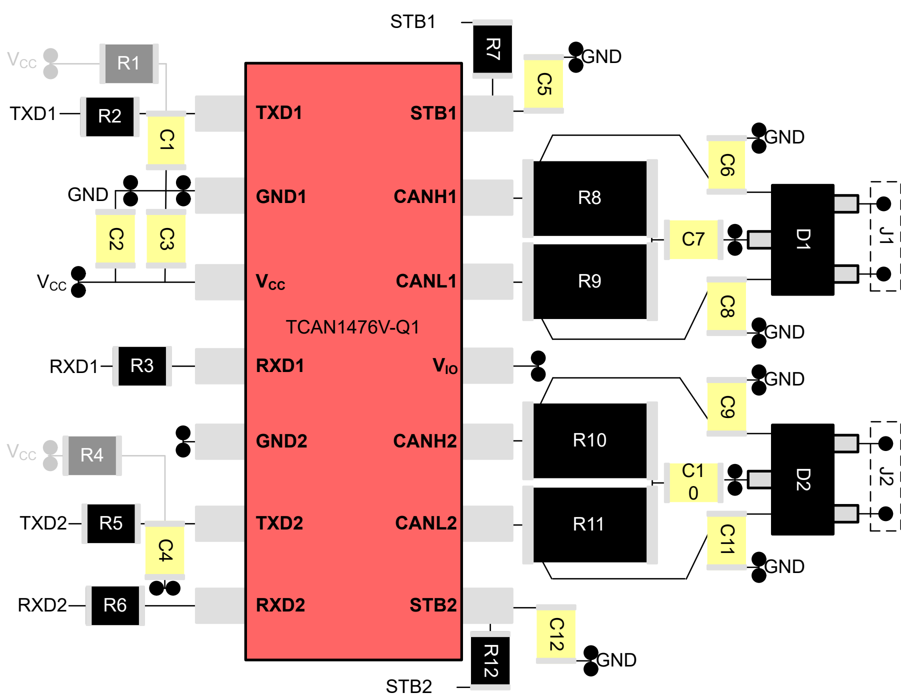


Figure 9-8. Layout Example

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2025) to Revision A (September 2025) — **Page**

- Changed the document from Advanced Information to *Production* data..1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TCAN1476DMTRQ1	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	TCAN 1476
TCAN1476VDMTRQ1	Active	Production	VSON (DMT) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	TCAN 1476V

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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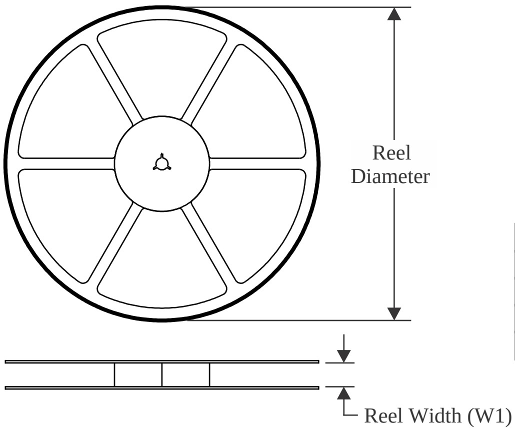
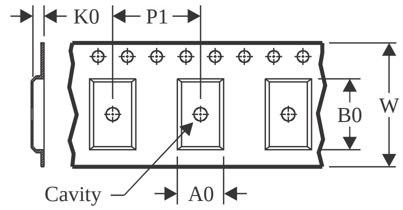
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

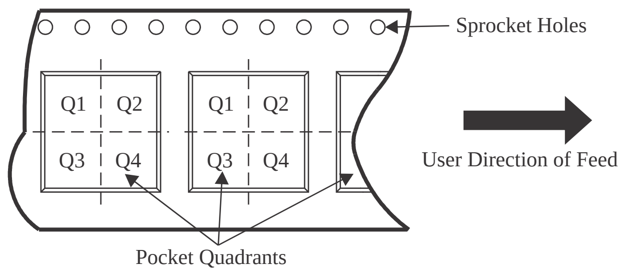


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

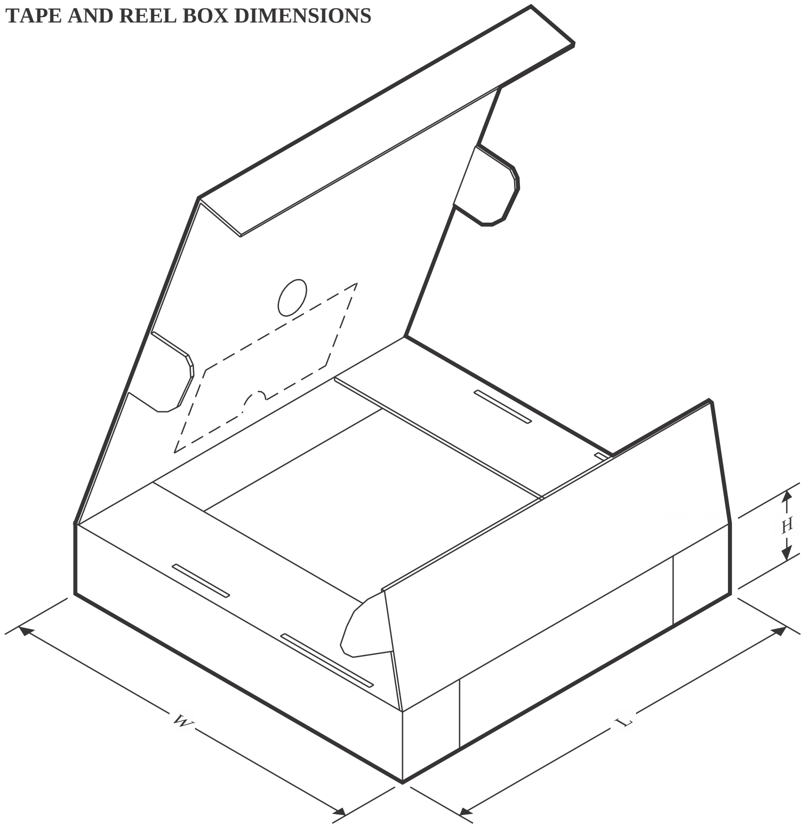
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCAN1476DMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1
TCAN1476VDMTRQ1	VSON	DMT	14	3000	330.0	12.4	3.3	4.8	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCAN1476DMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0
TCAN1476VDMTRQ1	VSON	DMT	14	3000	367.0	367.0	35.0

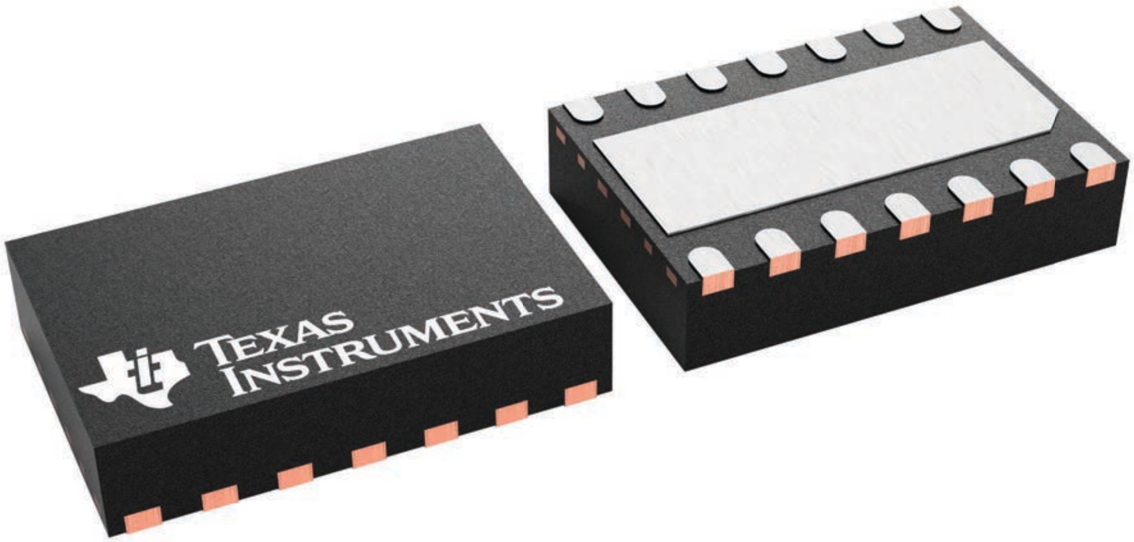
DMT 14

VSON - 0.9 mm max height

3 x 4.5, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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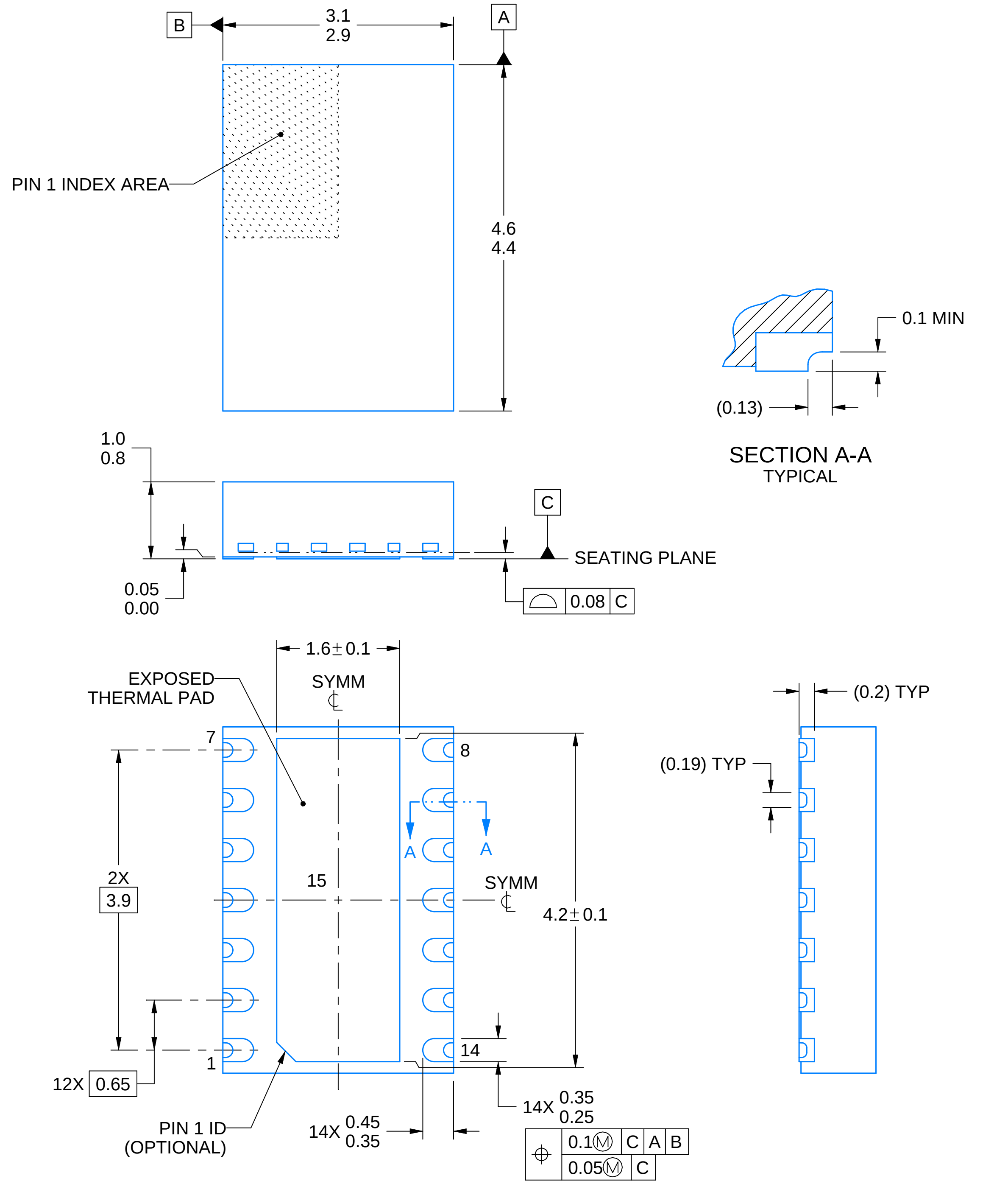

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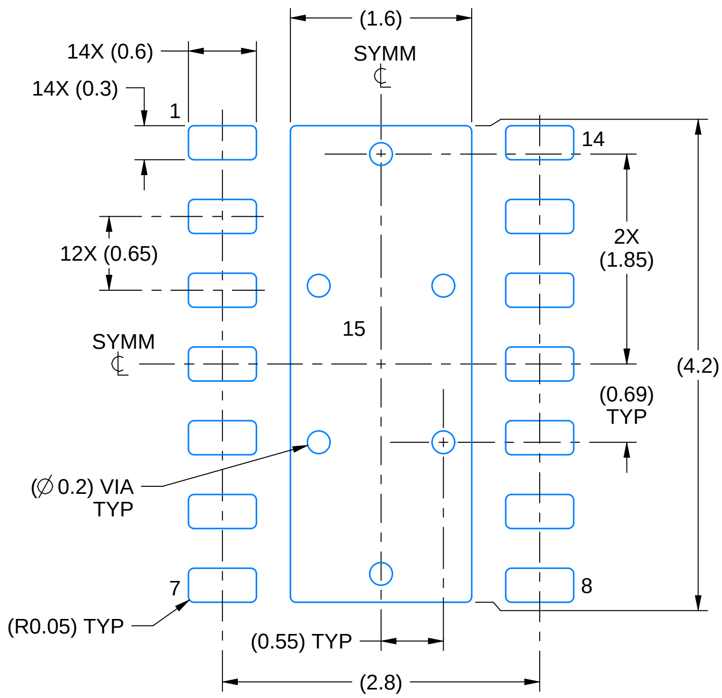
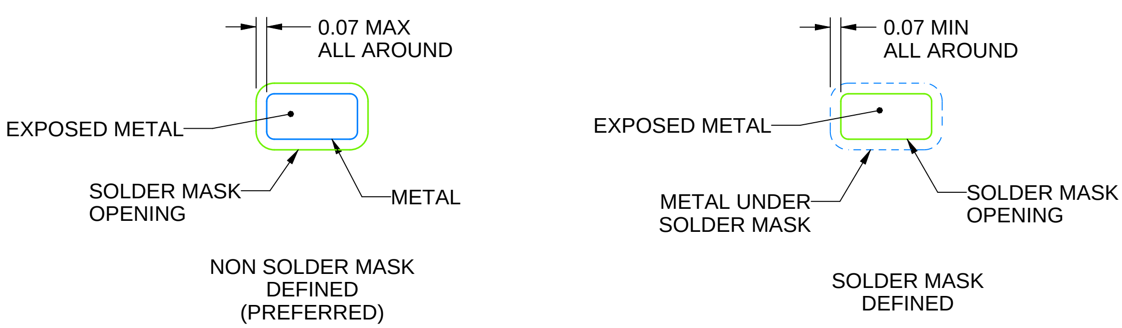
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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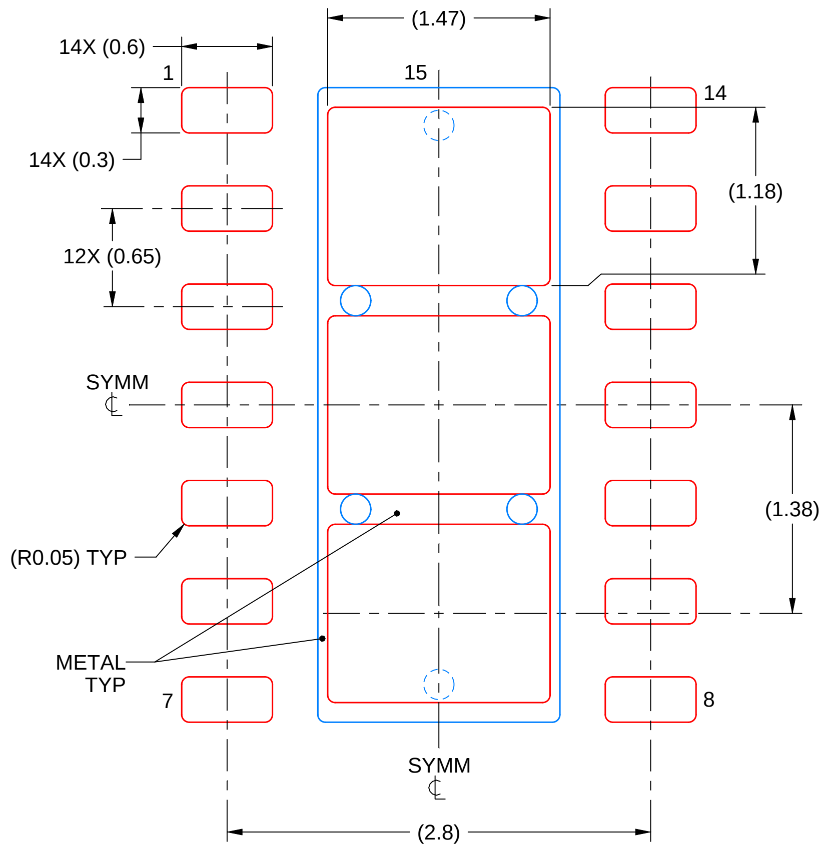
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 15
77.4% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.