# TCAN340x-Q1 3.3-V Automotive CAN FD Transceivers with Standby Mode

ADVANCE INFORMATION

## 1 Features

- AEC-Q100 (Grade 1) Qualified for automotive applications
- 3.3 V Single supply operation
  - Eliminates the 5 V regulator saving BOM cost and reducing PCB space
- Compatible with the requirements of ISO 11898-2:2016 physical layer standard
- Support of classical CAN and optimized CAN FD performance at 2, 5, and 8 Mbps
  - Short and symmetrical propagation delays for enhanced timing margin
- TCAN3403-Q1: I/O voltage range supports: 1.7 V to 3.6 V
- Receiver common mode input voltage: ±12 V
- Protection features:
  - Undervoltage protection
  - TXD-dominant time-out (DTO)
  - Thermal-shutdown protection (TSD)
- Operating modes:
  - Normal mode
  - Low power standby mode supporting remote wake-up request
  - Ultra-low power shutdown mode: TCAN3404-Q1 only
- Optimized behavior when unpowered
  - Bus and logic pins are high impedance (no load to operating bus or application)
  - Hot-plug capable: power up or down glitch-free operation on bus and RXD output
- 8-Pin SOIC, small footprint SOT-23 and lead less VSON-8 package with wettable flanks for automated optical inspection (AOI)

## 2 Applications

- Automotive and transportation
  - Body control modules
  - Automotive gateway
  - Advanced driver assistance system (ADAS)
  - Infotainment

## 3 Description

The TCAN3403-Q1 and TCAN3404-Q1 are 3.3 V controller area network (CAN) FD transceivers that are compatible with the physical layer requirements of the ISO 11898-2:2016 high-speed CAN specification.

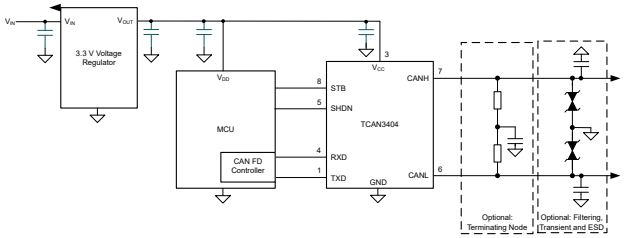
The transceivers have certified electromagnetic compatibility (EMC) operation for use with classical CAN and CAN FD networks up to 5 megabits per second (Mbps). Up to 8 Mbps operation in simpler networks is possible with these devices. The TCAN3403-Q1 includes an internal logic level translation through the $V_{IO}$ pin, allowing the direct interface of the transceiver I/Os to 1.8-V, 2.5-V, or 3.3-V logic levels. The TCAN3404-Q1 has shutdown feature where all blocks are powered off and device enters ultra-low power consumption mode. The transceivers support a low-power standby mode, and a wake over CAN which is compliant to the ISO 11898-2:2016 defined wake-up pattern (WUP).

The transceivers include thermal-shutdown (TSD), TXD-dominant time-out (DTO) and supply undervoltage detection. The devices have defined fail-safe behavior in supply undervoltage or floating pin scenarios. These devices are available in industry-standard SOIC-8, the VSON-8, and a space-saving small footprint SOT-23 packages.

**Package Information**

| PART NUMBER | PACKAGE(1) | BODY SIZE (NOM) |
|---|---|---|
| TCAN3403-Q1<br>TCAN3404-Q1 | SOIC (D) | 4.90 mm x 3.91 mm |
| | VSON (DRB) | 3.00 mm x 3.00 mm |
| | SOT-23 (DDF) | 2.90 mm x 1.60 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.




**Simplified Schematic**

ADVANCE INFORMATION

# Table of Contents



## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| December 2022 | * | Initial Release |

## 5 Device Comparison

| Part Number | Pin 5 | Pin 8 |
|---|---|---|
| TCAN3404-Q1 | Ultra-low power shutdown mode | Low Power Standby Mode with Remote Wake |
| TCAN3403-Q1 | Low voltage I/O support | |

## 6 Pin Configuration and Functions

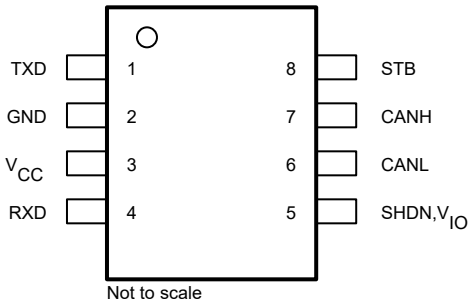



**Figure 6-1. DDF Package, 8-Pin SOT-23 (Top View)**

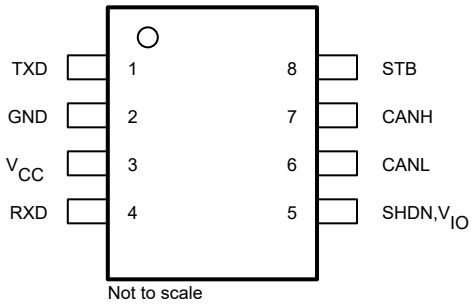



**Figure 6-2. D Package, 8-Pin SOIC (Top View)**

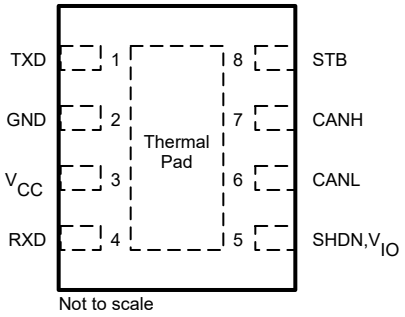



**Figure 6-3. DRB Package, 8-Pin VSON (Top View)**

**Table 6-1. Pin Functions**

| PINS | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| TXD | 1 | Digital Input | CAN transmit data input; integrated pull-up |
| GND | 2 | G | Ground connection |
| $V_{CC}$ | 3 | Supply | 3.3 V supply voltage |
| RXD | 4 | Digital Output | CAN receive data output, tri-stated when device powered off |
| SHDN | 5 | Digital Input | Device in ultra-low power shutdown mode if pin is high; integrated pull-down (TCAN3404-Q1 only) |
| $V_{IO}$ | | Supply | I/O supply voltage (TCAN3403-Q1 only) |
| CANL | 6 | Bus I/O | Low-level CAN bus input/output line |
| CANH | 7 | Bus I/O | High-level CAN bus input/output line |
| STB | 8 | Digital Input | Standby input for mode control; integrated pull-up |
| Thermal Pad (VSON only) | | — | Connect the thermal pad to any internal PCB ground plane using multiple vias for optimal thermal performance. |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground.

ADVANCE INFORMATION

# 7 Device and Documentation Support

## 7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 7.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 7.3 Trademarks

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## 7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 7.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

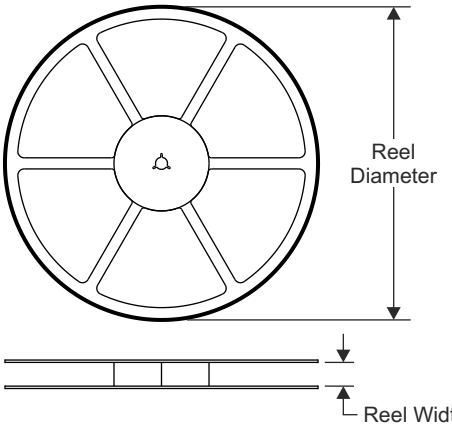
# 8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

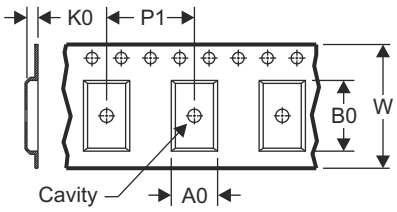
ADVANCE INFORMATION

## 8.1 Tape and Reel Information

**REEL DIMENSIONS**

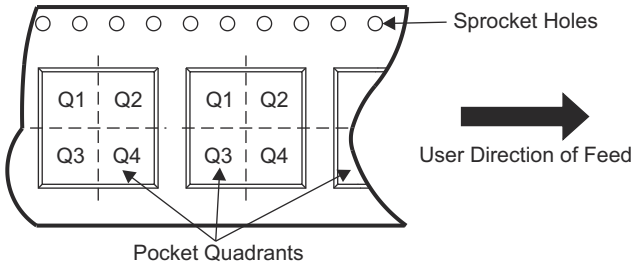



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

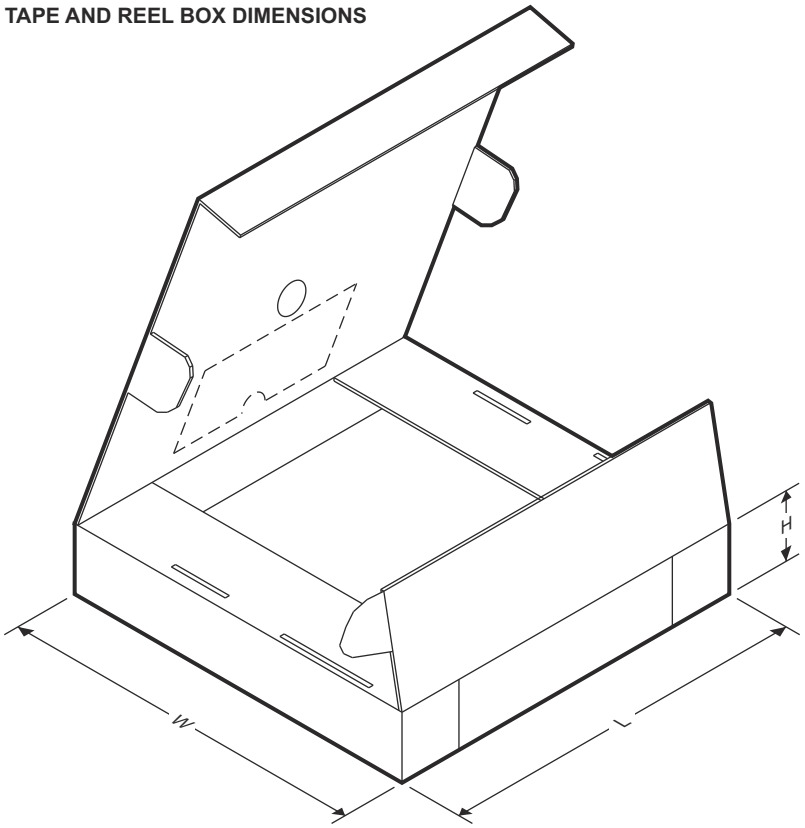



| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PTCAN3403DDFRQ1 | SOT-23-THN | DDF | 8 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| PTCAN3403DRBRQ1 | VSON | DRB | 8 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q1 |
| PTCAN3403DRBRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

ADVANCE INFORMATION

ADVANCE INFORMATION

**TAPE AND REEL BOX DIMENSIONS**



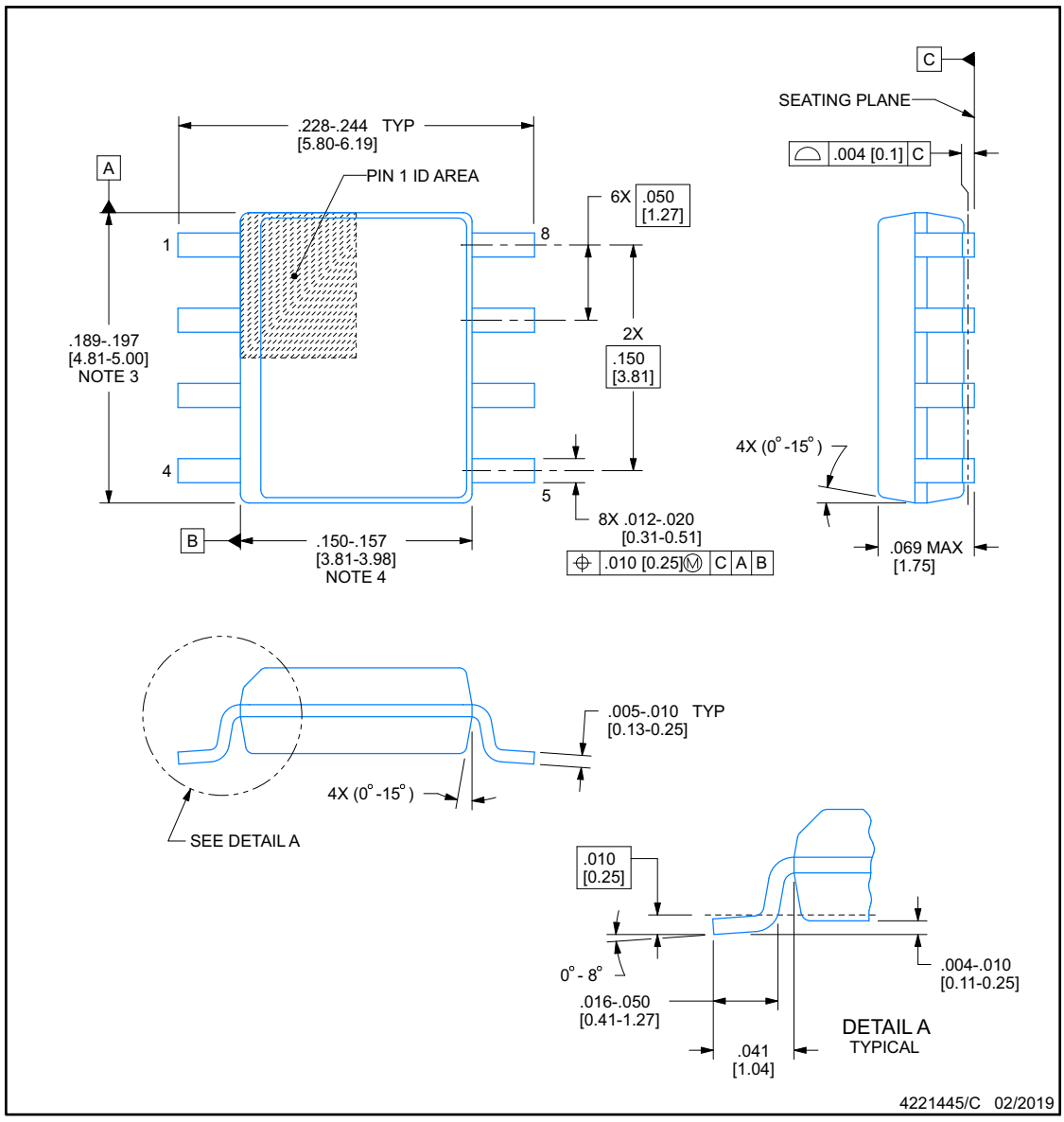

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| PTCAN3403DDFRQ1 | SOT-23-THN | DDF | 8 | 3000 | 210.0 | 185.0 | 35.0 |
| PTCAN3403DRBRQ1 | VSON | DRB | 8 | 3000 | 367.0 | 367.0 | 35.0 |
| PTCAN3403DRBRQ1 | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |

## 8.2 Mechanical Data

**PACKAGE OUTLINE**

**D0008B** — **SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT




NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

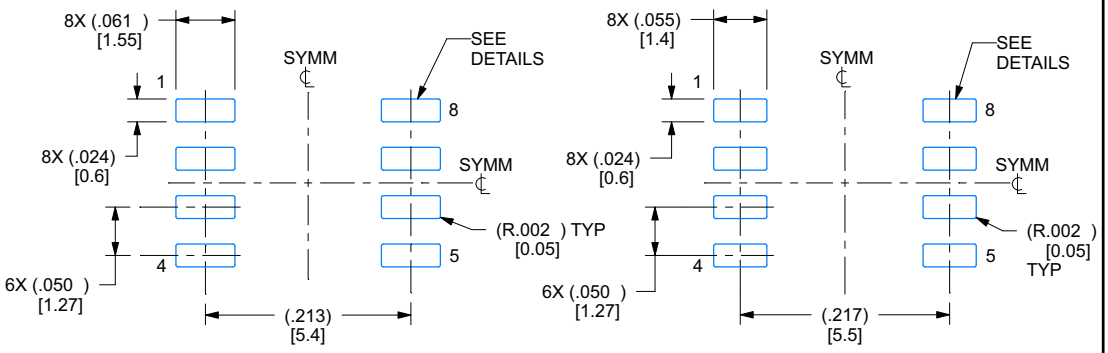
ADVANCE INFORMATION

## EXAMPLE BOARD LAYOUT

### D0008B

### SOIC - 1.75 mm max height

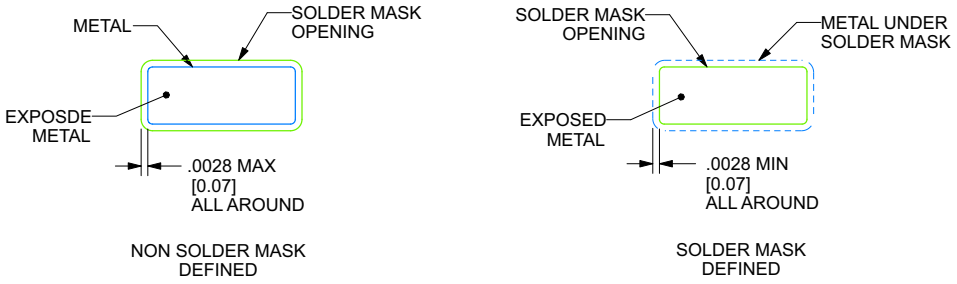
SMALL OUTLINE INTEGRATED CIRCUIT




IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X




NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4221445/C 02/2019

NOTES: (continued)

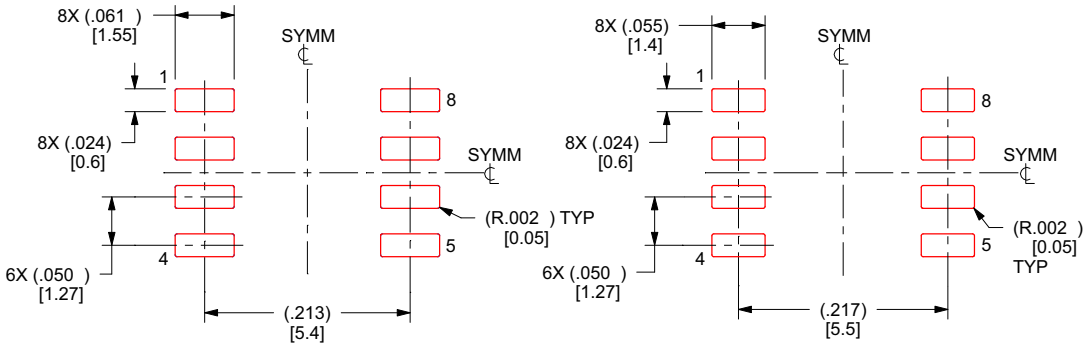
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008B

### SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




IPC-7351 NOMINAL
.150 [3.85] CLEARANCE / CREEPAGE

HV / ISOLATION OPTION
.162 [4.1] CLEARANCE / CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:6X

4221445/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

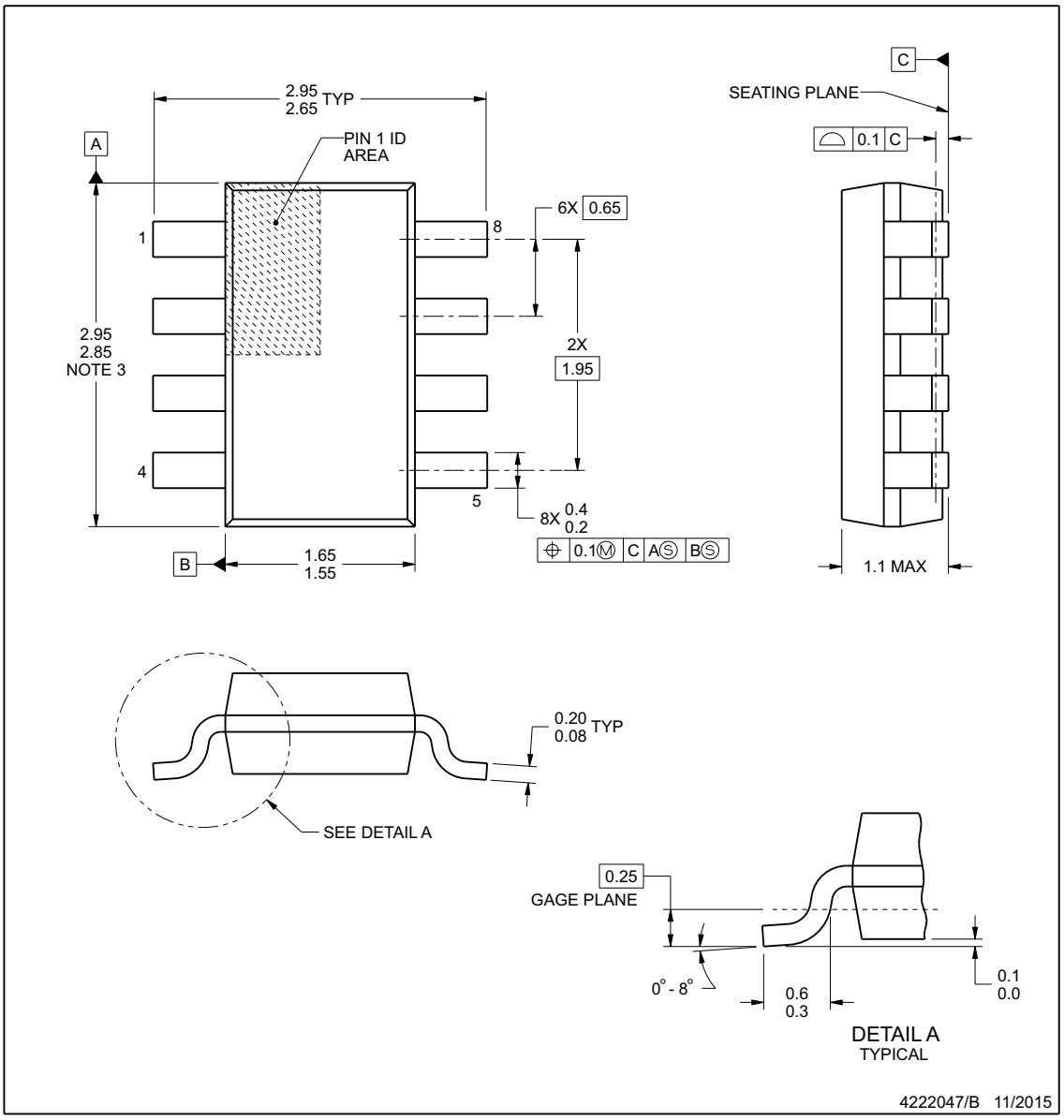
ADVANCE INFORMATION

# PACKAGE OUTLINE

## DDF0008A

## SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE




NOTES:

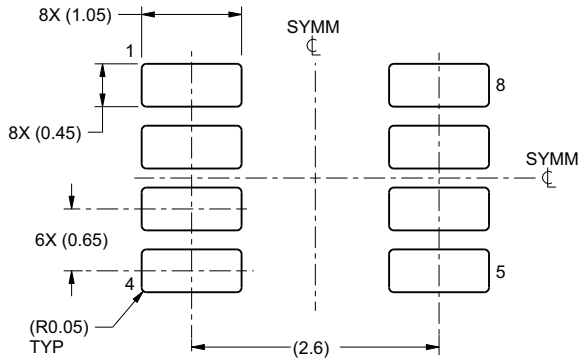
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

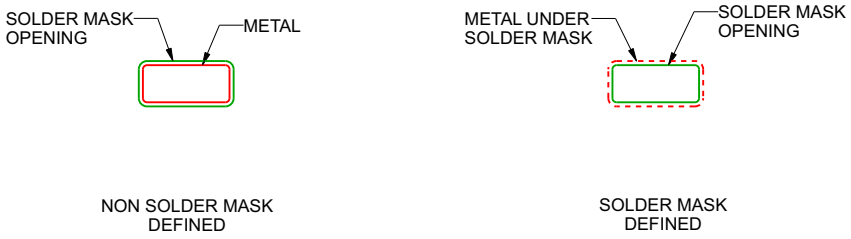
## DDF0008A

### SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE




LAND PATTERN EXAMPLE
SCALE:15X




SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

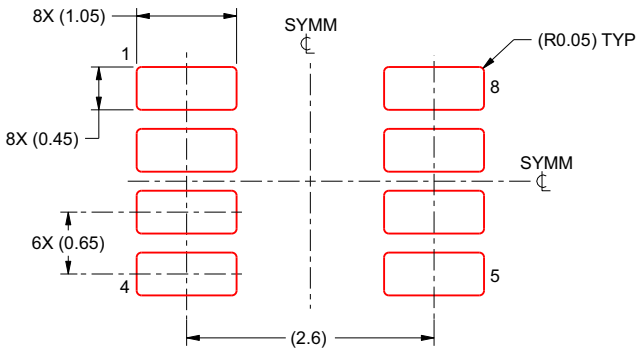
ADVANCE INFORMATION

ADVANCE INFORMATION

## EXAMPLE STENCIL DESIGN

**DDF0008A** — **SOT-23 - 1.1 mm max height**

PLASTIC SMALL OUTLINE




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

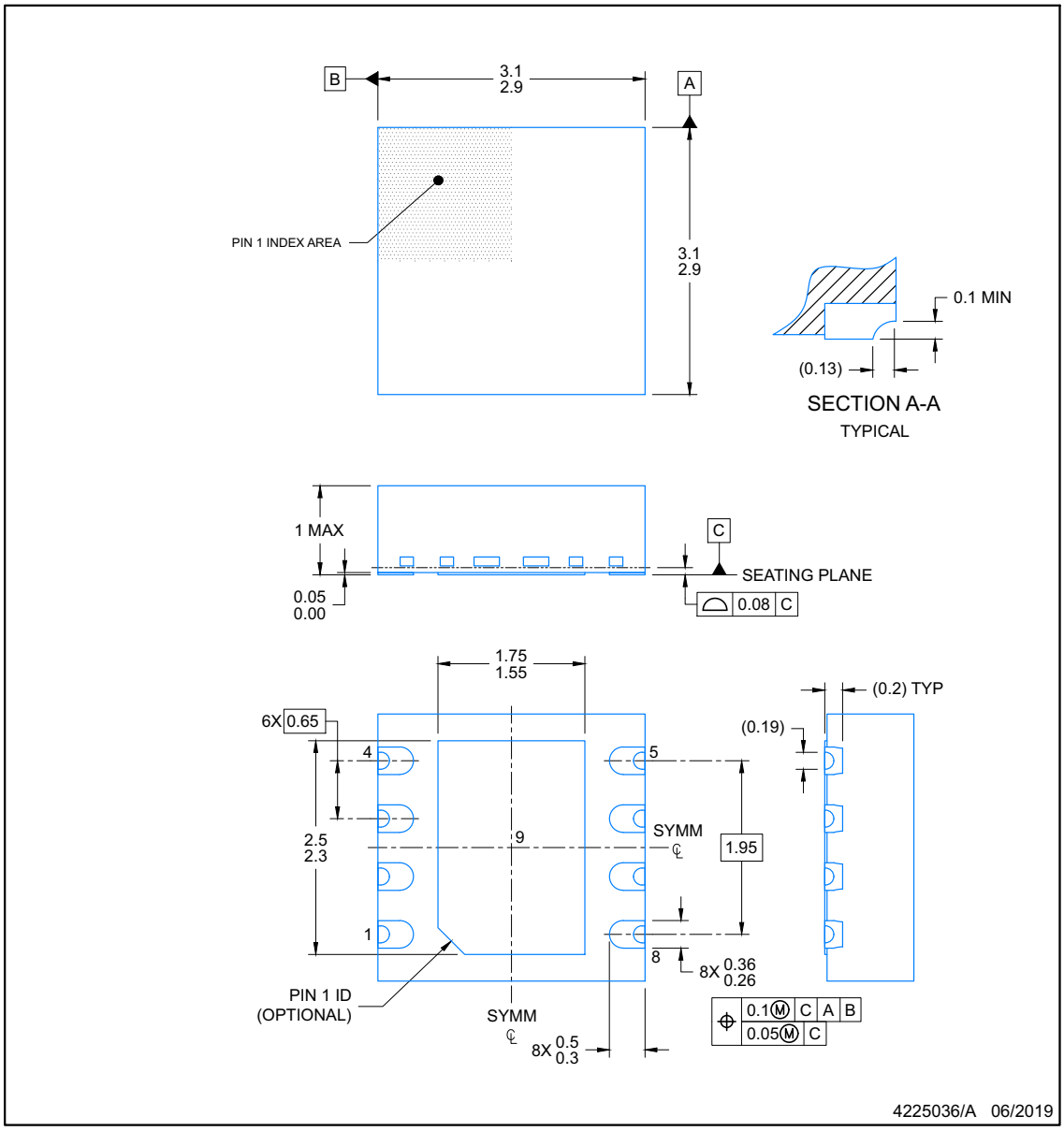
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

# PACKAGE OUTLINE

## DRB0008J

## VSON - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD




NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

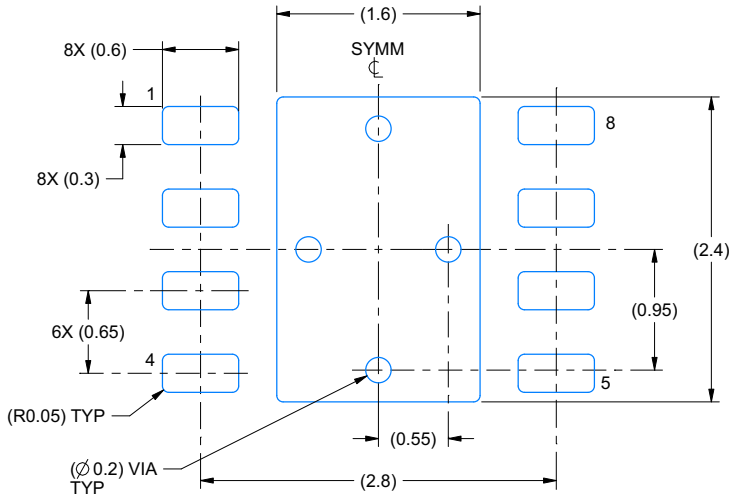
ADVANCE INFORMATION

## EXAMPLE BOARD LAYOUT

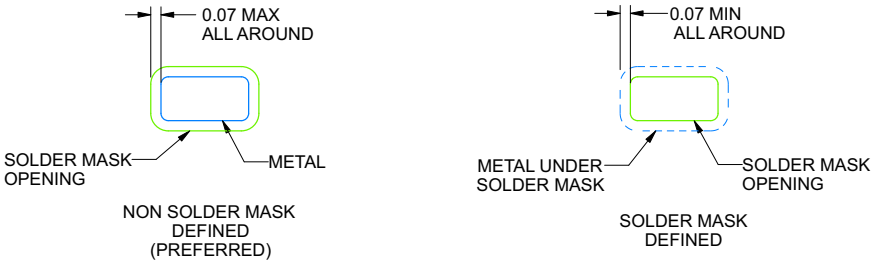
### DRB0008F

### VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




LAND PATTERN EXAMPLE
SCALE:20X




SOLDER MASK DETAILS

4222121/C 10/2016

NOTES: (continued)

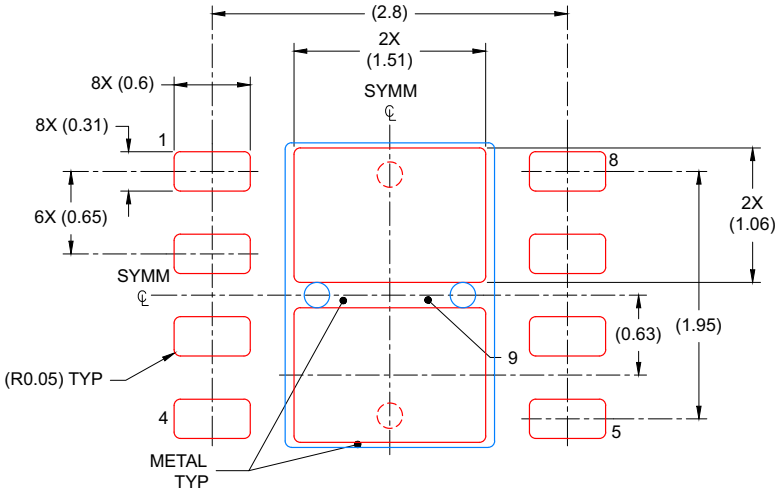
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

## DRB0008J

### VSON - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

4225036/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PTCAN3403DDFRQ1 | ACTIVE | SOT-23-THIN | DDF | 8 | 3000 | TBD | Call TI | Call TI | -40 to 150 | | Samples |
| PTCAN3403DRBRQ1 | ACTIVE | SON | DRB | 8 | 3000 | TBD | Call TI | Call TI | -40 to 150 | | Samples |
| PTCAN3403DRQ1 | ACTIVE | SOIC | D | 8 | 2500 | TBD | Call TI | Call TI | -40 to 150 | | Samples |
| PTCAN3404DDFRQ1 | ACTIVE | SOT-23-THIN | DDF | 8 | 3000 | TBD | Call TI | Call TI | -40 to 150 | | Samples |
| PTCAN3404DRBRQ1 | ACTIVE | SON | DRB | 8 | 3000 | TBD | Call TI | Call TI | -40 to 150 | | Samples |
| PTCAN3404DRQ1 | ACTIVE | SOIC | D | 8 | 2500 | TBD | Call TI | Call TI | -40 to 150 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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