TDA54x Jacinto™ Processors

1 Features

Processor cores:

- Up-to Eight Arm® Cortex®-A720AE MPUs
  - Lockstep capable

Real-Time processing CPUs :

- Up-to 6x Arm® Cortex®-R52+ (or 3x pairs in Lockstep)
  - Virtualization for multi-core processing

System/SOC CPUs:

- 8x Dual Arm® Cortex®-M55 (Lockstep)

DSP / AI processing :

- Up to 4x C7™ neural processing unit(NPU)
  - Up to 400 TOPS

Vision and video processing:

- Up to 16 cameras
- DMPAC: Dense Optical Flow, Stereo Disparity Engine
- 4x CSI-2 RX interface, 1x CSI-2 TX output

GPU and display processing:

- Imagination DXS Family GPU

Display subsystem:

- eDP1.5/DP2.1
  - Multi-Stream Transport (up to 4 displays, up to 4K60fps)
- 1x DSI CPHY-2.0/DPHY-2.1
  - Up to 4 lanes per port (muxed with CSI-TX)
- DSS Controller:
  - 4 pipelines + 1 Writeback path, up to 4k60 per pipe

Networking subsystem:

- NPAC (Network Processing Accelerator) specialized subsystem for Ethernet switching and packet transfer
- Integrated Ethernet Switch
  - 8 external ports
  - 10base-T1S (OA3P 3-wire i/f) supported on all ports
  - MACSEC per port, supports line rate

Memory:

- LPDDR4x/5/5x interface
  - In-line ECC
- 1x UFS3.0
- 1x eMMC5.1 HS200
- 2x XSPI interface up to 400MBps

Security:

- SHE/EVITA Full compliant HSM, ISO21434 compliant

Functional Safety:

- Functional Safety-Compliant targeted for ISO26262 and IEC61530
- AEC - Q100 qualified

Safety features:

- Support for full ASIL D or mixed ASIL D / ASIL B with FFI

High-speed serial interfaces:

- 2x PCIe up to 4L
  - Gen5 controller
  - Root complex or Endpoint
- 1x USB3.2 (Gen 2)/eUSB2.0

Video acceleration:

- H.264/H.265 Encode/Decode: 1.0GP/s encode or decode, up to 10b support

Serial interfaces:

- Up to 170 General-Purpose Input/Output (GPIO) pin capability

TPS6594-Q1 Companion Power Management ICs (PMIC):

- Functional Safety-Compliant support up to ASIL D/SIL 3
- Flexible mapping to support different use cases

ADVANCE INFORMATION

2 Applications

- **Automotive:**
- Autonomous sensor fusion / perception systems including camera, radar and LiDAR sensors
- ADAS Domain Controller
- Advanced surround view and park assistance systems
- Off-highway vehicle control
- **Industrial:**
- Industrial mobile robot (AGV/AMR) with safety functions
- Construction and agriculture
- Aerospace and defense

3 Description

The TDA5 high-performance compute SoC family is designed to deliver safe and efficient edge AI performance, with capabilities of up to 1200 TOPS, with integrated C7™ NPU and chiplet-ready architecture. This enables seamless progression to L3 autonomous driving in software-defined vehicles, where conditional automation is possible in both urban and highway environments. Additionally, the TDA5 SoCs are well-suited for similar applications in industrial transportation, humanoid and industrial robots, and aerospace and defense with their advanced sensor processing, cybersecurity, and functional safety features.

The TDA5 SoCs feature multiple specialized subsystems, each tailored to address the growing demand for high-performance compute and cross-domain applications. These subsystems include dedicated processing cores and hardware acceleration for security, vision processing, edge AI, display rendering, and networking. By offloading these tasks, the SoCs' MPU and MCU cores are freed up to focus on user application software. Furthermore, support for PCIe, Ethernet, and other automotive standard peripherals enables safe, secure, and high-speed data transfer between different components and systems.

Building on two decades of leadership in the automotive processor market, the TDA5 architecture is designed to provide a scalable and high-performance solution for a wide range of applications. As an evolution of the TDA4 family, software developed for TDA4 can be easily scaled to the TDA5 family, with minimal rework required. This allows for the reuse of software assets and enables the development of more complex and sophisticated applications. The TDA5 family's unique combination of high-performance real-time and analytics cores, along with the latest C7™ NPU and next-generation accelerators for image signal processing, makes it an optimized solution for various camera, radar, sensor fusion, and AI applications.

The TDA5 family provides high-performance compute capabilities for both traditional computer vision and deep learning algorithms, with industry-leading power/performance ratios. The high level of system integration enables lower costs for advanced automotive platforms, supporting multiple sensor modalities in centralized ECUs, multiple sensor domains, or a centralized automotive computer. Key processing and acceleration cores include the latest-generation C7™ DSP with scalar and vector cores, dedicated deep learning acceleration, latest application and GPU cores for general compute, a vision and imaging subsystem, video codec, network packet processing accelerator, and Ethernet switch, as well as a dedicated security subsystem. These cores are carefully integrated into an SoC architecture designed from the ground up to support functional safety at a system level, ensuring the highest level of reliability and performance in safety-critical applications.

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