TEXAS INSTRUMENTS
TDES4940
SNLS747 – NOVEMBER 2023

TDES4940 4K V^{3}Link Enhanced Video to Embedded DisplayPort Bridge Deserializer

1 Features

- DisplayPort (DP) / Embedded DisplayPort (eDP) Transmitter
  - VESA DP v1.4a/eDP v1.4b transmitter
  - HBR3/HBR2/HBR/RBR Link Bit Rates
  - Main link: 1, 2, or 4 lanes
  - Each lane up to 8.1Gbps
  - AUX CH 1Mbps
  - Hot Plug Detect (HPD)
  - Extracts aggregated video streams to local eDP display
  - Designed for 4 K @ 60 Hz video resolution
  - Stream synchronization and splitting
- V^{3}Link enhanced video interface
  - 13.5/12.528/10.8/6.75/3.375 Gbps per Channel; Up to 27 Gbps over dual channels
  - Coax/STP interconnect support
  - Selectable 1, 2 channels
  - Daisy-chain and splitting
  - Adaptive equalization
- Ultra-low latency control channel
  - Two fast-mode plus I2C up to 1 MHz (up to 3.4 MHz local bus access)
  - High-speed GPIOs
  - Supports SPI and UART pass through GPIOs
- Compatibility
  - Integrated HDCP v1.4 with on-chip keys
  - V^{3}Link video and V^{3}Link enhanced video product families
- Image enhancement (white balance and dithering)
- Security and diagnostics
  - Voltage and temperature monitoring
  - BIST and pattern generation
  - CRC and error diagnostics
  - ECC on control bits
  - Unique ID for counterfeit protection
- Advanced link robustness and EMC control
  - Spread spectrum clocking generation (SSCG)
  - Adaptive Receiver Equalization (AEQ)
- Low power operation
  - 1.8V and 1.15V dual power supply
- Qualifications
  - ISO 10605 and IEC 61000-4-2 ESD compliant
  - Temperature: -20°C to +85°C

2 Applications

- High resolution display:
  - Operating room displays
  - Seat back entertainment displays
  - High resolution HMI

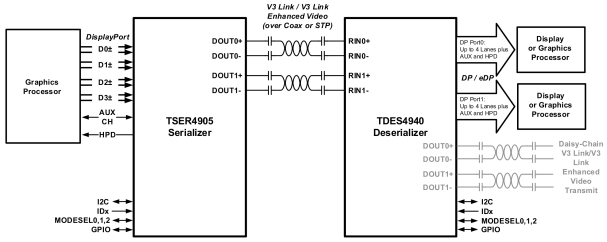
3 Description

The TDES4940 is a V^{3}Link Enhanced Video to DisplayPort (DP) / Embedded DisplayPort (eDP) bridge device. In conjunction with a V^{3}Link Enhanced Video serializer, the chipset receives a high-speed serialized interface over low-cost 50 Ω coax or STP/STQ cables. The TDES4940 is a VESA DP v1.4a/eDP v1.4b compatible device that supports advanced features such as HBR3, and SuperFrame formats. The device supports video resolutions of 4K 30-bit color and higher. The V^{3}Link Enhanced Video supports video and audio data transmission and full duplex control, including I2C, and GPIO data over the same link. Consolidation of video data and control over V^{3}Link Enhanced Video lanes reduces the interconnect size and weight and simplifies system design. EMI is minimized by the use of low voltage differential signaling, data scrambling, and randomization. In compatible V^{3}Link mode, the device supports up to 2K resolutions with 24-bit color depth over a single/dual link as well as HDCP v1.4 support when paired with an HDCP capable serializer.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TDES4940	VQFNP (88)	12 mm × 12 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



4 Device and Documentation Support

4.1 Documentation Support

4.1.1 Related Documentation

For related documentation see the following:

- *Soldering Specifications Application Report,* SNOA549
- *IC Package Thermal Metrics Application Report,* SPRA953
- *Leadless Leadframe Package (LLP) Application Report,* SNOA401

4.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

4.3 Trademarks

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4.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

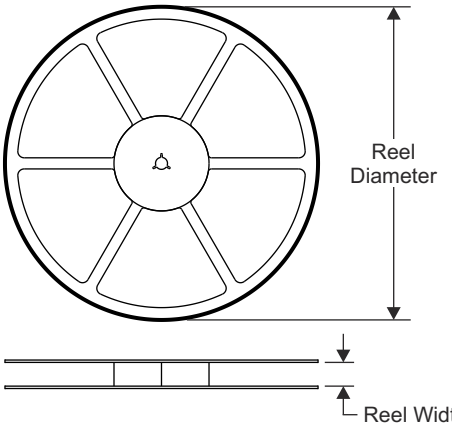
5.1 Package Option Addendum

Packaging Information

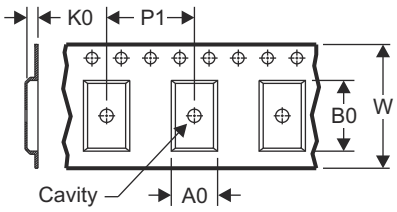
Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking
TDES4940RURTQ1	ACTIVE	VQFN	RUR0088D	88	250	RoHS & Green	NiPdAuAg	Level-3-260C-168 HR	-20 to 85	TDES4940
TDES4940RURRQ1	ACTIVE	VQFN	RUR0088D	88	2500	RoHS & Green	NiPdAuAg	Level-3-260C-168 HR	-20 to 85	TDES4940

5.2 Tape and Reel Information

REEL DIMENSIONS

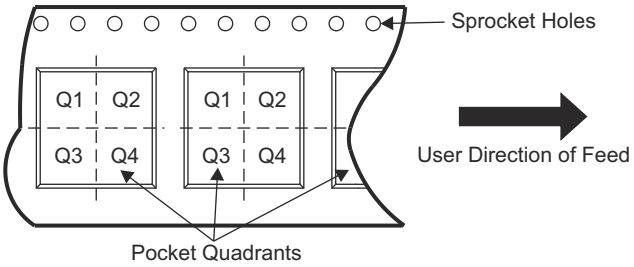


TAPE DIMENSIONS



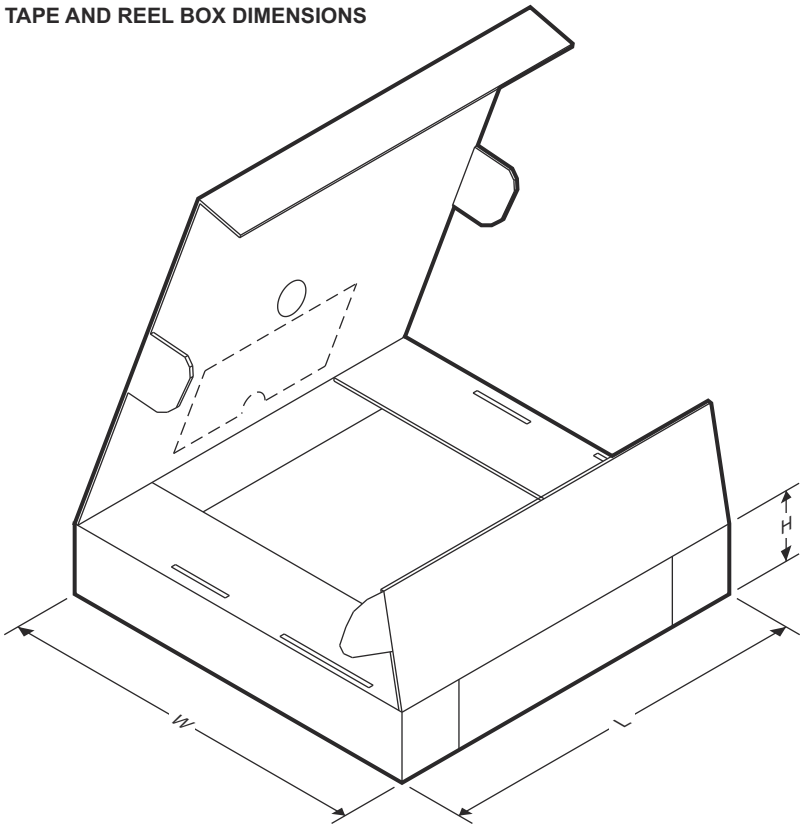
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TDES4940RURTQ1	VQFN	RUR0088D	88	250	180	24.4	12.30	12.30	1.10	16.00	24.00	Q2
TDES4940RURRQ1	VQFN	RUR0088D	88	2500	330	24.4	12.30	12.30	1.10	16.00	24.00	Q2

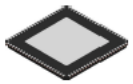
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TDES4940RURTQ1	VQFN	RUR0088D	88	250	210	185	35
TDES4940RURRQ1	VQFN	RUR0088D	88	2500	360	360	36
TDES4940RURRQ1	VQFN	RUR0088D	88	2500	367	367	35

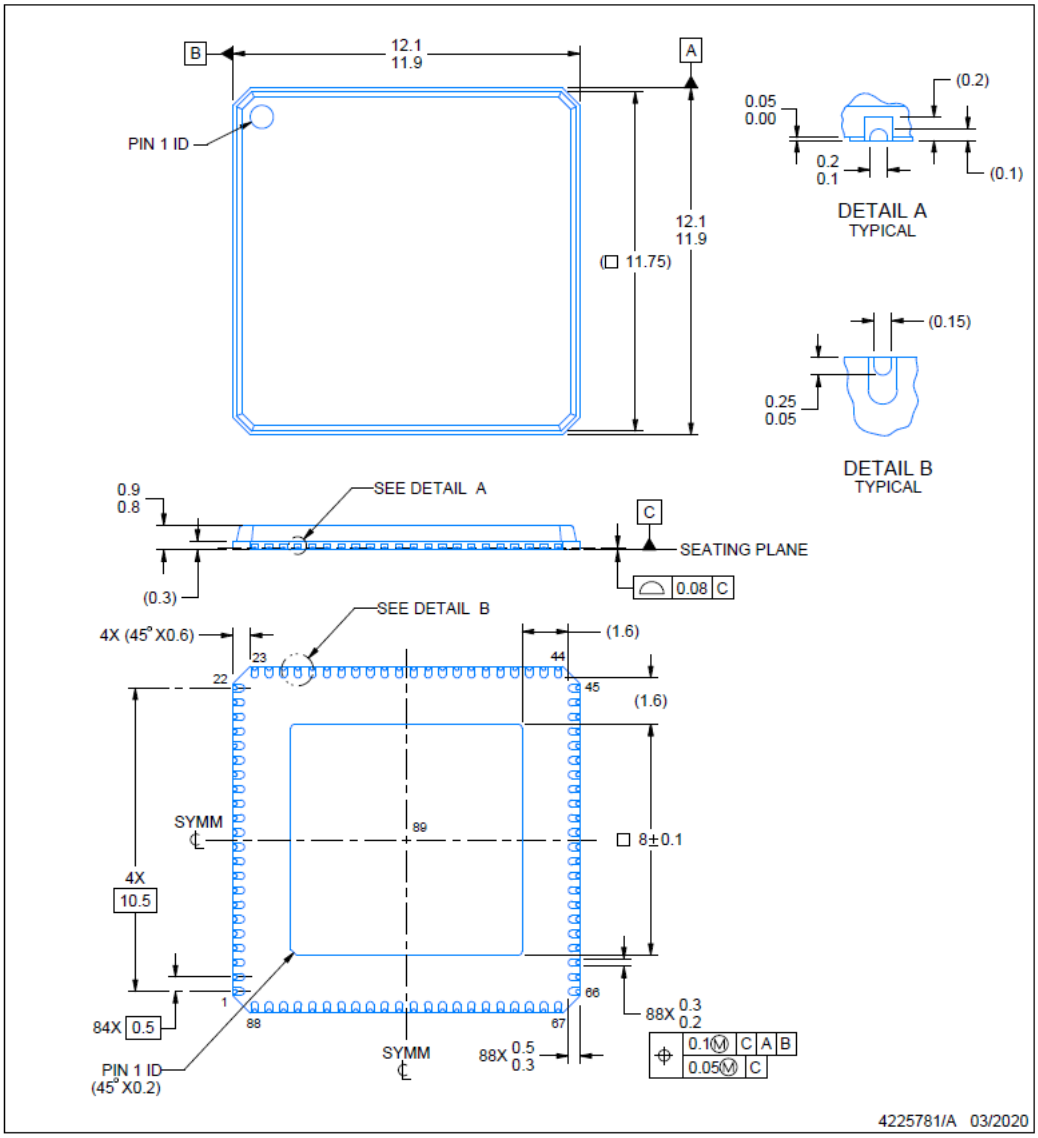
PACKAGE OUTLINE

RUR0088D



VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



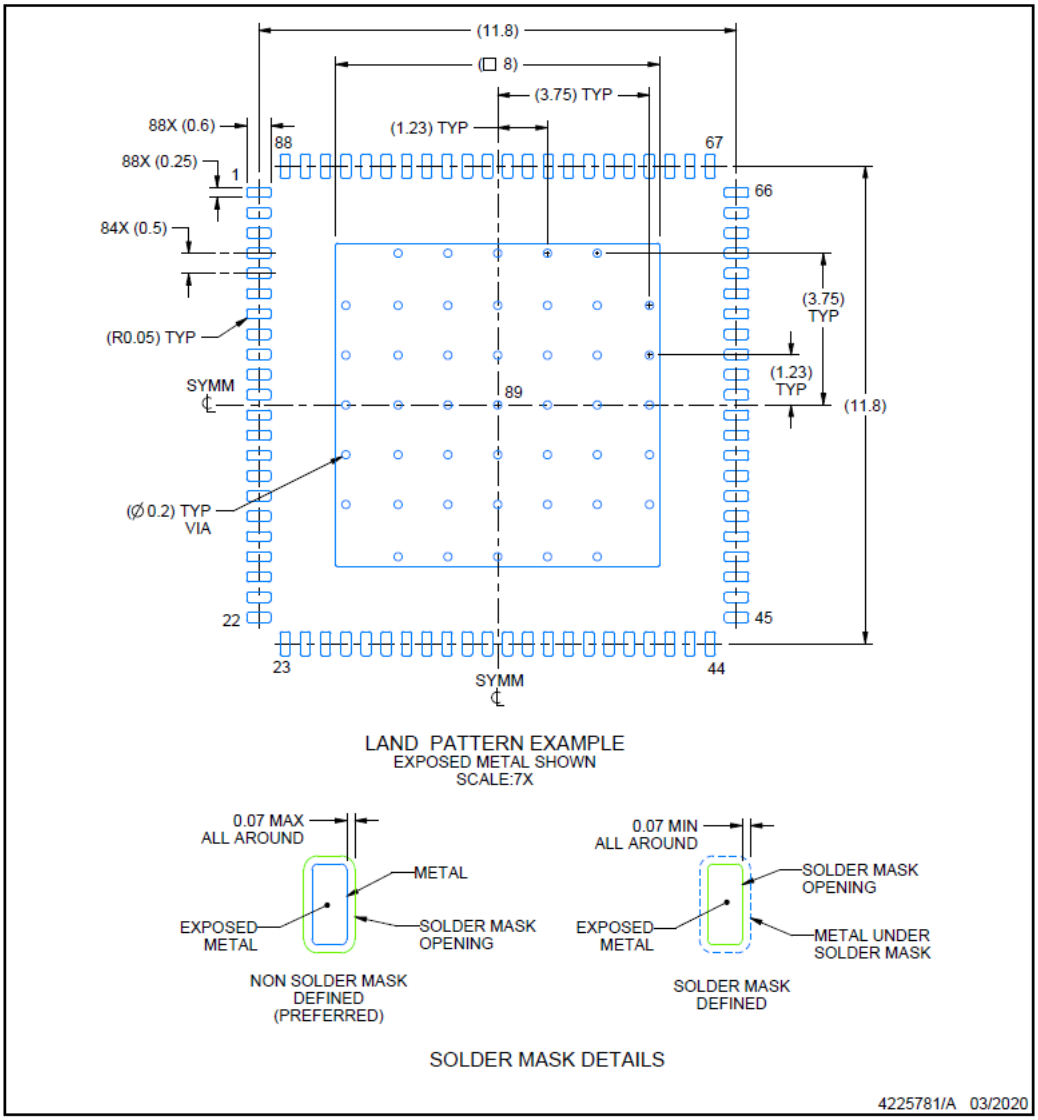
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RUR0088D — **VQFNP - 0.9 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



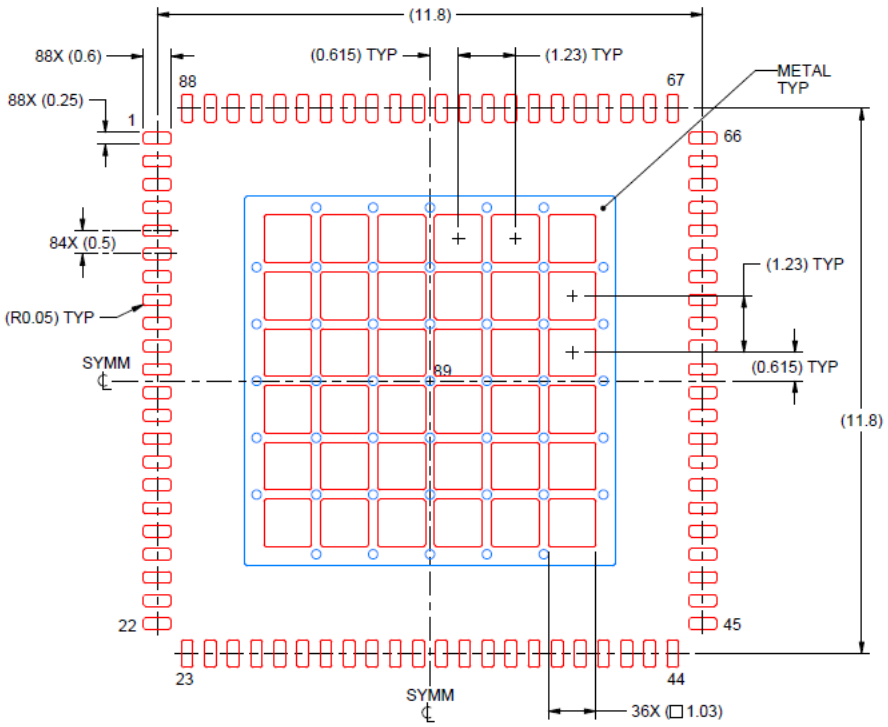
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUR0088D — **VQFNP - 0.9 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 89:
60% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TDES4940RURR	Active	Production	VQFNP (RUR) | 88	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-20 to 85	TDES4940
TDES4940RURR.A	Active	Production	VQFNP (RUR) | 88	2500 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-20 to 85	TDES4940
TDES4940RURT	Active	Production	VQFNP (RUR) | 88	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-20 to 85	TDES4940
TDES4940RURT.A	Active	Production	VQFNP (RUR) | 88	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-20 to 85	TDES4940

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

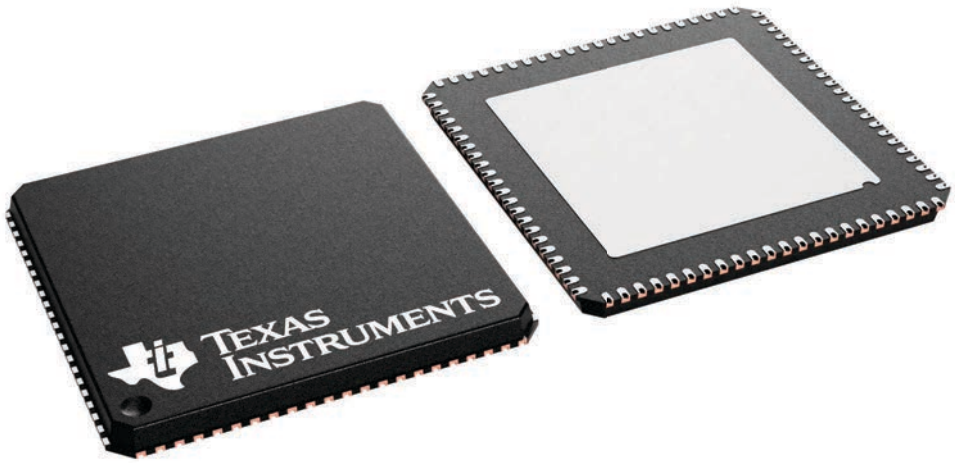
RUR 88

VQFN - 0.9 mm max height

12 x 12, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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