# TDP2004-Q1 Automotive Four-Channel 20Gbps DisplayPort 2.1 Linear Redriver

## 1 Features

- Automotive Q100 qualified
- –40 to 105°C (grade 2) ambient temperature support without heatsink
- Supports DisplayPort 2.1 up to 20Gbps (UHBR20)
- Integrated cross-point mux suitable for USB-C Alternate Mode
- Supports AC coupled HDMI 2.1 source up to 12Gbps
- Protocol agnostic linear equalizer supporting most AC coupled interfaces up to 20Gbps
- Excellent electrical performance at 20Gbps (10GHz Nyquist):
  - 20dB equalization
  - 1.65V DC linearity, 1.1V AC linearity
  - –11 / –18dB Rx / Tx return loss
  - 70fs low additive RJ with PRBS data
- Transparent to DisplayPort or HDMI FRL link training
- Single 3.3V supply with 160mW/chan active power
- Internal voltage regulator provides immunity to supply noise
- High linearity easing DP compliance ratio tests
- High BW resulting excellent linear EQ curves
- Pin-strap, $I^2C$ or EEPROM programming
  - 18 EQ boost and 5 flat gain settings

## 2 Applications

- Advanced driver assistance systems (ADAS)
- Infotainment & cluster
- Display
- Head Unit and Digital Cockpit
- Media Hub

## 3 Description

The TDP2004-Q1 is a four-channel low-power high-performance linear repeater or redriver designed to support DisplayPort 2.1 up to 20Gbps and AC coupled HDMI2.1 Source up to 12Gbps.

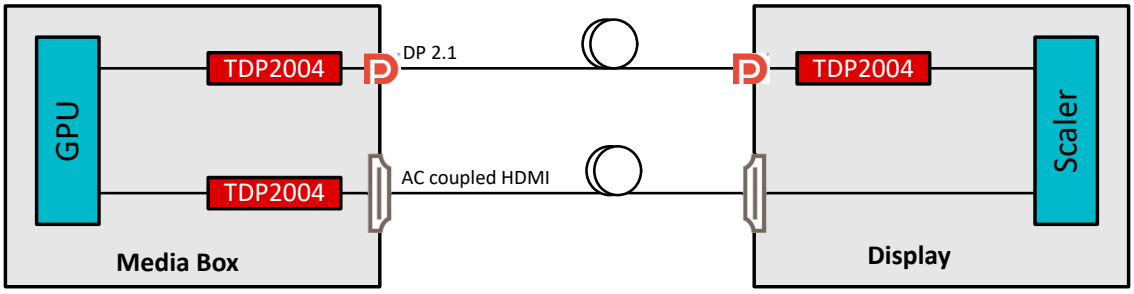
The TDP2004-Q1 receivers deploy continuous time linear equalizers (CTLE) to provide a programmable high-frequency boost. The equalizer can open an input eye that is completely closed due to inter-symbol interference (ISI) induced by an interconnect medium, such as PCB traces or cables. The linear data-paths of TDP2004-Q1 preserve transmit preset signal characteristics. High bandwidth, low channel-to-channel cross-talk, low additive jitter and excellent return loss makes the device almost a passive element in the link, but with useful equalization. The DisplayPort link training is effective through the linear redriver that becomes part of the passive channel in between source Tx and sink Rx. This transparency in the link training protocol results in optimum electrical link and lowest possible latency. The data-path of the device uses an internally regulated power rail that provides high immunity to any supply noise on the board.

The device also has low AC and DC gain variation providing consistent equalization in high volume platform deployment.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| TDP2004-Q1 | RGF (VQFN, 40) | 5mm × 7mm |

(1) For more information, see Section 9.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Typical Application**

# Table of Contents

# 4 Pin Configuration and Functions

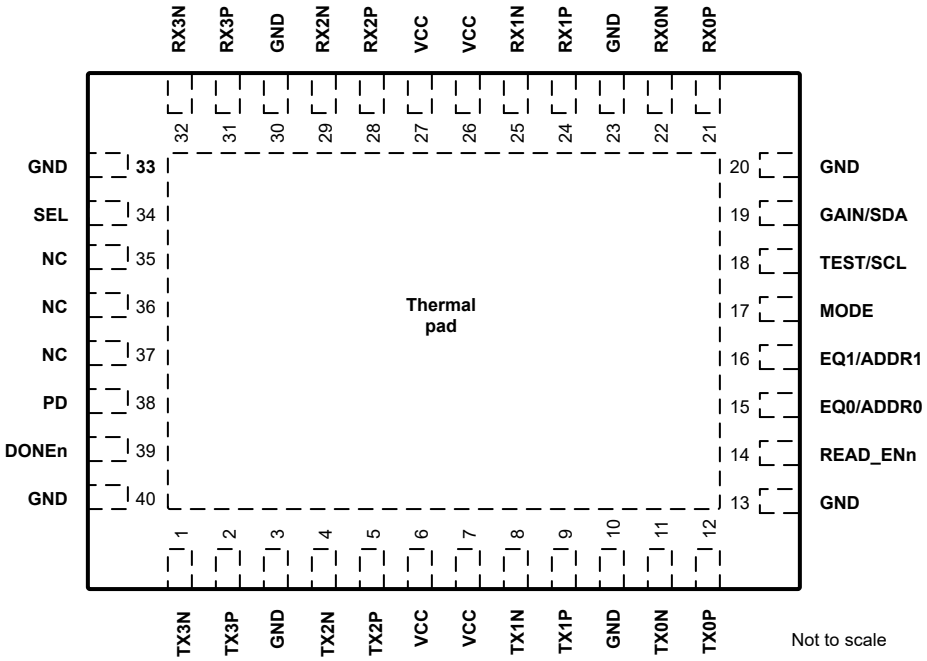



**Figure 4-1. RGF Package, 40-Pin VQFN (Top View)**

**Table 4-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| DONEn | 39 | O, 3.3V open drain | In **SMBus/I²C Controller mode**:<br>Indicates the completion of a valid EEPROM register load operation. External pullup resistor such as 4.7kΩ required for operation.<br>High: External EEPROM load failed or incomplete<br>Low: External EEPROM load successful and complete<br>In **SMBus/I²C Target/Pin mode**:<br>This output is High-Z. The pin can be left floating. |
| MODE | 17 | I, 5-level | Sets device control configuration modes. 5-level IO pin as provided in Table 6-3. The pin can be exercised at device power up or in normal operation mode.<br>L0: **Pin mode** – device control configuration is done solely by strap pins.<br>L1: **SMBus/I²C Controller mode** – device control configuration is read from external EEPROM. When the TDP2004-Q1 finishes reading from the EEPROM successfully, Don En pin is pulled LOW. SMBus/I²C Target operation is available in this mode before, during or after EEPROM reading. Note: during EEPROM reading if the external SMBus/I²C Controller wants to access TDP2004-Q1 registers, the external controller must support arbitration.<br>L2: **SMBus/I²C Target mode** – device control configuration is done by an external controller with SMBus/I²C Controller.<br>L3 and L4 (Float): RESERVED – TI internal test modes. |
| EQ0 / ADDR0 | 15 | I, 5-level | In **Pin mode:**<br>Sets receiver linear equalization (CTLE) boost for channels 0-3 as provided in Table 6-1. These pins are sampled at device power up only.<br>In **SMBus/I²C mode:**<br>Sets SMBus / I²C Target address as provided in Table 6-4. These pins are sampled at device power up only. |
| EQ1 / ADDR1 | 16 | I, 5-level | |
| GAIN / SDA | 19 | I, 5-level / I/O, 3.3V LVCMOS, open drain | In **Pin mode:**<br>Flat gain (DC and AC) from the input to the output of the device for channels 0-3. The pin is sampled at device power up only.<br>In **SMBus/I²C mode:**<br>3.3V SMBus/I²C data. External 1kΩ to 5kΩ pullup resistor is required as per SMBus / I²C interface standard. |

**Table 4-1. Pin Functions (continued)**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| GND | 3, 10, 13, 20, 23, 30, 33, 40, EP | G | Ground reference for the device.<br>EP: the Exposed Pad at the bottom of the QFN package, which is used as the GND return for the device. The EP must be connected to one or more ground planes through the low resistance path. A via array provides a low impedance path to GND. The EP also improves thermal dissipation. |
| PD | 38 | I, 3.3V LVCMOS | 2-level logic controlling the operating state of the redriver. Active in all device control modes. The pin has internal 1MΩ weak pull down resistor.<br>High: power down for channels 0-3<br>Low: power up, normal operation for channels 0-3 |
| READ_ENn | 14 | I, 3.3V LVCMOS | In **SMBus/I²C Controller mode**:<br>After power up, when the pin is low, the device initiates the SMBus / I²C Controller mode EEPROM read function. When EEPROM read is complete (indicated by assertion of Don En low), this pin can be held low for normal device operation. During the EEPROM load process the signal path of the device is disabled.<br>In **SMBus/I²C Target and Pin modes:**<br>In these modes the pin is not used. The pin can be left floating. The pin has internal 1MΩ weak pull down resistor. |
| SEL | 34 | | The pin selects the mux configuration.<br>Low: straight data path – RX[0/1/2/3][P/N] connected to TX[0/1/2/3][P/N] through the redriver.<br>High: cross data path – RX[0/1/2/3][P/N] connected to TX[1/0/3/2][P/N] through the redriver.<br>Active in all device control modes. 59kΩ internal pull down. |
| TEST / SCL | 18 | I, 5-level / I/O, 3.3V LVCMOS, open drain | In **Pin mode:**<br>TI test mode. External 1kΩ pull down resistor must be installed.<br>In **SMBus/I²C mode:**<br>3.3V SMBus/I²C clock. External 1kΩ to 5kΩ pullup resistor is required as per SMBus / I²C interface standard. |
| RX0N | 22 | I | Inverting differential inputs to the equalizer. Integrated 50Ω termination resistor from the pin to internal CM bias voltage. Channel 0. |
| RX0P | 21 | I | Non-inverting differential inputs to the equalizer. Integrated 50Ω termination resistor from the pin to internal CM bias voltage. Channel 0. |
| RX1N | 25 | I | Inverting differential inputs to the equalizer. Integrated 50Ω termination resistor from the pin to internal CM bias voltage. Channel 1. |
| RX1P | 24 | I | Non-inverting differential inputs to the equalizer. Integrated 50Ω termination resistor from the pin to internal CM bias voltage. Channel 1. |
| RX2N | 29 | I | Inverting differential inputs to the equalizer. Integrated 50Ω termination resistor from the pin to internal CM bias voltage. Channel 2. |
| RX2P | 28 | I | Non-inverting differential inputs to the equalizer. Integrated 50Ω termination resistor from the pin to internal CM bias voltage. Channel 2. |
| RX3N | 32 | I | Inverting differential inputs to the equalizer. Integrated 50Ω termination resistor from the pin to internal CM bias voltage. Channel 3. |
| RX3P | 31 | I | Non-inverting differential inputs to the equalizer. Integrated 50Ω termination resistor from the pin to internal CM bias voltage. Channel 3. |
| TX0N | 11 | O | Inverting pin for 100Ω differential driver output. Channel 0. |
| TX0P | 12 | O | Non-inverting pin for 100Ω differential driver output. Channel 0. |
| TX1N | 8 | O | Inverting pin for 100Ω differential driver output. Channel 1. |
| TX1P | 9 | O | Non-inverting pin for 100Ω differential driver output. Channel 1. |
| TX2N | 4 | O | Inverting pin for 100Ω differential driver output. Channel 2. |
| TX2P | 5 | O | Non-inverting pin for 100Ω differential driver output. Channel 2. |
| TX3N | 1 | O | Inverting pin for 100Ω differential driver output. Channel 3. |
| TX3P | 2 | O | Non-inverting pin for 100Ω differential driver output. Channel 3. |

**Table 4-1. Pin Functions (continued)**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| VCC | 6, 7, 26, 27 | P | Power supply pins. VCC = 3.3V ±10%. The VCC pins on this device must be connected through a low-resistance path to the board VCC plane. Install a decoupling capacitor to GND near each VCC pin. |

(1) I = input, O = output, P = power, G= ground

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $VCC_{ABSMAX}$ | Supply voltage (VCC) | –0.5 | 4.0 | V |
| $VIO_{CMOS,ABSMAX}$ | 3.3V LVCMOS and open drain I/O voltage | –0.5 | 4.0 | V |
| $VIO_{5LVL,ABSMAX}$ | 5-level input I/O voltage | –0.5 | 2.75 | V |
| $VIO_{HS-RX,ABSMAX}$ | High-speed I/O voltage (RXnP, RXnN) | –0.5 | 3.2 | V |
| $VIO_{HS-TX,ABSMAX}$ | High-speed I/O voltage (TXnP, TXnN) | –0.5 | 2.75 | V |
| $T_{J,ABSMAX}$ | Junction temperature | | 150 | °C |
| $T_{stg}$ | Storage temperature range | –65 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2) | ±500 | |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2kV may actually have higher performance.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VCC | Supply voltage, VCC to GND | DC plus AC power must not exceed these limits | 3.0 | 3.3 | 3.6 | V |
| $N_{VCC}$ (1) | Supply noise tolerance | DC to <50Hz, sinusoidal | | | 250 | mVpp |
| | | 50Hz to 500kHz, sinusoidal | | | 100 | mVpp |
| | | 500kHz to 2.5MHz, sinusoidal | | | 33 | mVpp |
| | | Supply noise, >2.5MHz, sinusoidal | | | 10 | mVpp |
| $T_{RampVCC}$ | VCC supply ramp time | From 0V to 3.0V | 0.150 | | 100 | ms |
| $T_A$ | Operating ambient temperature | | -40 | | 105 | °C |
| $T_J$ | Operating junction temperature | | | | 125 | °C |
| $PW_{LVCMOS}$ | Minimum pulse width required for the device to detect a valid signal on LVCMOS inputs | PD, SEL, and READ_ENn | 200 | | | µs |
| $VCC_{SMBUS}$ | SMBus/I²C SDA and SCL open-drain termination voltage | Supply voltage for open-drain pullup resistor | | | 3.6 | V |
| $F_{SMBus}$ | SMBus/I²C clock (SCL) frequency | SMBus Target mode | 10 | | 400 | kHz |
| $VID_{LAUNCH}$ | Source launch amplitude | Differential signaling | | | 1200 | mVpp |

## 5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| DR | Data rate | | 1 | | 20 | Gbps |

(1) Sinusoidal noise is superimposed to supply voltage with negligeable impact to device function or critical performance shown in the Electrical Table. Steps must be taken to ensure the combined AC plus DC supply noise meets the specified VDD supply voltage limits.

## 5.4 Thermal Information

| THERMAL METRIC[1] | | TDP2004-Q1 RGF, 40 Pins | UNIT |
|---|---|---|---|
| $R_{\theta JA\text{-}High\ K}$ | Junction-to-ambient thermal resistance | 29.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 19.0 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 11.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.4 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 11.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 3.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

## 5.5 DC Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Power** | | | | | | |
| $P_{ACT}$ | Device active power | 4 channels active, EQ = 0-2 | | 0.57 | 0.71 | W |
| | | 4 channels active, EQ = 5-19 | | 0.69 | 0.85 | W |
| $P_{STBY}$ | Device power consumption in standby power mode | All channels disabled (PD = H) | | 17 | 25 | mW |
| **Control IO** | | | | | | |
| $V_{IH}$ | High level input voltage | SDA, SCL, PD, READ_ENn, SEL pins | 2.1 | | | V |
| $V_{IL}$ | Low level input voltage | SDA, SCL, PD, READ_ENn, SEL pins | | | 1.08 | V |
| $V_{OH}$ | High level output voltage | $R_{pullup}$ = 4.7kΩ (SDA, SCL, DONEn pins) | 2.1 | | | V |
| $V_{OL}$ | Low level output voltage | $I_{OL}$ = –4mA (SDA, SCL, DONEn pins) | | | 0.4 | V |
| $I_{IH,SEL}$ | Input high leakage current for SEL pins | $V_{Input}$ = SEL pins | | | 100 | µA |
| $I_{IH}$ | Input high leakage current | $V_{Input}$ = VCC, (SCL, SDA, PD, READ_ENn pins) | | | 10 | µA |
| $I_{IL}$ | Input low leakage current | $V_{Input}$ = 0V, (SCL, SDA, PD, READ_ENn, SEL pins) | –10 | | | µA |
| $I_{IH,FS}$ | Input high leakage current for fail safe input pins | $V_{Input}$ = 3.6V, VCC = 0V, (SCL, SDA, PD, READ_ENn, SEL pins) | | | 200 | µA |
| $C_{IN\text{-}CTRL}$ | Input capacitance | SDA, SCL, PD, READ_ENn, SEL pins | | 1.6 | | pF |
| **5 Level IOs (MODE, GAIN, EQ0, EQ1 pins)** | | | | | | |
| $I_{IH\_5L}$ | Input high leakage current, 5-level IOs | VIN = 2.5V | | | 10 | µA |
| $I_{IL\_5L}$ | Input low leakage current for all 5-level IOs except MODE. | VIN = GND | –10 | | | µA |
| $I_{IL\_5L,MODE}$ | Input low leakage current for MODE pin | VIN = GND | –200 | | | µA |

## 5.5 DC Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Receiver** | | | | | | |
| $V_{RX-DC-CM}$ | RX DC common vode voltage | Device is in active or standby state | | 1.4 | | V |
| $Z_{RX-DC}$ | Rx DC single-ended impedance | | | 50 | | Ω |
| **Transmitter** | | | | | | |
| $Z_{TX-DIFF-DC}$ | DC differential Tx impedance | Impedance of Tx during active signaling, VID,diff = 1Vpp | | 100 | | Ω |
| $V_{TX-DC-CM}$ | Tx DC common mode voltage | | | 1.0 | | V |
| $I_{TX-SHORT}$ | Tx short circuit current | Total current the Tx can supply when shorted to GND | | 70 | | mA |

## 5.6 High Speed Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Receiver** | | | | | | |
| $RL_{RX-DIFF}$ | Input differential return loss | 50MHz | | –27 | | dB |
| | | 4.0GHz | | –15 | | dB |
| | | 5.0GHz | | –15 | | dB |
| | | 8.0GHz | | –15 | | dB |
| | | 10.0GHz | | –11 | | dB |
| $RL_{RX-CM}$ | Input common mode return loss | 50MHz | | –22 | | dB |
| | | 4.0GHz | | –12 | | dB |
| | | 5.0GHz | | –11 | | dB |
| | | 8.0GHz | | –10 | | dB |
| | | 10.0GHz | | –8 | | dB |
| $XT_{RX}$ | Receiver-side pair-to-pair isolation | Minimum over 10.0MHz to 10.0GHz range | | –50 | | dB |
| **Transmitter** | | | | | | |
| $RL_{TX-DIFF}$ | Output differential return loss | 50.0MHz | | –29 | | dB |
| | | 4.0GHz | | –16 | | dB |
| | | 5.0GHz | | –17 | | dB |
| | | 8.0GHz | | –20 | | dB |
| | | 10.0GHz | | –18 | | dB |
| $RL_{TX-CM}$ | Output common mode return loss | 50.0MHz | | –16 | | dB |
| | | 4.0GHz | | –11 | | dB |
| | | 5.0GHz | | –10 | | dB |
| | | 8.0GHz | | –9 | | dB |
| | | 10.0GHz | | –9 | | dB |
| $XT_{TX}$ | Transmit-side pair-to-pair isolation | Minimum over 10.0MHz to 10.0GHz range | | –46 | | dB |
| **Device Datapath** | | | | | | |
| $T_{PLHD/PHLD}$ | Input-to-output latency (propagation delay) through a data channel | For either low-to-high or high-to-low transition | | 100 | | ps |
| $T_{RJ-DATA}$ | Additive random jitter with data | Jitter through redriver minus the calibration trace. 20Gbps PRBS15. 800mVpp-diff input swing | | 70 | | fs |

## 5.6 High Speed Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| XT | Channel to channel xtalk (between adjacent active channels, FEXT | Minimum over 50.0MHz to 10.0Ghz range, normalized to EQ gain of 0dB | | –38 | | dB |
| LINEARITY-DC | Output DC linearity | | | 1650 | | mVpp |
| LINEARITY-AC | Output AC linearity at GAIN = L4 | 8Gbps | | 1250 | | mVpp |
| LINEARITY-AC | Output AC linearity at GAIN = L4 | 16Gbps | | 1200 | | mVpp |
| LINEARITY-AC | Output AC linearity at GAIN = L4 | 20Gbps | | 1100 | | mVpp |

## 5.7 SMBUS/I$^2$C Timing Charateristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Target Mode** | | | | | | |
| $t_{SP}$ | Pulse width of spikes which must be suppressed by the input filter | | | | 50 | ns |
| $t_{HD-STA}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated | | 0.6 | | | µs |
| $t_{LOW}$ | LOW period of the SCL clock | | 1.3 | | | µs |
| $T_{HIGH}$ | HIGH period of the SCL clock | | 0.6 | | | µs |
| $t_{SU-STA}$ | Setup time for a repeated START condition | | 0.6 | | | µs |
| $t_{HD-DAT}$ | Data hold time | | 0 | | | µs |
| $T_{SU-DAT}$ | Data setup time | | 0.1 | | | µs |
| $t_r$ | Rise time of both SDA and SCL signals | Pullup resistor = 4.7kΩ, Cb = 10pF | | 120 | | ns |
| $t_f$ | Fall time of both SDA and SCL signals | Pullup resistor = 4.7kΩ, Cb = 10pF | | 2 | | ns |
| $t_{SU-STO}$ | Setup time for STOP condition | | 0.6 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | | 1.3 | | | µs |
| $t_{VD-DAT}$ | Data valid time | | | | 0.9 | µs |
| $t_{VD-ACK}$ | Data valid acknowledge time | | | | 0.9 | µs |
| $C_b$ | Capacitive load for each bus line | | | | 400 | pF |
| **Controller Mode** | | | | | | |
| $f_{SCL-M}$ | SCL clock frequency | | | 303 | | kHz |
| $t_{LOW-M}$ | SCL low period | | | 1.90 | | µs |
| $T_{HIGH-M}$ | SCL high period | | | 1.40 | | µs |
| $t_{SU-STA-M}$ | Setup time for a repeated START condition | | | 2 | | µs |
| $t_{HD-STA-M}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated | | | 1.5 | | µs |
| $T_{SU-DAT-M}$ | Data setup time | | | 1.4 | | µs |
| $t_{HD-DAT-M}$ | Data hold time | | | 0.5 | | µs |
| $t_{R-M}$ | Rise time of both SDA and SCL signals | Pullup resistor = 4.7kΩ, Cb = 10pF | | 120 | | ns |

## 5.7 SMBUS/I$^2$C Timing Charateristics (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $T_{F-M}$ | Fall time of both SDA and SCL signals | Pullup resistor = 4.7kΩ, Cb = 10pF | | 2 | | ns |
| $t_{SU-STO-M}$ | Stop condition setup time | | | 1.5 | | µs |
| **EEPROM Timing** | | | | | | |
| $T_{EEPROM}$ | EEPROM configuration load time | Time to assert DONEn after READ_ENn has been asserted. | | 7.5 | | ms |
| $T_{POR}$ | Time to first SMBus access | Power supply stable after initial ramp. Includes initial power-on reset time. | | 50 | | ms |

## 5.8 Typical Characteristics

Figure 5-1 shows typical EQ gain curves versus frequency for different EQ settings. Figure 5-2 shows typical differential return loss for Rx and Tx pins.

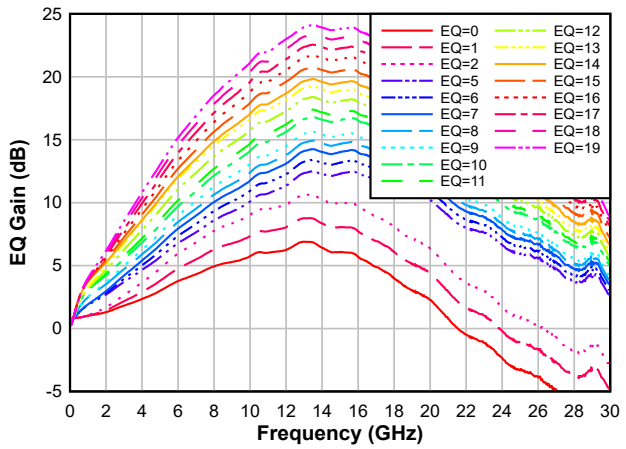



Figure 5-1. Typical EQ Boost vs Frequency

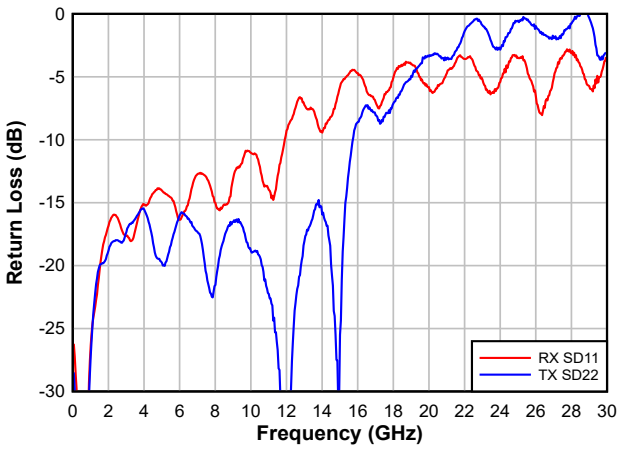



Figure 5-2. Typical Differential Return Loss

## 5.9 Typical Jitter Characteristics

Figure 5-3 and Figure 5-4 show eye diagrams at 20Gbps that compare jitter through calibration traces (left), and jitter through TDP2004-Q1 (right) at TI evaluation boards with minimal channels. The eye diagrams illustrate that TDP2004-Q1 adds very little random jitter (RJ) - below instrumentation acuracy. Total jitter improvements can be attributed to the residual equalization at EQ = 0 cleaning up DJ for input loss.

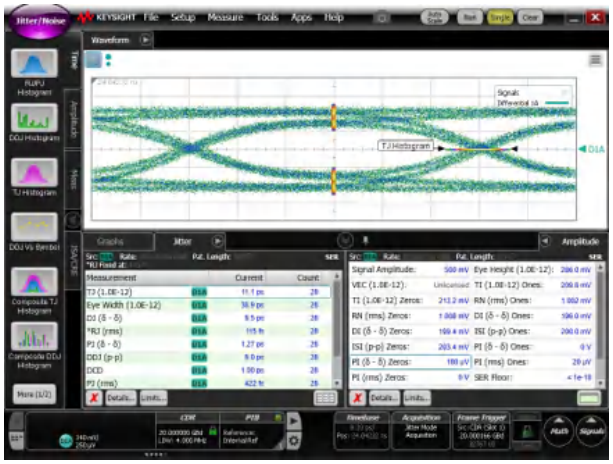


Figure 5-3. Through Baseline Calibration Trace Setup for 20Gbps

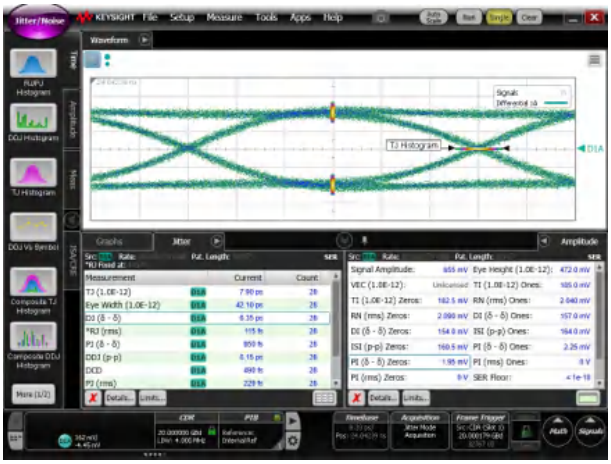


Figure 5-4. Through TDP2004-Q1 for 20Gbps

# 6 Detailed Description

## 6.1 Overview

The TDP2004-Q1 is a four-channel multi-rate linear redriver with integrated signal conditioning. The signal channels of the device operate independently from one another. Each channel includes a continuous-time linear equalizer (CTLE) and a linear output driver, which together compensate for a lossy transmission channel between the source transmitter and the final receiver. The linearity of the data path is specifically designed to preserve any transmit equalization while keeping receiver equalization effective.

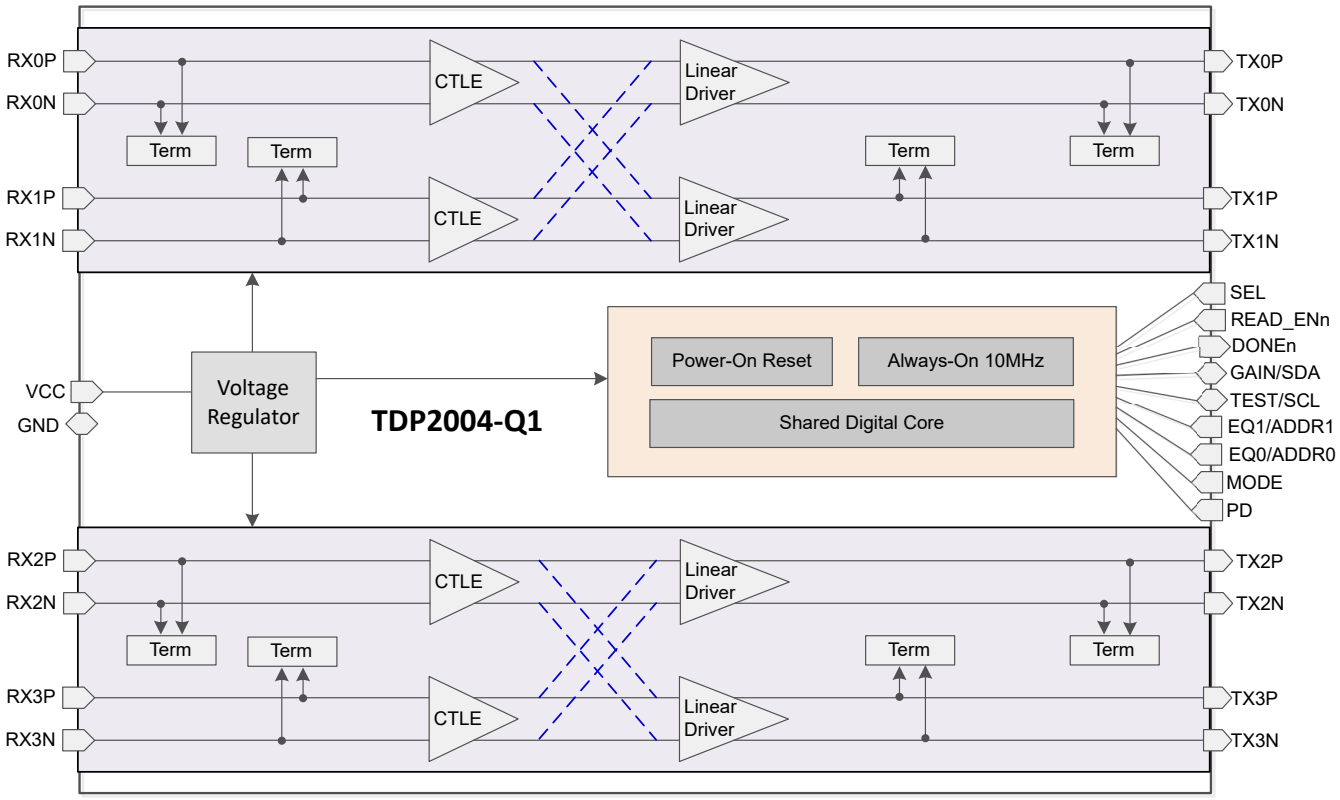
The TDP2004-Q1 can be configured three different ways:

**Pin mode** – device control configuration is done solely by strap pins. Pin mode is expected to be satisfactory `for many system implementation needs.

**SMBus/I$^2$C Controller mode** – device control configuration is read from external EEPROM. When the TDP2004-Q1 has finished reading from the EEPROM successfully, the device drives the DONEn pin LOW. SMBus/I$^2$C Target operation is available in this mode before, during, or after EEPROM reading. Note: during EEPROM reading, if the external SMBus/I$^2$C Controller wants to access TDP2004-Q1 registers, the external controller must support arbitration. The mode is preferred when software implementation is not desired.

**SMBus/I$^2$C Target mode** – provides most flexibility. Requires a SMBus/I$^2$C Controller device to configure TDP2004-Q1 though writing to the Target address.

## 6.2 Functional Block Diagram




## 6.3 Feature Description

### *6.3.1 RX Equalization Control Settings*

The TDP2004-Q1 receivers feature a continuous-time linear equalizer (CTLE) that applies high-frequency boost and low-frequency attenuation to help equalize the frequency-dependent insertion loss effects of the passive channel. The receivers implement two stage linear equalizer for wide range of equalization capability. The equalizer stages also provide flexibility to make subtle modifications of mid-frequency boost for best EQ gain

profile match with wide range of channel media characteristics. The EQ profile control feature is only available in SMBus/I$^2$C mode. In Pin mode the settings are optimized for FR4 traces.

Table 6-1 provides available equalization boost at 20Gbps (10GHz Nyquist frequency) through EQ control pins or SMBus/I$^2$C registers. In Pin Control mode EQ1 and EQ0 pins set equalization boost for channels 0-3. In I$^2$C mode individual channels can be independently programmed for EQ boost.

**Table 6-1. Equalization Control Settings**

| EQUALIZATION SETTING | | | | | | | TYPICAL EQ BOOST (dB) |
|---|---|---|---|---|---|---|---|
| | Pin mode | | SMBus/I$^2$C Mode | | | | |
| EQ INDEX | EQ1 | EQ0 | eq_stage1_3:0 | eq_stage2_2:0 | eq_profile_3:0 | eq_stage1_bypass | at 10GHz |
| 0 | L0 | L0 | 0 | 0 | 0 | 1 | 5.0 |
| 1 | L0 | L1 | 1 | 0 | 0 | 1 | 7.0 |
| 2 | L0 | L2 | 3 | 0 | 0 | 1 | 8.0 |
| 5 | L1 | L0 | 0 | 0 | 1 | 0 | 10.0 |
| 6 | L1 | L1 | 1 | 0 | 1 | 0 | 10.5 |
| 7 | L1 | L2 | 2 | 0 | 1 | 0 | 11.5 |
| 8 | L1 | L3 | 3 | 0 | 3 | 0 | 12.0 |
| 9 | L1 | L4 | 4 | 0 | 3 | 0 | 13.0 |
| 10 | L2 | L0 | 5 | 1 | 7 | 0 | 13.5 |
| 11 | L2 | L1 | 6 | 1 | 7 | 0 | 14.0 |
| 12 | L2 | L2 | 8 | 1 | 7 | 0 | 15.5 |
| 13 | L2 | L3 | 10 | 1 | 7 | 0 | 16.0 |
| 14 | L2 | L4 | 10 | 2 | 15 | 0 | 16.5 |
| 15 | L3 | L0 | 11 | 3 | 15 | 0 | 17.5 |
| 16 | L3 | L1 | 12 | 4 | 15 | 0 | 18.5 |
| 17 | L3 | L2 | 13 | 5 | 15 | 0 | 19.0 |
| 18 | L3 | L3 | 14 | 6 | 15 | 0 | 20.0 |
| 19 | L3 | L4 | 15 | 7 | 15 | 0 | 20.5 |

### *6.3.2 Flat-Gain*

The GAIN pin can be used to set the overall data-path flat gain (DC and AC) of the TDP2004-Q1 when the device is in Pin mode. The pin GAIN sets the flat-gain for channels 0-3. In I$^2$C mode each channel can be independently set. Table 6-2 provides flat gain control configuration settings. For most systems the default setting of GAIN = L4 (float) is recommended that provides flat gain of 0dB.

The flat-gain and equalization of the TDP2004-Q1 must be set such that the output signal swing at DC and high frequency does not exceed the DC and AC linearity ranges of the devices, respectively.

**Table 6-2. Flat Gain Configuration Settings**

| Pin mode: GAIN | I$^2$C Mode: flat_gain_2:0 | Datapath Flat Gain |
|---|---|---|
| L0 | 0 | –5.6dB |
| L1 | 1 | –3.8dB |
| L2 | 3 | –1.3dB |
| L4 (float) | 5 | 0.6dB (default recommendation) |

**Table 6-2. Flat Gain Configuration Settings (continued)**

| Pin mode: GAIN | I²C Mode: flat_gain_2:0 | Datapath Flat Gain |
|---|---|---|
| L3 | 7 | +2.6dB |

### 6.3.3 Cross Point

The TDP2004-Q1 provides 2x2 cross-point function. Using pin SEL pin the 4 channel signal paths can be configured as straight connection or cross connections as shown in Figure 6-1.

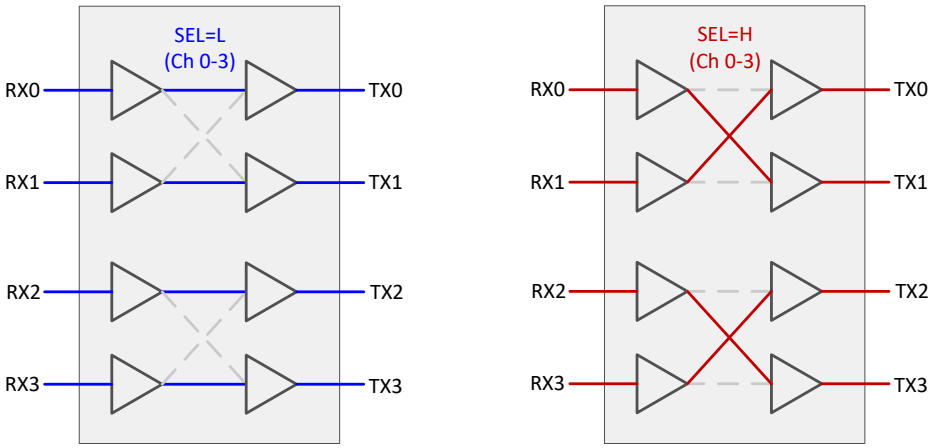



**Figure 6-1. Signal Flow Diagram for Cross-Point Mux Operation**

## 6.4 Device Functional Modes

### 6.4.1 Active Mode

The device is in normal operation. In this mode, the TDP2004-Q1 redrives and equalizes video mainlink signals to provide better signal integrity.

### 6.4.2 Standby Mode

The device is in standby mode invoked by PD = H. In this mode, the device is in standby mode conserving power.

## 6.5 Programming

### 6.5.1 Pin mode

The TDP2004-Q1 can be fully configured through pin-strap pins. In this mode the device uses 2-level and 5-level pins for device control and signal integrity optimum settings.

#### 6.5.1.1 Five-Level Control Inputs

The TDP2004-Q1 has 5-level input pins that are used to control the configuration of the device. These 5-level inputs use a resistor divider to help set the 5 valid levels and provide a wider range of control settings. External resistors must be of 10% tolerance or better. The 5-level pins except MODE are sampled at powerup only. The MODE pin can be exercised at device power up or in normal operation mode.

**Table 6-3. 5-Level Control Pin Settings**

| LEVEL | SETTING |
|---|---|
| L0 | 1kΩ to GND |
| L1 | 8.25kΩ to GND |
| L2 | 24.9kΩ to GND |
| L3 | 75kΩ to GND |
| L4 | F (Float) |

### 6.5.2 SMBUS/I²C Register Control Interface

If MODE = L2 (SMBus/I²C Target control mode), then the TDP2004-Q1 is configured through a standard I²C or SMBus interface that can operate up to 400kHz. The Target address of the TDP2004-Q1 is determined by the pin strap settings on the ADDR1 and ADDR0 pins. The sixteen possible Target addresses for channels 0-3 are provided in Table 6-4. In SMBus/I²C modes the SCL and SDA pins must be pulled up to a 3.3V supply with a pullup resistor. The value of the resistor depends on total bus capacitance. 4.7kΩ is a good first approximation for a bus capacitance of 10pF.

**Table 6-4. SMBUS/I²C Target Address Settings**

| ADDR1 | ADDR0 | 7-bit Target Address Channels 0-3 |
|---|---|---|
| L0 | L0 | 0x18 |
| L0 | L1 | 0x1A |
| L0 | L2 | 0x1C |
| L0 | L3 | 0x1E |
| L0 | L4 | Reserved |
| L1 | L0 | 0x20 |
| L1 | L1 | 0x22 |
| L1 | L2 | 0x24 |
| L1 | L3 | 0x26 |
| L1 | L4 | Reserved |
| L2 | L0 | 0x28 |
| L2 | L1 | 0x2A |
| L2 | L2 | 0x2C |
| L2 | L3 | 0x2E |
| L2 | L4 | Reserved |
| L3 | L0 | 0x30 |
| L3 | L1 | 0x32 |
| L3 | L2 | 0x34 |
| L3 | L3 | 0x36 |
| L3 | L4 | Reserved |

The TDP2004-Q1 has two types of registers:

- **Shared Registers:** these registers can be accessed at any time and are used for device-level configuration, status read back, control, or to read back the device ID information.
- **Channel Registers:** these registers are used to control and configure specific features for each individual channel. All channels have the same register set and can be configured independent of each other or configured as a group through broadcast writes to Channels 0-3.

**Table 6-5. Channel Register Access**

| Channel Registers Base Address | Channel 0-3 Access |
|---|---|
| 0x00 | Channel 0 registers |
| 0x20 | Channel 1 registers |
| 0x40 | Channel 2 registers |
| 0x60 | Channel 3 registers |
| 0x80 | Broadcast write channel 0-3 registers, read channel 0 registers |
| 0xA0 | Broadcast write channel 0-1 registers, read channel 0 registers |
| 0xC0 | Broadcast write channel 2-3 registers, read channel 2 registers |
| 0xE0 | Channel 0-3 share registers |

#### 6.5.2.1 Shared Registers

**Table 6-6. General Registers (Offset = 0xE2)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0x0 | Reserved |
| 6 | rst_i2c_regs | R/W/SC | 0x0 | Device reset control: Reset all $I^2C$ registers to default values (self-clearing). |
| 5 | rst_i2c_mas | R/W/SC | 0x0 | Reset $I^2C$ Controller (self-clearing). |
| 4-1 | RESERVED | R | 0x0 | Reserved |
| 0 | frc_eeprm_rd | R/W/SC | 0x0 | Override MODE and READ_ENn status to force manual EEPROM configuration load. |

**Table 6-7. EEPROM_Status Register (Offset = 0xE3)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | eecfg_cmplt | R | 0x0 | EEPROM load complete. |
| 6 | eecfg_fail | R | 0x0 | EEPROM load failed. |
| 5 | eecfg_atmpt_1 | R | 0x0 | Number of attempts made to load EEPROM image. |
| 4 | eecfg_atmpt_0 | R | 0x0 | |
| 3 | eecfg_cmplt | R | 0x0 | EEPROM load complete 2. |
| 2 | eecfg_fail | R | 0x0 | EEPROM load failed 2. |
| 1 | eecfg_atmpt_1 | R | 0x0 | Number of attempts made to load EEPROM image 2. |
| 0 | eecfg_atmpt_0 | R | 0x0 | |

**Table 6-8. DEVICE_ID0 Register (Offset = 0xF0)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RESERVED | R | 0x1 | Reserved |
| 3 | device_id0_3 | R | 0x0 | Device ID0 [3:1]: 001 |
| 2 | device_id0_2 | R | 0x0 | |
| 1 | device_id0_1 | R | 0x1 | |
| 0 | RESERVED | R | 0x0 | Reserved |

**Table 6-9. DEVICE_ID1 Register (Offset = 0xF1)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | device_id[7] | R | 0x0 | Device ID 0010 1001:<br>TDP2004 |
| 6 | device_id[6] | R | 0x0 | |
| 5 | device_id[5] | R | 0x1 | |
| 4 | device_id[4] | R | 0x0 | |
| 3 | device_id[3] | R | 0x1 | |
| 2 | device_id[2] | R | 0x0 | |
| 1 | device_id[1] | R | 0x0 | |
| 0 | device_id[0] | R | 0x1 | |

#### 6.5.2.2 Channel Registers

**Table 6-10. EQ Gain Control Register (Channel Register Base + Offset = 0x01)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | eq_stage1_bypass | R/W | 0x0 | Enable EQ stage 1 bypass:<br>0: Bypass disabled<br>1: Bypass enabled |

**Table 6-10. EQ Gain Control Register (Channel Register Base + Offset = 0x01) (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 6 | eq_stage1_3 | R/W | 0x0 | EQBoost stage 1 control<br>See Table 6-1 in the data sheet for details |
| 5 | eq_stage1_2 | R/W | 0x0 | |
| 4 | eq_stage1_1 | R/W | 0x0 | |
| 3 | eq_stage1_0 | R/W | 0x0 | |
| 2 | eq_stage2_2 | R/W | 0x0 | EQ Boost stage 2 control<br>See Table 6-1 in the data sheet for details |
| 1 | eq_stage2_1 | R/W | 0x0 | |
| 0 | eq_stage2_0 | R/W | 0x0 | |

**Table 6-11. EQ Gain, Flat Gain Control Register (Channel Register Base + Offset = 0x03)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0x0 | Reserved |
| 6 | eq_profile_3 | R/W | 0x0 | EQ mid-frequency boost profile<br>See Table 6-1 in the data sheet for details |
| 5 | eq_profile_2 | R/W | 0x0 | |
| 4 | eq_profile_1 | R/W | 0x0 | |
| 3 | eq_profile_0 | R/W | 0x0 | |
| 2 | flat_gain_2 | R/W | 0x1 | Flat gain select:<br>See Table 6-2 in the data sheet for details |
| 1 | flat_gain_1 | R/W | 0x0 | |
| 0 | flat_gain_0 | R/W | 0x1 | |

**Table 6-12. TI Test Mode Control Register (Channel Register Base + Offset = 0x04)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3, 1-0 | RESERVED | R | 0x0 | Reserved |
| 2 | TI test mode | R/W | 0x0 | Set TI test mode:<br>0: test mode is enabled<br>1: test mode is disabled. Must be set to "1" for normal operation. |

**Table 6-13. PD Override Register (Channel Register Base + Offset = 0x05)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | device_en_override | R/W | 0x0 | Enable power down overrides through SMBus/I$^2$C<br>0: Manual override disabled<br>1: Manual override enabled |
| 6-0 | device_en | R/W | 0x111111 | Manual power down of redriver various blocks of a channel – gated by device_en_override = 1<br>111111: All blocks in the channel are enabled<br>000000: All blocks in the channel are disabled |

**Table 6-14. Bias Register (Channel Register Base + Offset = 0x06)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 5-3 | Bias current | R/W | 0x100 | Control bias current<br>Set 001 for best performance |
| 7,6,2-0 | Reserved | R/W | 0x00000 | Reserved |

### *6.5.3 SMBus/I$^2$C Controller Mode Configuration (EEPROM Self Load)*

The TDP2004-Q1 can also be configured by reading from EEPROM. To enter into this mode MODE pin must be set to L1. The EEPROM load operation only happens once after the initial powerup of the device. If the TDP2004-Q1 is configured for SMBus Controller mode, the device remains in the SMBus IDLE state until the READ_ENn pin is asserted to LOW. After the READ_ENn pin is driven LOW, theTDP2004-Q1 becomes an SMBus Controller and attempts to self-configure by reading the device settings stored in an external EEPROM

(SMBus 8-bit address 0xA0). When the TDP2004-Q1 has finished reading from the EEPROM successfully, the device drives the DONEn pin LOW. SMBus/I$^2$C Target operation is available in this mode before, during, or after EEPROM reading. Note: during EEPROM reading, if the external SMBus/I$^2$C Controller wants to access TDP2004-Q1 registers, the external controller must support arbitration.

When designing a system for using the external EEPROM, the user must follow these specific guidelines:

- EEPROM size of 2Kb (256 × 8-bit) is recommended.
- Set MODE = L1, configure for SMBus Controller mode.
- The external EEPROM device address byte must be 0xA0 and capable of 400kHz operation at 3.3V supply
- In SMBus/I$^2$C modes the SCL and SDA pins must be pulled up to a 3.3V supply with a pullup resistor. The value of the resistor depends on total bus capacitance. 4.7kΩ is a good first approximation for a bus capacitance of 10pF.

Multiple TDP2004-Q1 can be cascaded to read from single EEPROM. Tie the READ_ENn pin of the first device low (GND) to automatically initiate EEPROM read at power up. DONEn of the first device can be fed into READ_ENn of the next device with 4.7kΩ pullup resistors. Leave the DONEn pin of the final device floating, or connect the pin to a micro-controller input to monitor the completion of the final EEPROM read.

# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

The TDP2004-Q1 is a high-speed linear redriver which extends the reach of differential channels impaired by loss from transmission media like PCBs and cables. The device can be deployed in a variety of different systems. The following sections outline typical applications and their associated design considerations.

## 7.2 Typical Applications

The TDP2004-Q1 is a linear redriver that can be used as DisplayPort main link signal conditioner as illustrated in Figure 7-1.

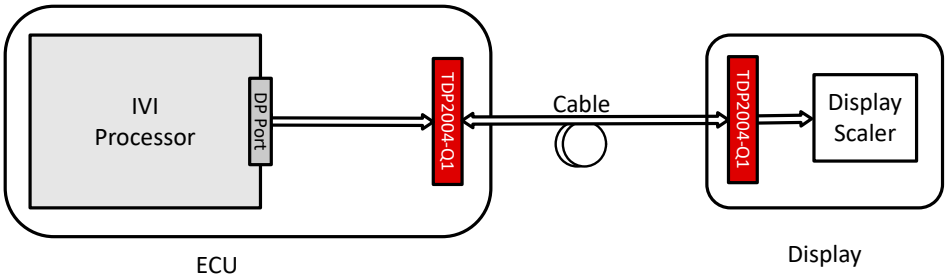



**Figure 7-1. Typical Application**

### *7.2.1 DP2.1 Main Link Signal Conditioning*

The TDP2004-Q1 can be used in a video source/sink systems such as ADAS, IVI, RSE among other applications to boost DisplayPort main link signals to increase the reach of the source and sink channel. The following sections outline detailed procedures and design requirements for a typical DP 2.1 application. However, the design recommendations can be used in other use cases.

#### 7.2.1.1 Design Requirements

As with any high-speed design, there are many factors which influence the overall performance. The following list indicates critical areas for consideration during design.

- Match the length between the P and N traces of the single-end segments of the differential pair.
- Use a uniform trace width and trace spacing for differential pairs.
- Place AC-coupling capacitors near the receiver end of each channel segment to minimize reflections.
- AC-coupling capacitors of 220nF are recommended. Set the maximum body size to 0402 and add a cutout void on the GND plane below the landing pad of the capacitor to reduce parasitic capacitance to GND.
- Surface mount connector is recommended. For through hole connection, back-drill connector vias and signal vias to minimize stub length.
- Use ground reference plane vias for a low inductance path for the return current.

#### 7.2.1.2 Detailed Design Procedure

The TDP2004-Q1 provides signal conditioning for four DP main link channels. The device is a linear redriver which is agnostic to DP link training. The DP link training negotiation between a display source and sink stays effective through the device. The redriver becomes part of the electrical channel along with passive traces, cables, and other channel elements, resulting in optimum source and sink parameters for best electrical link. Figure 7-2 shows a simplified schematic for DisplayPort application using TDP2004-Q1.

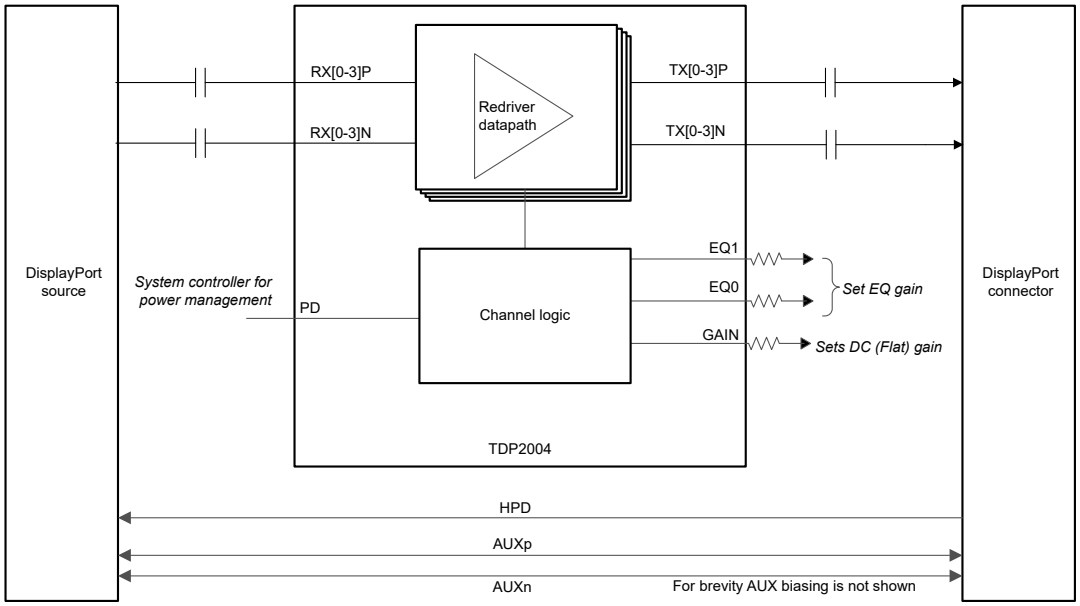



**Figure 7-2. Simplified Schematic for DP 2.1 Signal Conditioning**

#### 7.2.1.3 Application Curves

The TDP2004-Q1 is a linear redriver that can be used to extend channel reach of a DP link. The redriver can help to pass compliance by removing ISI deterministic jitter at data rates up to 20Gbps (UHBR20) for DP2.1. Figure 7-3 - Figure 7-6 shows a typical DP 2.1 Tx compliance channel setup along with compliance Eye Diagrams at TP3_EQ with or without redriver. The comparison of eye diagrams show that TDP2004-Q1 can provide signal conditioning by extending horizontal and vertical eye openings that makes a failing eye to pass.

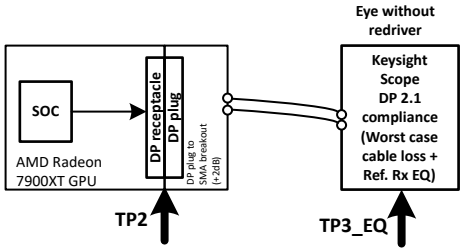



**Figure 7-3. A Typical 20Gbps (UHBR20) DP 2.1 Tx Compliance Channel Setup With No Redriver**

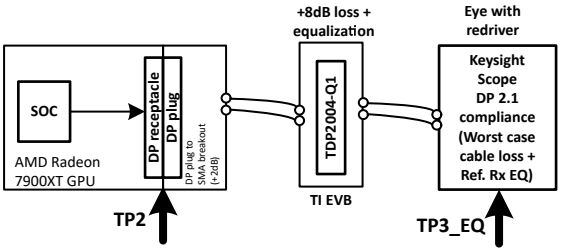



**Figure 7-4. A Typical 20Gbps (UHBR20) DP 2.1 Tx Compliance Channel Setup With Redriver**

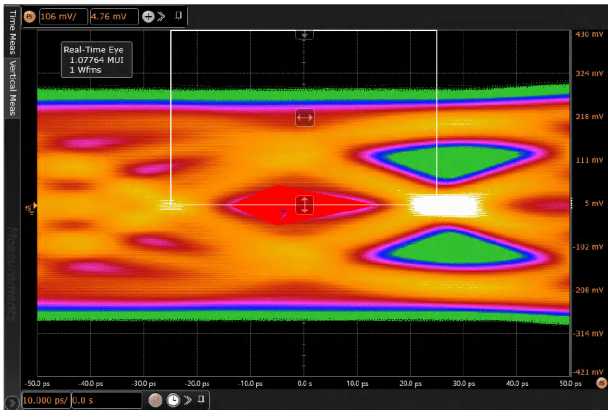



**Figure 7-5. DP 2.1 Tx Compliance Eye Diagram at TP3_EQ With No Redriver**

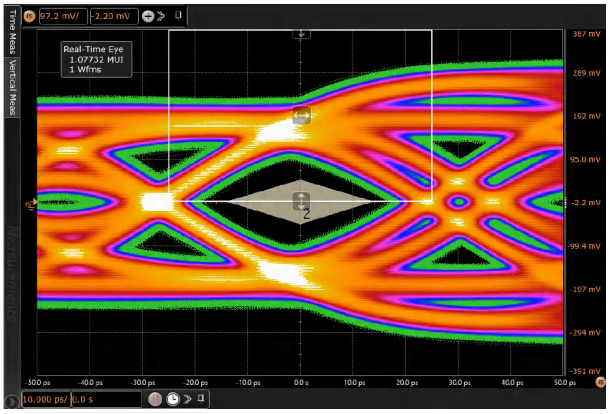



**Figure 7-6. DP 2.1 Tx Compliance Eye Diagram at TP3_EQ With TDP2004-Q1 for Signal Conditioning**

### *7.2.2 USB-C Cross Point Mux with Signal Conditioner*

The TDP2004-Q1 is a linear redriver with integrated cross-point mux. The device can be used to account for USB Type-C plug orientation as well as providing signal conditioing for DisplayPort mainlink signals. The TDP2004-Q1 can be used in both source and sink applications as illustrated in Figure 7-7. Using the SEL pin, typically driven by a USB PD controller in a system, the 4 channel signal paths can be configured as straight connection or cross connections as illustrated.

**Note**

The TDP2004-Q1 can only be used in USB-C applications where USB superspeed pins are used for DP alternate mode and USB3.x functionality is not required.

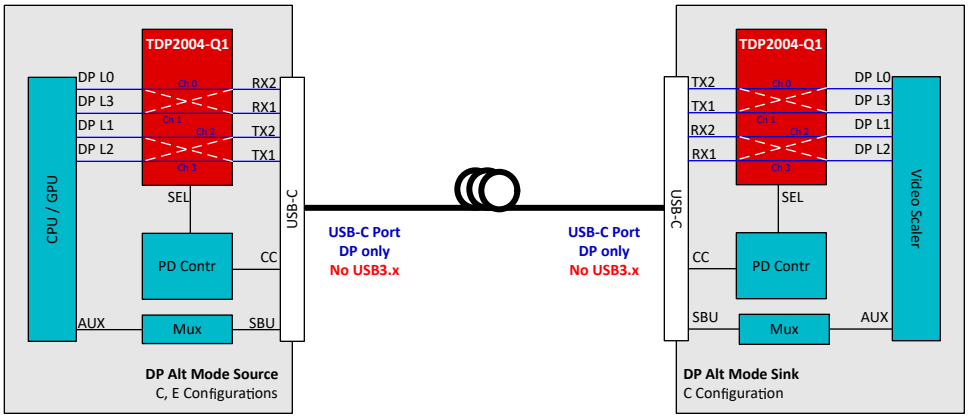



**Figure 7-7. USB-C Application**

## 7.3 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply must be designed to provide the operating conditions outlined in the recommended operating conditions section in terms of DC voltage, AC noise, and start-up ramp time.
2. The TDP2004-Q1 does not require any special power supply filtering, such as ferrite beads, provided that the recommended operating conditions are met. Only standard supply decoupling is required. Typical supply decoupling consists of a 0.1µF capacitor per VCC pin, one 1.0µF bulk capacitor per device, and one 10µF bulk capacitor per power bus that delivers power to one or more TDP2004-Q1 devices. The local decoupling (0.1µF) capacitors must be connected as close to the VCC pins as possible and with minimal path to the TDP2004-Q1 ground pad.

## 7.4 Layout

### *7.4.1 Layout Guidelines*

Refer to following guidelines when designing the layout of the system implementation:

1. Place the decoupling capacitors as close to the VCC pins as possible. Placing the decoupling capacitors directly underneath the device is recommended if the board design permits.
2. Make sure the high-speed differential signals TXnP/TXnN and RXnP/RXnN are tightly coupled, skew matched, and impedance controlled.
3. Avoid vias when possible on the high-speed differential signals. When vias must be used, take care to minimize the via stub, either by transitioning through most or all layers or by back drilling.
4. GND relief can be used (but is not required) beneath the high-speed differential signal pads to improve signal integrity by counteracting the pad capacitance.
5. Place GND vias directly beneath the device connecting the GND plane attached to the device to the GND planes on other layers. This has the added benefit of improving thermal conductivity from the device to the board.
6. Refer to land pattern example in the mechanical drawing section for the device thermal pad design recommendation.

### 7.4.2 Layout Example

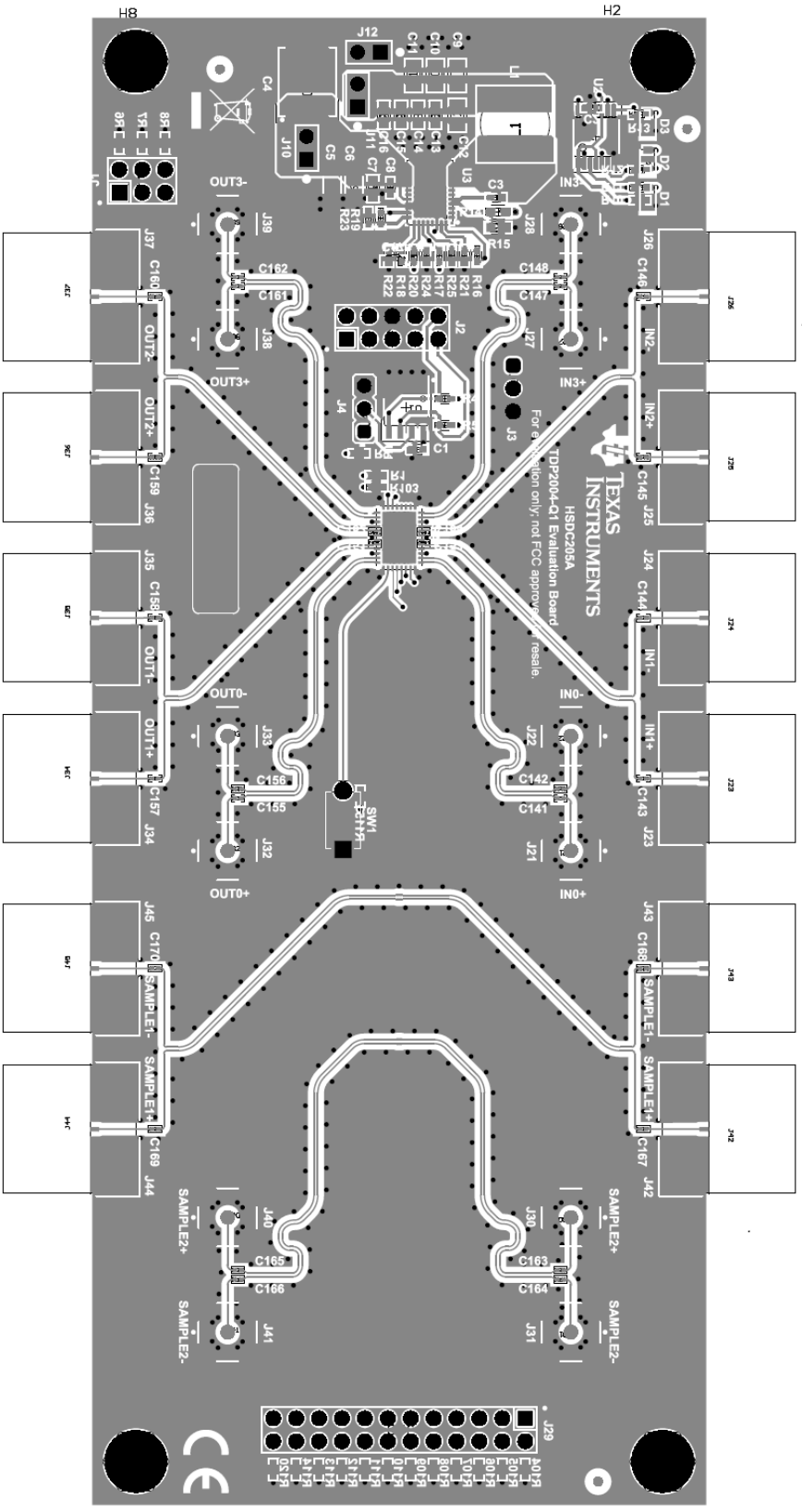



**Figure 7-8. TDP2004-Q1 Layout Example – Sub-Section of TI Evaluation Board**

# 8 Device and Documentation Support

## 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TDP2004RGFRQ1 | Active | Production | VQFN (RGF) \| 40 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TDP04Q1 |
| TDP2004RGFTQ1 | Active | Production | VQFN (RGF) \| 40 | 250 \| SMALL T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | TDP04Q1 |

**(1) Status:** For more details on status, see our product life cycle.

**(2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.



**OTHER QUALIFIED VERSIONS OF TDP2004-Q1 :**

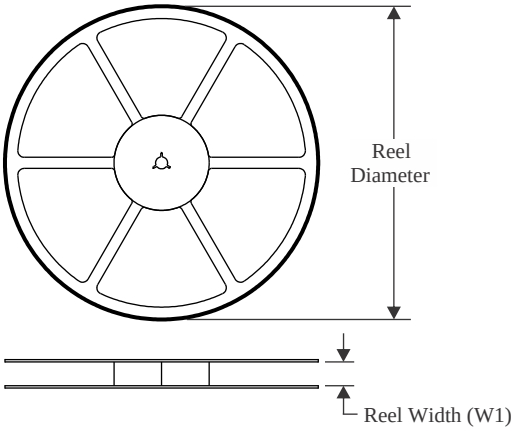
- Catalog : TDP2004

NOTE: Qualified Version Definitions:

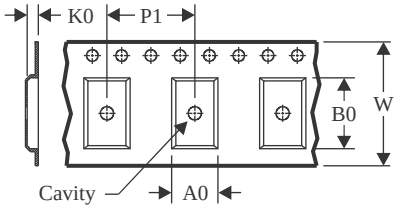
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

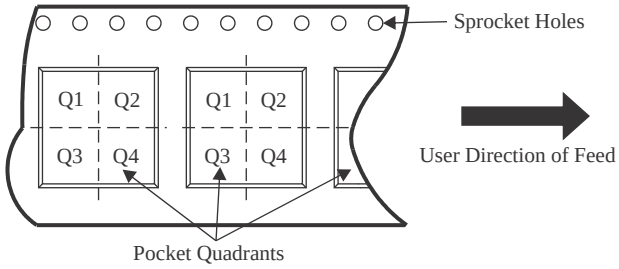



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

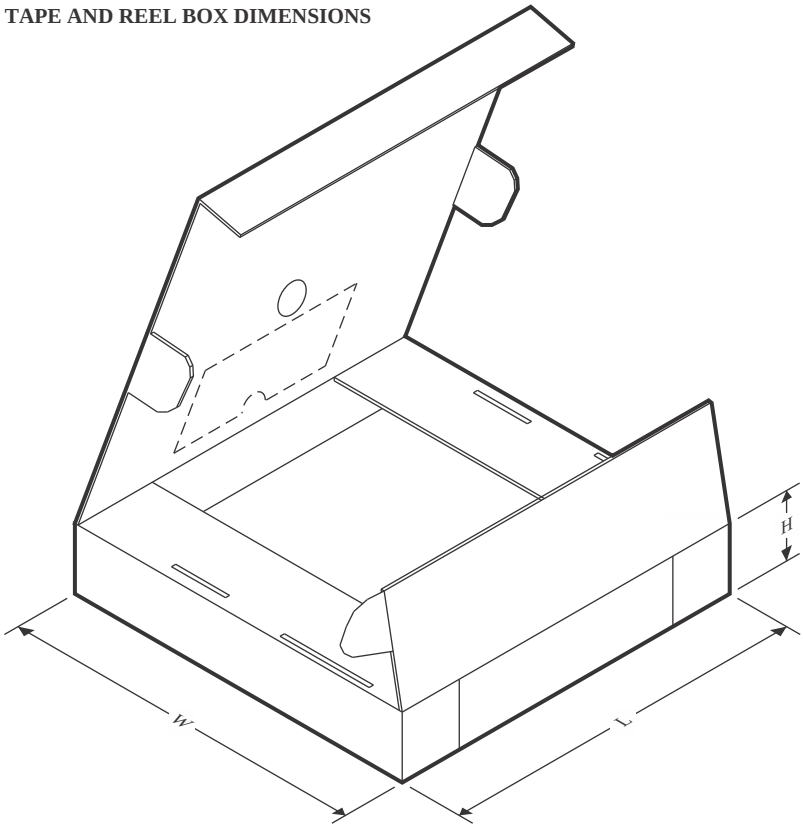
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TDP2004RGFRQ1 | VQFN | RGF | 40 | 3000 | 330.0 | 16.4 | 5.25 | 7.25 | 1.45 | 8.0 | 16.0 | Q1 |
| TDP2004RGFTQ1 | VQFN | RGF | 40 | 250 | 180.0 | 16.4 | 5.25 | 7.25 | 1.45 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TDP2004RGFRQ1 | VQFN | RGF | 40 | 3000 | 367.0 | 367.0 | 35.0 |
| TDP2004RGFTQ1 | VQFN | RGF | 40 | 250 | 210.0 | 185.0 | 35.0 |

# GENERIC PACKAGE VIEW

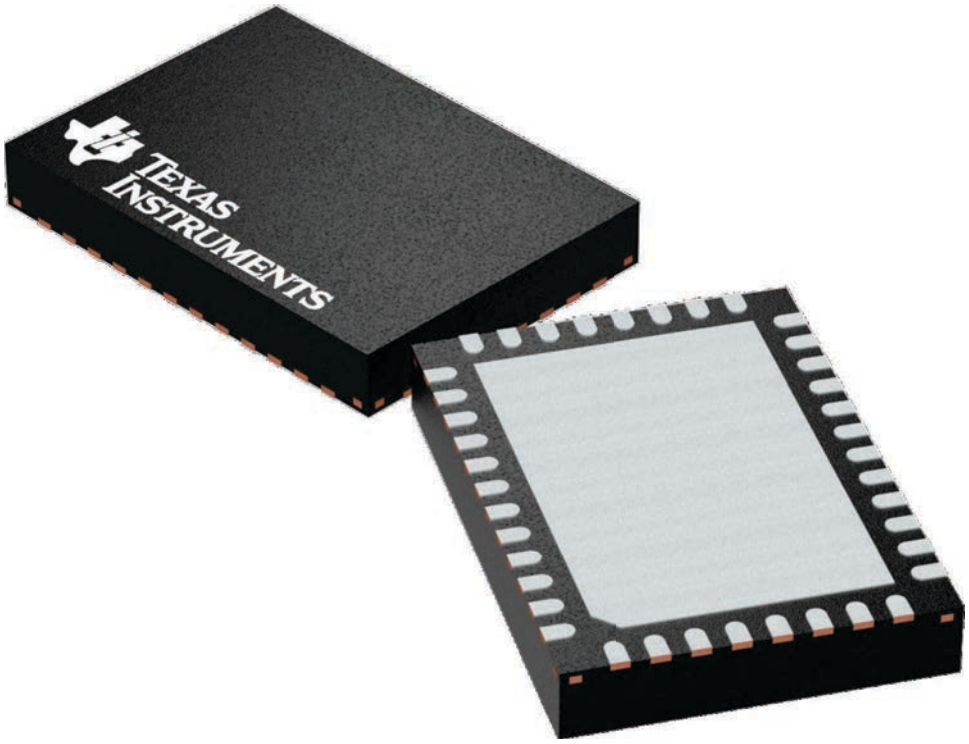
## RGF 40

## VQFN - 1 mm max height

**5 x 7, 0.5 mm pitch**

PLASTIC QUAD FLAT PACK- NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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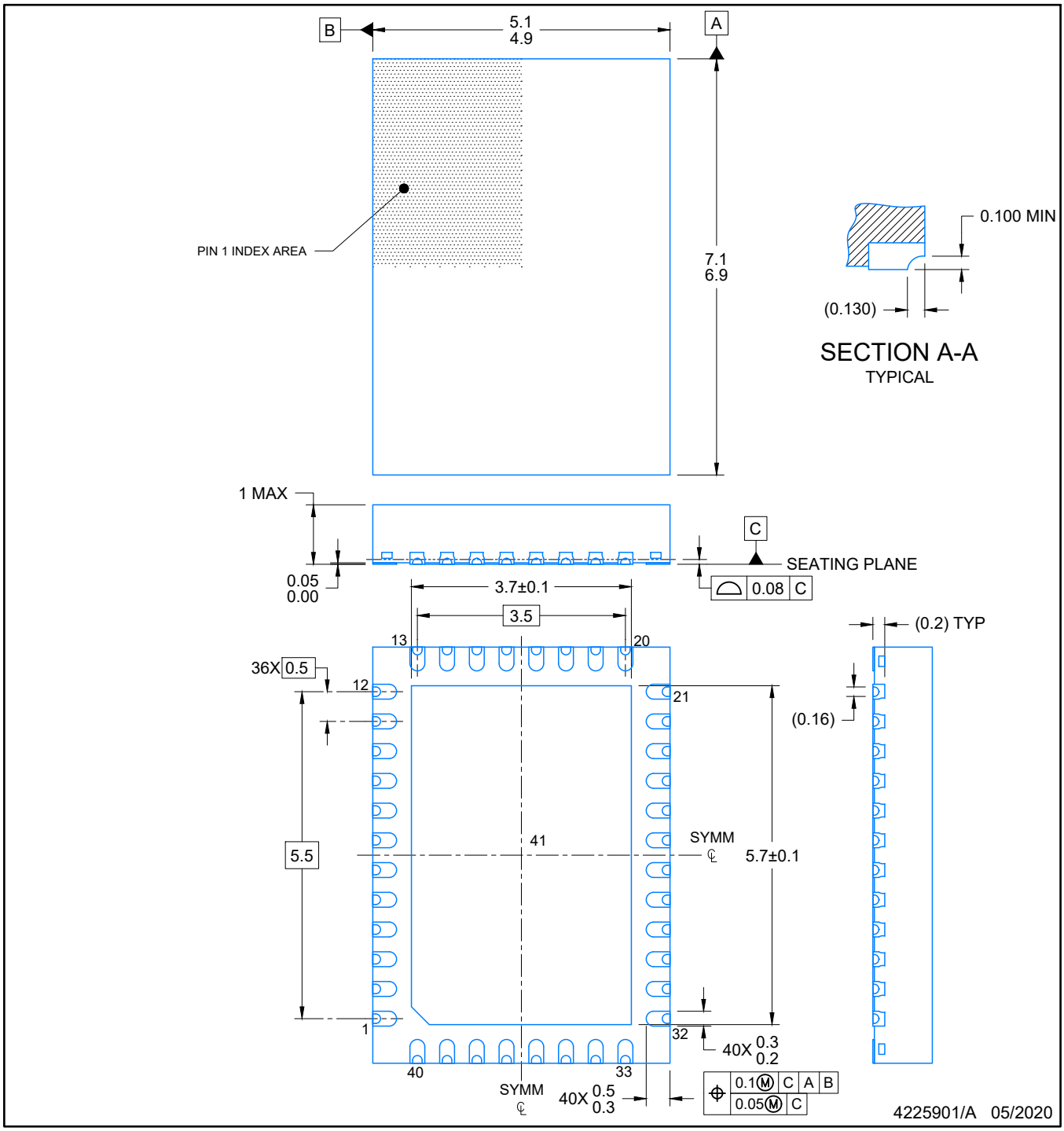
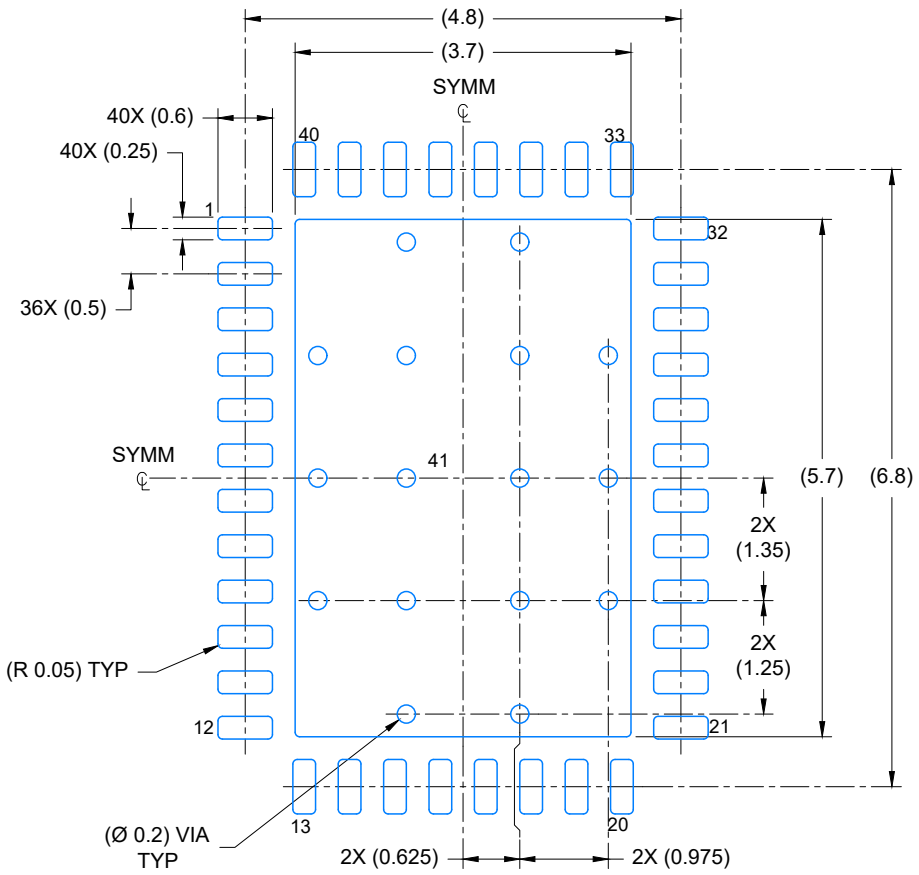
PLASTIC QUAD FLATPACK- NO LEAD

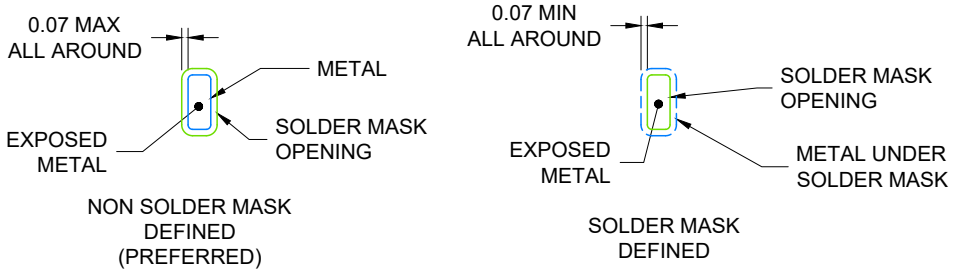



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

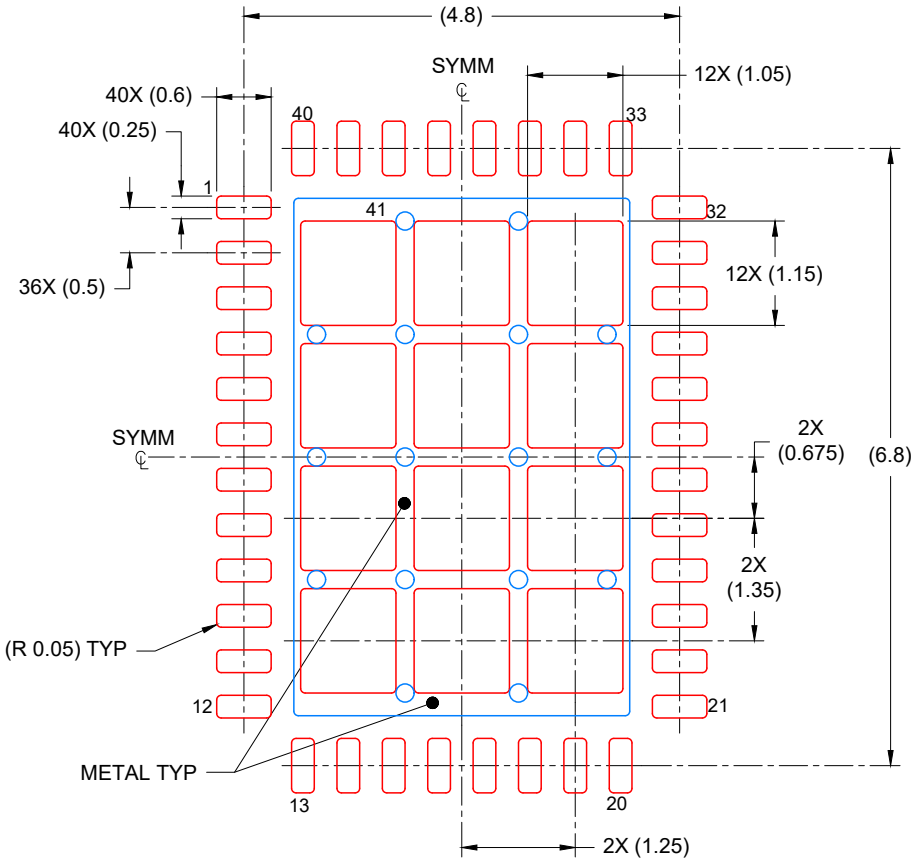



SOLDER MASK DETAILS

4225901/A 05/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
69% PRINTED COVERAGE BY AREA
SCALE: 12X

4225901/A 05/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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