RAD-TOLERANT CLASS V, WIDEBAND, FULLY DIFFERENTIAL AMPLIFIER

FEATURES

- **Fully Differential Architecture**
- **Common-Mode Input Range Includes Negative Rail**
- **Minimum Gain of 2 V/V (6 dB)**
- **Bandwidth: 1.1 GHz (Gain = 6 dB)**
- **Slew Rate: 5100 V/µs**
- **1% Settling Time: 5.5 ns**
- **HD_2: –76 dBc at 70 MHz**
- **HD_3: –88 dBc at 70 MHz**
- **OIP_2: 84 dBm at 70 MHz**
- **OIP_3: 42 dBm at 70 MHz**
- **Input Voltage Noise: 2 nV/$\sqrt{Hz}$ (f > 10 MHz)**
- **Noise Figure: 21.8 dB (50 Ω System, G = 6 dB)**
- **Output Common-Mode Control**
- **5 V Power Supply Current: 39.2 mA**
- **Power-Down Capability: 0.65 mA**
- **Rad-Tolerant: 150 kRad (Si) TID**
- **QML-V Qualified, SMD 5962-07222**

APPLICATIONS

- **5 V Data-Acquisition Systems**
- **High Linearity ADC Amplifier**
- **Wireless Communication**
- **Medical Imaging**
- **Test and Measurement**

RELATED PRODUCTS

DEVICE	MINIMUM GAIN	COMMON-MODE RANGE OF INPUT(1)
THS4511-SP	6 dB	–0.3 V to 2.3 V
THS4513-SP	6 dB	0.75 V to 4.25 V

(1) Assumes a 5 V single-ended power supply

DESCRIPTION/ORDERING INFORMATION

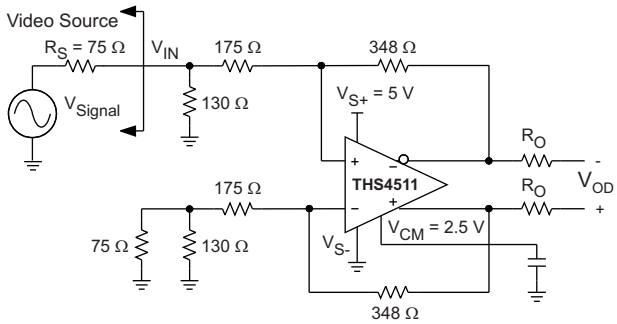
The THS4511 is a fully differential operational amplifier designed for single-supply 5 V data-acquisition systems. It has very low noise at 2 nV/$\sqrt{Hz}$, and extremely low harmonic distortion of –76 dBc HD_2 and –88 dBc HD_3 at 70 MHz with 2 Vpp, G = 14 dB, and 100 Ω load. Slew rate is very high at 5100 V/µs and with settling time of 5.5 ns to 1% (2 V step) it is ideal for pulsed applications. It is designed for minimum gain of 6 dB.

To allow for dc coupling to ADCs, its unique output common-mode control circuit maintains the output common-mode voltage within 5 mV offset (typical) from the set voltage, when set within ±0.5 V of mid-supply. The common-mode set point is set to mid-supply by internal circuitry, which may be over-driven from an external source.

The THS4511 is a high-performance amplifier that has been optimized for use in 5 V single-supply data acquisition systems. The output has been optimized for best performance with its common-mode voltages set to mid-supply, and the input has been optimized for performance over a wide range of common-mode input voltages. High performance at a low power-supply voltage enables single-supply 5 V data-acquisition systems while minimizing component count.

The THS4511 is offered in a 16-pin ceramic flatpack package (W), and is characterized for operation over the full military temperature range from –55°C to 125°C.

Video Buffer, Single Ended to Differential



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION(1)

TEMPERATURE	PACKAGED DEVICES	
	CERAMIC FLATPACK W (16)(2)	SYMBOL
–55°C to 125°C	5962-0722201VFA	5962-0722201VFA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			UNIT
$V_{S–}$ to V_{S+}	Supply voltage		6 V
V_I	Input voltage		$\pm V_S$
V_{ID}	Differential input voltage		4 V
I_O	Output current		200 mA
	Continuous power dissipation		See Dissipation Rating Table
T_J	Maximum junction temperature(2)		150°C
T_A	Operating free-air temperature range		–55°C to 125°C
T_{stg}	Storage temperature range		–65°C to 150°C
	ESD ratings	HBM	2000 V
		CDM	1500 V
		MM	100 V

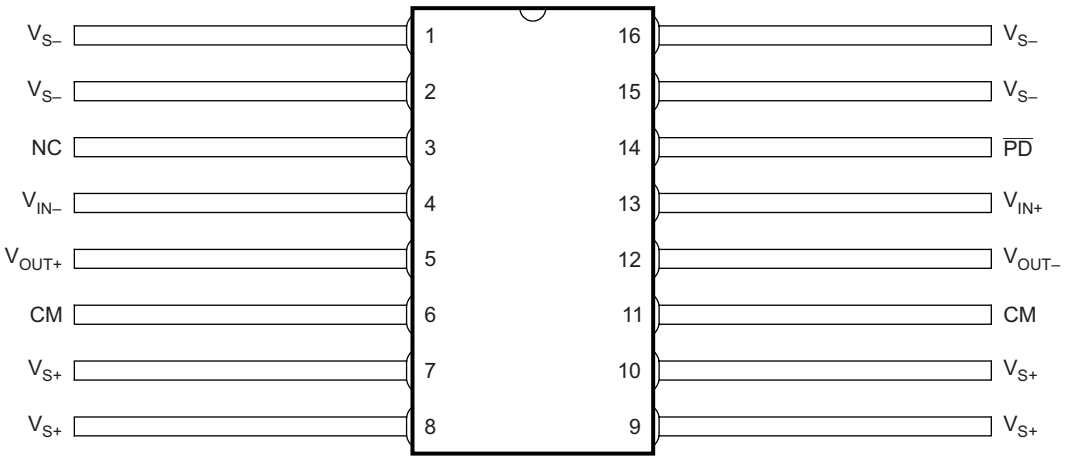
(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The absolute maximum temperature under any condition is limited by the constraints of the silicon process.

DISSIPATION RATINGS TABLE

PACKAGE	θ_{JC}	θ_{JA}	POWER RATING	
			$T_A \le 25°C$	$T_A = 125°C$
W (16)	14.7°C/W	189°C/W	661 mW	132 mW

DEVICE INFORMATION

W PACKAGE
TOP VIEW



TERMINAL FUNCTIONS

TERMINAL (W PACKAGE)		DESCRIPTION
NO.	NAME	
3	NC	No internal connection
4	V_{IN-}	Inverting amplifier input
5	V_{OUT+}	Non-inverting amplifier output
6, 11	CM	Common-mode voltage input
7, 8, 9, 10	V_{S+}	Positive amplifier power supply input
12	V_{OUT-}	Inverting amplifier output
13	V_{IN+}	Non-inverting amplifier input
14	$\overline{PD}$	Powerdown, $\overline{PD}$ = logic low puts part into low power mode, $\overline{PD}$ = logic high or open for normal operation
1, 2, 15, 16	V_{S-}	Negative amplifier power supply input

ELECTRICAL CHARACTERISTICS; $V_{S+} - V_{S-} = 5$ V (Unchanged after 150 kRad):

Test conditions unless otherwise noted: $V_{S+} = 5$ V, $V_{S-} = 0$ V, G = 14 dB, CM = open, $V_{OD} = 2$ Vpp, $R_F = 348\ \Omega$, $R_L = 200\ \Omega$ Differential, $T_A = 25°C$, Single-Ended Input, Differential Output, Input Referenced to Ground, and Output Referenced to Mid-Supply

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
AC PERFORMANCE						
Small-Signal Bandwidth	G = 6 dB, V_O = 100 mVpp			1.1		GHz
	G = 10 dB, V_O = 100 mVpp			1.0		
	G = 14 dB, V_O = 100 mVpp			720		MHz
Gain-Bandwidth Product	G = 10 dB			3		GHz
Bandwidth for 0.1 dB flatness	G = 10 dB, V_O = 2 Vpp			65		MHz
	G = 14 dB, V_O = 2 Vpp			115		
Large-Signal Bandwidth	G = 6 dB, V_O = 2 Vpp			1.1		GHz
Slew Rate (Differential)	V_O = 2 V Step			5100		V/µs
Rise Time				0.5		ns
Fall Time				0.5		ns
Settling Time to 1%				5.5		ns
2nd Order Harmonic Distortion	f = 10 MHz, R_L = 100 Ω			–106		
	f = 50 MHz, R_L = 100 Ω			–90		dBc
	f = 100 MHz, R_L = 100 Ω			–87		
3rd Order Harmonic Distortion	f = 10 MHz, R_L = 100 Ω			–108		
	f = 50 MHz, R_L = 100 Ω			–106		
	f = 100 MHz, R_L = 100 Ω			–83		
2nd Order Intermodulation Distortion	200 kHz tone spacing, R_L = 100 Ω	f_C = 50 MHz		–83		dBc
		f_C = 100 MHz		–75		
3rd Order Intermodulation Distortion		f_C = 50 MHz		–83		
		f_C = 100 MHz		–74		
2nd Order Output Intercept Point	200 kHz tone spacing, R_L = 100 Ω	f_C = 50 MHz		84		dBm
		f_C = 100 MHz		77		
3rd Order Output Intercept Point		f_C = 50 MHz		42		
		f_C = 100 MHz		38		
Noise Figure	50 Ω system, 10 MHz			21.8		dB
Input Voltage Noise	f > 10 MHz			2		nV/√Hz
Input Current Noise	f > 10 MHz			1.5		pA/√Hz
DC PERFORMANCE						
Open-Loop Voltage Gain (A_{OL})				63		dB
Input Offset Voltage	T_A = 25°C			1	4	mV
	T_A = –55°C to 125°C				5.5	
Average Offset Voltage Drift				2.3		µV/°C
Input Bias Current	T_A = 25°C			8	15.5	µA
	T_A = –55°C to 125°C				20	
Average Bias Current Drift				20		nA/°C
Input Offset Current	T_A = 25°C			0.5	3.6	µA
	T_A = –55°C to 125°C				7	
Average Offset Current Drift				7		nA/°C

ELECTRICAL CHARACTERISTICS; $V_{S+} - V_{S-} = 5$ V (Unchanged after 150 kRad): (continued)

Test conditions unless otherwise noted: $V_{S+} = 5$ V, $V_{S-} = 0$ V, G = 14 dB, CM = open, $V_{OD} = 2$ Vpp, $R_F = 348\ \Omega$, $R_L = 200\ \Omega$ Differential, $T_A = 25°C$, Single-Ended Input, Differential Output, Input Referenced to Ground, and Output Referenced to Mid-Supply

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
INPUT						
Common-Mode Input Range High				2.3		V
Common-Mode Input Range Low				–0.3		
Common-Mode Rejection Ratio				80		dB
Differential Input Impedance				18.2 || 0.5		MΩ || pF
Common-Mode Input Impedance				4.0 || 1.5		
OUTPUT						
Maximum Output Voltage High	Each output with 100 Ω to mid-supply	$T_A = 25°C$	3.7	3.8		V
		$T_A = –55°C$ to 125°C	3.5			
Minimum Output Voltage Low		$T_A = 25°C$		1.2	1.3	
		$T_A = –55°C$ to 125°C			1.5	
Differential Output Voltage Swing	$T_A = 25°C$		4.8	5.2		V
	$T_A = –55°C$ to 125°C		4.0			
Differential Output Current Drive	$R_L = 10\ \Omega$			96		mA
Output Balance Error	$V_O = 100$ mV, f = 1 MHz			–52		dB
Closed-Loop Output Impedance	f = 1 MHz			0.3		Ω
OUTPUT COMMON-MODE VOLTAGE CONTROL						
Small-Signal Bandwidth				250		MHz
Slew Rate				110		V/µs
Gain				1		V/V
Output Common-Mode Offset from CM input	1.5 V < CM < 3.5 V			5		mV
CM Input Bias Current	1.5 V < CM < 3.5 V			±40		µA
CM Input Voltage Range				1.25 to 3.75		V
CM Input Impedance				32 || 2.8		kΩ || pF
CM Default Voltage	CM pins floating			2.5		V
POWER SUPPLY						
Specified Operating Voltage			3.75(1)	5	5.25	V
Maximum Quiescent Current	$T_A = 25°C$			39.2	42.5	mA
	$T_A = –55°C$ to 125°C				44	
Minimum Quiescent Current	$T_A = 25°C$		35.9	39.2		
	$T_A = –55°C$ to 125°C		34			
Power Supply Rejection (±PSRR)	To differential output			90		dB
POWER DOWN	Referenced to V_{S-}					
Enable Voltage Threshold	Device assured *on* above 2.1 V			> 2.1		V
Disable Voltage Threshold	Device assured *off* below 0.7 V			< 0.7		
Powerdown Quiescent Current	$T_A = 25°C$			0.65	0.9	mA
	$T_A = –55°C$ to 125°C				1.2	
Input Bias Current	$\overline{PD} = V_{S-}$			100		µA
Input Impedance				50 || 2		kΩ || pF
Turn-On Time Delay	Measured to output on			55		ns
Turn-Off Time Delay	Measured to output off			10		µs

(1) See the *Application Information* section of this data sheet for device operation with full supply voltages less than 5 V.

TYPICAL CHARACTERISTICS

TYPICAL AC PERFORMANCE: $V_{S+} - V_{S-} = 5$ V

Test conditions unless otherwise noted: $V_{S+} = 5$ V, $V_{S-} = 0$ V, G = 14 dB, CM = open, $V_{OD} = 2$ Vpp, $R_F = 348\ \Omega$, $R_L = 200\ \Omega$ Differential, Single-Ended Input, Input Referenced to Ground and Output Referenced to Mid-Rail

Small-Signal Frequency Response	G = 6 dB, $V_{OD} = 100\ mV_{PP}$		Figure 1
	G = 10 dB, $V_{OD} = 100\ mV_{PP}$		Figure 2
	G = 14 dB, $V_{OD} = 100\ mV_{PP}$		Figure 3
Large Signal Frequency Response	G = 6 dB, $V_{OD} = 2\ V_{PP}$		Figure 4
	G = 10 dB, $V_{OD} = 2\ V_{PP}$		Figure 5
	G = 14 dB, $V_{OD} = 2\ V_{PP}$		Figure 6
Harmonic Distortion	HD_2, G = 14 dB, $V_{OD} = 2\ V_{PP}$	vs Frequency	Figure 7
	HD_3, G = 14 dB, $V_{OD} = 2\ V_{PP}$	vs Frequency	Figure 8
	HD_2, G = 14 dB	vs Output Voltage	Figure 9
	HD_3, G = 14 dB	vs Output Voltage	Figure 10
Intermodulation Distortion	IMD_2, G = 14 dB	vs Frequency	Figure 11
	IMD_3, G = 14 dB	vs Frequency	Figure 12
Output Intercept Point	OIP_2	vs Frequency	Figure 13
	OIP_3	vs Frequency	Figure 14
Transition Rate		vs Output Voltage	Figure 15
Transient Response			Figure 16
Rejection Ratios		vs Frequency	Figure 17
Overdrive Recovery			Figure 18
Output Voltage Swing		vs Load Resistance	Figure 19
Turn-Off Time			Figure 20
Turn-On Time			Figure 21
Input Offset Voltage		vs Input Common-Mode Voltage	Figure 22
Input Referred Noise		vs Frequency	Figure 23
Noise Figure		vs Frequency	Figure 24
Quiescent Current		vs Supply Voltage	Figure 25
Output Balance Error		vs Frequency	Figure 26
CM Input Bias Current		vs CM Input Voltage	Figure 27
Differential Output Offset Voltage		vs CM Input Voltage	Figure 28
Output Common-Mode Offset		vs CM Input Voltage	Figure 29

SMALL-SIGNAL FREQUENCY RESPONSE

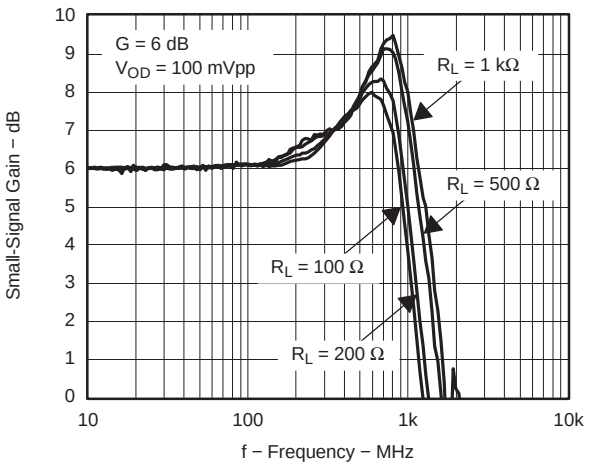


Figure 1.

SMALL-SIGNAL FREQUENCY RESPONSE

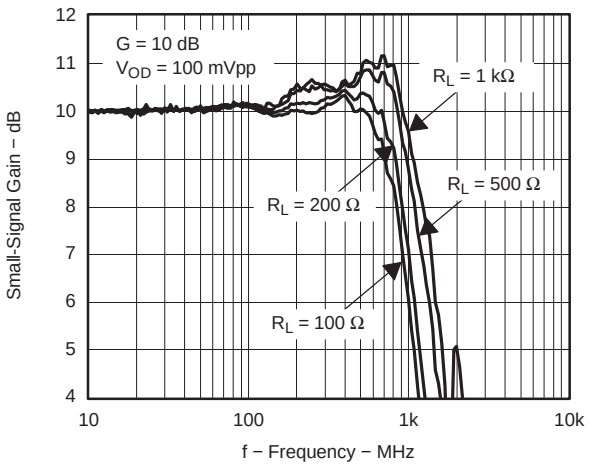


Figure 2.

SMALL-SIGNAL FREQUENCY RESPONSE

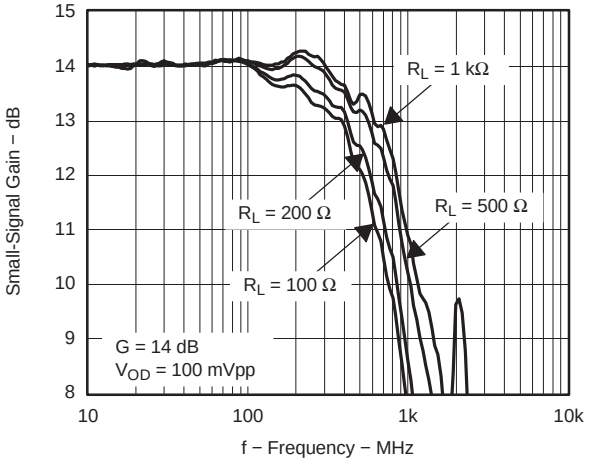


Figure 3.

LARGE-SIGNAL FREQUENCY RESPONSE

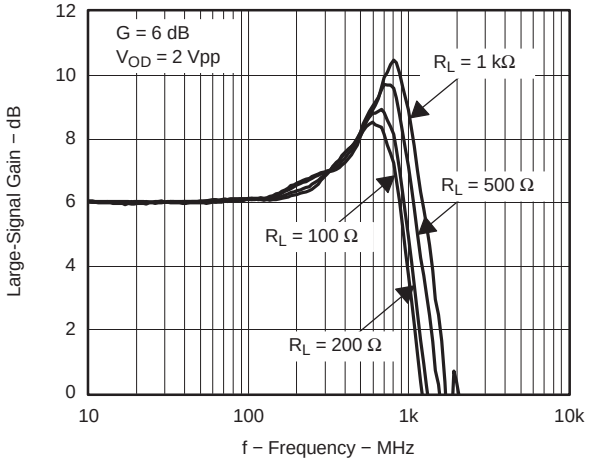


Figure 4.

LARGE-SIGNAL FREQUENCY RESPONSE

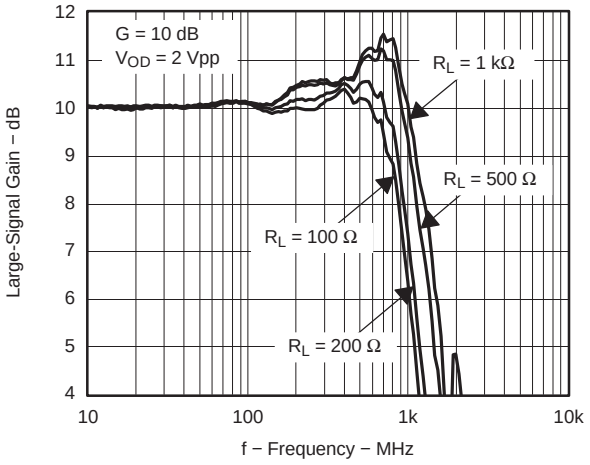


Figure 5.

LARGE-SIGNAL FREQUENCY RESPONSE

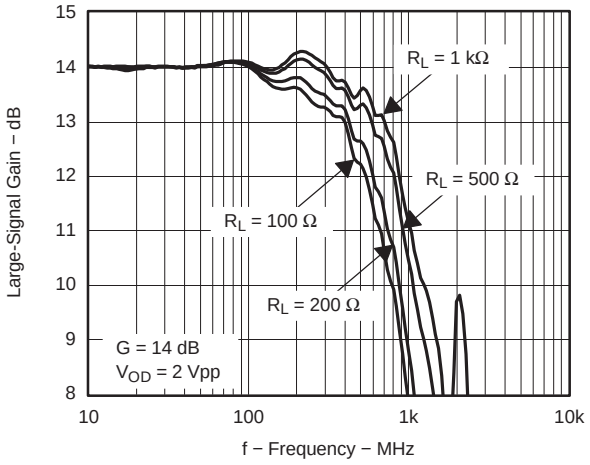


Figure 6.

HD$_2$ vs FREQUENCY

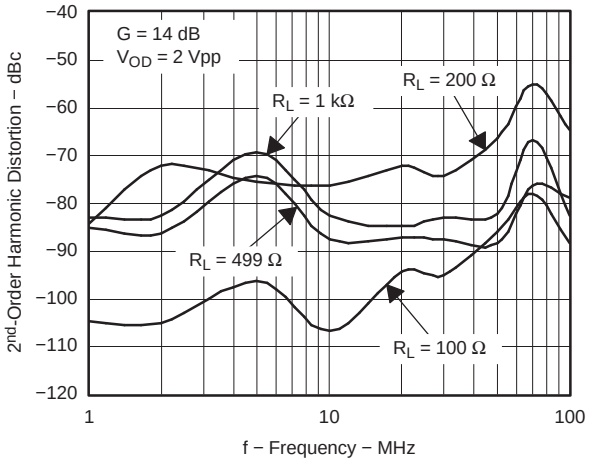


Figure 7.

HD$_3$ vs FREQUENCY

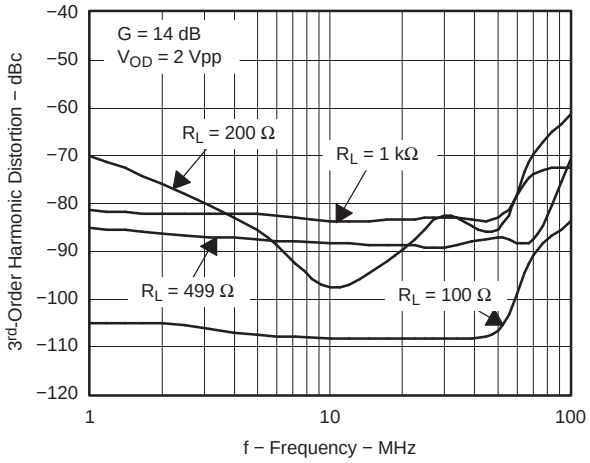


Figure 8.

HD$_2$ vs OUTPUT VOLTAGE

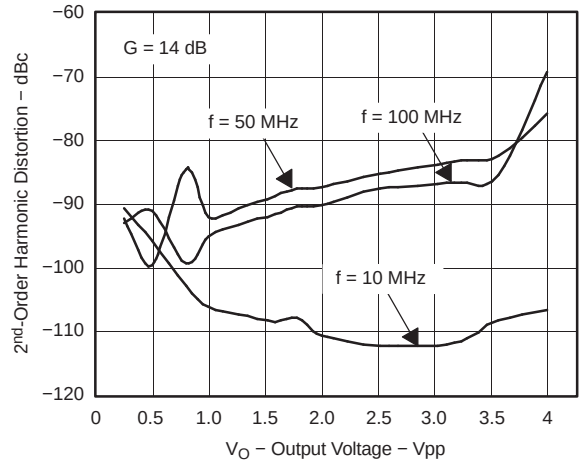


Figure 9.

HD$_3$ vs OUTPUT VOLTAGE

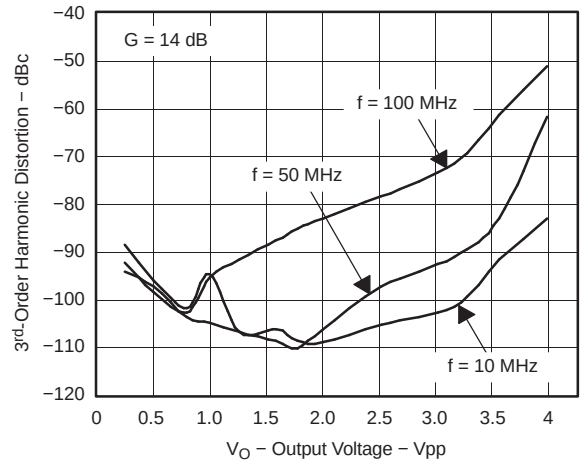


Figure 10.

IMD$_2$ vs FREQUENCY

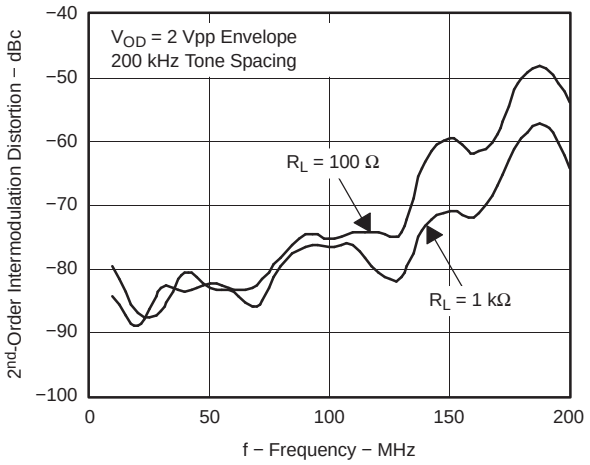


Figure 11.

IMD$_3$ vs FREQUENCY

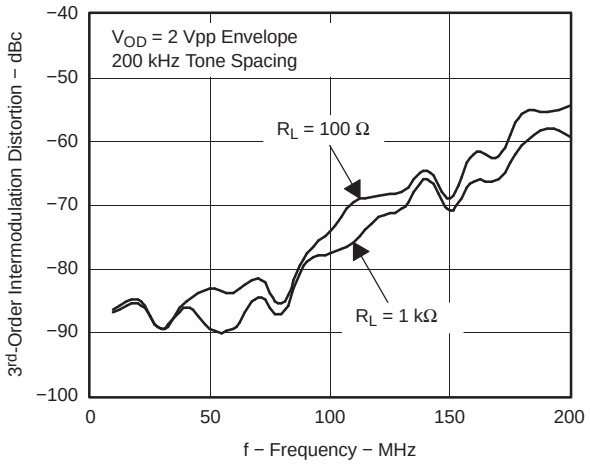


Figure 12.

OIP_2 vs FREQUENCY

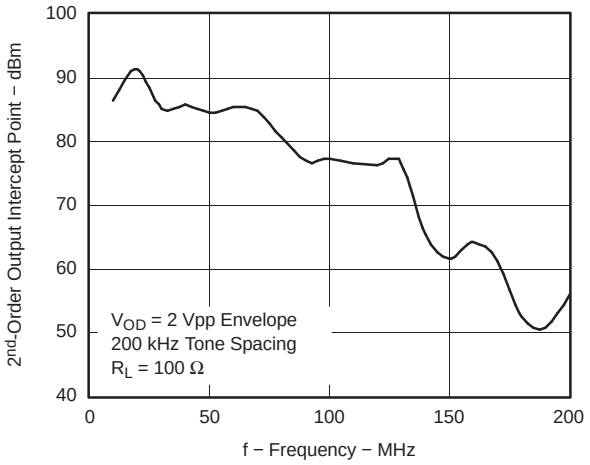


Figure 13.

OIP_3 vs FREQUENCY

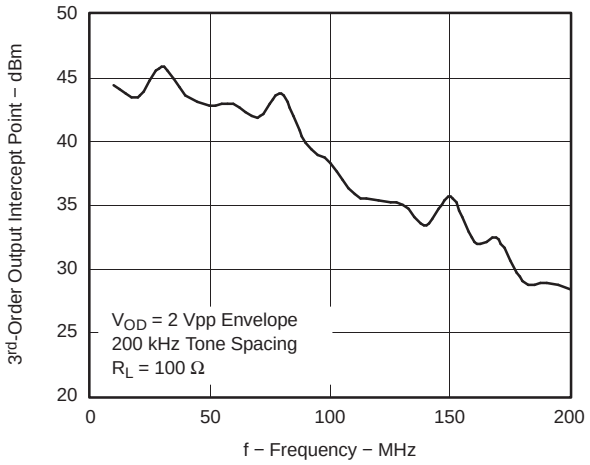


Figure 14.

TRANSITION RATE vs OUTPUT VOLTAGE

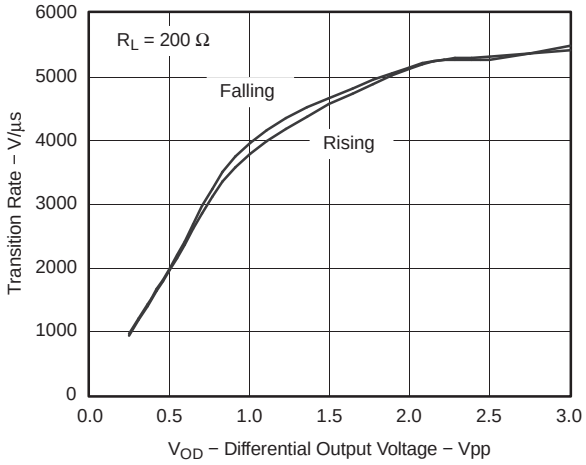


Figure 15.

TRANSIENT RESPONSE

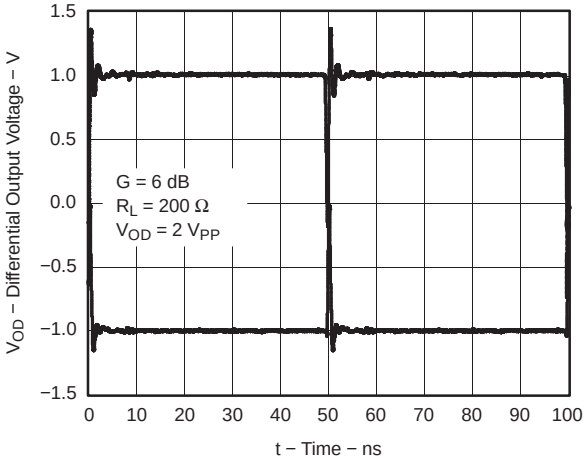


Figure 16.

REJECTION RATIOS vs FREQUENCY

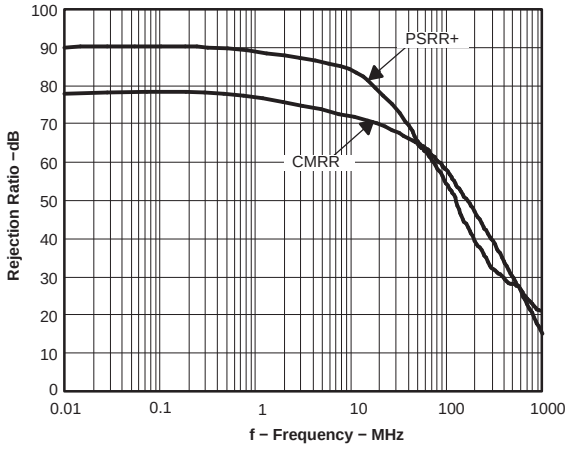


Figure 17.

OVERDRIVE RECOVERY

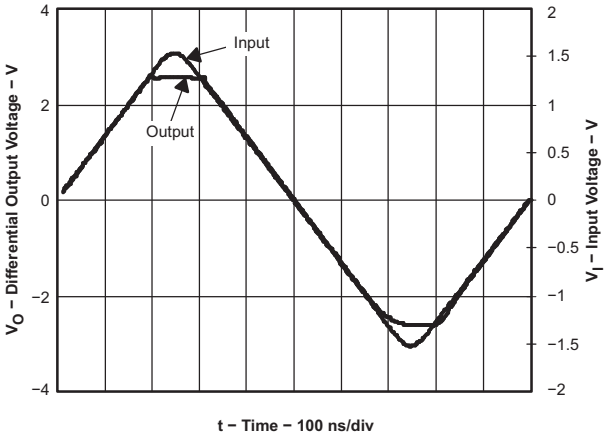


Figure 18.

OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

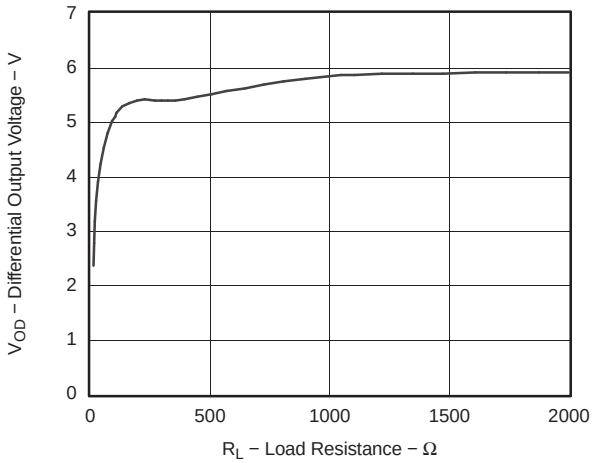


Figure 19.

TURN-OFF TIME

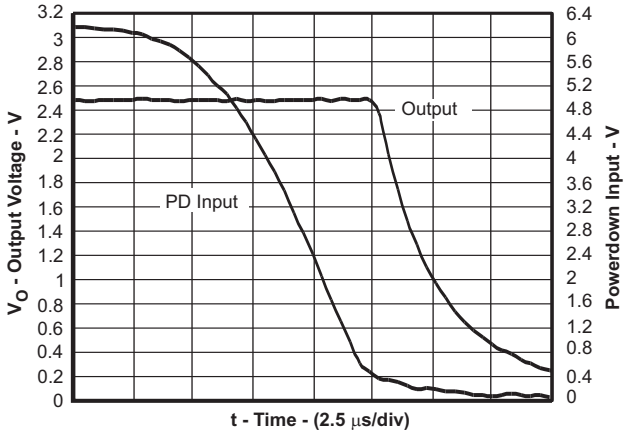


Figure 20.

TURN-ON TIME

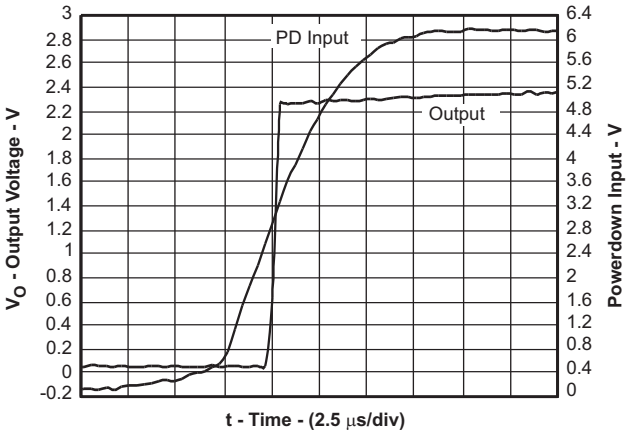


Figure 21.

INPUT OFFSET VOLTAGE vs INPUT COMMON-MODE VOLTAGE

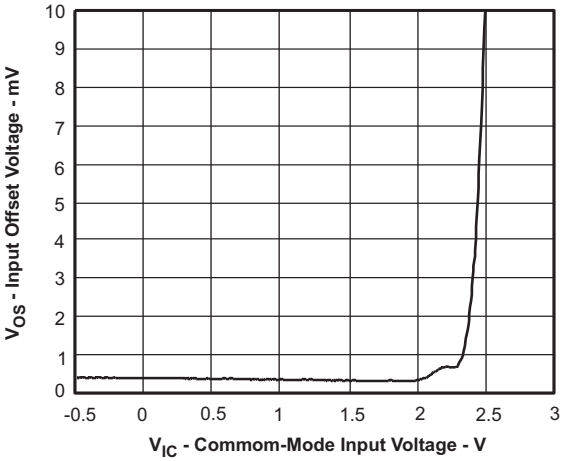


Figure 22.

INPUT REFERRED NOISE vs FREQUENCY

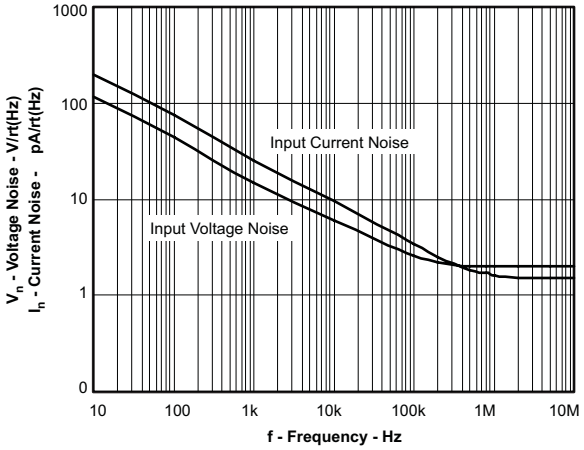


Figure 23.

NOISE FIGURE vs FREQUENCY

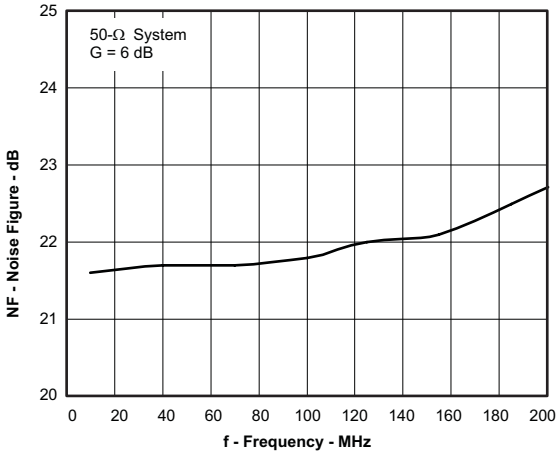


Figure 24.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

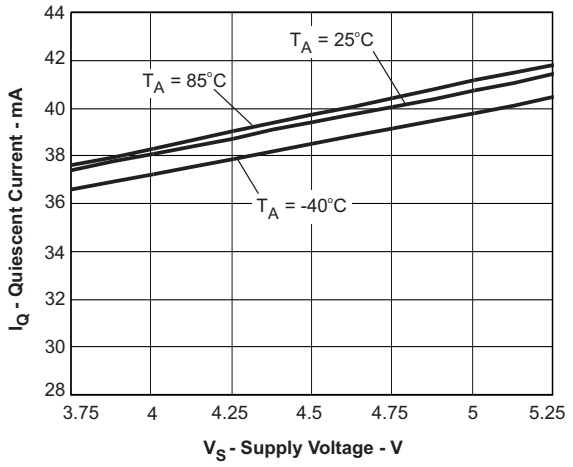


Figure 25.

OUTPUT BALANCE ERROR vs FREQUENCY

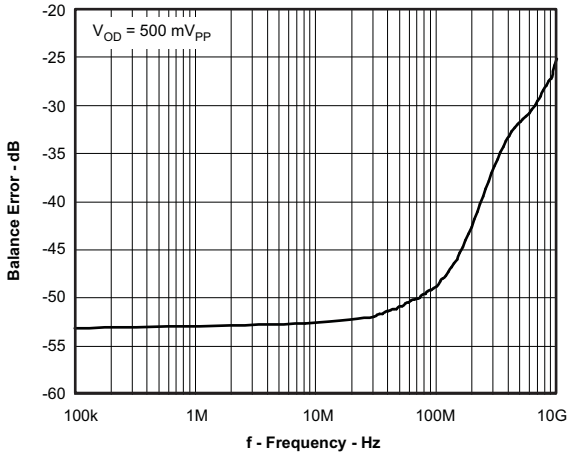


Figure 26.

CM INPUT BIAS CURRENT vs CM INPUT VOLTAGE

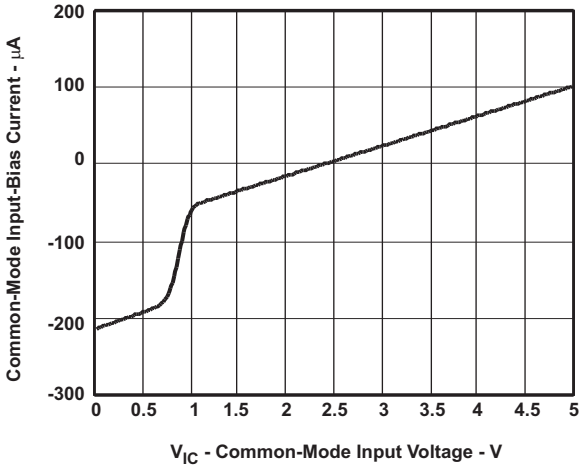


Figure 27.

DIFFERENTIAL OUTPUT OFFSET VOLTAGE vs CM INPUT VOLTAGE

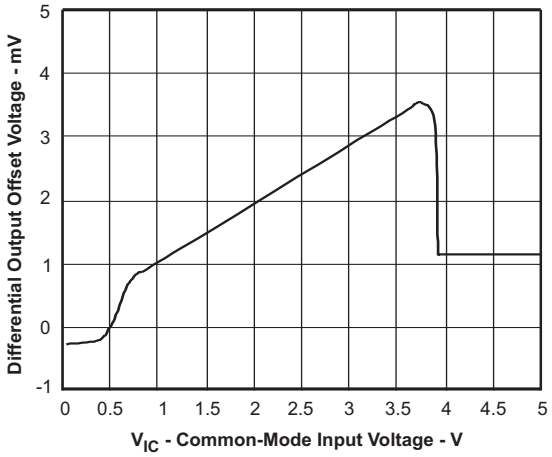


Figure 28.

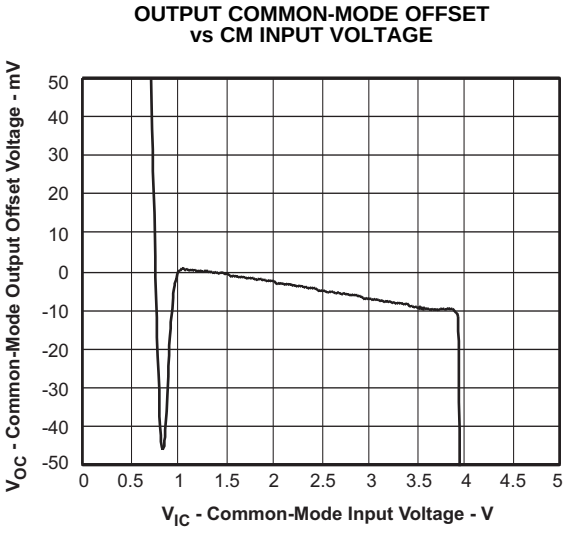


Figure 29.

TEST CIRCUITS

The THS4511 is tested with the following test circuits. For simplicity, the power supply decoupling is not shown – see the layout in the *application information* section for recommendations. Depending on the test conditions, component values are changed per the following tables, or as otherwise noted. The signal generators used are ac coupled 50 Ω sources, and a 0.22 µF capacitor and a 49.9 Ω resistor to ground are inserted across R_{IT} on the alternate input to balance the circuit.

Table 1. Gain Component Values

GAIN	R_F	R_G	R_{IT}
6 dB	348 Ω	165 Ω	61.9 Ω
10 dB	348 Ω	100 Ω	69.8 Ω
14 dB	348 Ω	56.2 Ω	88.7 Ω
20 dB	348 Ω	16.5 Ω	287 Ω

Note: The gain setting includes 50 Ω source impedance. Components are chosen to achieve gain and 50 Ω input termination.

Table 2. Load Component Values

R_L	R_O	R_{OT}	Atten
100 Ω	25 Ω	open	6 dB
200 Ω	86.6 Ω	69.8 Ω	16.8 dB
499 Ω	237 Ω	56.2 Ω	25.5 dB
1k Ω	487 Ω	52.3 Ω	31.8 dB

Note: The total load includes 50 Ω termination by the test equipment. Components are chosen to achieve load and 50 Ω line termination through a 1:1 transformer.

Due to the voltage divider on the output formed by the load component values, the amplifier's output is attenuated. The column *Atten* in Table 2 shows the attenuation expected from the resistor divider. When using a transformer at the output as shown in Figure 31, the signal will see slightly more loss, and these numbers will be approximate.

Frequency Response

The circuit shown in Figure 30 is used to measure the frequency response of the circuit.

A network analyzer is used as the signal source and as the measurement device. The output impedance of the network analyzer is 50 Ω. R_{IT} and R_G are chosen to impedance match to 50 Ω, and to maintain the proper gain. To balance the amplifier, a 0.22 µF capacitor and 49.9 Ω resistor to ground are inserted across R_{IT} on the alternate input.

The output is probed using a high-impedance differential probe across the 100 Ω resistor. The gain is referred to the amplifier output by adding back the 6 dB loss due to the voltage divider on the output.

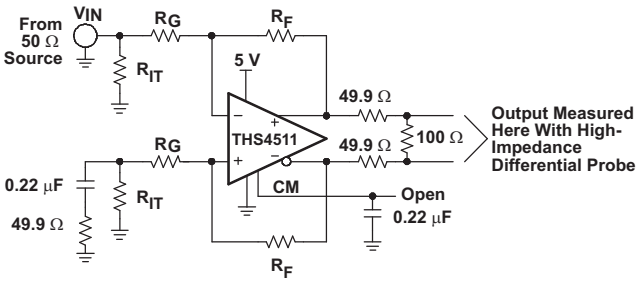


Figure 30. Frequency Response Test Circuit

Distortion

The circuit shown in Figure 31 is used to measure harmonic distortion and intermodulation distortion of the amplifier.

A signal generator is used as the signal source, and the output is measured with a spectrum analyzer. The output impedance of the signal generator is 50 Ω. R_{IT} and R_G are chosen to impedance-match to 50 Ω and to maintain the proper gain. To balance the amplifier, a 0.22 µF capacitor and 49.9 Ω resistor to ground are inserted across R_{IT} on the alternate input.

A low-pass filter is inserted in series with the input to reduce harmonics generated at the signal source. The level of the fundamental is measured, then a high-pass filter is inserted at the output to reduce the fundamental so that it does not generate distortion in the input of the spectrum analyzer.

The transformer used in the output to convert the signal from differential to single ended is an ADT1-1WT. It limits the frequency response of the circuit so that measurements cannot be made below approximately 1 MHz.

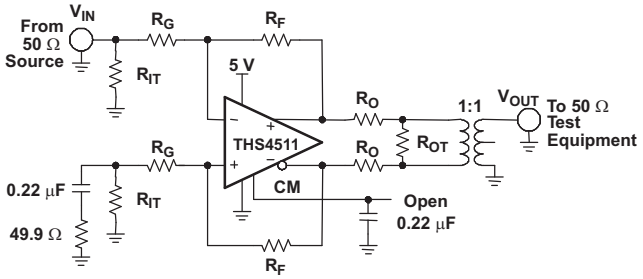


Figure 31. Distortion Test Circuit

Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive, Output Voltage,

and Turn-On/Off Time

The circuit shown in Figure 32 is used to measure slew rate, transient response, settling time, output impedance, overdrive recovery, output voltage swing, and turn-on/turn-off times of the amplifier. For output impedance, the signal is injected at V_{OUT} with V_{IN} left open, and the drop across the 49.9 Ω resistor is used to calculate the impedance seen looking into the amplifier's output.

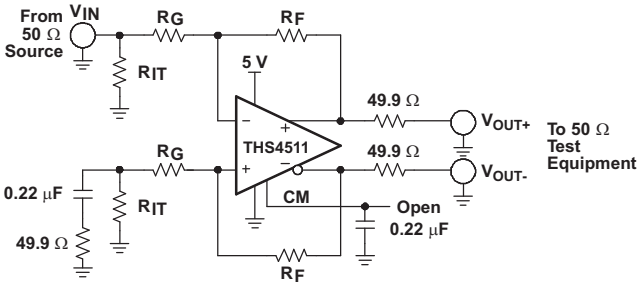


Figure 32. SR, Transient Response, Settling Time, Z_O, Overdrive Recovery, V_{OUT} Swing, and Turn-on/off Test Circuit

CM Input

The circuit shown in Figure 33 is used to measure the frequency response and input impedance of the CM input. Frequency response is measured single-ended at V_{OUT+} or $V_{OUT–}$ with the input injected at V_{IN}, R_{CM} = 0 Ω and R_{CMT} = 49.9 Ω. The input impedance is measured with R_{CM} = 49.9 Ω with R_{CMT} = open, and calculated by measuring the voltage drop across R_{CM} to determine the input current.

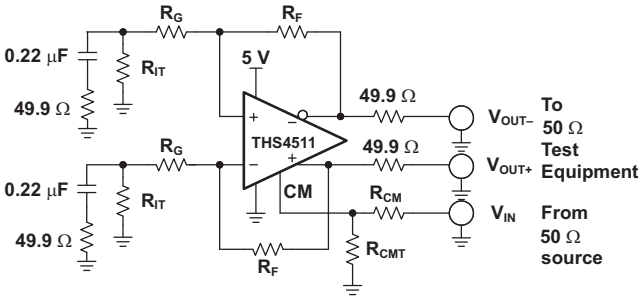


Figure 33. CM Input Test Circuit

CMRR and PSRR

The circuit shown in Figure 34 is used to measure the CMRR and PSRR of V_{S+} and $V_{S–}$. The input is switched appropriately to match the test being performed.

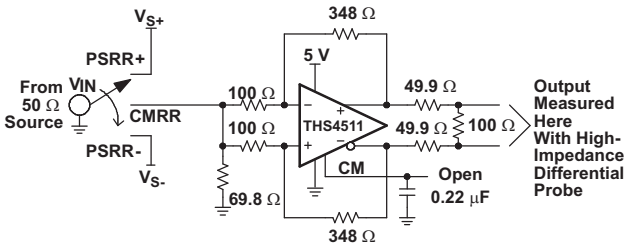


Figure 34. CMRR and PSRR Test Circuit

APPLICATION INFORMATION

APPLICATIONS

The following circuits show application information for the THS4511. For simplicity, power supply decoupling capacitors are not shown in these diagrams. For more detail on the use and operation of fully differential operational amplifiers, refer to application report *Fully-Differential Amplifiers* (SLOA054) .

Differential Input to Differential Output Amplifier

The THS4511 is a fully differential operational amplifier, and can be used to amplify differential input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 35 (CM input not shown). The gain of the circuit is set by R_F divided by R_G.

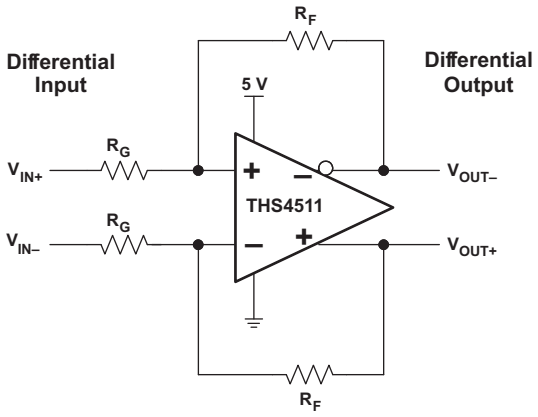


Figure 35. Differential Input to Differential Ouput Amplifier

Depending on the source and load, input and output termination can be accomplished by adding R_{IT} and R_O.

Single-Ended Input to Differential Output Amplifier

The THS4511 can be used to amplify and convert single-ended input signals to differential output signals. A basic block diagram of the circuit is shown in Figure 36 (CM input not shown). The gain of the circuit is again set by R_F divided by R_G.

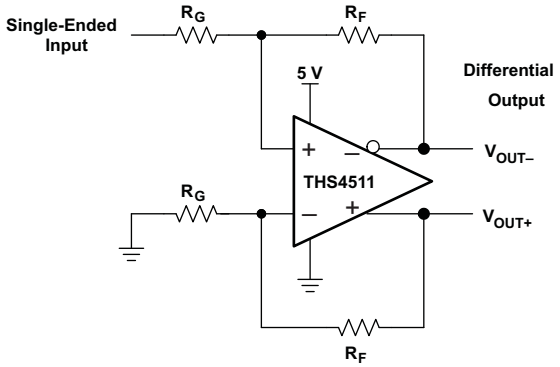


Figure 36. Single-Ended Input to Differential Output Amplifier

Input Common-Mode Voltage Range

The input common-mode voltage of a fully differential operational amplifier is the voltage at the (+) and (–) input pins of the operational amplifier.

It is important to not violate the input common-mode voltage range (V_{ICR}) of the operational amplifier. Assuming the operational amplifier is in linear operation, the voltage across the input pins is only a few millivolts at most. Finding the voltage at one input pin determines the input common-mode voltage of the operational amplifier.

Treating the negative input as a summing node, the voltage is given by Equation 1:

$$V_{IC} = \left(V_{OUT+} \times \frac{R_G}{R_G + R_F} \right) + \left(V_{IN-} \times \frac{R_F}{R_G + R_F} \right) \quad (1)$$

To determine the V_{ICR} of the operational amplifier, the voltage at the negative input is evaluated at the extremes of V_{OUT+}.

As the gain of the operational amplifier increases, the input common-mode voltage becomes closer and closer to the input common-mode voltage of the source.

Setting the Output Common-Mode Voltage

The output common-mode voltage is set by the voltage at the CM pin(s). The internal common-mode control circuit maintains the output common-mode voltage within 5 mV offset (typical) from the set voltage, when set within 0.5 V of mid-supply. If left unconnected, the common-mode set point is set to mid-supply by internal circuitry, which may be over-driven from an external source. Figure 37 is representative of the CM input. The internal CM circuit has about 700 MHz of –3 dB bandwidth, which is required for best performance, but it is intended to be a dc-bias input pin. Bypass capacitors are recommended on this pin to reduce noise at the output. The external current required to overdrive the internal resistor divider is given by Equation 2:

$$I_{EXT} = \frac{2V_{CM} - (V_{S+} - V_{S-})}{50\ k\Omega} \quad (2)$$

where V_{CM} is the voltage applied to the CM pin, and V_{S+} ranges from 3.75 V to 5 V, and V_{S-} is 0 V (ground).

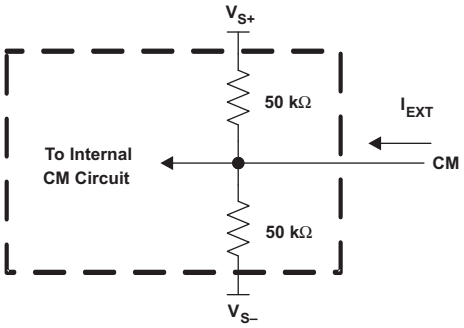


Figure 37. CM Input Circuit

Device Operation with Single Power Supplies Less than 5 V

The THS4511 is optimized to work in systems using 5 V single supplies, and the characterization data presented in this data sheet was taken with 5 V single-supply inputs. For ac-coupled systems or dc-coupled systems operating with supplies less than 5 V and greater than 3.75 V, the amplifier input common-mode range is maximized by adding pull-down resistors at the device inputs. The pull-down resistors provide additional loading at the input, and lower the common-mode voltage that is fed back into the device input through resistor R_F. Figure 38 shows the circuit configuration for this mode of operation where R_{PD} is added to the dc-coupled circuit to avoid violating the V_{ICR} of the operational amplifier. Note R_S and R_{IT} are added to the alternate input from the signal input to balance the amplifier. One resistor that is equal to the combined value $R_I = R_G + R_S||R_{IT}$ can be placed at the alternate input.

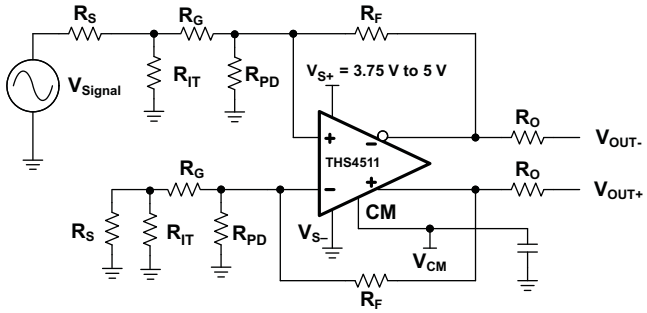


Figure 38. THS4511 DC Coupled Single-Source Supply Range From 3.75 V to 5 V With R_{PD} Used To Set V_{IC}

Note that in Figure 38, the source is referenced to ground as is the input termination resistor R_{IT}. The proper value of resistance to add can be calculated from Equation 3:

$$R_{PD} = \frac{1}{\frac{1}{R_F}\left[\frac{1.6}{\frac{V_{S+}}{2} - 1.6}\right] - \frac{1}{R_I}} \quad (3)$$

where $R_I = R_G + R_S||R_{IT}$.

V_{S+} is the power-supply voltage, R_F is the feedback resistance, R_G is the gain-setting resistance, R_S is the signal source resistance, and R_{IT} is the termination resistance.

Table 3 is a modification of Table 1 to add the proper values with R_{PD} assuming V_{S+} = 3.75 V, a dc-coupled 50 Ω source impedance, and setting the output common-mode voltage to mid-supply.

Table 3. R_{PD} Values for Various Gains, V_{S+} = 3.75 V, DC-coupled Signal Source

Gain	R_F	R_G	R_{IT}	R_{PD}
6 dB	348 Ω	169 Ω	64.9 Ω	80.6 Ω
10 dB	348 Ω	102 Ω	78.7 Ω	90.9 Ω
14 dB	348 Ω	61.9 Ω	115 Ω	90.9 Ω
20 dB	348 Ω	40.2 Ω	221 Ω	77.6 Ω

If the signal originates from an ac-coupled 50 Ω source (see Figure 39), the equivalent dc-source

resistance is an open circuit, and $R_I = R_G + R_{IT}$. Table 4 is a modification of Table 1 to add the proper values with R_{PD} assuming V_{S+} = 3.75 V, an ac-coupled 50 Ω source impedance, and setting the output common-mode voltage to mid-supply.

Table 4. R_{PD} Values for Various Gains, V_{S+} = 3.75 V, AC-Coupled Signal Source

Gain	R_F	R_G	R_{IT}	R_{PD}
6 dB	348 Ω	169 Ω	64.9 Ω	86.6 Ω
10 dB	348 Ω	102 Ω	78.7 Ω	110 Ω
14 dB	348 Ω	61.9 Ω	115 Ω	158 Ω
20 dB	348 Ω	40.2 Ω	221 Ω	226 Ω

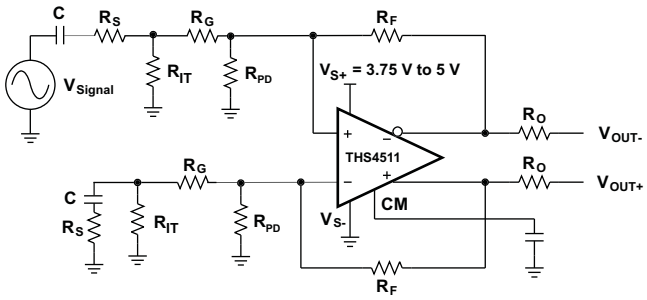


Figure 39. THS4511 AC Coupled Single-Source Supply Range From 3.75 V to 5 V With R_{PD} Used to Set V_{IC}

Video Buffer

Figure 40 shows a possible application of the THS4511 as a DC-coupled video buffer with a gain of 2. Figure 41 shows a plot of the Y' signal originating from a HDTV 720p video system. The input signal includes a tri-level sync (minimum level at –0.3 V) and the portion of a video signal with maximum amplitude of 0.7 V. Although the buffer draws its power from a 5 V single-ended power supply, internal level shifters allow the buffer to support input signals, which are as much as –0.3 V below ground. This allows maximum design flexibility while maintaining a minimum parts count. Figure 42 shows the differential output of the buffer. Note that the DC-coupled amplifier can introduce a DC offset on a signal applied at its input.

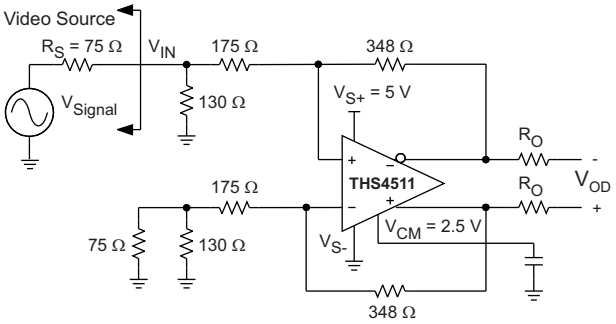


Figure 40. Single-Supply Video Buffer, Gain = 2

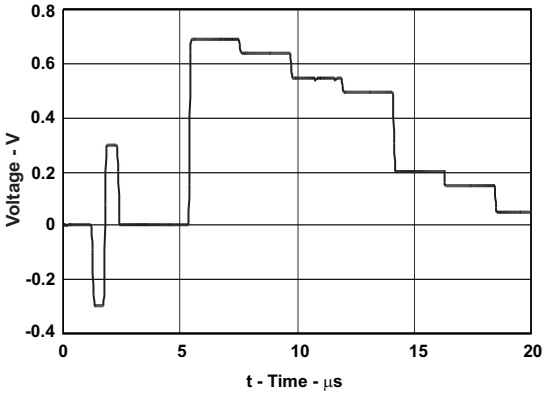


Figure 41. Y' Signal With 3-Level Sync and Video Signal

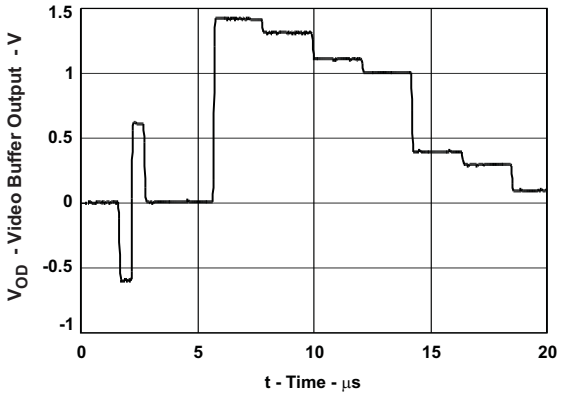


Figure 42. Video Buffer Differential Output Signal

THS4511 + ADS5500 Combined Performance

The THS4511 is designed to be a high-performance drive amplifier for high-performance data converters like the ADS5500 14 bit 125 MSPS ADC. Figure 43 shows a circuit combining the two devices. The THS4511 amplifier circuit provides 10 dB of gain and converts the single-ended input signal to a differential output signal. The default common-mode output of the THS4511 (2.5 V) is not compatible with the required common-mode input of the ADS5500 (1.55 V), so dc-blocking capicitors are added (0.22 µF). Note that a biasing circuit (not shown in Figure 43) is needed to provide the required common-mode, dc-input for the ADS5500. The 100 Ω resistors and 2.7 pF capacitor between the THS4511 outputs and ADS5500 inputs, along with the input capacitance of the ADS5500, limit the bandwidth of the signal to 115 MHz (–3 dB). For testing, a signal generator is used for the signal source. The generator is an ac-coupled 50 Ω source. A band-pass filter is inserted in series with the input to reduce harmonics and noise from the signal source. Input termination is accomplished via the 69.8 Ω resistor and 0.22 µF capacitor to ground in conjunction with the input impedance of the amplifier circuit. A 0.22 µF capacitor and 49.9 Ω resistor are inserted to ground across the 69.8 Ω resistor and 0.22 µF capacitor on the alternate input to balance the circuit. Gain is a function of the source impedance, termination, and 348 Ω feedback resistor. See Table 1 for component values to set proper 50 Ω termination for other common gains.

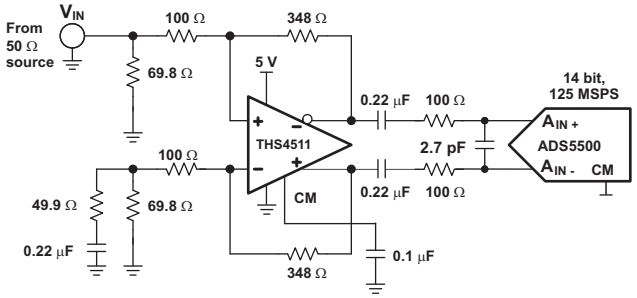


Figure 43. THS4511 + ADS5500 Circuit

THS4511 + ADS5424 Combined Performance

Figure 44 shows the THS4511 driving the ADS5424 ADC.

The THS4511 amplifier provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5424. Input termination and circuit testing is the same as described above for the THS4511 + ADS5500 circuit.

The 225 Ω resistors and 2.7 pF capacitor between the THS4511 outputs and ADS5424 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 100MHz (–3dB).

When the THS4511 is operated from a single power supply with V_{S+} = 5 V and V_{S-} = ground, the 2.5 V output common-mode voltage is compatable with the recommended value of the ADS5424 input common-mode voltage (2.4 V).

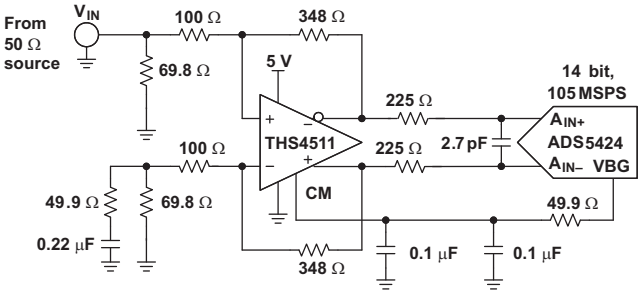


Figure 44. THS4511 + ADS5424 Circuit

Layout Recommendations

It is recommended to follow the layout of the external components near the amplifier, ground plane construction, and power routing of the EVM as closely as possible. General guidelines are:

1. Signal routing should be direct and as short as possible into and out of the operational amplifier circuit.
2. The feedback path should be short and direct avoiding vias.
3. Ground or power planes should be removed from directly under the amplifier's input and output pins.
4. An output resistor is recommended on each output, as near the output pin as possible.
5. Two 10 µF and two 0.1 µF power-supply decoupling capacitors should be placed as near the power-supply pins as possible.
6. Two 0.1 µF capacitors should be placed between the CM input pins and ground. This limits noise coupled into the pins. One each should be placed to ground near pin 4 and pin 9.
7. It is recommended to split the ground pane on layer 2 (L2) as shown below and to use a solid ground on layer 3 (L3). A single-point connection should be used between each split section on L2 and L3.
8. A single-point connection to ground on L2 is recommended for the input termination resistors R1 and R2. This should be applied to the input gain resistors if termination is not used.

THS4511 EVM

Figure 45 is the THS4511 EVAL1 EVM schematic for the plastic QFN (RGT) package. Layers 1 through 4 of the PCB are shown in Figure 46, and Table 5 is the bill of material for the EVM as supplied from TI. The same layout recommendations should be followed for the THS4511 ceramic flatpack devices. Contact your TI representative for availability of the THS4511 EVM.

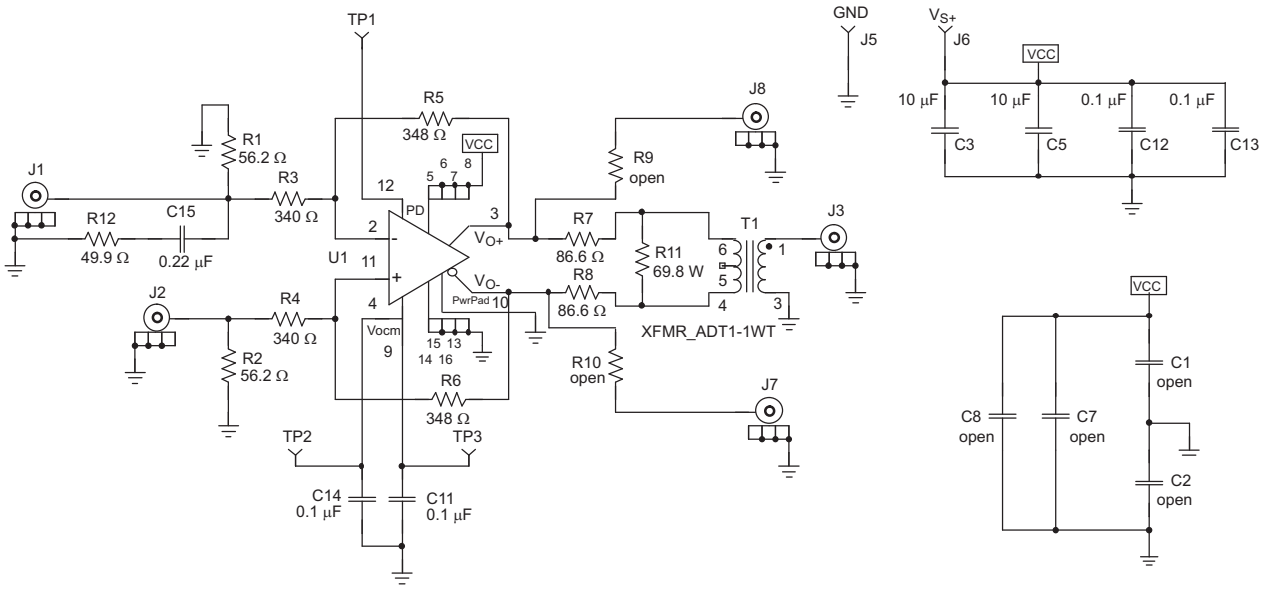


Figure 45. THS4511 EVAL1 EVM Schematic

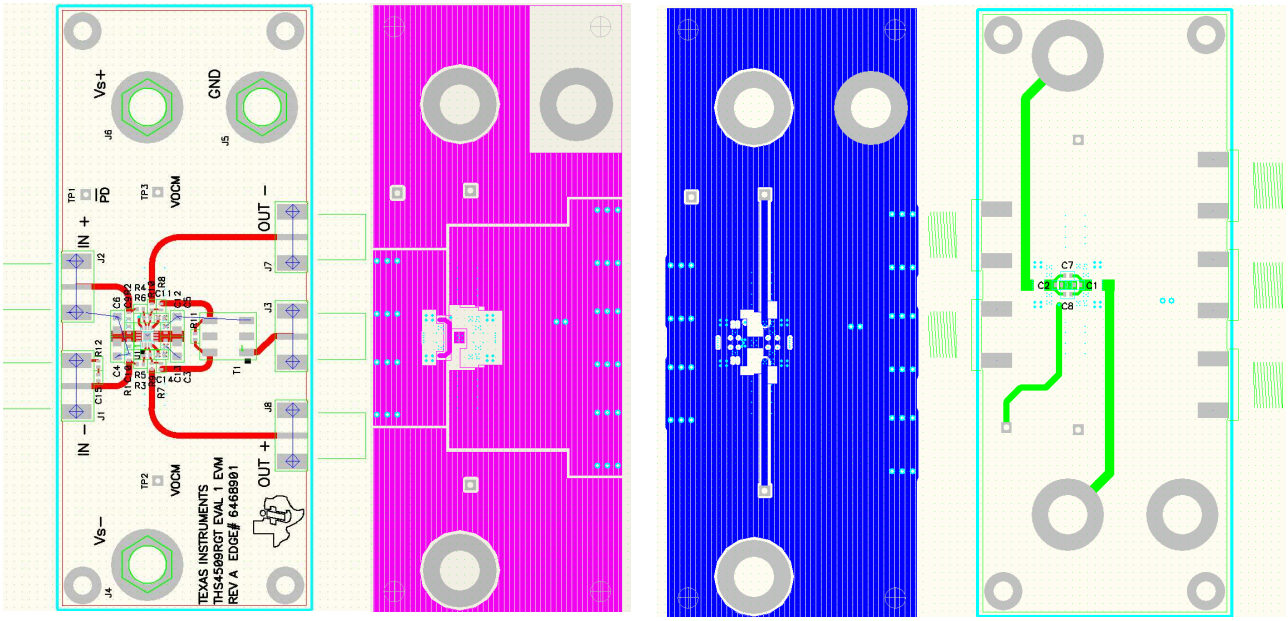


Figure 46. THS4511 EVAL1 EVM Layer 1 Through 4

Table 5. THS4511RGT EVM Bill of Materials

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	PCB QTY	MANUFACTURER'S PART NUMBER(1)
1	CAP, 10.0 µF, Ceramic, X5R, 6.3V	0805	C3, C5	2	(AVX) 08056D106KAT2A
2	CAP, 0.1 µF, Ceramic, X5R, 10V	0402	C11, C12, C13, C14	4	(AVX) 0402ZD104KAT2A
3	CAP, 0.22 µF, Ceramic, X5R, 6.3V	0402	C15	1	(AVX) 04026D224KAT2A
4	OPEN	0402	C1, C2, C7, C8, C9, C10	6	
5	OPEN	0402	R9, R10	2	
6	Resistor, 49.9 Ω, 1/16W, 1%	0402	R12	1	(KOA) RK73H1ETTP49R9F
7	Resistor, 56.2 Ω, 1/16W, 1%	0402	R1, R2		(KOA) RK73H1ETTP56R2F
8	Resistor, 69.8 Ω, 1/16W, 1%	0402	R11	3	(KOA) RK73H1ETTP69R8F
9	Resistor, 86.6 Ω, 1/16W, 1%	0402	R7, R8	2	(KOA) RK73H1ETTP86R6F
10	Resistor, 340 Ω, 1/16W, 1%	0402	R3, R4	2	(KOA) RK73H1ETTP3400F
11	Resistor, 348 Ω, 1/16W, 1%	0402	R5, R6	2	(KOA) RK73H1ETTP3480F
12	Resistor, 0 Ω, 5%	0805	C4, C6	2	(KOA) RK73Z2ATTD
13	Transformer, RF		T1	1	(MINI-CIRCUITS) ADT1-1WT
14	Jack, banana receptance, 0.25" diameter hole		J5, J6	2	(HH SMITH) 101
15	OPEN		J1, J7, J8	3	
16	Connector, edge, SMA PCB Jack		J2, J3	2	(JOHNSON) 142-0701-801
17	Test point, Red		TP1, TP2, TP3	3	(KEYSTONE) 5000
18	IC, THS4511		U1	1	(TI) THS4511RGT
19	Standoff, 4-40 HEX, 0.625" length			4	(KEYSTONE) 1808
20	SCREW, PHILLIPS, 4-40, 0.250"			4	SHR-0440-016-SN
21	Printed circuit board			1	(TI) EDGE# 6475513

(1) The manufacturer's part numbers were used for test purposes only.

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input and output voltage ranges as specified in the following table.

Input Range, V_{S+} to V_{S-}	**3.0 V to 6.0 V**
Input Range, V_I	3.0 V to 6.0 V NOT TO EXCEED V_{S+} or V_{S-}
Output Range, V_O	3.0 V to 6.0 V NOT TO EXCEED V_{S+} or V_{S-}

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the product data sheet or EVM user's guide (if user's guide is available) prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the material provided. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-0722201VFA	Active	Production	CFP (HKT) | 16	25 | TUBE	Yes	NIAU	N/A for Pkg Type	-55 to 125	5962-0722201VF A THS4511M
THS4511HKT/EM	Active	Production	CFP (HKT) | 16	25 | TUBE	Yes	NIAU	N/A for Pkg Type	25 to 25	THS4511HKT/EM EVAL ONLY

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

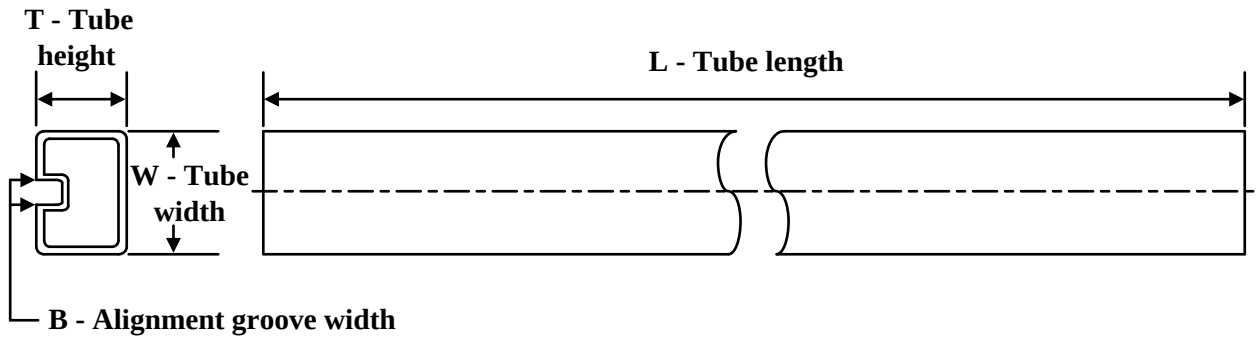
OTHER QUALIFIED VERSIONS OF THS4511-SP :

- Catalog : THS4511

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TUBE



*All dimensions are nominal

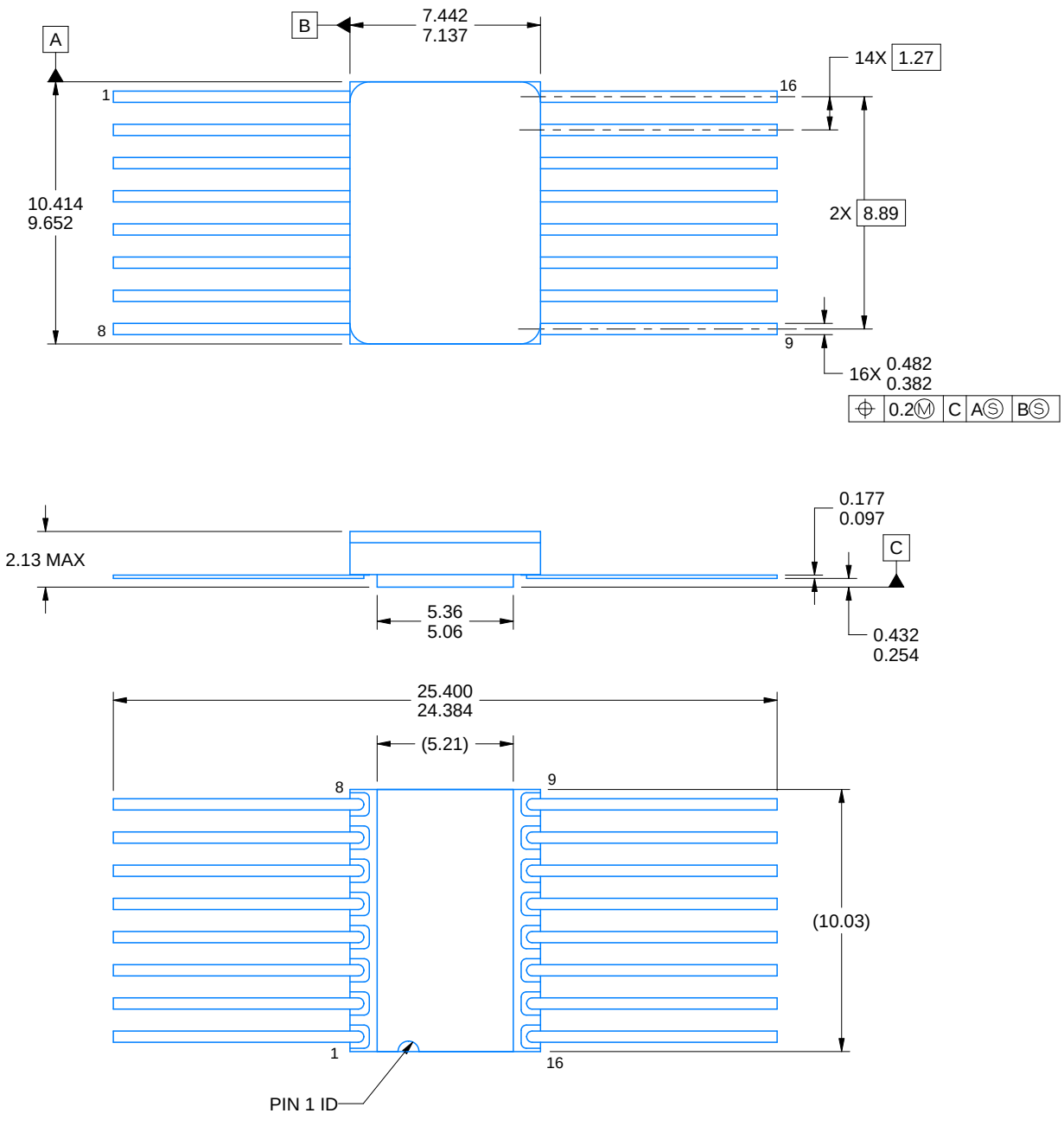
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-0722201VFA	HKT	CFP (HSL)	16	25	506.98	26.16	6220	NA
THS4511HKT/EM	HKT	CFP (HSL)	16	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

HKT0016A

CFP - 2.13 mm max height

CERAMIC DUAL FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. Lid and cavity are electrically isolated
4. The terminals are gold plated.
5. Falls within MIL-STD-1835 CDFP-F11A.

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