THVD1505 Bus-Polarity Correcting RS-485 Transceiver With IEC-ESD Protection

1 Features

- Meets or exceeds the requirements of the TIA/EIA-485A standard and the State Grid Corporation of China (SGCC) Part 11 Serial Communication Protocol RS-485 standard
- 4.5-V to 5.5-V supply voltage
- Half-duplex RS-422 / RS-485
- Bus polarity correction within 45 ms
- Works with or without fail-safe biasing resistors
- Data rate: up to 1 Mbps
- Bus I/O protection:
  - ±16-kV HBM ESD
  - ±8-kV IEC 61000-4-2 contact discharge
  - ±8-kV IEC 61000-4-2 air-gap discharge
  - ±2-kV IEC 61000-4-4 fast transient burst
- Open, short, and idle bus fail-safe
- Large receiver hysteresis for noise rejection: 120 mV
- Up to 256 nodes on a bus (1/8 unit load)
- Extended ambient temperature range: -40°C to 125°C
- Low power consumption
  - Standby supply current: < 1 µA
  - Operational supply current: < 1.1 mA
- Glitch-free power-up / down for hot plug-in capability

2 Applications

- Electricity meters
- HVAC systems
- Inverters
- Video surveillance

3 Description

The THVD1505 is a low-power RS-485 transceiver with automatic bus-polarity correction and transient protection. Upon hot plug-in, the device detects and corrects the bus polarity within the first 45 ms of bus idling. The bus pins are robust to electrostatic discharge (ESD) events, with high levels of protection to human-body model (HBM), IEC 61000-4-2 contact discharge and air-gap discharge specifications.

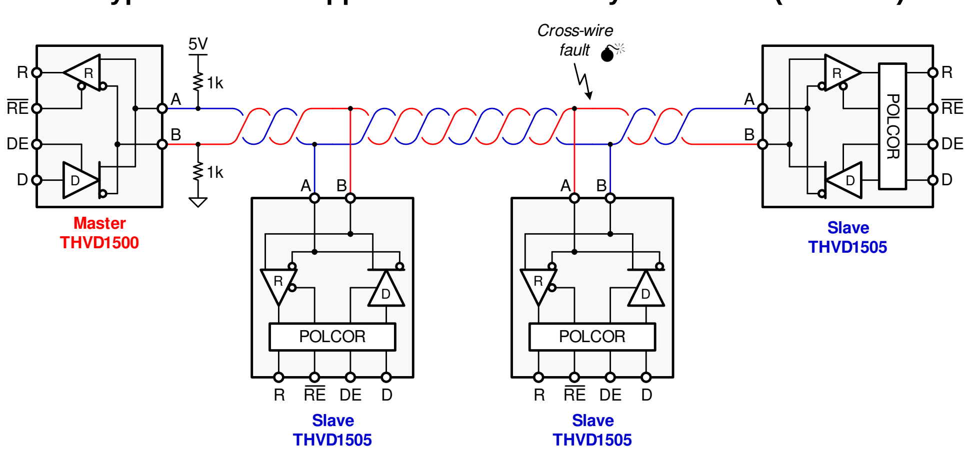
The device combines a differential driver and a differential receiver, which operate together from a single 5-V power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. The device features a wide common-mode voltage range making the device suitable for multi-point applications over long cable runs. The THVD1505 is available in an SOIC-8 package, and is characterized for free-air temperatures from –40°C to 125°C.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
THVD1505	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Network Application With Polarity Correction (POLCOR)



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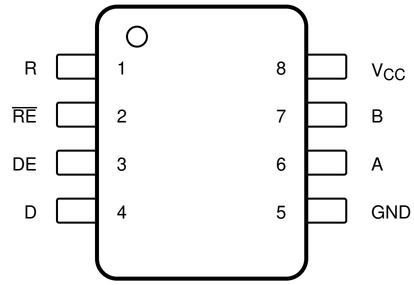
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2019	*	Initial release.

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input (internal 5-MΩ pull-up)
DE	3	Digital input	Driver enable, active high (internal 5-MΩ pull-down)
GND	5	Ground	Device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low (internal 5-MΩ pull-up)
V_{CC}	8	Supply	4.5-V to 5.5-V supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	7	V
V_L	Input voltage at any logic pin (D, DE or $\overline{RE}$)	–0.3	5.7	V
V_A, V_B	Voltage at A or B inputs, as differential or common-mode with respect to GND	–18	18	V
I_O	Receiver output current	–24	24	mA
T_J	Junction temperature		170	°C
T_{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditionsbeyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions forextended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus terminals and GND	±16,000	V
			All other pins	±4,000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1,500	
		Machine model (MM), per JEDEC JESD22-A115-A		±400	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings [IEC]

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 ESD contact discharge, bus terminals and GND	±8,000	V
		IEC 61000-4-2 ESD air-gap discharge, bus terminals and GND	±8,000	
		IEC 61000-4-4 EFT fast transient, bus terminals and GND	±2,000	

6.4 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{ID}	Differential input voltage		–12		12	V
V_I	Input voltage at any bus terminal(1)		–7		12	V
V_{IH}	High-level input voltage (driver, driver-enable, and receiver-enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver-enable, and receiver-enable inputs)		0		0.8	V
I_O	Output current	Driver	–60		60	mA
		Receiver	–8		8	
R_L	Differential load resistance		54	60		Ω
$1/t_{UI}$	Signaling rate		0.3		1000	kbps
T_J	Junction temperature		–40		150	°C
T_A(2)	Operating ambient temperature (see *Thermal Information* for additional information)		–40		125	°C

(1) The algebraic convention in which the least positive (most negative) limit is designated as minimum is used in this datasheet.
(2) Operation is specified for internal (junction) temperatures upto 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shutdown (TSD) circuit which disables the device when the junction temperature reaches 170°C.

6.5 Thermal Information

THERMAL METRIC(1)		THVD1505 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	125.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	20.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.8	°C/W

(1) For more information about traditional and new thermalmetrics, see the *Semiconductor and ICPackage Thermal Metrics* application report.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
$\lvert V_{OD} \rvert$	Driver differential-output voltage magnitude	V_{test} from –7 to +12 V	See Figure 7	1.5	2.5		V
		R_L = 54 Ω (RS-485), C_L = 50 pF	See Figure 8	1.5	2.5		
		R_L = 100 Ω (RS-422), C_L = 50 pF		2	3		
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of driver differential-output voltage	R_L = 54 Ω, C_L = 50 pF	See Figure 8	–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	R_L = 54 Ω, C_L = 50 pF	See Figure 8	1	V_{CC} / 2	3	V
ΔV_{OC}	Change in differential driver common-mode output voltage			–50		50	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage				250		mV
$\lvert I_{OS} \rvert$	Driver short-circuit output current	DE = V_{CC}, -7 V ≤ [V_A or V_B] ≤ 12 V, or A pin shorted to B pin				150	mA
C_{OD}	Differential output capacitance				8		pF
Receiver							
I_I	Bus input current (driver disabled)	DE = 0 V, V_{CC} = 0 V or 5.5 V	V_I = 12 V		75	110	µA
			V_I = –7 V	–90	–70		
R_A, R_B	Bus input impedance	V_A = -7 V, V_B = 12 V and V_A = 12 V, V_B = -7 V	See Figure 12	96			kΩ
V_{IT+}	Positive-going receiver differential-input voltage threshold				60	100	mV
V_{IT-}	Negative-going receiver differential-input voltage threshold			–100	–60		mV
V_{HYS} (1)	Receiver differential-input voltage threshold hysteresis ($V_{IT+} – V_{IT–}$)			40	120		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA		4	V_{CC} – 0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA			0.2	0.4	V
I_{OZ}	Receiver high-impedance output current	V_O = 0 V or V_{CC}, $\overline{RE}$ = V_{CC}		–1		1	µA
I_{OSR}	Receiver output short-circuit current	$\overline{RE}$ = 0, DE = 0	See Figure 13			95	mA
Logic							
I_{IN}	Input current (D, DE, $\overline{RE}$)			–2		2	µA
Supply							
I_{CC}	Supply current (quiescent)	Driver and receiver enabled	DE = V_{CC}, $\overline{RE}$ = 0, no load		820	1100	µA
		Driver enabled, receiver disabled	DE = V_{CC}, $\overline{RE}$ = V_{CC}, no load		520	660	
		Driver disabled, receiver enabled	DE = 0, $\overline{RE}$ = 0, no load		520	660	
		Driver and receiver disabled	DE = 0, $\overline{RE}$ = V_{CC}, no load		0.03	1	

(1) Under any specific conditions, V_{IT+} is specified to be at least V_{HYS} higher than$V_{IT–}$.

6.7 Power Dissipation Characteristics

PARAMETER			TEST CONDITIONS	VALUE	UNIT
PD	Power dissipation, driver and receiver enabled, V_{CC} = 5.5 V, T_A = 125°C, 50% duty cycle square-wave signal at maximum signaling rate	Unterminated	R_L = 300 Ω, C_L = 50 pF	120	mW
		RS-422 load	R_L = 100 Ω, C_L = 50 pF	160	
		RS-485 load	R_L = 54 Ω, C_L = 50 pF	200	

6.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Driver differential output rise and fall times		See Figure 9	100	115	300	ns
t_{PHL}, t_{PLH}	Driver propagation delay		See Figure 9		90	350	ns
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} – t_{PLH}\|$		See Figure 9		25	40	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 10 and Figure 11		70	160	ns
t_{PHZ}, t_{PLZ}	Driver enable time	Receiver enabled	See Figure 10 and Figure 11		220	400	ns
		Receiver disabled	See Figure 10 and Figure 11		1.5	3	µs
Receiver							
t_r, t_f	Receiver output rise and fall times		See Figure 14		6	30	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time		See Figure 14		80	120	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} – t_{PLH}\|$		See Figure 14		2	7	ns
t_{PHZ}, t_{PLZ}	Receiver disable time		See Figure 15		15	30	ns
$t_{PZL(1)}$, $t_{PZH(1)}$	Receiver enable time	Driver enabled	See Figure 15		180	370	ns
$t_{PZL(2)}$, $t_{PZH(2)}$		Driver disabled	See Figure 16		1	5	µs
t_{FS}	Bus fail-safe time	Driver disabled	See Figure 17	25	35	45	ms

6.9 Typical Characteristics

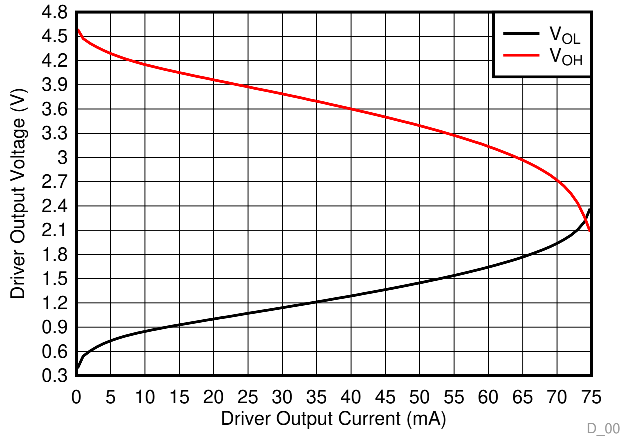


Figure 1. Driver Output Voltage vs Driver Output Current

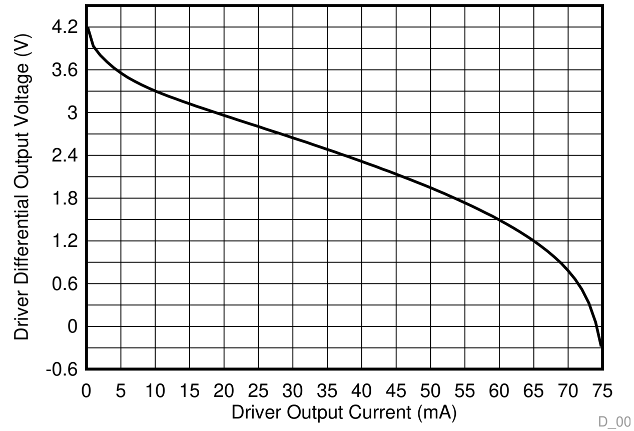


Figure 2. Driver Differential Output Voltage vs Driver Output Current

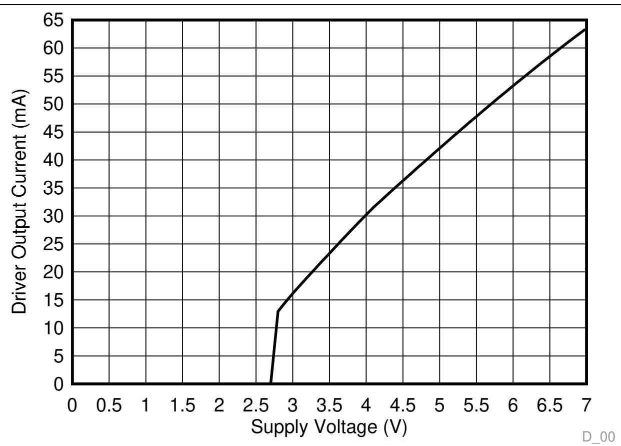


Figure 3. Driver Output Current vs Supply Voltage

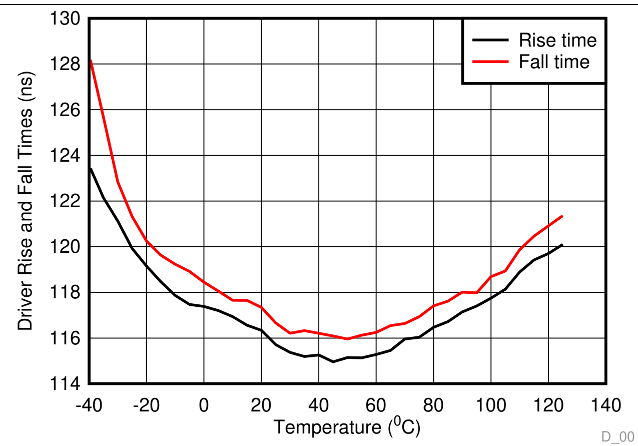


Figure 4. Driver Rise or Fall Time vs Temperature

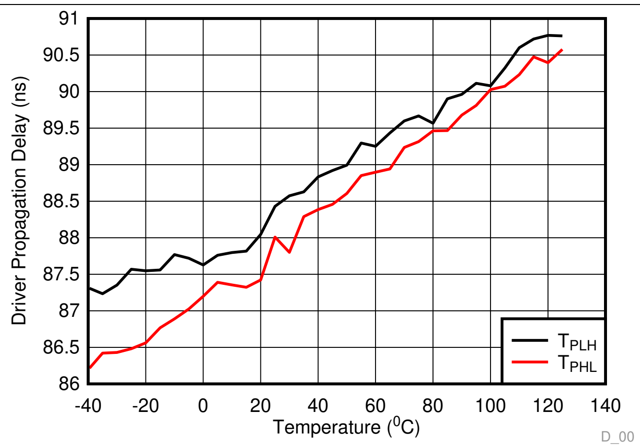


Figure 5. Driver Propagation Delay vs Temperature

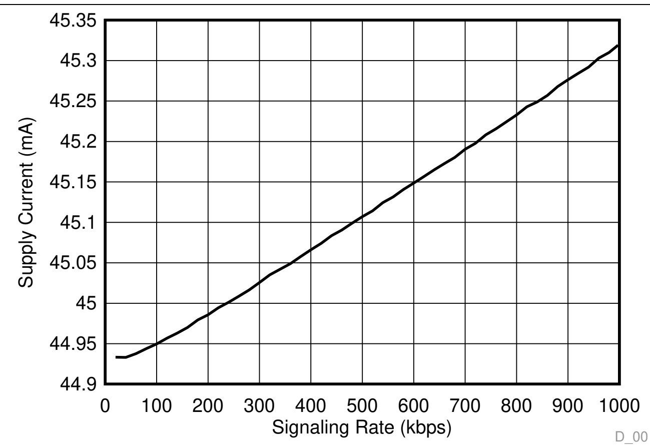


Figure 6. Supply Current vs Signaling Rate

7 Parameter Measurement Information

7.1 Driver

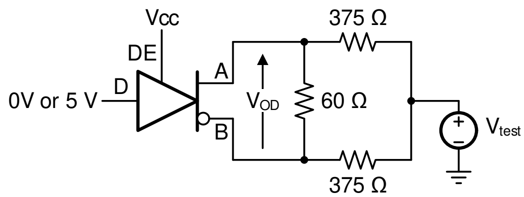


Figure 7. Measurement of Driver Differential-Output Voltage With Common-Mode Load

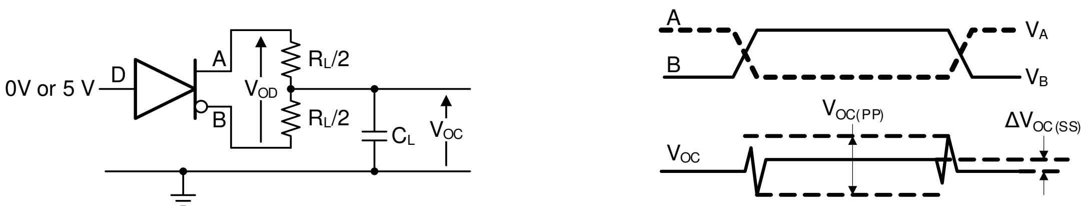


Figure 8. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

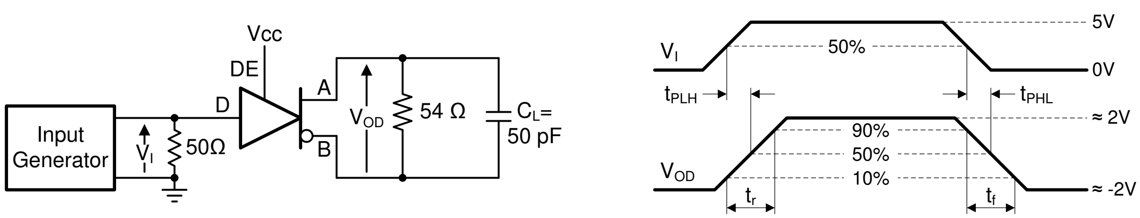


Figure 9. Measurement of Driver Differential-Output Rise and Fall Times and Propagation Delays

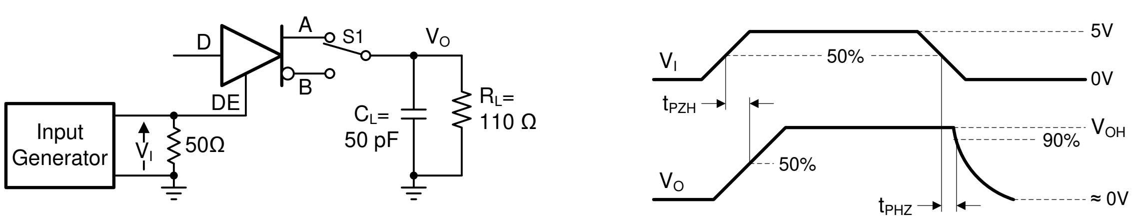


Figure 10. Measurement of Driver Enable and Disable Times With Active-High Output and Pull-Down Load

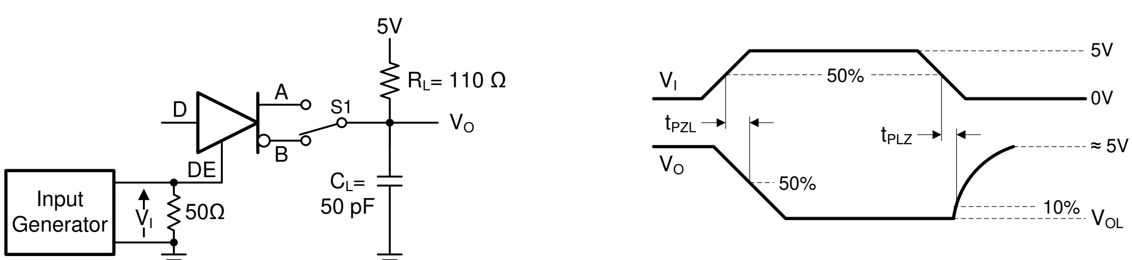
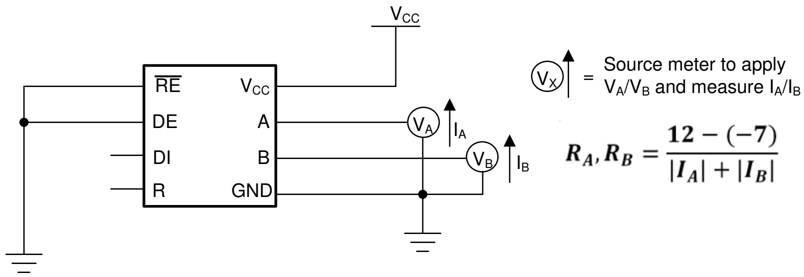


Figure 11. Measurement of Driver Enable and Disable Times With Active-Low Output and Pull-up Load

7.2 Receiver



$$R_A, R_B = \frac{12 - (-7)}{|I_A| + |I_B|}$$

Figure 12. Measurement of Bus Impedance

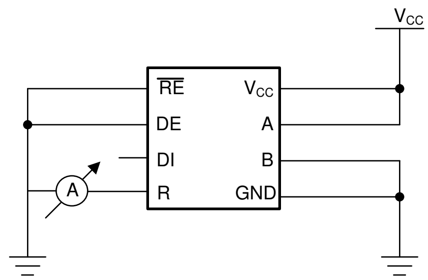


Figure 13. Measurement of Receiver Output Short Circuit Current

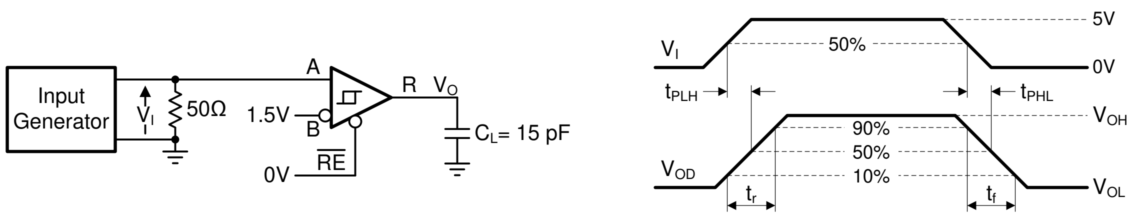


Figure 14. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

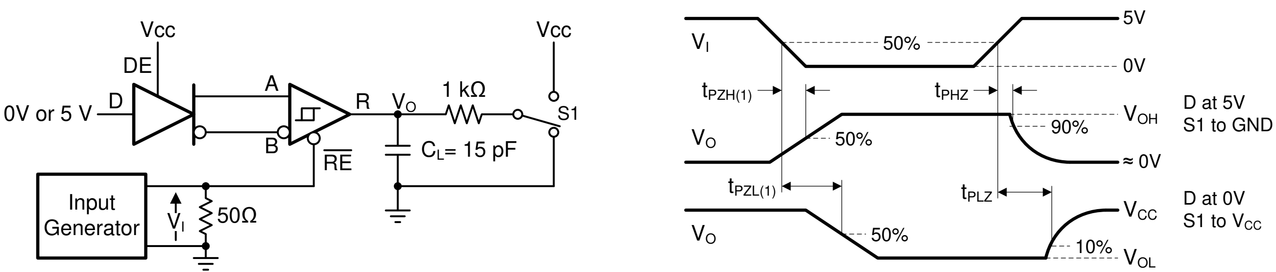


Figure 15. Measurement of Receiver Enable and Disable Times With Driver Enabled

Receiver (continued)

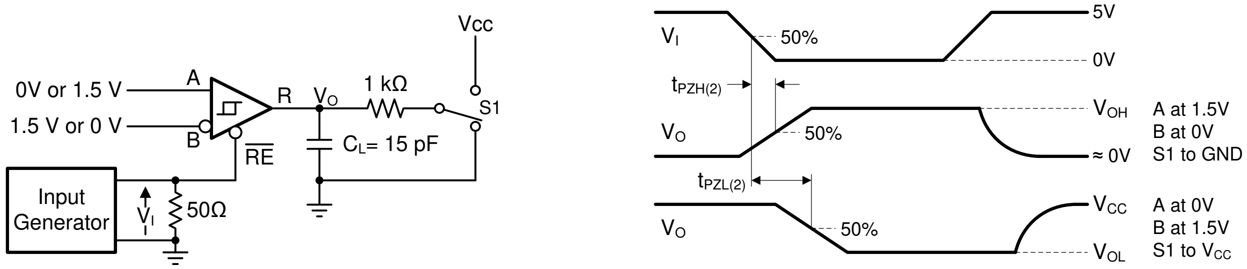


Figure 16. Measurement of Receiver Enable Times With Driver Disabled

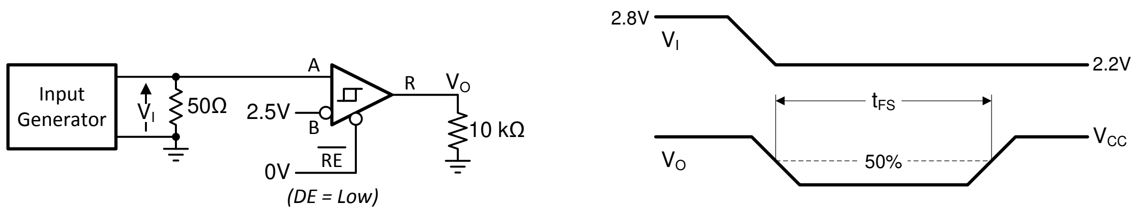


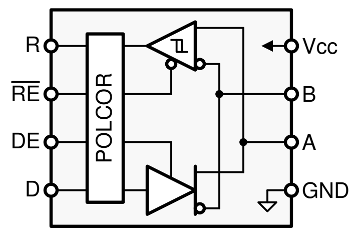
Figure 17. Measurement of Receiver Polarity-Correction Time With Driver Disabled

8 Detailed Description

8.1 Overview

The THVD1505 device is a half-duplex RS-485 transceiver suitable for data transmission at rates up to 1 Mbps over controlled-impedance transmission media (such as twisted-pair cabling). The device features a high level of internal transient protection, making it able to withstand ESD strikes up to ±8 kV (per IEC 61000-4-2) and EFT transients up to ±2 kV (per IEC 61000-4-4) without incurring damage. Up to 256 units of THVD1500 and/or THVD1505 may share a common RS-485 bus due to the devices' low bus input currents. THVD1505 features automatic polarity correction, which detects bus mis-wiring and swaps A and B.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bus Polarity Correction

THVD1505 automatically corrects a wrong bus-signal polarity caused by a mis-wire fault. In order to detect the bus polarity, the following conditions must be met.

- A slave node must enable the receiver ($\overline{RE}$ = low). Driver can be in either enabled or disabled state
- A and B signals should be static for longer than fail-safe time (t_{FS})
- The absolute value of the differential voltage at the receiver input should be greater than the receiver thresholds ($|V_{IT+}|$ or $|V_{IT-}|$)

The receiver input voltage can be defined either by using passive fail-safe resistors or by the master node actively driving the bus.

8.3.1.1 Passive Polarity Definition Using Fail-Safe Biasing Network

Figure 18 shows a simple point-to-point data link between a master node and a slave node with mis-wire fault.

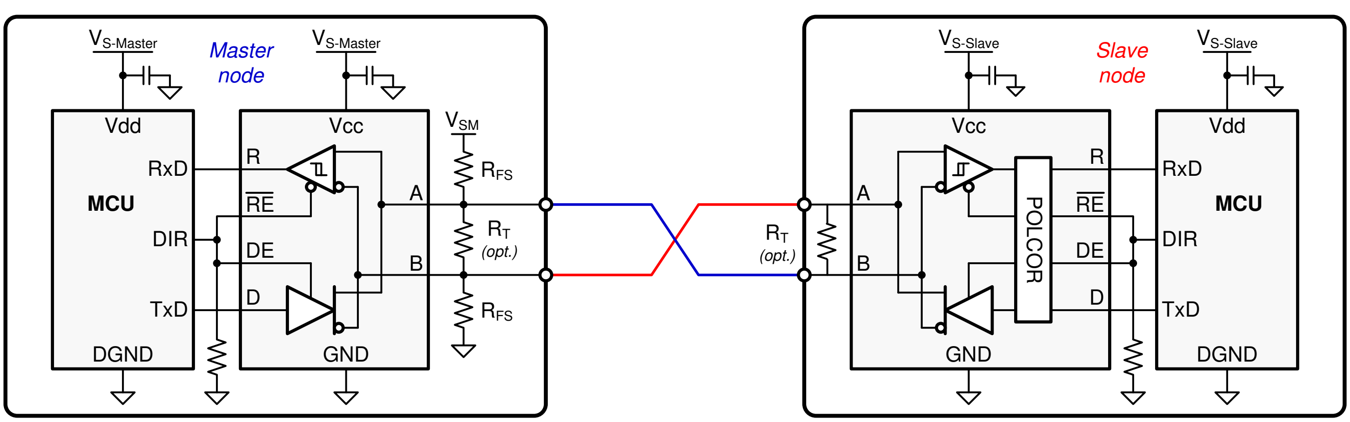


Figure 18. Passive Polarity Definition

Feature Description (continued)

During passive polarity definition, an external fail-safe resistor network (R_{FS}) must be used to ensure fail-safe operation during an idle bus state. When the bus is not actively driven, the differential receiver inputs could float allowing the receiver output to assume a random output. A proper fail-safe network forces the receiver inputs to exceed the V_{IT} threshold, thus forcing the THVD1505 receiver output into the high state.

Figure 19 shows the timing diagram for passive polarity definition.

Prior to initiating data transmission the master transceiver must idle for a time span that exceeds the maximum fail-safe time, t_{FS}, of a slave transceiver. This idle time is accomplished by driving the direction control line (the output of the MCU in Figure 19 that is driving DE and $\overline{RE}$ pins), DIR, low. After a time, t > t_{FS}, the master begins transmitting data.

Because of the indicated mis-wire fault between master and slave, the slave node receives bus signals with reversed polarity. Assuming the slave node has just been connected to the bus, the direction-control pin is pulled-down during power-up and then is actively driven low by the slave MCU. The polarity correction begins as soon as the slave supply is established and ends after t_{FS}.

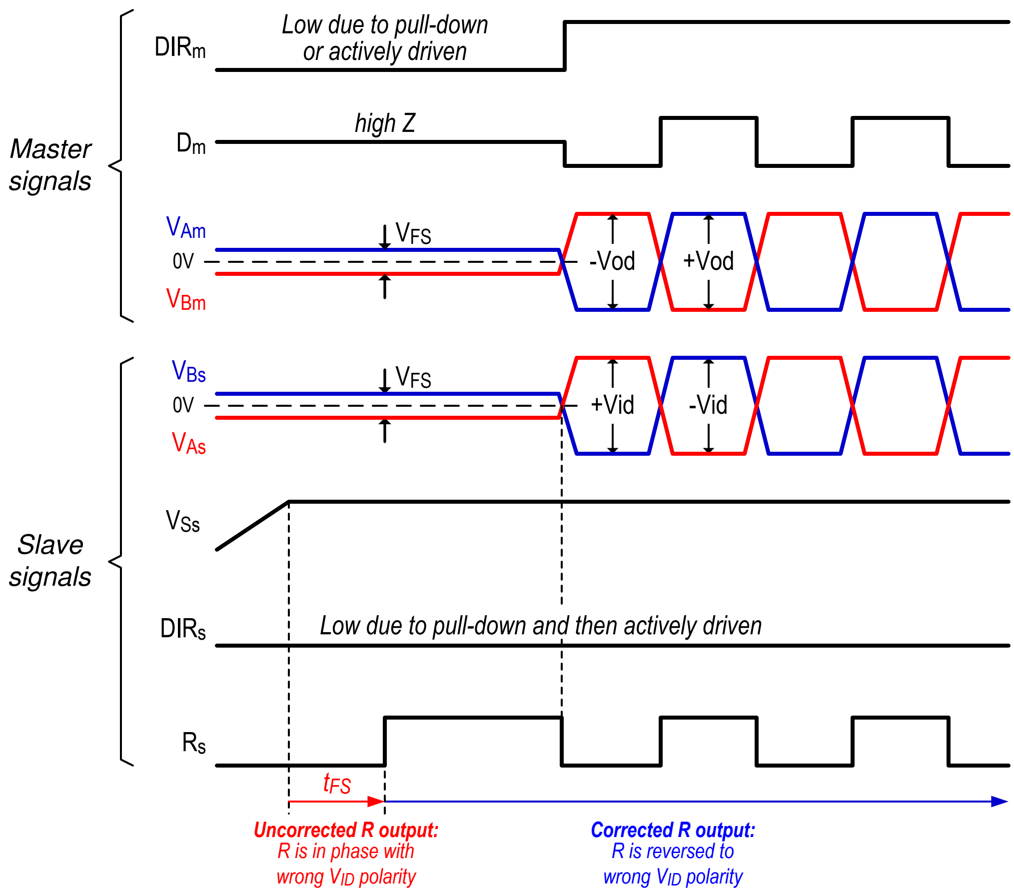


Figure 19. Polarity Correction Timing With Passive Polarity Definition

Initially, the slave receiver assumes that the correct bus polarity is applied to the inputs and performs no polarity reversal. Because of the reversed polarity of the bus-failsafe voltage, the output of the slave receiver, R_S, turns low. After t_{FS} has passed and the receiver has detected the wrong bus polarity, the internal POLCOR logic reverses the input signal and R_S turns high.

At this point, all incoming bus data with reversed polarity are polarity corrected within the transceiver. Because polarity correction is also applied to the transmit path, the data sent by the slave MCU are reversed by the POLCOR logic and then fed into the driver.

Feature Description (continued)

The reversed data from the slave MCU are reversed again by the mis-wire fault in the bus, and the correct bus polarity is reestablished at the master end.

THVD1505 retains the state of the polarity logic as long as V_{CC} is present to the device. However, the device POLCOR logic powers up in the default no polarity reversal mode at each device power up. POLCOR logic remains active as long as V_{CC} is applied to the device.

NOTE

Data string durations of consecutive 0s or 1s exceeding the minimum t_{FS} can accidently trigger a wrong polarity correction and must be avoided.

8.3.1.2 Active Polarity Definition by the Master Node

THVD1505 polarity correction can also work without a fail-safe resistor network. See Figure 20.

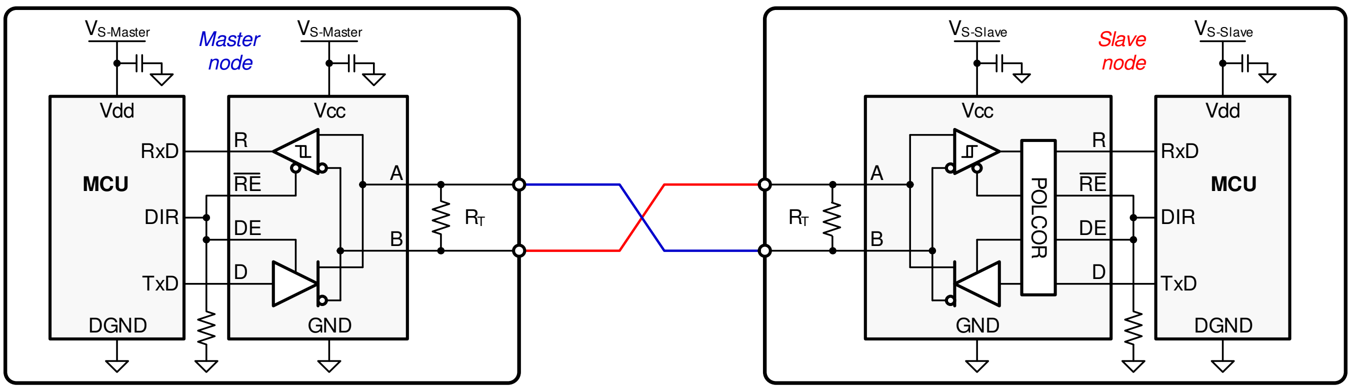


Figure 20. Active Polarity Definition

In this scenario, the master node drives the bus for longer than t_{FS}. After a time, $t > t_{FS}$, the master begins transmitting data. Figure 21 shows the timing diagram for active polarity definition. DIR pin refers to the output of the MCU that is driving DE and $\overline{RE}$ pins in Figure 21.

Feature Description (continued)

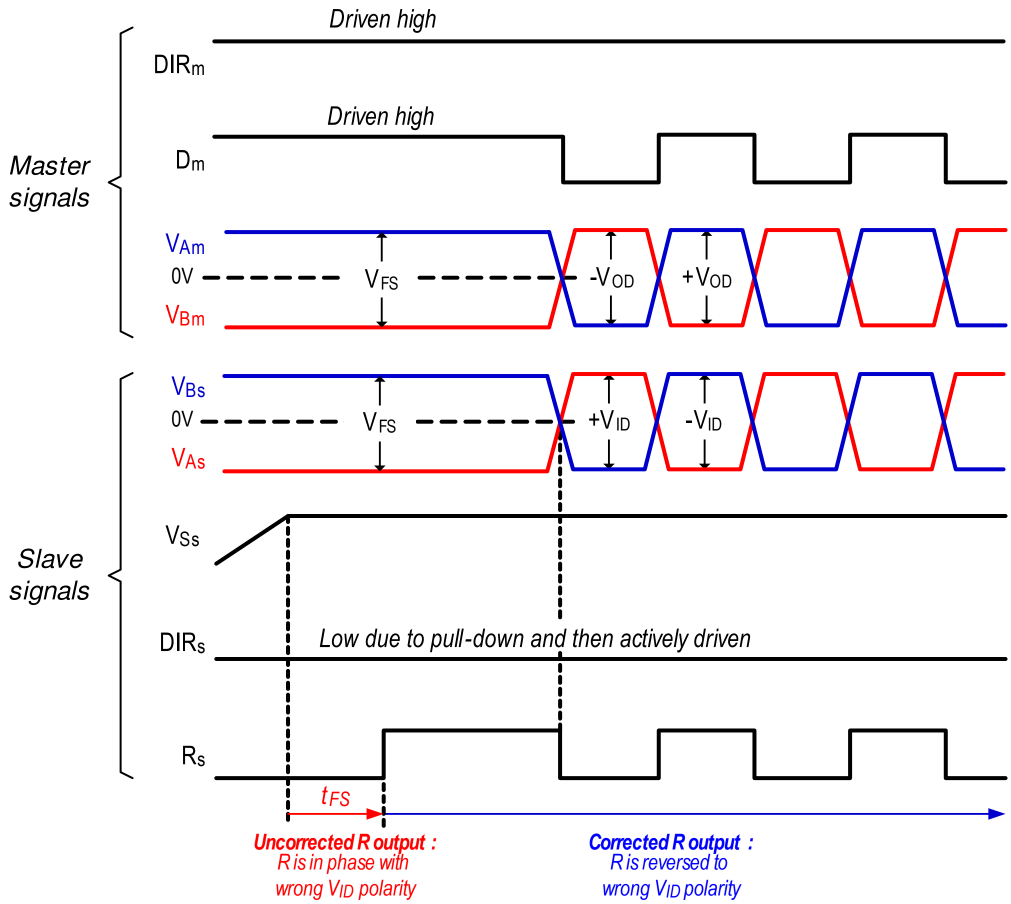


Figure 21. Polarity Correction Timing With Active Polarity Definition

POLCOR logic behavior with active polarity definition is identical to the POLCOR logic behavior with passive polarity definition.

8.4 Device Functional Modes

Table 1. Driver Pin Functions

INPUT	ENABLE	OUTPUTS		DESCRIPTION
D	DE	A	B	
NORMAL MODE				
H	H	H	L	Actively drives bus high
L	H	L	H	Actively drives bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drives bus high
POLARITY-CORRECTING MODE				
H	H	L	H	Actively drives bus low
L	H	H	L	Actively drives bus high
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	L	H	Actively drives bus low

Table 2. Receiver Pin Functions

DIFFERENTIAL INPUT	ENABLE		OUTPUT	DESCRIPTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	DE	R	
$V_{ID} > V_{IT+}$	L	X	H	Receive valid bus high
$V_{IT-} > V_{ID}$	L	X	L during t_{FS} H after t_{FS}	Receive valid bus low if lasting for less than t_{FS}, polarity correcting if lasting for more than t_{FS}
X	H	X	Z	Receiver disabled
X	OPEN	X	Z	Receiver disabled
Open, short or $V_{IT+} > V_{ID} > V_{IT-}$	L	X	H after t_{FS}	Receiver fail-safe high

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Device Configuration

The THVD1505 is a half-duplex RS-485 transceiver operating from a single 5-V ±10% supply. The driver and receiver enable pins allow for the configuration of different operating modes.

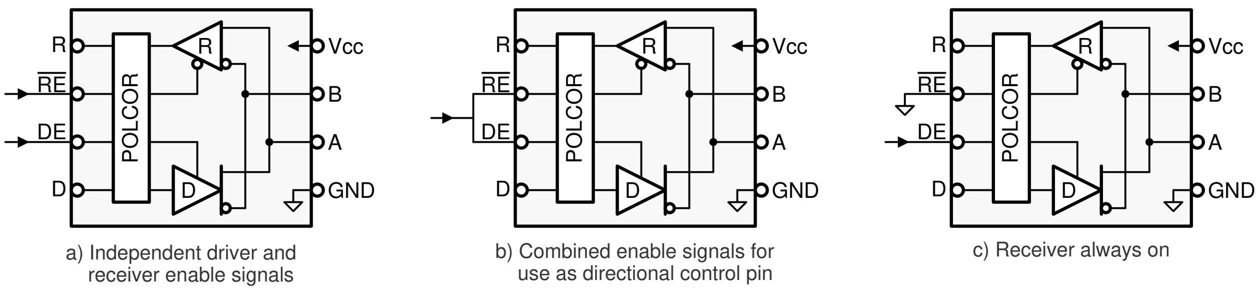


Figure 22. Transceiver Configurations

Using independent enable lines provides the most flexible control as the lines allow for the driver and the receiver to be turned on and turned off individually. While this configuration requires two control lines, it allows for selective listening to the bus traffic, whether the driver is transmitting data or not. Only this configuration allows the THVD1505 to enter low-power standby mode because it allows both the driver and receiver to be disabled simultaneously.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. Thus, when the direction-control line is high, the transceiver is configured as a driver, while for a low the device operates as a receiver.

Tying the receiver enable to ground and controlling only the driver-enable input also uses only one control line. In this configuration, a node not only receives the data on the bus sent by other nodes but also receives the data sent on the bus, enabling the node to verify the correct data has been transmitted.

9.1.2 Bus Design

An RS-485 bus consists of multiple transceivers connected in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for relatively high data rates over long cable length.

Common cables used are unshielded twisted pair (UTP), such as low-cost CAT-5 cable with $Z_0 = 100\ \Omega$, and RS-485 cable with $Z_0 = 120\ \Omega$. Typical cable sizes are AWG 22 and AWG 24.

The maximum bus length is typically given as 4000 ft or 1200 m, and represents the length of an AWG 24 cable whose cable resistance approaches the value of the termination resistance, thus reducing the bus signal by half or 6 dB. Actual maximum usable cable length depends on the signaling rate, cable characteristics, and environmental conditions.

Application Information (continued)

9.1.3 Fail-Safe Biasing for Passive Polarity Definition

External biasing resistor network of R_{FS} along with R_T define the V_{FS} during the polarity correction time, t_{FS}. See Passive Polarity Definition Using Fail-Safe Biasing Network for more details.

R_{FS} resistors should be selected such that $V_{FS} > |V_{IT}| = 100$ mV. The equation below can be used to calculate R_{FS}. Note that too low of a R_{FS} value increases the bus loading that reduces the number of nodes on the RS-485 bus.

$$R_{FS} < 0.5 \times [(R_T \times V_{CC\text{-}min}) / 0.1 - R_T] \quad (1)$$

9.1.4 Cable Length Versus Data Rate

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, applications such as e-metering often operate at rates of up to 250 kbps even at distances of 4000 ft and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

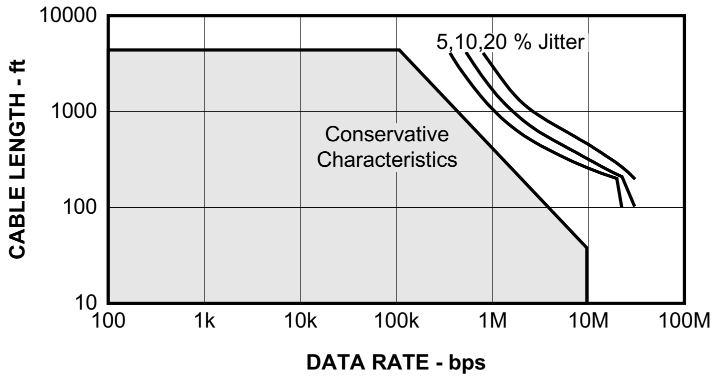


Figure 23. Cable Length vs Data Rate Characteristic

9.1.5 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. The reason for the short distance is because a stub presents a non-terminated piece of bus line which can introduce reflections if the distance is too long. As a general guideline, the electrical length or round-trip delay of a stub should be less than one-tenth of the rise time of the driver, thus leading to a maximum physical stub length of as shown in Equation 2.

$$L_S \leq 0.1 \times t_r \times v \times c$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s or 9.8×10^8 ft/s)
- v is the signal velocity of the cable (v = 78%) or trace (v = 45%) as a factor of c (2)

Based on Equation 2, with a minimum rise time of 400 ns, Equation 3 shows the maximum cable-stub length of the THVD1505.

$$L_S \leq 0.1 \times 400 \times 10^{-9} \times 3\ 10^8 \times 0.78 = 9.4 \text{ m (or 30.6 ft)} \quad (3)$$

Application Information (continued)

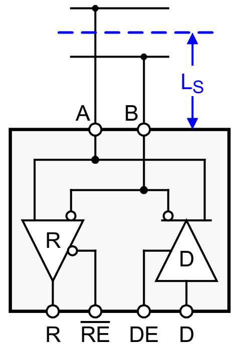


Figure 24. Stub Length

9.1.6 Transient Protection

The bus terminals of the THVD1505 transceiver family possess on-chip ESD protection against ±16 kV HBM, ±8 kV IEC 61000-4-2 contact discharge and ±2 kV IEC 61000-4-4 EFT. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, C_S, and 78% lower discharge resistance, R_D of the IEC model produce significantly higher discharge currents than the HBM model.

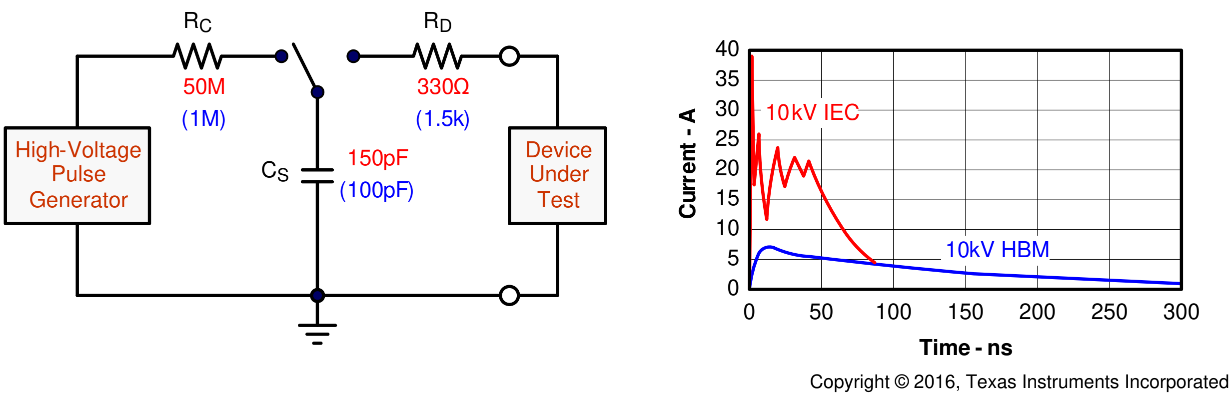


Figure 25. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD and EFT protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. EFTs are generally caused by relay-contact bounce or the interruption of inductive loads.

Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 26 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation. The right hand diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

Designers may choose to implement protection against longer duration surge transients. Figure 28 suggests two circuit designs providing protection against short and long duration surge transients. Table 3 lists the bill of materials for the external protection devices.

Application Information (continued)

NOTE

The unit of the pulse-power changes from kW to MW, thus making the power of the 500-V surge transient almost dropping off the scale.

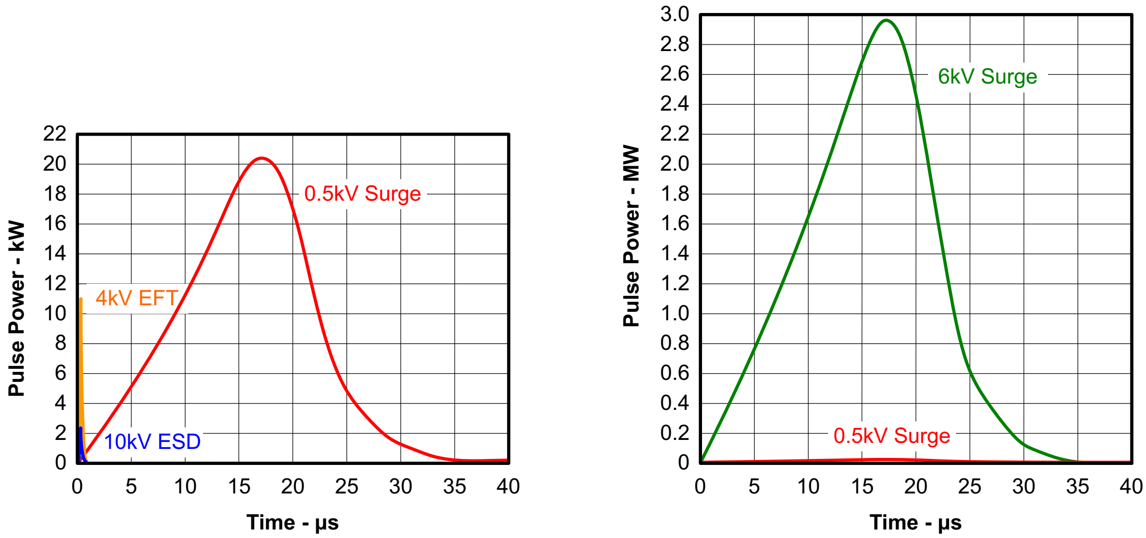


Figure 26. Power Comparison of ESD, EFT, and Surge Transients

In the case of surge transients, high-energy content is signified by long pulse duration and slow decaying pulse power.

The electrical energy of a transient that is dumped into the internal protection cells of the transceiver is converted into thermal energy. This thermal energy heats the protection cells and literally destroys them, thus destroying the transceiver. Figure 27 shows the large differences in transient energies for single ESD, EFT, and surge transients as well as for an EFT pulse train, commonly applied during compliance testing.

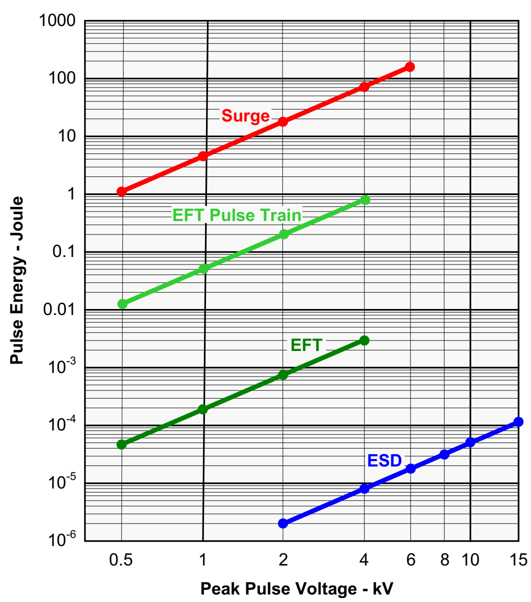


Figure 27. Comparison of Transient Energies

Application Information (continued)

Table 3. List of Components

DEVICE	FUNCTION	ORDER NUMBER(1)	MANUFACTURER
XCVR	5-V, 1-Mbps RS-485 Transceiver	THVD1505DR	TI
R1, R2	10-Ω, Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400-W Transient Voltage Suppressor	CDSOT23-SM712	Bourns
TBU1, TBU2	Bidirectional 200mA Transient Blocking Unit	TBU-CA-065-200-WH	Bourns
MOV1, MOV2	200-mA Transient Blocking Unit 200-V, Metal-Oxide Varistor	MOV-10D201K	Bourns

(1) See Third Party Disclaimer

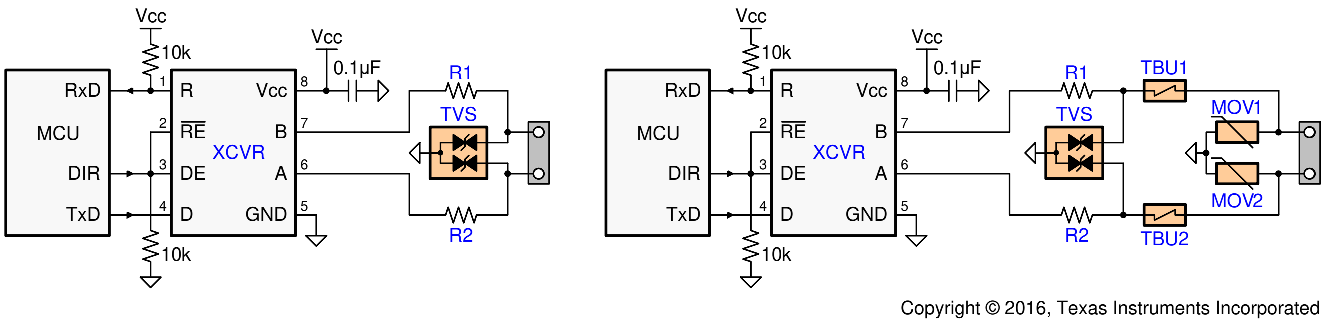
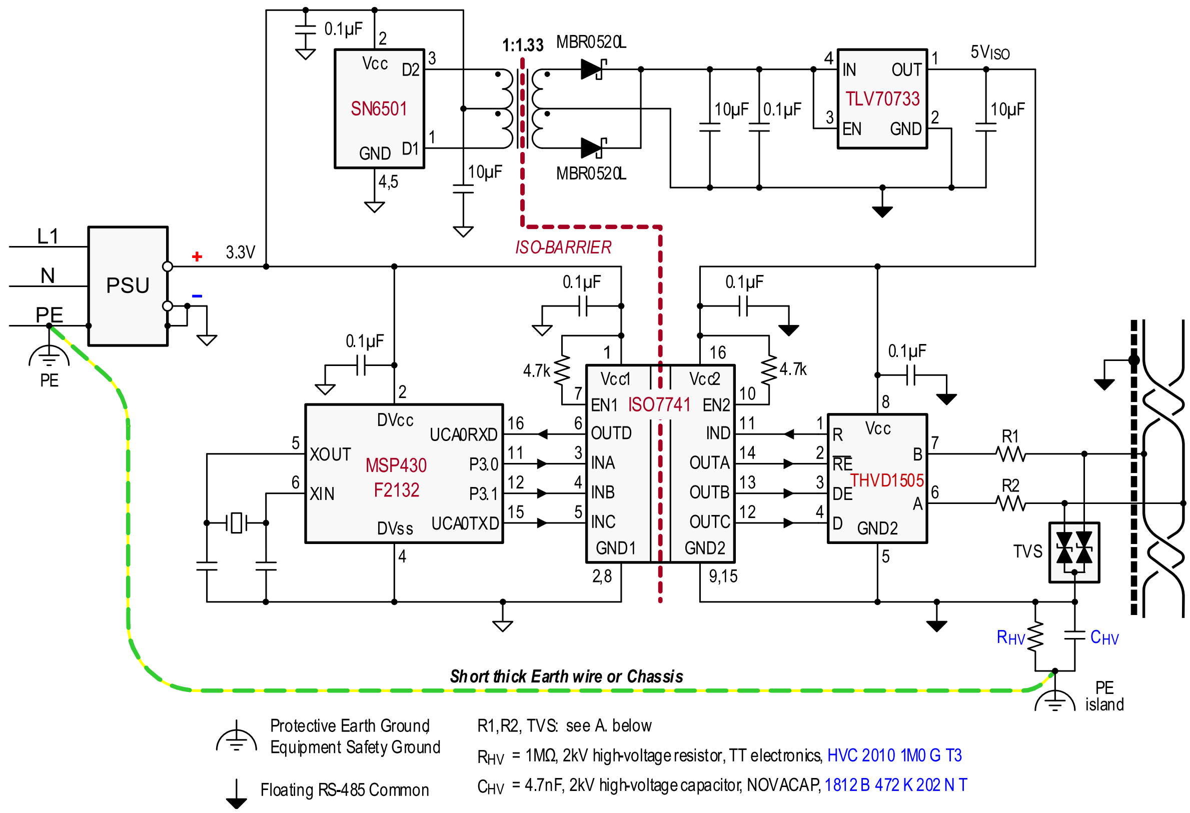


Figure 28. Transient Protections Against Surge Transients

The left circuit shown in Figure 28 provides surge protection of 1-kV transients, while the right protection circuits can withstand surge transients of 5 kV.

9.2 Typical Application

Many RS-485 networks use isolated bus nodes to prevent the creation of unintended ground loops and their disruptive impact on signal integrity. An isolated bus node typically includes a micro controller that connects to the bus transceiver through a multi-channel, digital isolator (Figure 29).



A. See Table 3.

Figure 29. Isolated Bus Node With Transient Protection

9.2.1 Design Requirements

Example Application: Isolated Bus Node with Transient Protection

- RS-485-compliant bus interface.
- Galvanic isolation of both signal and power supply lines.
- Able to withstand surge transients up to 1 kV (per IEC 61000-4-5).
- Full control of data flow on bus in order to prevent contention (for half-duplex communication).

9.2.2 Detailed Design Procedure

Power isolation is accomplished using the push-pull transformer driver SN6501, a low-cost LDO and TLV70733.

Signal isolation uses the quadruple digital isolator ISO7741. Notice that both enable inputs, EN1 and EN2, are pulled-up via 4.7-kΩ resistors to limit input currents during transient events.

While the transient protection is similar to the one in Figure 28 (left circuit), an additional high-voltage capacitor diverts transient energy from the floating RS-485 common further towards protective earth (PE) ground. This diversion is necessary as noise transients on the bus are usually referred to Earth potential.

R_{VH} refers to a high-voltage resistor, and in some applications even a varistor. This resistance is applied to prevent charging of the floating ground to dangerous potentials during normal operation.

Occasionally varistors are used instead of resistors in order to rapidly discharge C_{HV}, if expected that fast transients might charge C_{HV} to high-potentials.

Typical Application (continued)

Note that the PE island represents a copper island on the PCB for the provision of a short, thick Earth wire connecting this island to PE ground at the entrance of the power supply unit (PSU).

In equipment designs using a chassis, the PE connection is usually provided through the chassis itself. Typically the PE conductor is tied to the chassis at one end while the high-voltage components, C_{HV} and R_{HV}, are connecting to the chassis at the other end.

9.2.3 Application Curve

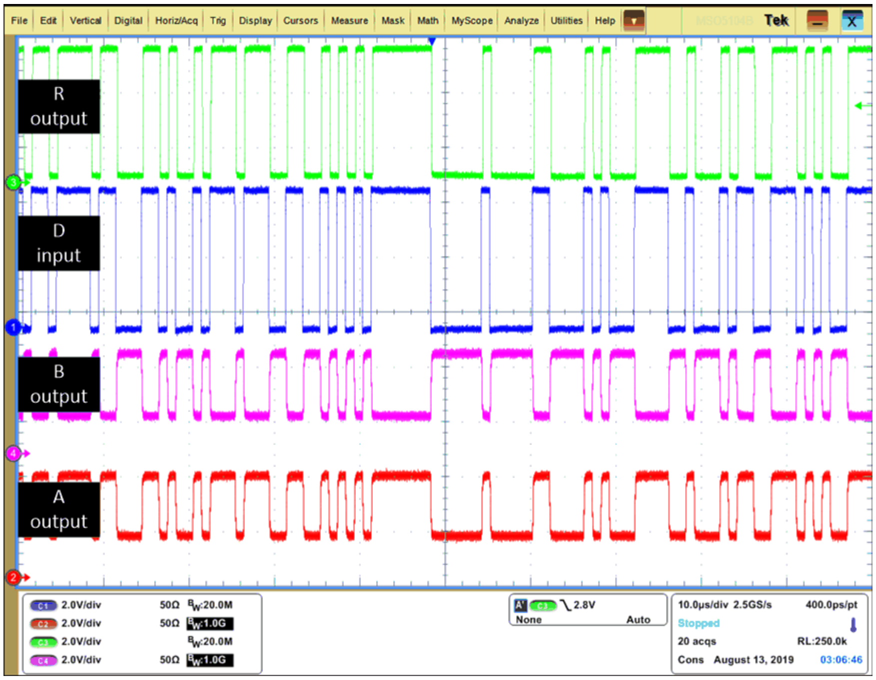


Figure 30. Waveforms at 1 Mbps Operation, PRBS7 Data Pattern

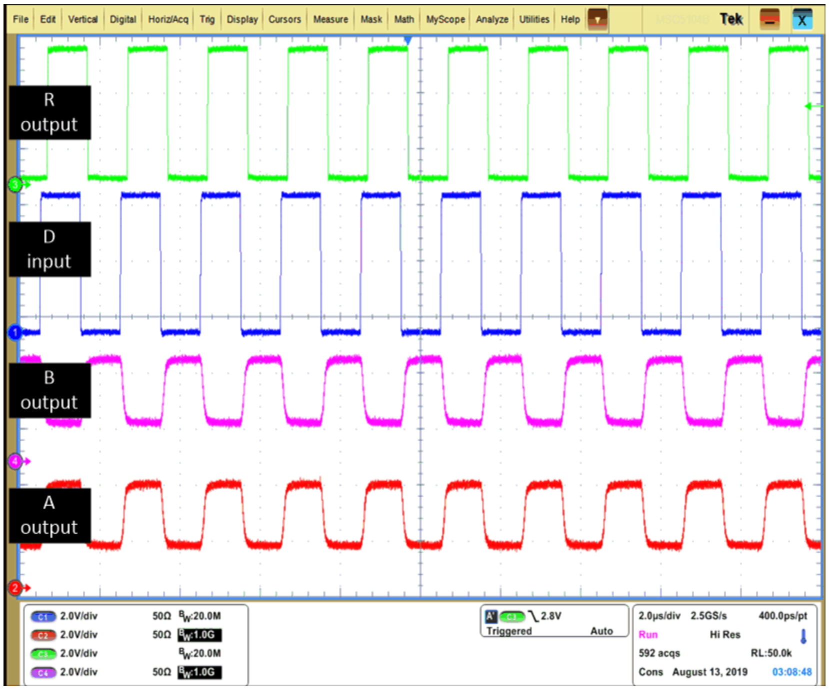


Figure 31. Waveforms at 1 Mbps Operation, Clock Data Pattern

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100-nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

11 Layout

11.1 Layout Guidelines

11.1.1 Design and Layout Considerations For Transient Protection

Robust and reliable bus node design often requires the use of external transient protection devices in order to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3 MHz to 300 MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use Vcc and ground planes to provide low inductance. Note that high frequency currents follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
4. Apply 100 to 220-nF decoupling capacitors as close as possible to the V_{CC} pins of transceiver and UART or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Use 1 to 10-k pull-up or pull-down resistors for enable lines to limit noise currents in theses lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
   – While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few-hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to about 200 mA.

11.2 Layout Example

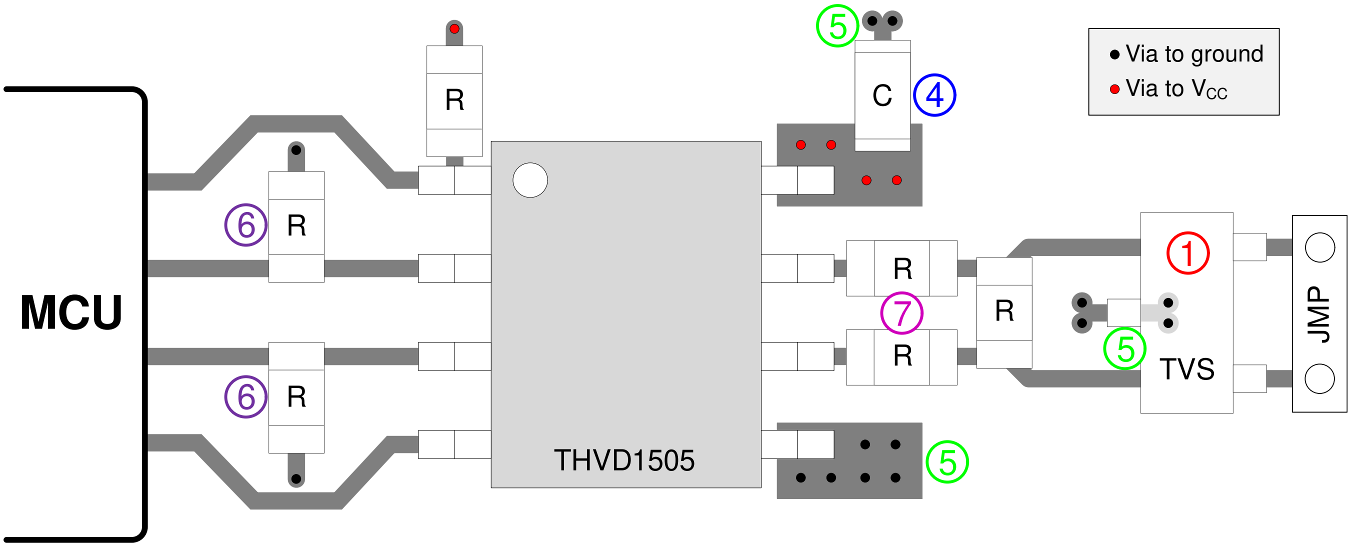


Figure 32. THVD1505 Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THVD1505DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1505
THVD1505DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1505

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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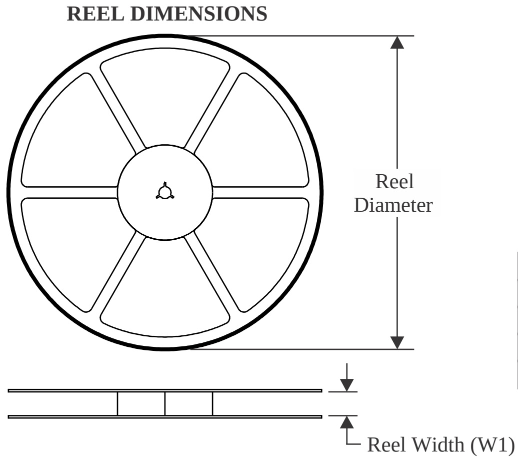
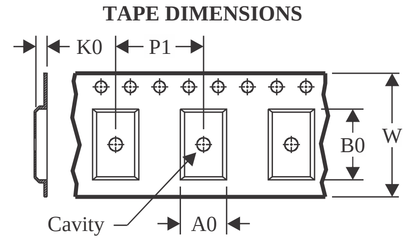
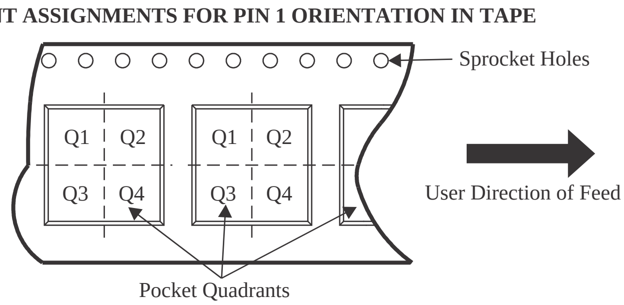
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





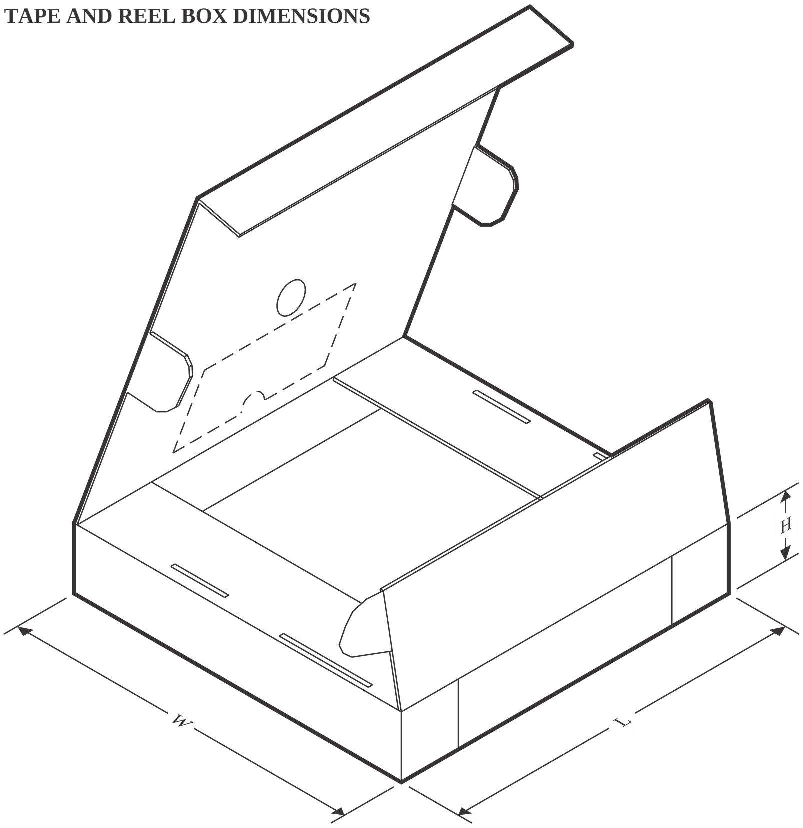
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

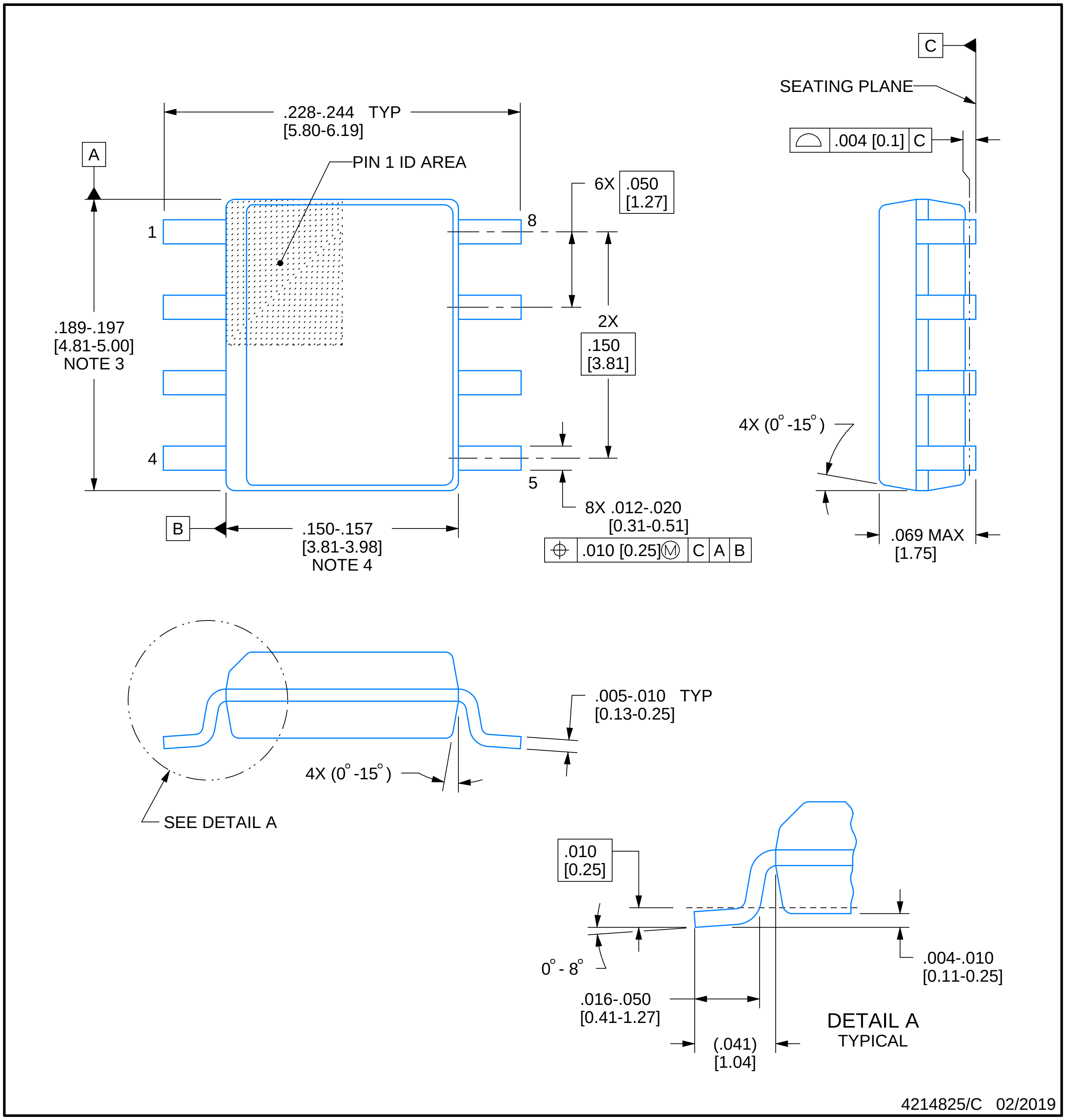
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD1505DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



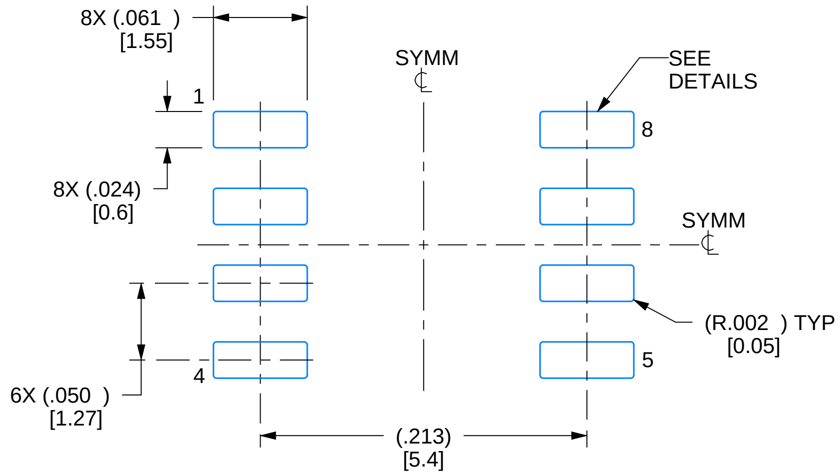
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD1505DR	SOIC	D	8	2500	353.0	353.0	32.0

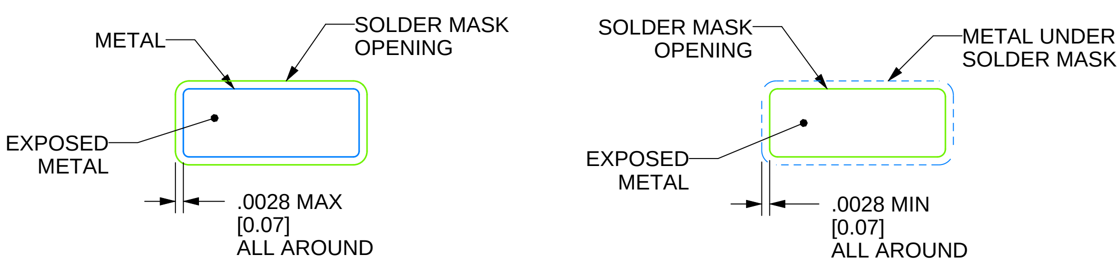


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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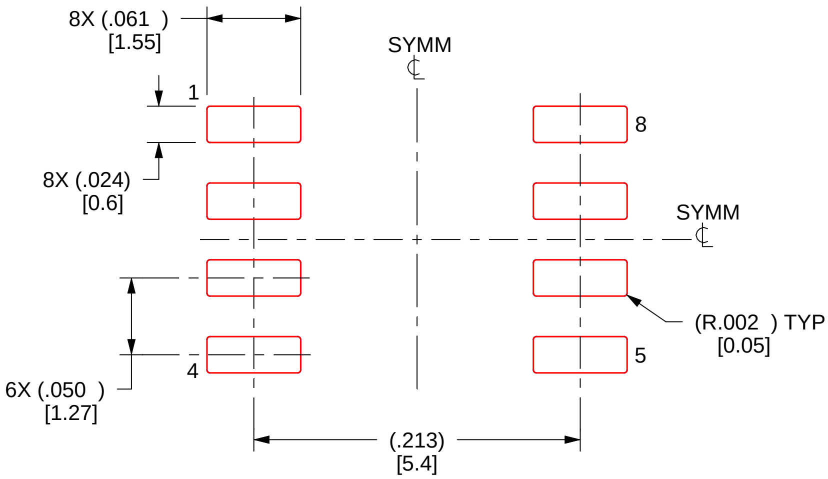
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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