

THVD24xxV-EP Enhanced 3V to 5.5V RS-485 Transceivers With 1.8V VIO Capability

1 Features

- Meets or exceeds the requirements of the TIA/EIA-485A and TIA/EIA-422B standards
- Enhanced Product
 - Military temperature range (-55°C to 125°C)
 - One wafer fabrication site and one assembly and test site
 - Gold bond wire, NiPdAu lead finish
 - Wafer lot traceability
 - Extended product life cycle
- 3V to 5.5V supply voltage
- Differential output exceeds 2.1V for PROFIBUS compatibility with 5V supply
- 1.65V to 5.5V Supply for data and enable signals
- SLR Pin Selectable Data Rates:
 - THVD2410V-EP : 250kbps and 1Mbps
 - THVD2450V-EP, THVD2452V-EP: 20Mbps and 50Mbps
- Bus I/O protection
 - $\pm 70\text{V}$ DC bus fault
 - $\pm 16\text{kV}$ HBM ESD
 - THVD2410V-EP, THVD2450V-EP
 - $\pm 15\text{kV}$ IEC 61000-4-2 contact and air-gap discharge
 - THVD2452V-EP
 - $\pm 8\text{kV}$ IEC 61000-4-2 contact and air-gap discharge
 - $\pm 4\text{kV}$ IEC 61000-4-4 fast transient burst
- Half-duplex and full-duplex devices available in two speed grades
- Symmetric common mode voltage range: $\pm 12\text{V}$
- Enhanced receiver hysteresis for noise immunity
- Low power consumption
 - Low shutdown supply current: $< 1\mu\text{A}$
 - Current during operation: $< 5.3\text{mA}$
- Glitch-free power-up/down for hot plug-in capability
- Open, short, and idle bus failsafe
- Thermal shutdown
- 1/8 unit load (up to 256 bus nodes)
- Small mm x 3mm VSON package (half-duplex) to save board space, or 14-D (full-duplex) for drop-in compatibility

3 Description

THVD24xxV-EP are $\pm 70\text{V}$ fault-protected, half and full-duplex RS-422/RS-485 transceivers using a 1.65V to 5.5V logic supply for data and enable logic signals, and a 3V to 5.5V bus side supply. These devices have slew rate select feature that enables them to be used at two maximum speeds based on the SLR pin setting

These devices feature integrated IEC ESD protection, eliminating the need for external system-level protection components. The $\pm 12\text{V}$ input common-mode range makes reliable data communication over longer cable run lengths and/or in the presence of large ground loop voltages. Enhanced 250mV receiver hysteresis provides high noise rejection. In addition, the receiver fail-safe feature makes sure of a logic high when the inputs are open or shorted together.

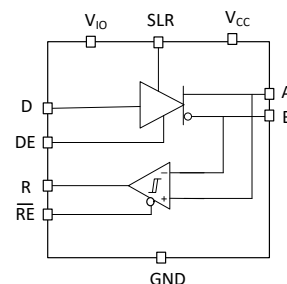
THVD24xxV-EP half-duplex devices are available in small VSON package for space-constrained applications. The devices are available in standard 14-SOIC package.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
THVD2410V-EP THVD2450V-EP	VSON (10)	3mm × 3mm
THVD2452V-EP	SOIC (14)	8.65mm × 6mm

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



THVD2410V-EP and THVD2450V-EP Simplified Schematic

2 Applications

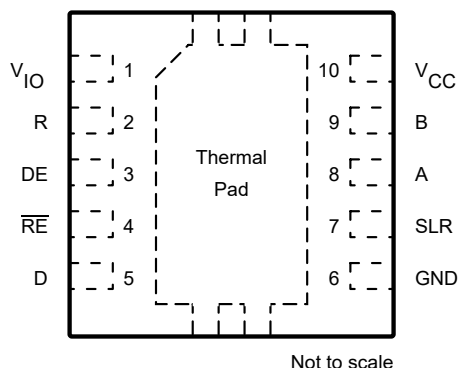
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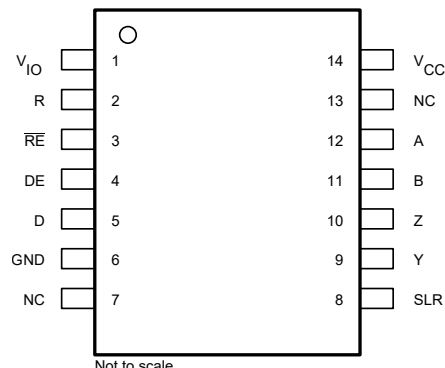
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4 Pin Configuration and Functions



**Figure 4-1. THVD2410V-EP, THVD2450V-EP
10-Pin DRC Package (VSON)
(Top View)**



**Figure 4-2. THVD2452V-EP
14-Pin D Package (SOIC)
(Top View)**

Table 4-1. Pin Functions

NAME	PIN NO.		TYPE	DESCRIPTION
	DRC	D		
V _{IO}	1	1	Logic Supply	1.65V to 5.5V supply for logic I/O signals R, \overline{RE} , D, DE, and SLR)
R	2	2	Digital Output	Receive data output
DE	3	4	Digital Input	Driver enable input; integrated pull-down
\overline{RE}	4	3	Digital Input	Receiver enable input; integrated pull-up
D	5	5	Digital Input	Transmission data input; integrated pull-up
GND	6	6	Reference Potential	Local device ground
SLR	7	8	Digital Input	Slew rate select ; integrated pull-down. For THVD2410V-EP: Low = 1Mbps, High = 250kbps. Defaults to 1Mbps if SLR is left floating. For THVD2450V-EP and THVD2452V-EP: Low = 50Mbps, High = 20Mbps. Defaults to 50Mbps if left floating.
A	8	12	Bus Input	Bus I/O (half-duplex), bus input (full-duplex)
B	9	11	Bus Input	Bus I/O (half-duplex), bus input (full-duplex)
V _{CC}	10	14	Bus Supply	3V to 5.5V supply for the transceiver
Y	-	9	Bus Output	Bus output, Y
Z	-	10	Bus Output	Bus output, Z
NC	-	7, 13		No connect pin. Internally not connected

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ^{(1) (2)}

		MIN	MAX	UNIT
Logic supply voltage	V_{IO}	-0.5	$V_{CC} + 0.2$	V
Bus supply voltage	V_{CC}	-0.5	6.5	V
Bus voltage	Range at any bus pin as differential or common-mode with respect to GND	-70	70	V
Input voltage	Range at any logic pin (D, DE, SLR or \overline{RE})	-0.3	$V_{IO} + 0.2$	V
Receiver output current	I_O	-24	24	mA
Storage temperature	T_{stg}	-65	170	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

5.2 ESD Ratings

				VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	Bus terminals and GND	±16,000	V
			All pins except bus terminals and GND	±4,000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾		±1,500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings [IEC]

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge, Half duplex devices THVD2410V/2450V-EP ⁽¹⁾	Contact discharge, per IEC 61000-4-2	Bus terminals and GND	±15,000	V
		Air-gap discharge, per IEC 61000-4-2	Bus terminals and GND	±15,000	
$V_{(ESD)}$	Electrostatic discharge, Full duplex devices THVD2452V-EP ⁽¹⁾	Contact discharge, per IEC 61000-4-2	Bus terminals and GND	±8,000	V
		Air-gap discharge, per IEC 61000-4-2	Bus terminals and GND	±8,000	
$V_{(EFT)}$	Electrical fast transient	Per IEC 61000-4-4	Bus terminals	±4,000	V

- (1) For optimized IEC ESD performance, it is recommended to have series resistor ($\geq 50 \Omega$) on all logic inputs to minimize transient currents going into or out of the logic pins.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		3		5.5	V
V _{IO}	I/O supply voltage		1.65		V _{CC}	V
V _I	Input voltage at any bus terminal (separately or common mode) ⁽¹⁾		–12		12	V
V _{IH}	High-level input voltage (driver, driver enable, receiver enable and slew rate select inputs)		0.7*V _{IO}		V _{IO}	V
V _{IL}	Low-level input voltage (driver, driver enable, receiver enable and slew rate select inputs)		0		0.3*V _{IO}	V
V _{ID}	Differential input voltage bus pins		–25		25	V
I _O	Output current, driver		–60		60	mA
I _{OR}	Output current, receiver	V _{IO} = 1.8 V or 2.5 V	–4		4	mA
I _{OR}	Output current, receiver	V _{IO} = 3.3 V or 5 V	–8		8	mA
R _L	Differential load resistance		54	60		Ω
1/t _{UI}	Signaling rate	THVD2410V, THVD2412V with SLR = V _{IO}			250	kbps
		THVD2410V, THVD2412V with SLR = GND or floating			1	Mbps
		THVD2450V, THVD2452V with SLR = V _{IO}			20	Mbps
		THVD2450V, THVD2452V with SLR = GND or floating			50	Mbps
T _A	Operating ambient temperature		–55		125	°C
T _J	Junction temperature		–55		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

5.5 Thermal Information

THERMAL METRIC ⁽¹⁾		THVD2410V-EP THVD2450V-EP	THVD2452V-EP	UNIT
		DRC (VSON)	D (SOIC)	
		10 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	46.7	87.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	47.7	41.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	19.1	43.7	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.7	8.1	°C/W
ψ _{JB}	Junction-to-board characterization parameter	19.1	43.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	4.6	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.6 Power Dissipation

PARAMETER		TEST CONDITIONS			VALUE	UNIT
P _D	Driver and receiver enabled, loopback for full duplex devices (A connected to Y, B connected to Z) V _{CC} = 5.5 V, T _A = 125 °C, square wave at 50% duty cycle	Unterminated R _L = 300 Ω, C _L = 50 pF (driver)	THVD2410V-EP	250 kbps	160	mW
				1Mbps	250	
			THVD2450V-EP	20Mbps	310	
			THVD2452V-EP	50 Mbps	630	
		RS-422 load R _L = 100 Ω, C _L = 50 pF (driver)	THVD2410V-EP	250 kbps	170	mW
				1Mbps	250	
			THVD2450V-EP	20Mbps	290	
			THVD2452V-EP	50 Mbps	570	
		RS-485 load R _L = 54 Ω, C _L = 50 pF (driver)	THVD2410V-EP	250 kbps	220	mW
				1Mbps	280	
			THVD2450V-EP	20Mbps	325	
			THVD2452V-EP	50 Mbps	560	

5.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of $V_{CC} = 5\text{ V}$, $V_{IO} = 3.3\text{ V}$, unless otherwise noted. ⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver						
$ V_{OD} $	Driver differential output voltage magnitude	$R_L = 60\ \Omega$, $-25\text{ V} \leq V_{\text{test}} \leq 25\text{ V}$ (See Figure 6-1)	1.5	3.3		V
		$R_L = 60\ \Omega$, $-25\text{ V} \leq V_{\text{test}} \leq 25\text{ V}$, $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ (See Figure 6-1)	2.1	3.3		V
		$R_L = 100\ \Omega$ (See Figure 6-2)	2	4		V
		$R_L = 54\ \Omega$ (See Figure 6-2)	1.5	3.5		V
$\Delta V_{OD} $	Change in differential output voltage	$R_L = 54\ \Omega$ or $100\ \Omega$ (See Figure 6-2)	-50		50	mV
V_{OC}	Common-mode output voltage	$R_L = 54\ \Omega$ or $100\ \Omega$ (See Figure 6-2)	1	$V_{CC}/2$	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	$R_L = 54\ \Omega$ or $100\ \Omega$ (See Figure 6-2)	-50		50	mV
I_{OS}	Short-circuit output current	$DE = V_{IO}$, $-70\text{ V} \leq (V_A \text{ or } V_B) \leq 70\text{ V}$, or A shorted to B (A,B are driver terminals for half duplex, Y/Z are for full duplex)	-250		250	mA
Receiver						
I_I	Bus input current	$DE = 0\text{ V}$, V_{CC} and $V_{IO} = 0\text{ V}$ or 5.5 V	$V_I = 12\text{ V}$	90	125	μA
			$V_I = 25\text{ V}$	200	250	μA
			$V_I = -7\text{ V}$	-100	-80	μA
			$V_I = -25\text{ V}$	-350	-220	μA
V_{TH+}	Positive-going input threshold voltage ⁽²⁾	Over common-mode range of $\pm 12\text{ V}$	40	125	200	mV
V_{TH-}	Negative-going input threshold voltage ⁽²⁾		-200	-125	-40	mV
V_{HYS}	Input hysteresis			250		mV
V_{TH_FSH}	Input fail-safe threshold		-40		40	mV
$C_{A,B}$	Input differential capacitance	Measured between A and B, $f = 1\text{ MHz}$		50		pF
V_{OH}	Output high voltage	$I_{OH} = -8\text{ mA}$, $V_{IO} = 3\text{ to }3.6\text{ V}$ or $4.5\text{ V to }5.5\text{ V}$	$V_{IO} - 0.4$	$V_{IO} - 0.2$		V
V_{OL}	Output low voltage	$I_{OL} = 8\text{ mA}$, $V_{IO} = 3\text{ to }3.6\text{ V}$ or $4.5\text{ V to }5.5\text{ V}$		0.2	0.4	V
V_{OH}	Output high voltage	$I_{OH} = -4\text{ mA}$, $V_{IO} = 1.65\text{ to }1.95\text{ V}$ or $2.25\text{ V to }2.75\text{ V}$	$V_{IO} - 0.4$	$V_{IO} - 0.2$		V
V_{OL}	Output low voltage	$I_{OL} = 4\text{ mA}$, $V_{IO} = 1.65\text{ to }1.95\text{ V}$ or $2.25\text{ V to }2.75\text{ V}$		0.2	0.4	V
I_{OZ}	Output high-impedance current, R pin	$V_O = 0\text{ V}$ or V_{IO} , $RE = V_{IO}$	-1		1	μA
Logic						
I_{IN}	Input current (DE, SLR)	$1.65\text{ V} \leq V_{IO} \leq 5.5\text{ V}$, $0\text{ V} \leq V_{IN} \leq V_{IO}$			5	μA
I_{IN}	Input current (D, RE)	$1.65\text{ V} \leq V_{IO} \leq 5.5\text{ V}$, $0\text{ V} \leq V_{IN} \leq V_{IO}$	-5			μA
Thermal Protection						
T_{SHDN}	Thermal shutdown threshold	Temperature rising	150	180		°C
T_{HYS}	Thermal shutdown hysteresis			10		°C
Supply						
UV_{VCC} (rising)	Rising under-voltage threshold on V_{CC}			2.3	2.6	V
UV_{VCC} (falling)	Falling under-voltage threshold on V_{CC}		1.95	2.2		V
$UV_{VCC(hys)}$	Hysteresis on under-voltage of V_{CC}			150		mV
UV_{VIO} (rising)	Rising under-voltage threshold on V_{IO}			1.4	1.6	V
UV_{VIO} (falling)	Falling under-voltage threshold on V_{IO}		1.2	1.3		V

5.7 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of $V_{CC} = 5\text{ V}$, $V_{IO} = 3.3\text{ V}$, unless otherwise noted. ⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$UV_{VIO(hys)}$	Hysteresis on under-voltage of V_{IO}				30		mV
I_{CC}	Supply current (quiescent), $V_{CC} = 4.5\text{ V}$ to 5.5 V	Driver and receiver enabled	$\overline{RE} = 0\text{ V}$, $DE = V_{IO}$, No load		3.5	5.3	mA
		Driver enabled, receiver disabled	$RE = V_{IO}$, $DE = V_{IO}$, No load		2.5	4.2	mA
		Driver disabled, receiver enabled	$\overline{RE} = 0\text{ V}$, $DE = 0\text{ V}$, No load		1.8	2.4	mA
		Driver and receiver disabled	$\overline{RE} = V_{IO}$, $DE = 0\text{ V}$, D = open, No load		0.1	1.2	μA
I_{CC}	Supply current (quiescent), $V_{CC} = 3\text{ V}$ to 3.6 V	Driver and receiver enabled	$\overline{RE} = 0\text{ V}$, $DE = V_{IO}$, No load		3	4.1	mA
		Driver enabled, receiver disabled	$\overline{RE} = V_{IO}$, $DE = V_{IO}$, No load		2	3	mA
		Driver disabled, receiver enabled	$\overline{RE} = 0\text{ V}$, $DE = 0\text{ V}$, No load		1.6	2.2	mA
		Driver and receiver disabled	$\overline{RE} = V_{IO}$, $DE = 0\text{ V}$, D = open, No load		0.1	1	μA
I_{IO}	Logic supply current (quiescent), $V_{IO} = 3$ to 3.6 V	Driver disabled, Receiver enabled, SLR = GND	$DE = 0\text{ V}$, $\overline{RE} = 0\text{ V}$, No load		4.5	8.4	μA
		Driver disabled, Receiver enabled, SLR = V_{IO}	$DE = 0\text{ V}$, $\overline{RE} = 0\text{ V}$, No load		3.3	8.4	μA
		Driver disabled, Receiver disabled, SLR = GND	$DE = 0\text{ V}$, $\overline{RE} = V_{IO}$, No load		0.1	1	μA
		Driver disabled, Receiver disabled, SLR = V_{IO}	$DE = 0\text{ V}$, $\overline{RE} = V_{IO}$, No load		1.8	4	μA

(1) A, B are driver output and receiver input terminals for Half duplex devices; A/B are Receiver input, Y/Z are driver output terminals for Full duplex devices

(2) Under any specific conditions, V_{TH+} is assured to be at least V_{HYS} higher than V_{TH-} .

5.8 Switching Characteristics - 250 kbps

250-kbps (THVD2410V-EP with SLR = V_{IO}) over recommended operating conditions. All typical values are at 25°C and supply voltage of $V_{CC} = 5\text{ V}$, $V_{IO} = 3.3\text{ V}$, unless otherwise noted. ⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time	$V_{CC} = 3$ to 3.6 V, Typical at 3.3V	$R_L = 54\ \Omega, C_L = 50\text{ pF}$ See Figure 6-3	450	560	1200	ns
		$V_{CC} = 4.5$ to 5.5 V, Typical at 5 V		500	625	1200	ns
t_{PHL}, t_{PLH}	Propagation delay	$V_{CC} = 3$ to 3.6 V, Typical at 3.3V			500	720	ns
		$V_{CC} = 4.5$ to 5.5 V, Typical at 5 V			540	770	ns
$t_{SK(P)}$	Pulse skew, $ t_{PHL} - t_{PLH} $	$V_{CC} = 3$ to 3.6 V, Typical at 3.3V			10	70	ns
		$V_{CC} = 4.5$ to 5.5 V, Typical at 5 V			10	70	ns
t_{PHZ}, t_{PLZ}	Disable time	$RE = X$	See Figure 6-4 and Figure 6-5		40	75	ns
t_{PZH}, t_{PZL}	Enable time	$RE = 0\text{ V}$			70	280	ns
		$RE = V_{IO}$			2.5	4.5	μs
t_{SHDN}	Time to shutdown	$RE = V_{IO}$			50		500
Receiver							
t_r, t_f	Output rise/fall time	$C_L = 15\text{ pF}$	See Figure 6-6		7	20	ns
t_{PHL}, t_{PLH}	Propagation delay				800	1270	ns
$t_{SK(P)}$	Pulse skew, $ t_{PHL} - t_{PLH} $				5	45	ns
t_{PHZ}, t_{PLZ}	Disable time	$DE = X$			30	40	ns
$t_{PZH(1)}$	Enable time	$V_{IO} = 3\text{ V to }3.6\text{ V}; DE = V_{IO}$	See Figure 6-7		90	120	ns
		$V_{IO} = 1.65\text{ V to }1.95\text{ V}; DE = V_{IO}$			100	130	ns
$t_{PZL(1)}$		$V_{IO} = 3\text{ V to }3.6\text{ V}; DE = V_{IO}$			900	1320	ns
		$V_{IO} = 1.65\text{ V to }1.95\text{ V}; DE = V_{IO}$			900	1320	ns
$t_{PZH(2)}, t_{PZL(2)}$	Enable time	$DE = 0\text{ V}$	See Figure 6-8		3.3	5.4	μs
$t_{D(OFS)}$	Delay to enter fail-safe operation	$C_L = 15\text{ pF}$	See Figure 6-9	7	11	18	μs
$t_{D(FSO)}$	Delay to exit fail-safe operation				540	800	1260
t_{SHDN}	Time to shutdown	$DE = 0\text{ V}$	See Figure 6-8	50		500	ns

(1) A, B are driver output and receiver input terminals for Half duplex devices; A/B are Receiver input, Y/Z are driver output terminals for Full duplex device

5.9 Switching Characteristics - 1 Mbps

1Mbps (THVD2410V-EP with SLR = 0 or floating) over recommended operating conditions. All typical values are at 25°C and supply voltage of $V_{CC} = 5\text{ V}$, $V_{IO} = 3.3\text{ V}$, unless otherwise noted. ⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r , t_f	Differential output rise/fall time	$V_{CC} = 3$ to 3.6 V, Typical at 3.3 V	$R_L = 54\ \Omega$, $C_L = 50\text{ pF}$ See Figure 6-3	125	150	300	ns
		$V_{CC} = 4.5$ to 5.5 V, Typical at 5 V		130	160	300	ns
t_{PHL} , t_{PLH}	Propagation delay	$V_{CC} = 3$ to 3.6 V, Typical at 3.3 V			160	240	ns
		$V_{CC} = 4.5$ to 5.5 V, Typical at 5 V			185	280	ns
$t_{SK(P)}$	Pulse skew, $ t_{PHL} - t_{PLH} $	$V_{CC} = 3$ to 3.6 V, Typical at 3.3 V			2	20	ns
		$V_{CC} = 4.5$ to 5.5 V, Typical at 5 V			2	15	ns
t_{PHZ} , t_{PLZ}	Disable time	$\overline{RE} = X$	See Figure 6-4 and Figure 6-5		40	95	ns
t_{PZH} , t_{PZL}	Enable time	$\overline{RE} = 0\text{ V}$			90	275	ns
		$\overline{RE} = V_{IO}$			3	4.6	μs
t_{SHDN}	Time to shutdown	$\overline{RE} = V_{IO}$		50		500	ns
Receiver							
t_r , t_f	Output rise/fall time	$C_L = 15\text{ pF}$	See Figure 6-6		7	15	ns
t_{PHL} , t_{PLH}	Propagation delay				50	85	ns
$t_{SK(P)}$	Pulse skew, $ t_{PHL} - t_{PLH} $				4	12.5	ns
t_{PHZ} , t_{PLZ}	Disable time	$DE = X$			30	40	ns
$t_{PZH(1)}$, $t_{PZL(1)}$	Enable time	$V_{IO} = 3\text{ V to }3.6\text{ V}$; $DE = V_{IO}$	See Figure 6-7		90	120	ns
		$V_{IO} = 1.65\text{ V to }1.95\text{ V}$; $DE = V_{IO}$			90	130	ns
$t_{PZH(2)}$, $t_{PZL(2)}$	Enable time	$DE = 0\text{ V}$	See Figure 6-8		3	4.5	μs
$t_{D(OFS)}$	Delay to enter fail-safe operation	$C_L = 15\text{ pF}$	See Figure 6-9	7	10	18	μs
$t_{D(FSO)}$	Delay to exit fail-safe operation			27	40	60	ns
t_{SHDN}	Time to shutdown	$DE = 0\text{ V}$	See Figure 6-8	50		500	ns

(1) A, B are driver output and receiver input terminals for Half duplex devices; A/B are Receiver input, Y/Z are driver output terminals for Full duplex device

5.10 Switching Characteristics - 20 Mbps

20-Mbps (THVD2450V-EP, THVD2452V-EP with SLR = V_{IO}) over recommended operating conditions. All typical values are at 25°C and supply voltage of $V_{CC} = 5\text{ V}$, $V_{IO} = 3.3\text{ V}$, unless otherwise noted. ⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t _r , t _f	Differential output rise/fall time	V _{CC} = 3 to 3.6 V, Typical at 3.3 V	R _L = 54 Ω, C _L = 50 pF See Figure 6-3	4	8	15	ns
		V _{CC} = 4.5 to 5.5 V, Typical at 5 V		4	7	15	ns
t _{PHL} , t _{PLH}	Propagation delay	V _{CC} = 3 to 3.6 V, Typical at 3.3 V		6	12	30	ns
		V _{CC} = 4.5 to 5.5 V, Typical at 5 V		4	9	26	ns
t _{SK(P)}	Pulse skew, t _{PHL} – t _{PLH}	V _{CC} = 3 to 3.6 V, Typical at 3.3 V			1	3	ns
		V _{CC} = 4.5 to 5.5 V, Typical at 5 V			1	3	ns
t _{PHZ} , t _{PLZ}	Disable time	RE = X	See Figure 6-4 and Figure 6-5		17	35	ns
t _{PZH} , t _{PZL}	Enable time	RE = 0 V			14	39	ns
		RE = V _{IO}			3	4.5	μs
t _{SHDN}	Time to shutdown	RE = V _{IO}		50		500	ns
Receiver							
t _r , t _f	Output rise/fall time	C _L = 15 pF	See Figure 6-6		1.5	6	ns
t _{PHL} , t _{PLH}	Propagation delay	V _{IO} = 3 V to 3.6 V		25	33	58	ns
		V _{IO} = 1.65 V to 1.95 V		25	35	60	ns
t _{SK(P)}	Pulse skew, t _{PHL} – t _{PLH}	C _L = 15 pF			0.5	5	ns
t _{PHZ} , t _{PLZ}	Disable time	DE = X			12	25	ns
t _{PZH(1)} , t _{PZL(1)}	Enable time	DE = V _{IO}	See Figure 6-7		50	82	ns
t _{PZH(2)} , t _{PZL(2)}	Enable time	DE = 0 V	See Figure 6-8		2.8	5	μs
t _{D(OFS)}	Delay to enter fail-safe operation	C _L = 15 pF	See Figure 6-9	7	10	18	μs
t _{D(FSO)}	Delay to exit fail-safe operation			19	32	50	ns
t _{SHDN}	Time to shutdown	DE = 0 V	See Figure 6-8	50		500	ns

(1) A, B are driver output and receiver input terminals for Half duplex devices; A/B are Receiver input, Y/Z are driver output terminals for Full duplex device

5.11 Switching Characteristics - 50 Mbps

50-Mbps (THVD2450V-EP, THVD2452V-EP with SLR = 0 or floating) over recommended operating conditions. All typical values are at 25°C and supply voltage of $V_{CC} = 5\text{ V}$, $V_{IO} = 3.3\text{ V}$, unless otherwise noted. ⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t _r , t _f	Differential output rise/fall time	V _{IO} = 3 V to 3.6 V, V _{CC} = 3 to 3.6 V, Typical at 3.3 V	R _L = 54 Ω, C _L = 50 pF See Figure 6-3	1	5	7	ns
		V _{CC} = 4.5 to 5.5 V, Typical at 5 V		1	5	6	ns
t _{PHL} , t _{PLH}	Propagation delay	V _{IO} = 3 V to 3.6 V, V _{CC} = 3 to 3.6 V, Typical at 3.3 V		5	11	19	ns
		V _{IO} = 1.65 V to 1.95 V, V _{CC} = 3 to 3.6 V, Typical at 3.3 V		7	12	22	ns
		V _{IO} = 3 V to 3.6 V, V _{CC} = 4.5 to 5.5 V, Typical at 5 V		4	8	15	ns
		V _{IO} = 1.65 V to 1.95 V, V _{CC} = 4.5 to 5.5 V, Typical at 5 V		6	10	19	ns
		t _{SK(P)}		Pulse skew, t _{PHL} – t _{PLH}	V _{CC} = 3 to 3.6 V, Typical at 3.3 V	1	3
V _{CC} = 4.5 to 5.5 V, Typical at 5 V	1				3	ns	
t _{PHZ} , t _{PLZ}	Disable time	RE = X		See Figure 6-4 and Figure 6-5	14	30	ns
t _{PZH} , t _{PZL}	Enable time	RE = 0 V ; V _{IO} = 1.65 V to 1.95 V, 2.25 V to 2.75 V			20	35	ns
		RE = 0 V ; V _{IO} = 3 V to V _{CC} V	15		32	ns	
		RE = V _{IO}	2.5		4.5	μs	
t _{SHDN}	Time to shutdown	RE = V _{IO}	50		500	ns	
Receiver							
t _r , t _f	Output rise/fall time	C _L = 15 pF	See Figure 6-6	1.5	6	ns	
t _{PHL} , t _{PLH}	Propagation delay	C _L = 15 pF, V _{IO} = 3 V to 3.6 V	See Figure 6-6	25	33	58	ns
t _{PHL} , t _{PLH}	Propagation delay	C _L = 15 pF, V _{IO} = 1.65 V to 1.95 V	See Figure 6-6	25	35	60	ns
t _{SK(P)}	Pulse skew, t _{PHL} – t _{PLH}	C _L = 15 pF	See Figure 6-6	0.5	5	ns	
t _{PHZ} , t _{PLZ}	Disable time	DE = X		12	25	ns	
t _{PZH(1)} , t _{PZL(1)}	Enable time	DE = V _{IO}	V _{IO} = 1.65 V to 1.95 V, See Figure 6-7	50	82	ns	
			V _{IO} = 3 V to 3.6 V, See Figure 6-7	50	75	ns	
t _{PZH(2)} , t _{PZL(2)}	Enable time	DE = 0 V	See Figure 6-8	2.8	5	μs	
t _{D(OFS)}	Delay to enter fail-safe operation	C _L = 15 pF	See Figure 6-9	7	10	18	μs
t _{D(FSO)}	Delay to exit fail-safe operation			19	32	50	ns
t _{SHDN}	Time to shutdown	DE = 0 V	See Figure 6-8	50	500	ns	

(1) A, B are driver output and receiver input terminals for Half duplex devices; A/B are Receiver input, Y/Z are driver output terminals for Full duplex device

5.12 Typical Characteristics

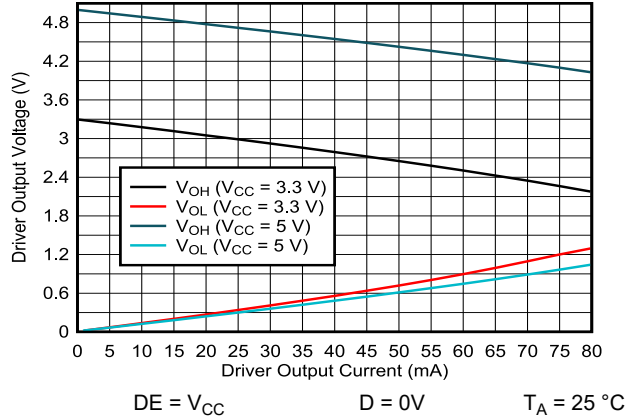


Figure 5-1. Driver Output Voltage vs Driver Output Current

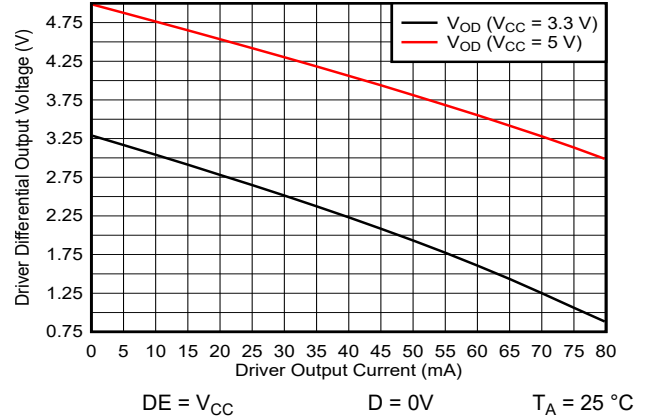


Figure 5-2. Driver Differential Output voltage vs Driver Output Current

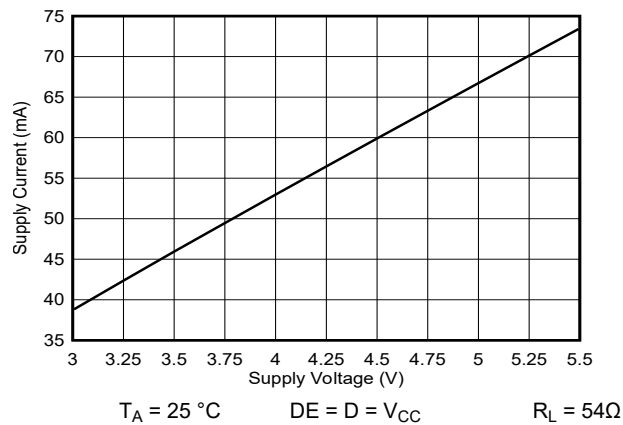


Figure 5-3. Driver Output Current vs Supply Voltage

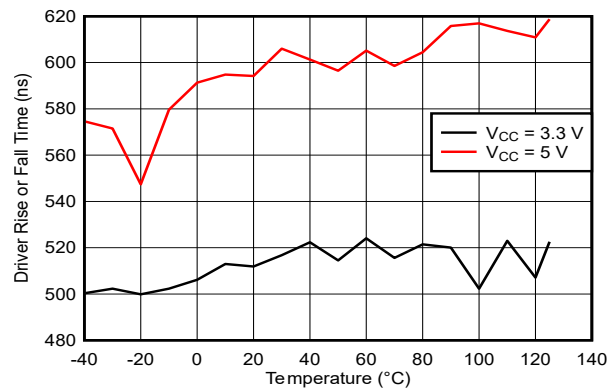


Figure 5-4. THVD2410V-EP Driver Rise or Fall Time vs Temperature

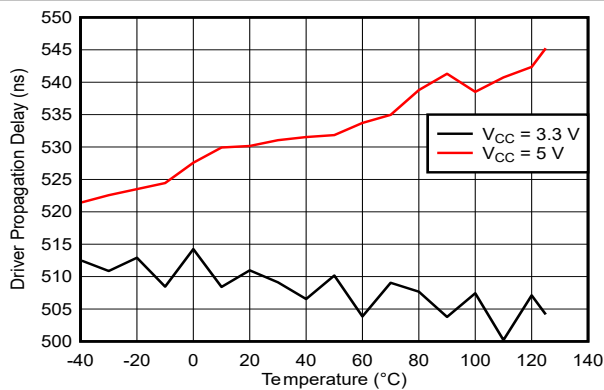


Figure 5-5. THVD2410V-EP Driver Propagation Delay vs Temperature

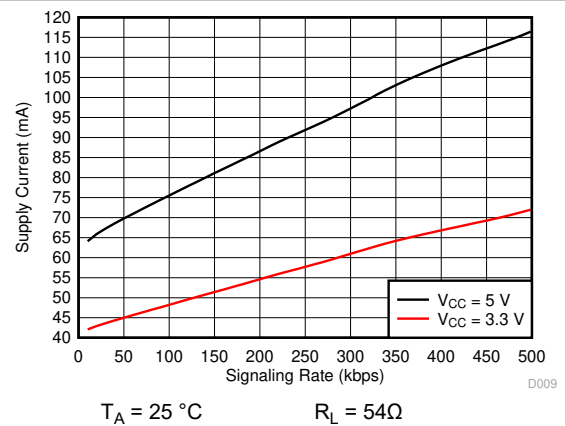


Figure 5-6. THVD2410V-EP Supply Current vs Signal Rate

5.12 Typical Characteristics (continued)

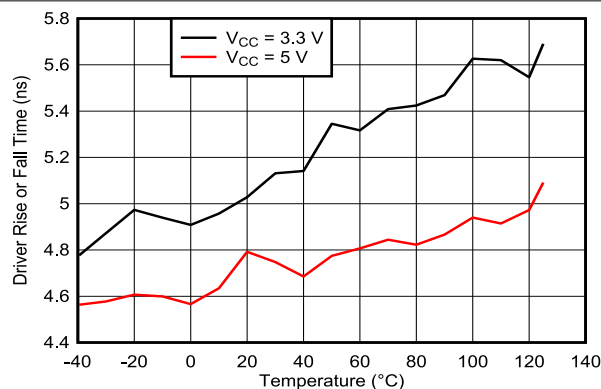


Figure 5-7. THVD2450V-EP: 50Mbps Driver Rise or Fall Time vs Temperature

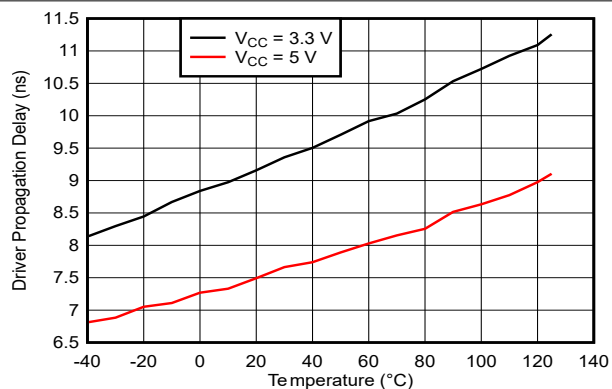


Figure 5-8. THVD2450V-EP: 50Mbps Driver Propagation Delay vs Temperature

6 Parameter Measurement Information

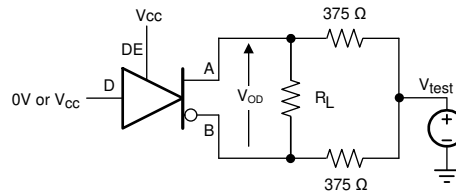


Figure 6-1. Measurement of Driver Differential Output Voltage With Common-Mode Load

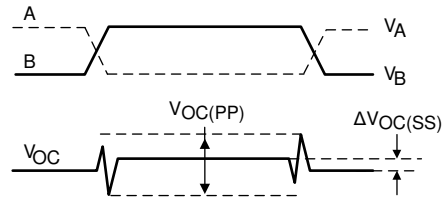
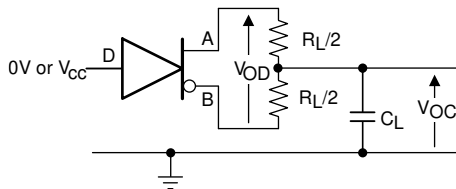


Figure 6-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

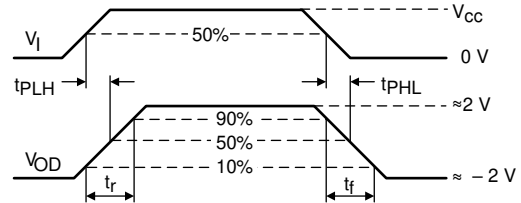
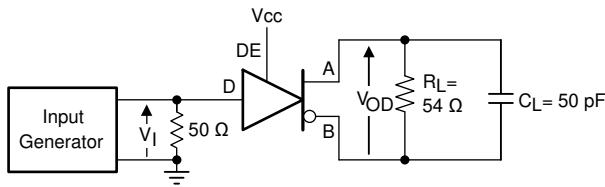
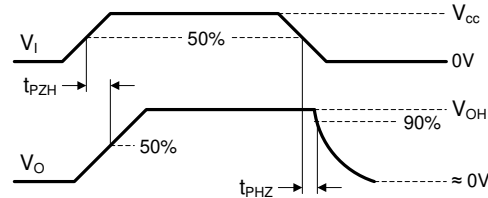
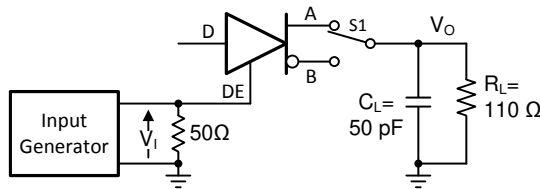
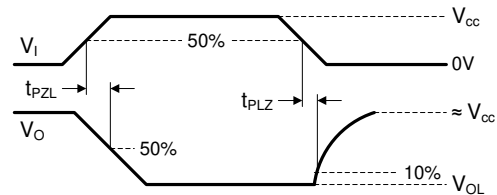
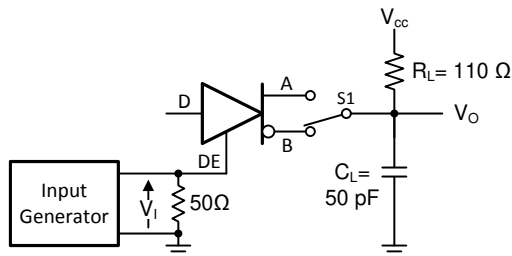


Figure 6-3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



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Figure 6-4. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load



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Figure 6-5. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

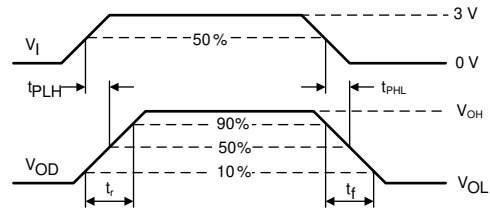
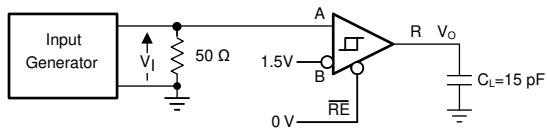


Figure 6-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

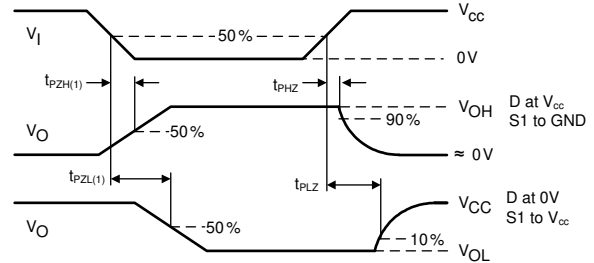
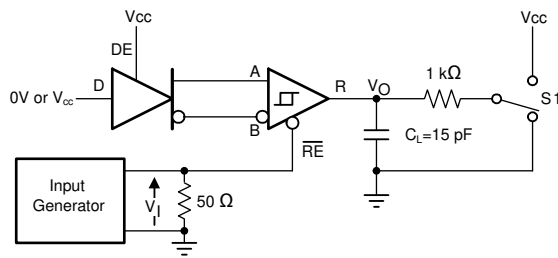
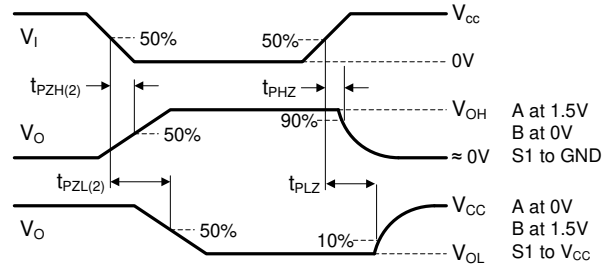
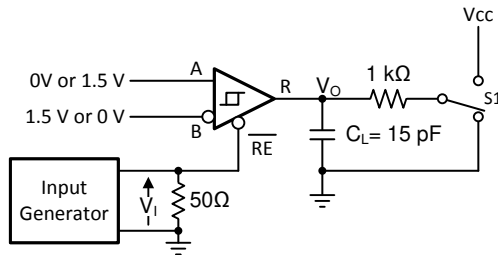
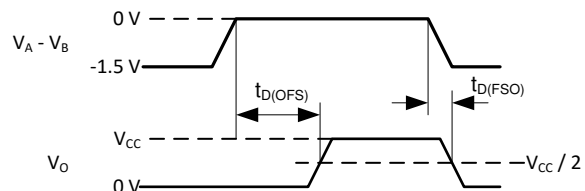
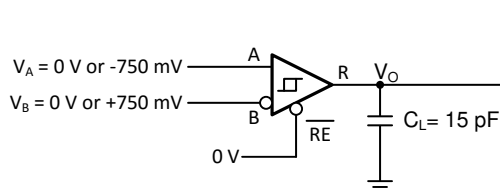


Figure 6-7. Measurement of Receiver Enable/Disable Times With Driver Enabled



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Figure 6-8. Measurement of Receiver Enable Times With Driver Disabled



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Figure 6-9. Measurement of Fail-Safe Delay

7 Detailed Description

7.1 Overview

THVD2410V-EP and THVD2450V-EP are fault-protected, half duplex RS-485 transceivers available in two speed grades suitable for data transmission up to 1Mbps and 50Mbps respectively. THVD2452V-EP is a full-duplex transceiver that can be configured for two speeds using the SLR pin: 20Mbps and 50Mbps. The devices have active-high driver enables and active-low receiver enables. A shutdown current of less than 1 μ A can be achieved by disabling both driver and receiver.

7.2 Functional Block Diagrams

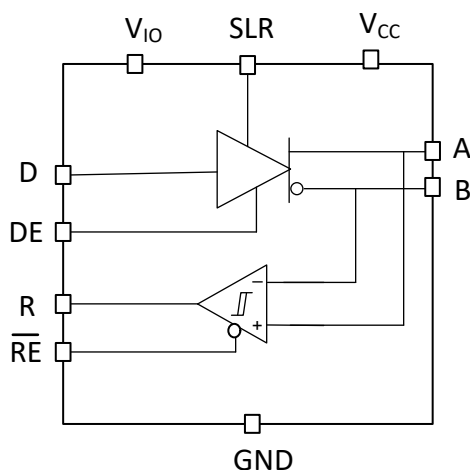


Figure 7-1. THVD2410V-EP and THVD2450V-EP Block Diagram

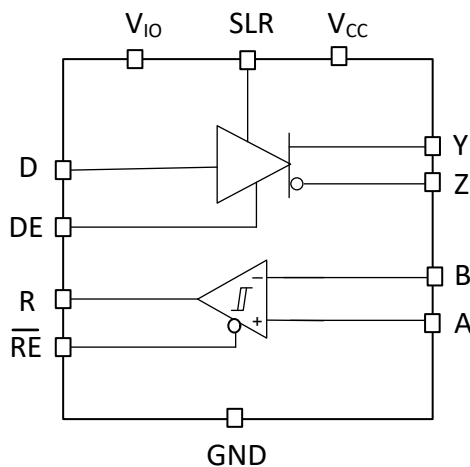


Figure 7-2. THVD2452V-EP Block Diagram

7.3 Feature Description

7.3.1 ± 70 -V Fault Protection

THVD24xxV-EP transceivers have extended bus fault protection compared to standard RS-485 devices. Transceivers that operate in rugged industrial environments are often exposed to voltage transients greater than the -7V to +12V defined by the TIA/EIA-485A standard. To protect against such conditions, the generic RS-485 devices with lower absolute maximum ratings requires expensive external protection components. To simplify system design and reduce overall system cost, THVD24xxV-EP devices are protected up to ± 70 V without the need for any external components.

7.3.2 Integrated IEC ESD and EFT Protection

Internal ESD protection circuits protect the transceivers against electrostatic discharges (ESD) according to IEC 61000-4-2 of up to $\pm 12\text{kV}$ and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to $\pm 4\text{kV}$. THVD24xxV-EP ESD structures help to limit voltage excursions and recover from them quickly that they allow EFT Criterion A at the system level (no data loss when transient noise is present).

7.3.3 Driver Overvoltage and Overcurrent Protection

The THVD24xxV-EP drivers are protected against any DC supply shorts in the range of -70V to $+70\text{V}$. The devices internally limit the short circuit current to $\pm 250\text{mA}$ to comply with the TIA/EIA-485A standard. In addition, a fold-back current limiting circuit further reduces the driver short circuit current to less than $\pm 5\text{mA}$ if the output fault voltage exceeds $|\pm 25\text{V}|$.

All devices feature thermal shutdown protection that disables the driver and the receiver if the junction temperature exceeds the T_{SHDN} threshold due to excessive power dissipation.

7.3.4 Enhanced Receiver Noise Immunity

The differential receivers of THVD24xxV-EP feature fully symmetric thresholds to maintain duty cycle of the signal even with small input amplitudes. In addition, 250mV (typical) hysteresis provides noise immunity.

7.3.5 Receiver Fail-Safe Operation

The receivers are fail-safe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the receiver outputs a fail-safe logic high state if the input amplitude stays for longer than $t_{\text{D(OFs)}}$ at less than $|V_{\text{TH_FSH}}|$.

7.3.6 Low-Power Shutdown Mode

Driving $\overline{\text{DE}}$ low and $\overline{\text{RE}}$ high for longer than 500ns puts the devices into the shutdown mode. If either $\overline{\text{DE}}$ goes high or $\overline{\text{RE}}$ goes low, the counters reset. The devices does not enter the shutdown mode if the enable pins are in disable state for less than 50ns . This feature prevents the devices from accidentally going into shutdown mode due to skew between $\overline{\text{DE}}$ and $\overline{\text{RE}}$.

7.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse: B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC} , thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 7-1. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A/Y	B/Z	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, \overline{RE} , is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is higher than the positive input threshold, V_{TH+} , the receiver output, R, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-} , the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-} the output is indeterminate.

When \overline{RE} is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

Table 7-2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A - V_B$	\overline{RE}	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

Table 7-3 shows SLR (slew rate select) pin functionality. SLR has integrated pull-down, so the device remains in higher speed mode until SLR is pulled high which limits the slew rate and puts the device in slower speed mode.

Table 7-3. SLR pin control

Device	Functionality w.r.t SLR pin
THVD2410V-EP	SLR = Low or floating: Both transmitter (TX) and receiver (RX) maximum speed is 1Mbps SLR = High: Both TX and RX maximum speed is limited to 250kbps
THVD2450V-EP, THVD2452V-EP	SLR = Low or floating: Both transmitter (TX) and receiver (RX) maximum speed is 50Mbps SLR = High: Both TX and RX maximum speed is limited to 20Mbps

Table 7-4 shows the device behavior in undervoltage scenarios:

Table 7-4. Supply Function Table

Supply Function Table	V _{IO}	Driver Output	Receiver Output
> UV _{VCC} (rising)	> UV _{VIO} (rising)	Determined by DE and D inputs	Determined by \overline{RE} and A-B
< UV _{VCC} (falling)	> UV _{VIO} (rising)	High impedance	High impedance
> UV _{VCC} (rising)	< UV _{VIO} (falling)	High impedance	High impedance
< UV _{VCC} (falling)	< UV _{VIO} (falling)	High impedance	High impedance

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

THVD2410 and THVD2450 are fault-protected, half-duplex RS-485 transceivers commonly used for asynchronous data transmissions. For these devices, the driver and receiver enable pins allow for the configuration of different operating modes.

8.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T , whose value matches the characteristic impedance, Z_0 , of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

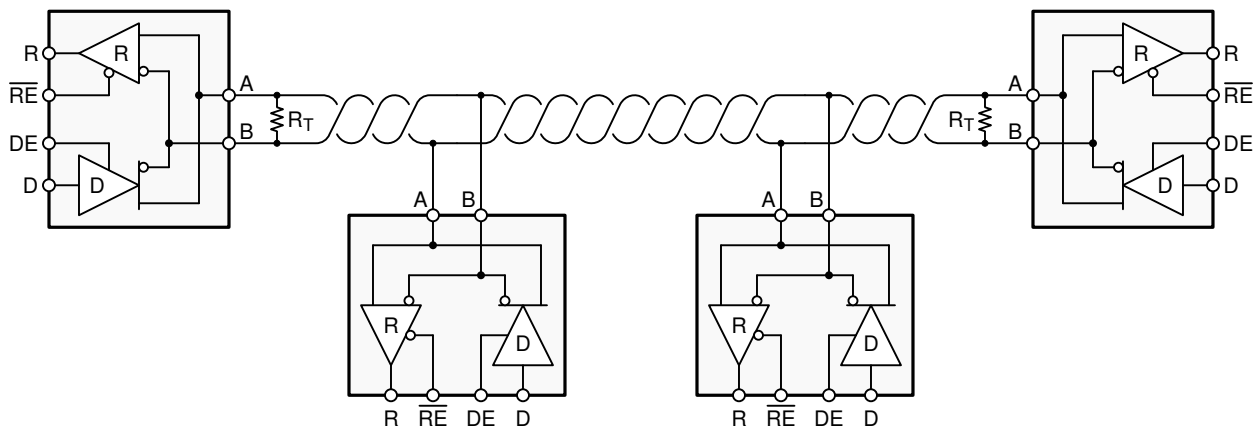


Figure 8-1. Typical RS-485 Network With Half-Duplex Transceivers

8.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

8.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10kbps and 100kbps, some applications require data rates up to 250kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

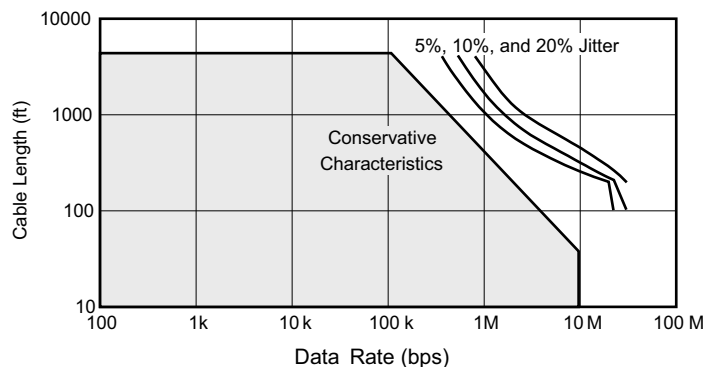


Figure 8-2. Cable Length vs Data Rate Characteristic

Even higher data rates are achievable (that is, 50Mbps for the THVD2450) in cases where the interconnect is short enough (or has suitably low attenuation at signal frequencies) to not degrade the data.

8.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections of varying phase as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{\text{(STUB)}} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

8.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12kΩ. Because the THVD24xxV-EP devices consist of 1/8 UL transceivers, connecting up to 256 receivers to the bus is possible.

8.2.1.4 Transient Protection

The bus pins of the THVD24xxV-EP transceivers include on-chip ESD protection against $\pm 30\text{kV}$ HBM and $\pm 12\text{kV}$ IEC 61000-4-2 contact discharge. The International Electrotechnical Commission (IEC) ESD test is far more severe than the HBM ESD test. The 50% higher charge capacitance, $C_{(S)}$, and 78% lower discharge resistance, $R_{(D)}$, of the IEC model produce significantly higher discharge currents than the HBM model. As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method.

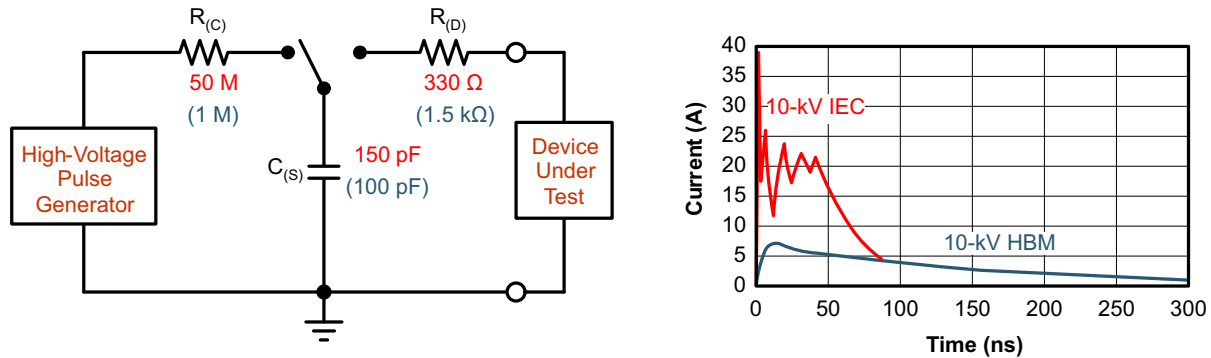


Figure 8-3. HBM and IEC ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur because of human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 8-4 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left side diagram shows the relative pulse-power for a 0.5kV surge transient and 4kV EFT transient, both of which dwarf the 10kV ESD transient visible in the lower-left corner. 500V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right side diagram shows the pulse power of a 6kV surge transient, relative to the same 0.5kV surge transient. 6kV surge transients are most likely to occur in power generation and power-grid systems.

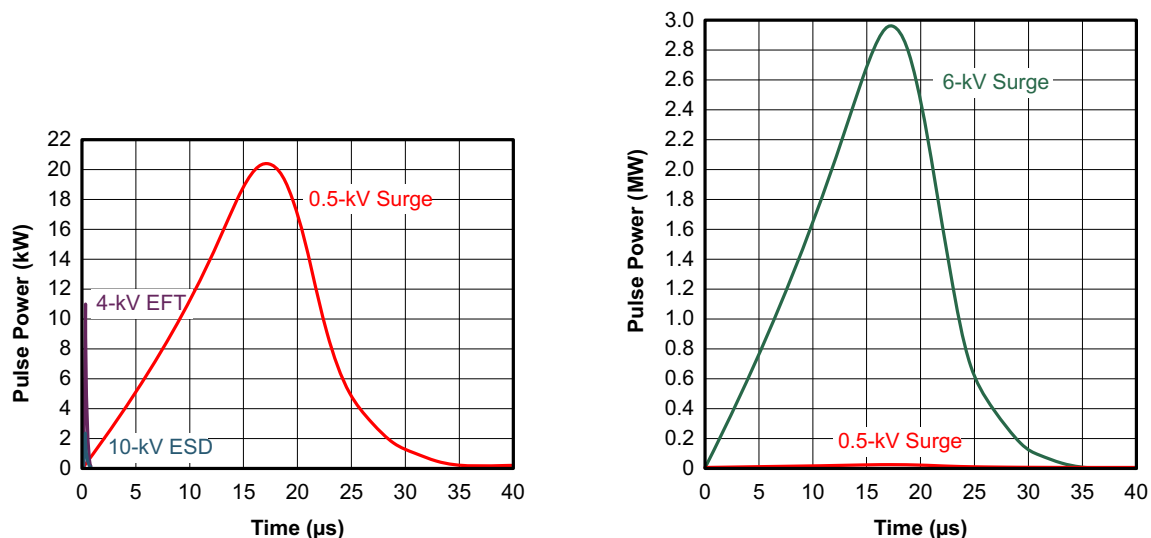


Figure 8-4. Power Comparison of ESD, EFT, and Surge Transients

For surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy, which heats and destroys the protection cells, thus destroying the transceiver. Figure 8-5 shows the large differences in transient energies for single ESD, EFT, surge transients, and an EFT pulse train that is commonly applied during compliance testing.

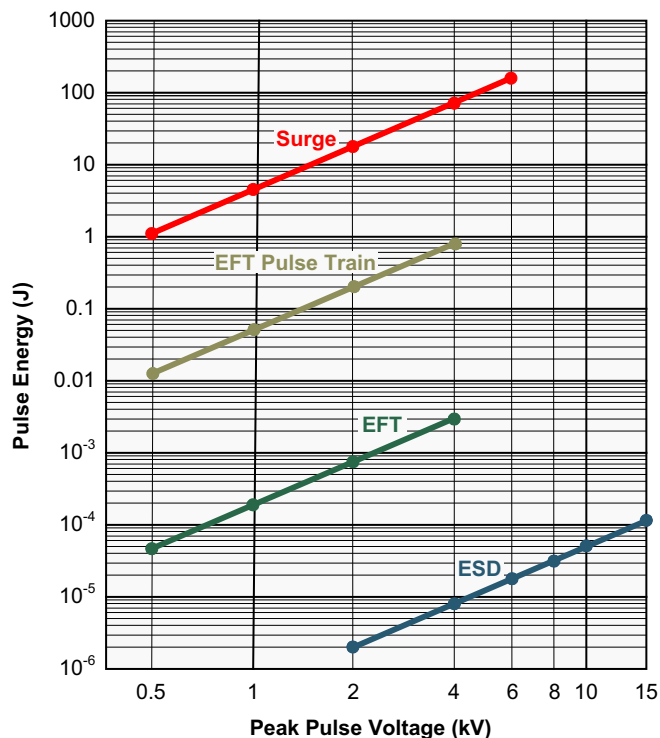


Figure 8-5. Comparison of Transient Energies

8.2.2 Detailed Design Procedure

Figure 8-6 suggests a protection circuit against 1kV surge (IEC 61000-4-5) transients. Table 8-1 shows the associated bill of materials. SMAJ30CA TVS diodes are rated to operate up to 30V. This makes sure the protection diodes do not conduct if a direct RS-485 bus shorts to 24V DC industrial power rail.

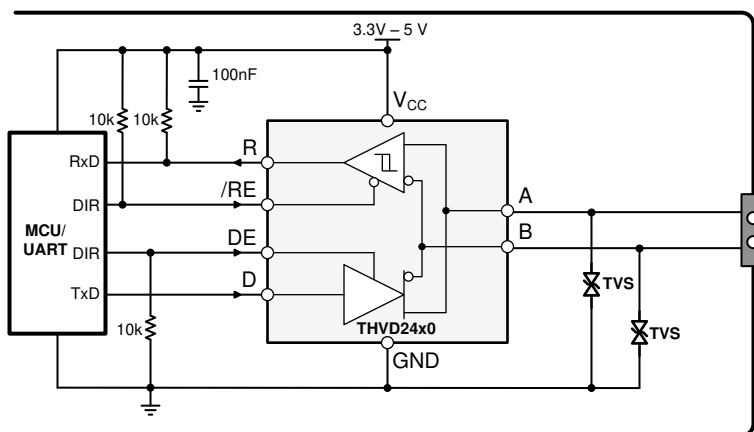


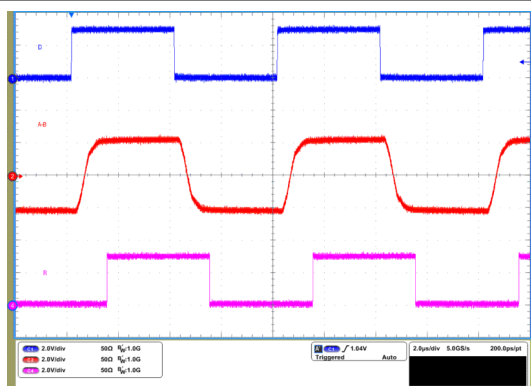
Figure 8-6. Transient Protection Against Surge Transients for Half-Duplex Devices

Table 8-1. Components List

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER ⁽¹⁾
XCVR	RS-485 transceiver	THVD2410V-EP Or THVD2450V-EP	TI
TVS	Bidirectional 400-W transient suppressor	SMAJ30CA	Littelfuse

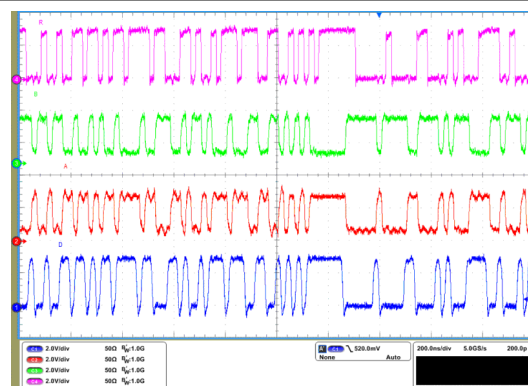
(1) See [Third-Party Products Disclaimer](#)

8.2.3 Application Curves



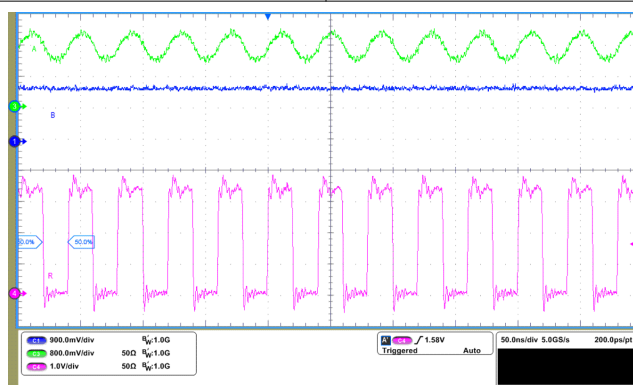
THVD2410V-EP $V_{CC} = 3.3V$ $R_L = 50\Omega$
Random (PRBS7) data at 250kbps

Figure 8-7. THVD2410V-EP Waveforms at $V_{CC} = 3.3V$



THVD2450V-EP $V_{CC} = 3.3V$ $R_L = 50\Omega$
Random (PRBS7) data at 50Mbps

Figure 8-8. THVD2450V-EP Waveforms at $V_{CC} = 3.3V$



THVD2450V-EP Pin A is supplied with $\pm 200mV$ with 1.5V
DC bias

Pin B = 1.5V

Figure 8-9. THVD2450V-EP Receiver Waveforms with $\pm 200mV V_{ID}$

8.3 Power Supply Recommendations

For reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

8.4 Layout

8.4.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices to protect against surge transients that may occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3MHz to 300MHz), high-frequency layout techniques should be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100nF to 220nF decoupling capacitors as close as possible to the V_{CC} and V_{IO} pins of transceiver, UART and/or controller ICs on the board.
5. Use at least two vias for the ground connections of the decoupling capacitors at the power pins and the protection devices to minimize the effective via inductance.
6. Use 1k Ω to 10k Ω pull-up and pull-down resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.

8.4.2 Layout Example

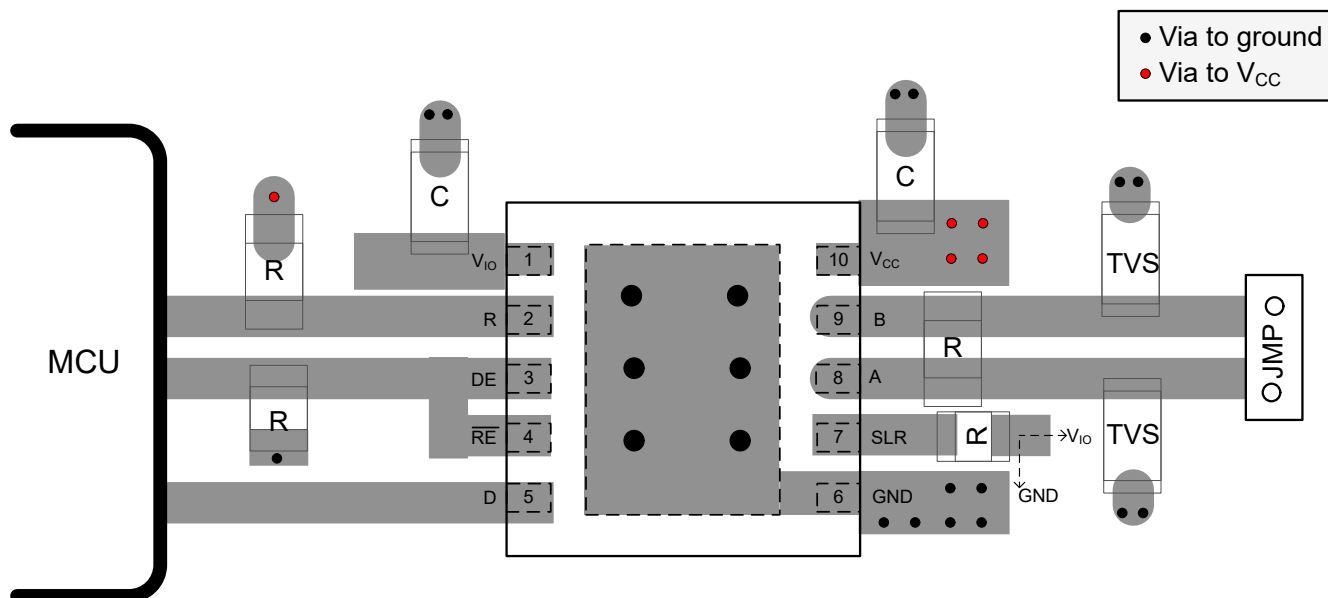


Figure 8-10. THVD2410V-EP, THVD2450V-EP (Half-Duplex) Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from Revision A (August 2024) to Revision B (October 2024) Page

- Changed the D-package pin numbers: Pin A from 11 to 12 and Pin B from 12 to 11 in [Table 4-1](#) 3

Changes from Revision * (May 2024) to Revision A (August 2024) Page

- Changed the Bus I/O protection list in the *Features* 1
- Changed Current during operation: < 5.6mA to <5.3mA in the *Features* 1
- Added table note 1 to THVD2452V-EP in the *IEC ESD Ratings* table..... 4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
THVD2410VDRCREP	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	V2410
THVD2410VDRCREP.A	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	V2410
THVD2450VDRCREP	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	V2450
THVD2450VDRCREP.A	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	V2450
THVD2452VDREP	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T2452V
THVD2452VDREP.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T2452V
V62/22613-01XE	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	V2410
V62/22613-02XE	Active	Production	VSON (DRC) 10	5000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	V2450
V62/22613-03XE	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T2452V
V62/22613-03YE	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	T2452V

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF THVD2410V-EP, THVD2450V-EP, THVD2452V-EP :

- Catalog : [THVD2410V](#), [THVD2450V](#), [THVD2452V](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THVD2410VDRCREP	VSON	DRC	10	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THVD2450VDRCREP	VSON	DRC	10	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
THVD2452VDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THVD2410VDRCREP	VSON	DRC	10	5000	346.0	346.0	33.0
THVD2450VDRCREP	VSON	DRC	10	5000	346.0	346.0	33.0
THVD2452VDREP	SOIC	D	14	2500	353.0	353.0	32.0

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

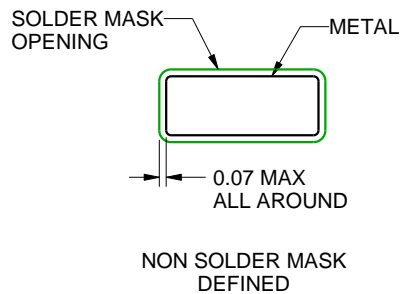
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



EXAMPLE BOARD LAYOUT

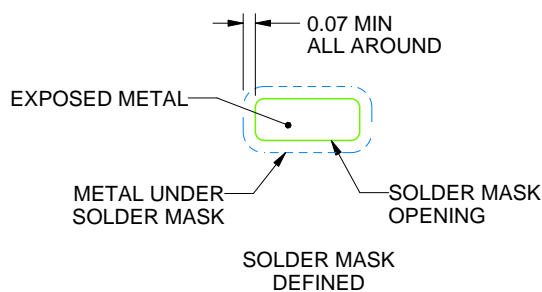
DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218878/B 07/2018

NOTES: (continued)

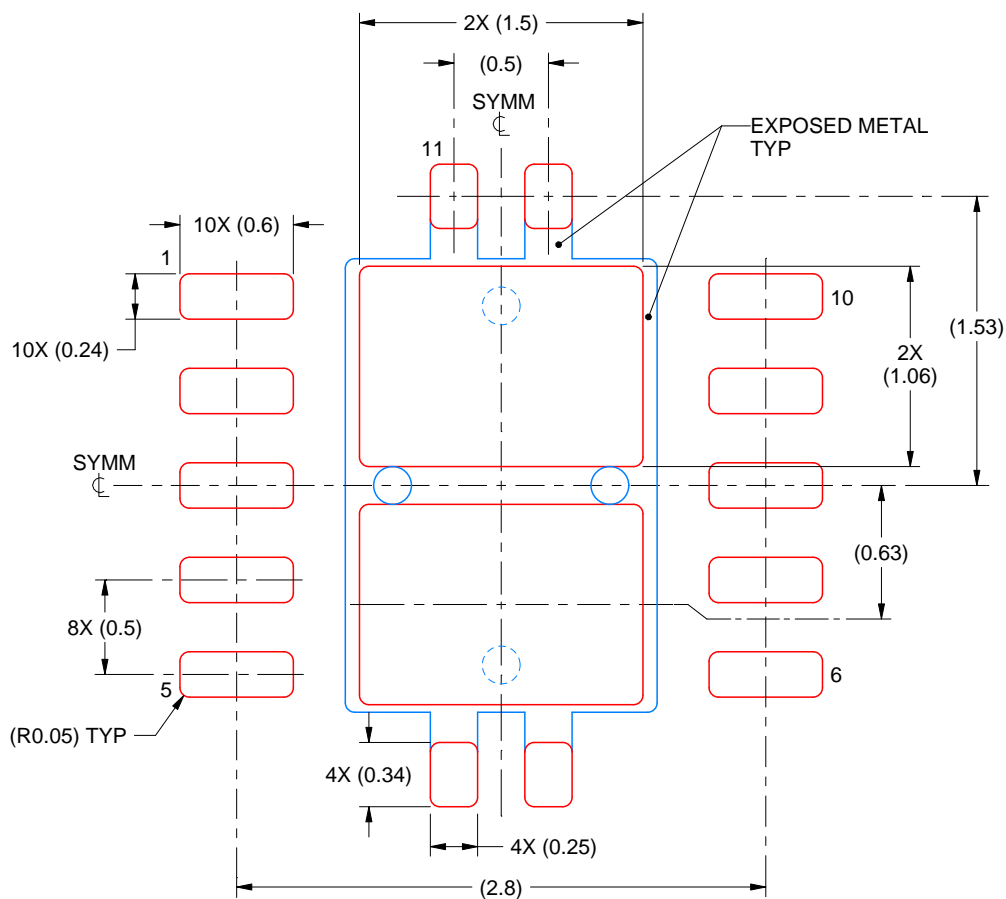
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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