THVD9491-SP Radiation-Hardened ±40V Fault-Protected 3V to 5.5V RS-485 Transceiver with Flexible I/O Supply and IEC ESD

1 Features

- Meets or exceeds the requirements of the TIA/EIA-485A and TIA/EIA-422B standards
- 3V to 5.5V supply voltage
- Differential output exceeds 2.1V for PROFIBUS compatibility with 5V supply
- Total ionizing dose (TID) characterized
  - Radiation hardness assurance (RHA) up to total ionizing dose (TID) of 100krad (Si)
- Single-event effects (SEE) characterized
  - Single event latch-up (SEL) immune to linear energy transfer (LET) = 75MeV·cm2 /mg at 125°C
- SMD# 5962R2522201PXE
- Space grade plastic (SP)
  - Controlled baseline
  - One assembly and test site
  - One fabrication site
  - Gold bond wire
  - NiPdAu lead finish
  - Military temp range (-55°C to 125°C)
  - Extended product life cycle
  - Product traceability
  - Meets the NASA ASTM E595 outgassing specification
- 1.65V to 5.5V Supply for data and enable signals
- SLR Pin Selectable Data Rates:
  - 20Mbps and 50Mbps
- Bus I/O protection
  - ±40V DC bus fault
  - ±16kV HBM ESD
  - ±12kV IEC 61000-4-2 contact discharge
  - ±12kV IEC 61000-4-2 air-gap discharge
  - ±4kV IEC 61000-4-4 fast transient burst
- Glitch-free power-up and down for hot plug-in capability
- Open, short, and idle bus failsafe
- Thermal shutdown
- 1/8 unit load (up to 256 bus nodes)
- 14-pin SOIC package for drop-in compatibility

2 Applications

- Geo-stationary Earth Orbit (GEO) space applications
- Command & data handling
- Communications payload systems
- Optical and Imaging radar payload

3 Description

THVD9491-SP is a ±40V fault-protected, half and full-duplex RS-422/RS-485 transceivers using a 1.65V to 5.5V logic supply for data and enable logic signals, and a 3V to 5.5V bus side supply. The devices have slew rate select feature that enables the devices to be used at two maximum speeds based on the SLR pin setting

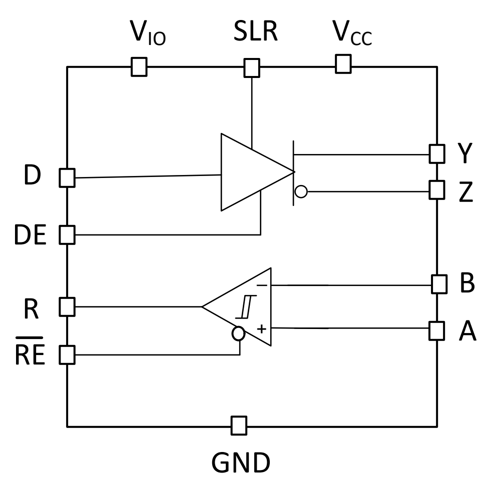
These devices feature integrated IEC ESD protection, eliminating the need for external system-level protection components. Symmetric ±12V input common-mode range makes reliable data communication over longer cable run lengths and/or in the presence of large ground loop voltages. Enhanced 250mV receiver hysteresis provides high noise rejection. In addition, the receiver fail-safe feature makes sure of a logic high when the inputs are open or shorted together.

The half-duplex device is available in small VSON package for space-constrained applications. The full-duplex device is available in standard 14-SOIC package.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
THVD9491-SP	SOIC (14)	8.65mm × 6mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block

ADVANCE INFORMATION

Table of Contents

ADVANCE INFORMATION

4 Pin Configuration and Functions

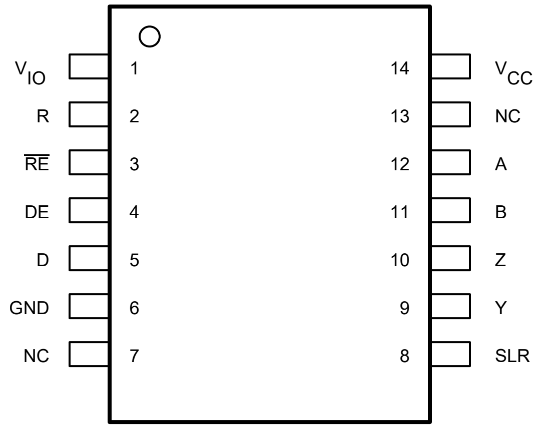


Figure 4-1. THVD9491-SP 14-Pin D Package (SOIC) Top View

Table 4-1. Pin Functions

NAME	NO.	TYPE	DESCRIPTION
V_{IO}	1	Logic Supply	1.65V to 5.5V supply for logic I/O signals (R, $\overline{RE}$, D, DE, and SLR)
R	2	Digital Output	Receive data output
$\overline{RE}$	3	Digital Input	Receiver enable input
DE	4	Digital Input	Driver enable input
D	5	Digital Input	Transmission data input
GND	6	Reference Potential	Local device ground
NC	7,13	No Connect	Not connected internally.
SLR	8	Digital Input	Slew rate selection pin: Low = 50Mbps, High = 20Mbps. Defaults to 50Mbps if left floating.
Y	9	Bus Output	RS-485 bus output, Y
Z	10	Bus Output	RS-485 bus output, Z
B	11	Bus Input	RS-485 bus input, B
A	12	Bus Input	RS-485 bus input, A
V_{CC}	14	Bus Supply	3V to 5.5V supply for A and B bus lines

ADVANCE INFORMATION

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Logic supply voltage	V_{IO}	–0.5	V_{CC} + 0.2	V
Bus supply voltage	V_{CC}	–0.5	6.5	V
Bus voltage	Range at any bus pin (A or B) as differential or common-mode with respect to GND	-40	40	V
Input voltage	Range at any logic pin (D, DE, SLR or $\overline{RE}$)	–0.3	V_{IO} + 0.2	V
Receiver output current	I_O	–24	24	mA
Storage temperature	T_{stg}	–65	170	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	Bus terminals and GND	±16,000	V
			All pins except bus terminals and GND	±4,000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]		±1,500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings [IEC]

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Contact discharge, per IEC 61000-4-2 [1]	Bus terminals and GND	±8,000	V
		Air-gap discharge, per IEC 61000-4-2 [1]	Bus terminals and GND	±8,000	
$V_{(EFT)}$	Electrical fast transient	Per IEC 61000-4-4	Bus terminals	±4,000	V

(1) For optimized IEC ESD performance, it is recommended to have series resistor (≥ 50Ω), on all logic inputs directly connected to power or ground, to minimize the transient currents going into or out of the logic pins.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		5.5	V
V_{IO}	I/O supply voltage		1.65		V_{CC}	V
V_I	Input voltage at any bus terminal (separately or common mode)[(1)]		–12		12	V
V_{IH}	High-level input voltage (driver, driver enable, receiver enable and slew rate select inputs)		0.7*V_{IO}		V_{IO}	V
V_{IL}	Low-level input voltage (driver, driver enable, receiver enable and slew rate select inputs)		0		0.3*V_{IO}	V
V_{ID}	Differential input voltage		–12		12	V
I_O	Output current, driver		–60		60	mA
I_{OR}	Output current, receiver	V_{IO} = 1.8V or 2.5V	–4		4	mA
I_{OR}	Output current, receiver	V_{IO} = 3.3V or 5V	–8		8	mA
R_L	Differential load resistance		54	60		Ω
$1/t_{UI}$	Signaling rate	SLR = V_{IO}			20	Mbps
		SLR = 0 or floating			50	Mbps
T_A	Operating ambient temperature		-55		125	°C
T_J	Junction temperature		-55		150	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

5.5 Thermal Information

THERMAL METRIC[(1)]		THVD9491-SP D (SOIC) 14-PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	43.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.6 Power Dissipation

PARAMETER		TEST CONDITIONS		VALUE	UNIT
P_D	Driver and receiver enabled, loopback for full duplex devices (A connected to Y, B connected to Z) V_{CC} = 5.5V, T_A = 125°C, square wave at 50% duty cycle	Unterminated R_L = 300Ω, C_L = 50pF (driver)	20Mbps	335	mW
			50Mbps	571	
		RS-422 load R_L = 100Ω, C_L = 50pF (driver)	20Mbps	325	mW
			50Mbps	522	
		RS-485 load R_L = 54Ω, C_L = 50pF (driver)	20Mbps	355	mW
			50Mbps	526	

ADVANCE INFORMATION

5.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5V, V_{IO} = 3.3V , unless otherwise noted. [(2)]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
$\|V_{OD}\|$	Driver differential output voltage magnitude	R_L = 60Ω, –12V ≤ V_{test} ≤ 12V. See Figure 6-1		1.5	2.8		V
		R_L = 60Ω, –12V ≤ V_{test} ≤ 12V, 4.5V ≤ V_{CC} ≤ 5.5V. See Figure 6-1		2.1	3.3		V
		R_L = 100Ω See Figure 6-2		2	4		V
		R_L = 54Ω. See Figure 6-2		1.5	3.3		V
$\Delta\|V_{OD}\|$	Change in differential output voltage	R_L = 54Ω or 100Ω. See Figure 6-2		–200		200	mV
V_{OC}	Common-mode output voltage	R_L = 54Ω or 100Ω (See Figure 6-2		1	$V_{CC}/2$	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	R_L = 54Ω or 100Ω. See Figure 6-2		–50		50	mV
I_{OS}	Short-circuit output current	DE = V_{IO}, -40V ≤ (V_Y or V_Z) ≤ 40V, or Y shorted to Z		–250		250	mA
Receiver							
I_I	Bus input current	DE = 0V, V_{CC} and V_{IO} = 0V or 5.5V	V_I = 12V		75	125	μA
			V_I = –7V	–100	–60		μA
V_{TH+}	Positive-going input threshold voltage[(1)]	Over common-mode range of ± 12V		40	125	200	mV
V_{TH-}	Negative-going input threshold voltage[(1)]			–200	–125	-40	mV
V_{HYS}	Input hysteresis				250		mV
V_{TH_FSH}	Input fail-safe threshold			–40		40	mV
$C_{A,B}$	Input differential capacitance	Measured between A and B, f = 1MHz			50		pF
V_{OH}	Output high voltage	I_{OH} = –8mA, V_{IO} = 3to 3.6V or 4.5V to 5.5V		V_{IO} – 0.4	V_{IO} – 0.2		V
V_{OL}	Output low voltage	I_{OL} = 8mA, V_{IO} = 3to 3.6V or 4.5V to 5.5V			0.2	0.4	V
V_{OH}	Output high voltage	I_{OH} = –4mA, V_{IO} = 1.65to 1.95V or 2.25V to 2.75V		V_{IO} – 0.4	V_{IO} – 0.2		V
V_{OL}	Output low voltage	I_{OL} = 4mA, V_{IO} = 1.65to 1.95V or 2.25V to 2.75V			0.2	0.4	V
I_{OZ}	Output high-impedance current, R pin	V_O = 0V or V_{IO}, $\overline{RE}$ = V_{IO}		–1		1	μA
Logic							
I_{IN}	Input current (DE , SLR)	1.65V ≤ V_{IO} ≤ 5.5V, 0V ≤ V_{IN} ≤ V_{IO}				5	μA
I_{IN}	Input current (D, $\overline{RE}$)	1.65V ≤ V_{IO} ≤ 5.5V, 0V ≤ V_{IN} ≤ V_{IO}		–5			μA
Thermal Protection							
T_{SHDN}	Thermal shutdown threshold	Temperature rising		150	180		°C
T_{HYS}	Thermal shutdown hysteresis				10		°C
Supply							
I_{CC}	Supply current (quiescent), V_{CC} = 4.5V to 5.5V	Driver and receiver enabled	$\overline{RE}$ = 0V, DE = V_{IO}, No load		4	7.2	mA
		Driver enabled, receiver disabled	$\overline{RE}$ = V_{IO}, DE = V_{IO}, No load		4	6	mA
		Driver disabled, receiver enabled	$\overline{RE}$ = 0V, DE = 0V, No load		4	6	mA
		Driver and receiver disabled	$\overline{RE}$ = V_{IO}, DE = 0V, D = open, No load		2	4	mA

5.7 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and supply voltage of V_{CC} = 5V, V_{IO} = 3.3V , unless otherwise noted. (2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Supply current (quiescent), V_{CC} = 3V to 3.6V	Driver and receiver enabled	$\overline{RE}$ = 0V, DE = V_{IO}, No load		3.5	6	mA
		Driver enabled, receiver disabled	$\overline{RE}$ = V_{IO}, DE = V_{IO}, No load		3	5	mA
		Driver disabled, receiver enabled	$\overline{RE}$ = 0V, DE = 0V, No load		3	5	mA
		Driver and receiver disabled	$\overline{RE}$ = V_{IO}, DE = 0V, D = open, No load		2	4	mA
I_{IO}	Logic supply current (quiescent), V_{IO} = 3to 3.6V	Driver disabled, Receiver enabled, SLR = GND	DE = 0V, $\overline{RE}$ = 0V, No load		45	100	μA
		Driver disabled, Receiver enabled, SLR = V_{IO}			33	100	μA
		Driver disabled, Receiver disabled, SLR = GND	DE = 0V, $\overline{RE}$ = V_{IO}, No load		45	100	μA
		Driver disabled, Receiver disabled, SLR = V_{IO}			33	100	μA

(1) Under any specific conditions, V_{TH+} is assured to be at least V_{HYS} higher than V_{TH-}.
(2) A and B are receiver inputs, Y and Z are driver output terminals for the device

5.8 Switching Characteristics: 20Mbps

20Mbps (SLR = V_{IO}) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5V, V_{IO} = 3.3V, unless otherwise noted. (2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time (1)	R_L = 54Ω, C_L = 50pF	See Figure 6-3	4	8	15	ns
t_{PHL}, t_{PLH}	Propagation delay (1)			6	15	30	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$ (1)				1	3	ns
t_{PHZ}, t_{PLZ}	Disable time (1)	$\overline{RE}$ = X	See Figure 6-4 and Figure 6-3		17	35	ns
t_{PZH}, t_{PZL}	Enable time (1)	$\overline{RE}$ = 0V			14	39	ns
		$\overline{RE}$ = V_{IO}			3	4.5	μs
t_{SHDN}	Time to shutdown (1)	$\overline{RE}$ = V_{IO}		50	300	500	ns
Receiver							
t_r, t_f	Output rise/fall time (1)	C_L = 15pF	See Figure 6-6		1.5	6	ns
t_{PHL}, t_{PLH}	Propagation delay (1)			25	35	60	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} - t_{PLH}\|$ (1)				1	5	ns
t_{PHZ}, t_{PLZ}	Disable time (1)	DE = X			12	25	ns
$t_{PZH(1)}$, $t_{PZL(1)}$	Enable time (1)	DE = V_{IO}	See Figure 6-7		50	82	ns
$t_{PZH(2)}$, $t_{PZL(2)}$	Enable time (1)	DE = 0V	See Figure 6-8		2.8	5	μs
$t_{D(OFS)}$	Delay to enter fail-safe operation (1)	C_L = 15pF	See Figure 6-9	7	11	18	μs
$t_{D(FSO)}$	Delay to exit fail-safe operation (1)			19	32	50	ns
t_{SHDN}	Time to shutdown (1)	DE = 0V	See Figure 6-8	50	300	500	ns

(1) Specified by design and characterization
(2) A and B are receiver inputs, Y and Z are driver output terminals for the device

ADVANCE INFORMATION

ADVANCE INFORMATION

5.9 Switching Characteristics: 50Mbps

50Mbps (SLR = 0) over recommended operating conditions. All typical values are at 25°C and supply voltage of V_{CC} = 5V, V_{IO} = 3.3V, unless otherwise noted. (2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Driver							
t_r, t_f	Differential output rise/fall time (1)	R_L = 54Ω, C_L = 50pF	See Figure 6-3	1	5	7	ns
t_{PHL}, t_{PLH}	Propagation delay (1)			7	12	22	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} – t_{PLH}\|$ (1)				1	3	ns
t_{PHZ}, t_{PLZ}	Disable time (1)	$\overline{RE}$ = X	See Figure 6-4 and Figure 6-3		14	30	ns
t_{PZH}, t_{PZL}	Enable time (1)	$\overline{RE}$ = 0V			20	35	ns
		$\overline{RE}$ = V_{IO}			2.5	4.5	μs
t_{SHDN}	Time to shutdown (1)	$\overline{RE}$ = V_{IO}		50	300	500	ns
Receiver							
t_r, t_f	Output rise/fall time (1)	C_L = 15pF	See Figure 6-6		1.5	6	ns
t_{PHL}, t_{PLH}	Propagation delay (1)			25	35	60	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL} – t_{PLH}\|$ (1)				1	5	ns
t_{PHZ}, t_{PLZ}	Disable time (1)	DE = X			12	25	ns
$t_{PZH(1)}$, $t_{PZL(1)}$	Enable time (1)	DE = V_{IO}	See Figure 6-7		50	82	ns
		DE = 0V	See Figure 6-8		3	5	μs
$t_{D(OFS)}$	Delay to enter fail-safe operation (1)	C_L = 15pF	See Figure 6-9	7	10	18	μs
$t_{D(FSO)}$	Delay to exit fail-safe operation (1)			19	35	50	ns
t_{SHDN}	Time to shutdown (1)	DE = 0V	See Figure 6-8	50	300	500	ns

(1) Specified by design and characterization
(2) A and B are receiver inputs, Y and Z are driver output terminals for the device

6 Parameter Measurement Information

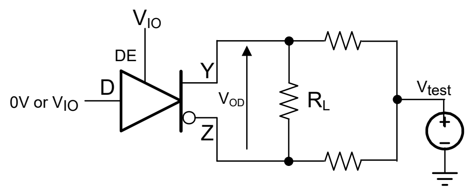


Figure 6-1. Measurement of Driver Differential Output Voltage With Common-Mode Load

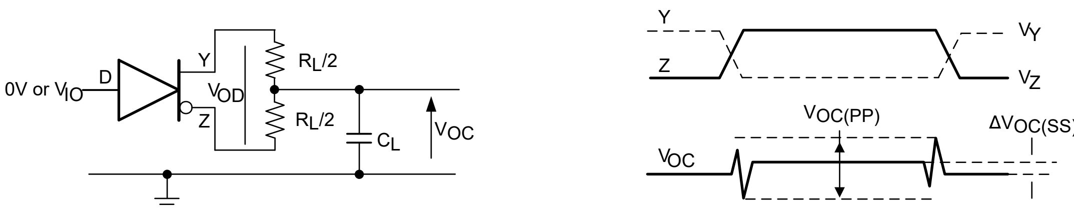


Figure 6-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

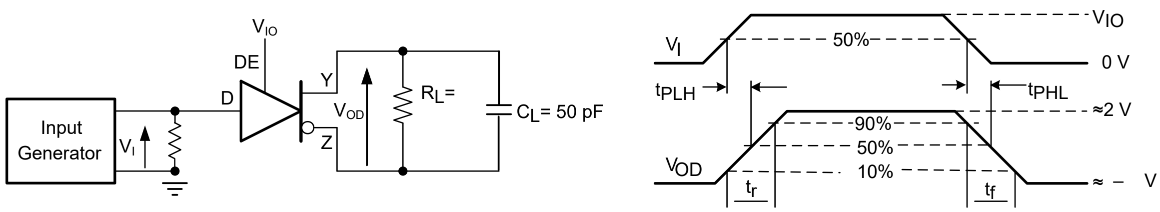


Figure 6-3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

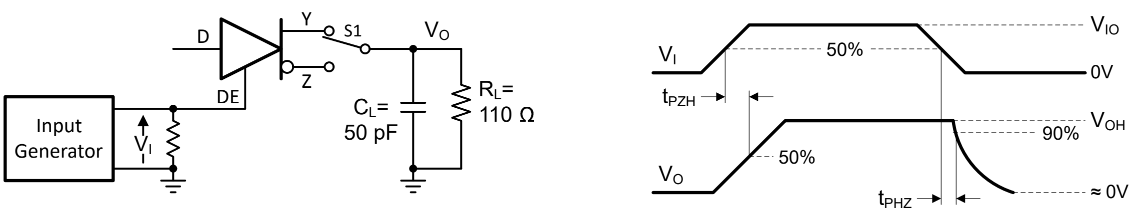


Figure 6-4. Measurement of Driver Enable and Disable Times With Active High Output and Pull-Down Load

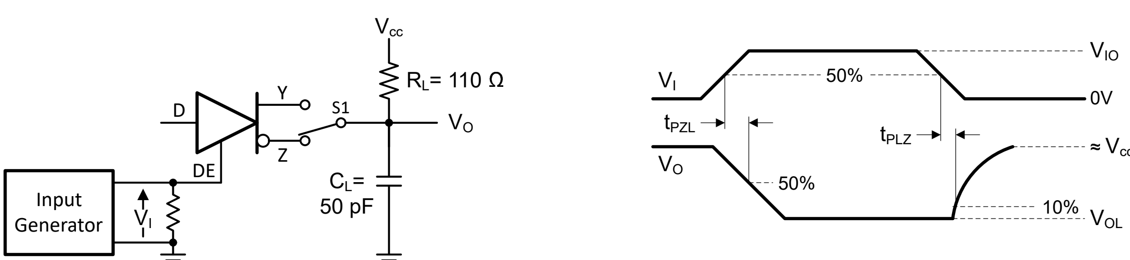


Figure 6-5. Measurement of Driver Enable and Disable Times With Active Low Output and Pull-up Load

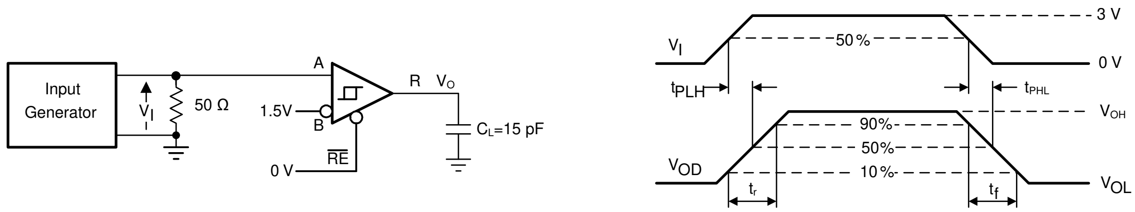


Figure 6-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

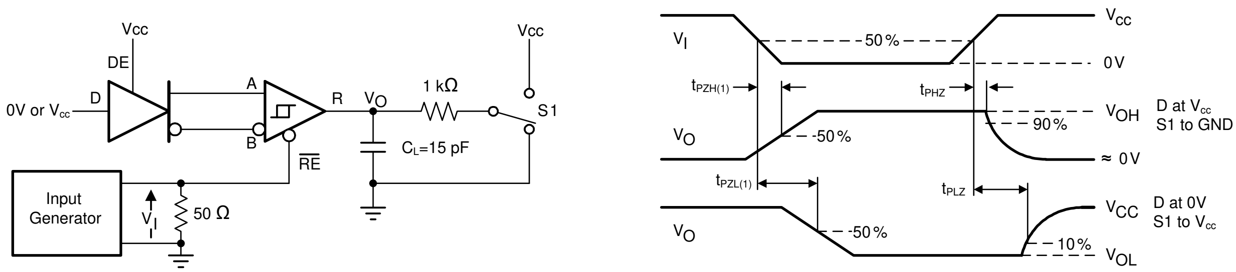


Figure 6-7. Measurement of Receiver Enable/Disable Times With Driver Enabled

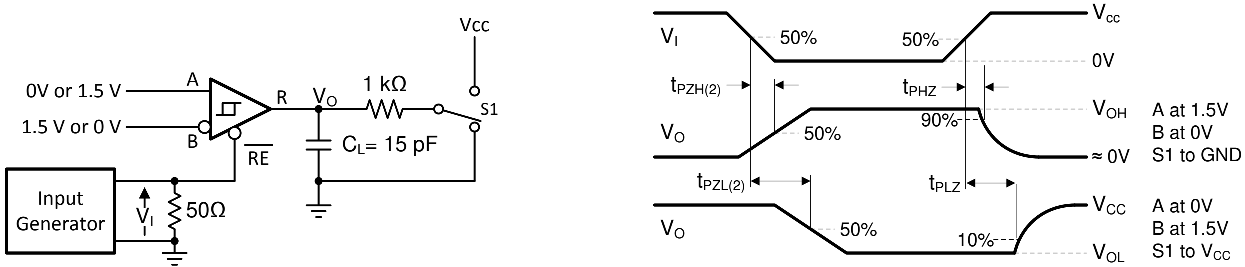


Figure 6-8. Measurement of Receiver Enable Times With Driver Disabled

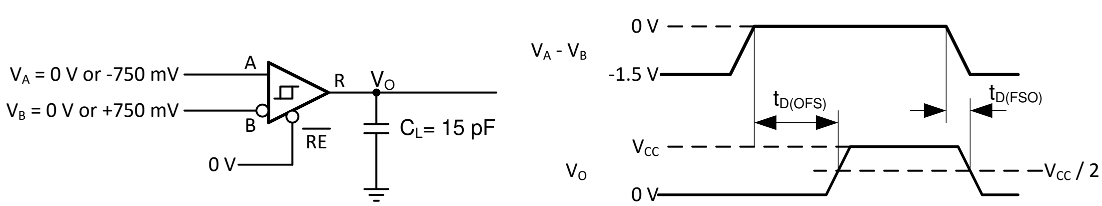


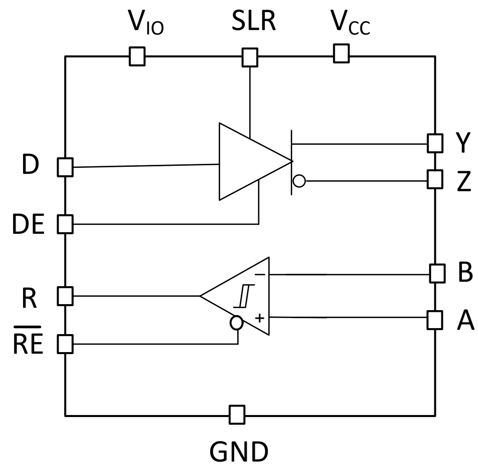
Figure 6-9. Measurement of Fail-Safe Delay

7 Detailed Description

7.1 Overview

THVD9491-SP is a fault-protected, half duplex RS-485 transceivers available in two speed grades designed for data transmission up to 500kbps and 50Mbps respectively. The devices have active-high driver enables and active-low receiver enables. A shutdown current of less than 1µA can be achieved by disabling both driver and receiver.

7.2 Functional Block Diagrams



7.3 Feature Description

7.3.1 Bus Fault Protection

THVD9491-SP transceivers have extended bus fault protection compared to standard RS-485 devices. Transceivers that operate in rugged industrial environments are often exposed to voltage transients greater than the -7V to +12V defined by the TIA/EIA-485A standard. To protect against such conditions, the generic RS-485 devices with lower absolute maximum ratings requires expensive external protection components. To simplify system design and reduce overall system cost, the device is protected up to ±40V without the need for any external components.

7.3.2 Integrated IEC ESD and EFT Protection

Internal ESD protection circuits protect the transceivers against electrostatic discharges (ESD) according to IEC 61000-4-2 of up to ±12kV and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ±4kV. The ESD protection circuits help to limit voltage excursions, and recover quickly allowing EFT Criterion A at the system level (no data loss when transient noise is present).

7.3.3 Driver Overvoltage and Overcurrent Protection

The THVD9491-SP drivers are protected against any DC supply shorts in the range of -40V to +40V. The devices internally limit the short circuit current to ±250mA to comply with the TIA/EIA-485A standard. In addition, a fold-back current limiting circuit further reduces the driver short circuit current to less than ±5mA if the output fault voltage exceeds |±25V|.

All devices feature thermal shutdown protection that disables the driver and the receiver if the junction temperature exceeds the T_{SHDN} threshold due to excessive power dissipation.

7.3.4 Enhanced Receiver Noise Immunity

The differential receivers of THVD9491-SP feature fully symmetric thresholds to maintain duty cycle of the signal even with small input amplitudes. In addition, 250mV (typical) hysteresis provides excellent noise immunity.

ADVANCE INFORMATION

7.3.5 Receiver Fail-Safe Operation

The receivers are fail-safe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the receiver outputs a fail-safe logic high state if the input amplitude stays for longer than $t_{D(OFS)}$ at less than $|V_{TH\_FSH}|$.

7.3.6 Low-Power Shutdown Mode

Driving DE low and $\overline{RE}$ high for longer than 500ns puts the devices into the shutdown mode. If either DE goes high or $\overline{RE}$ goes low, the counters reset. The devices does not enter the shutdown mode if the enable pins are in disable state for less than 50ns. This feature prevents the devices from accidentally going into shutdown mode due to skew between DE and $\overline{RE}$.

7.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes Y to turn high and Z to turn low. In this case, the differential output voltage defined as $V_{OD} = V_Y – V_Z$ is positive. When D is low, the output states reverse: Z turns high, Y becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground; thus, when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{IO}, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

Table 7-1. Driver Function Table

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	Y	Z	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is higher than the positive input threshold, V_{TH+}, the receiver output, R, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-}, the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

Table 7-2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	FUNCTION
$V_{ID} = V_A – V_B$	$\overline{RE}$	R	
$V_{TH+} < V_{ID}$	L	H	Receive valid bus high
$V_{TH-} < V_{ID} < V_{TH+}$	L	?	Indeterminate bus state
$V_{ID} < V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

Table 7-3 shows SLR (slew rate select) pin functionality. SLR has integrated pull-down, so the device remains in higher speed mode until SLR is pulled high which limits the slew rate and puts the device in slower speed mode.

Table 7-3. SLR pin control

Device	Functionality w.r.t SLR pin
THVD9491-SP	SLR = Low or floating: Both transmitter (TX) and receiver (RX) maximum speed is 50Mbps SLR = High: Both TX and RX maximum speed is limited to 20Mbps

ADVANCE INFORMATION

ADVANCE INFORMATION

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

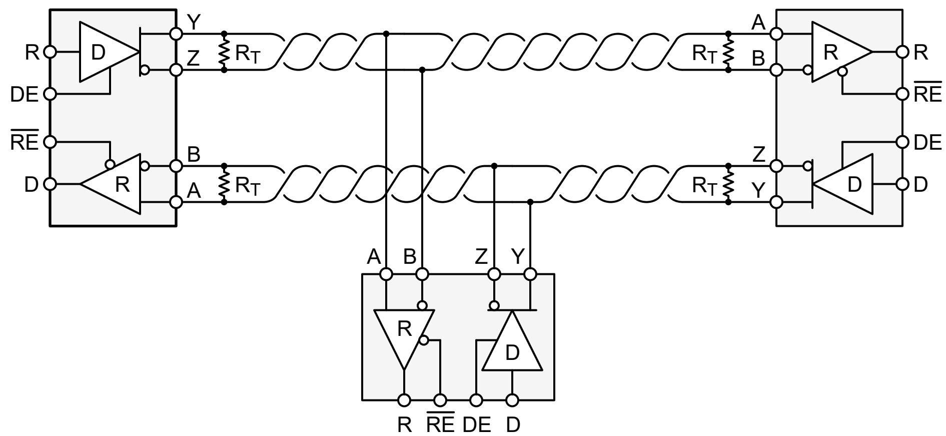


Figure 8-1. Typical RS-485 Network With Full-Duplex Transceivers

8.1.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

8.1.2 Detailed Design Procedure

Figure 8-2 suggests a protection circuit against 1kV surge (IEC 61000-4-5) transients. Table 8-1 shows the associated bill of materials. SMAJ30CA TVS diodes are rated to operate up to 30V. This provides the protection diodes do not conduct if a direct RS-485 bus shorts to 24V DC industrial power rail.

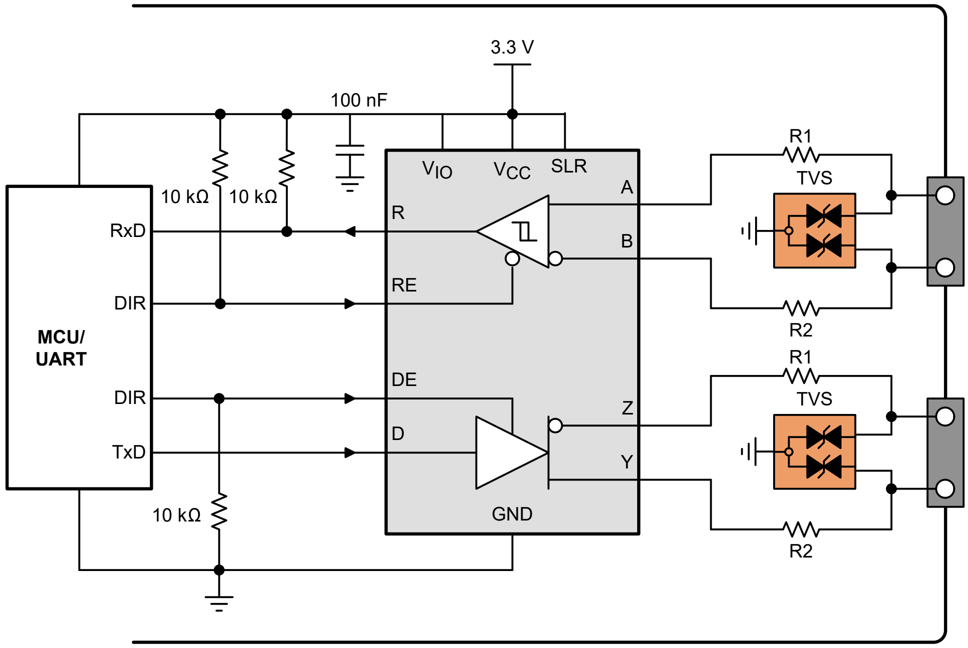


Figure 8-2. Transient Protection Against Surge Transients for Full-Duplex Devices

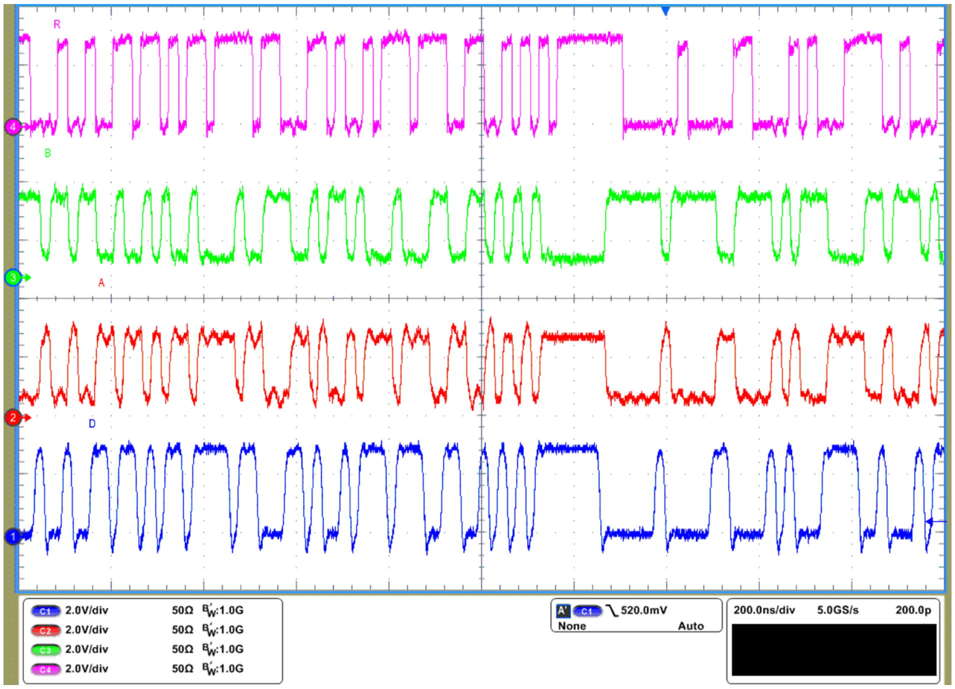
Table 8-1. Components List

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER(1)
XCVR	RS-485 transceiver	THVD9491-SP	TI
TVS	Bidirectional 400W transient suppressor	SMAJ30CA	Littelfuse

(1) See *Third-Party Products Disclaimer*.

ADVANCE INFORMATION

8.1.3 Application Curve



PRBS data at 50 Mbps $V_{CC} = V_{IO}$= 3.3V SLR = GND R_L = 50Ω

Figure 8-3. Driver input (D), bus (A/Y,B/Z) and receiver output (R) waveforms

8.2 Power Supply Recommendations

For reliable operation at all data rates and supply voltages, each supply must be decoupled with a 100nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

8.3 Layout

8.3.1 Layout Guidelines

Robust and reliable bus node design often requires the use of external transient protection devices to protect against surge transients that can occur in industrial environments. Since these transients have a wide frequency bandwidth (from approximately 3MHz to 300MHz), high-frequency layout techniques are applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from propagating across the board.
2. Use V_{CC} and ground planes to provide low inductance. Note that high-frequency currents tend to follow the path of least impedance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100nF to 220nF decoupling capacitors as close as possible to the V_{CC} pins of transceiver, UART and/or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of decoupling capacitors and protection devices to minimize effective via inductance.
6. Use 1kΩ to 10kΩ pull-up and pull-down resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof resistors into the A,B, Y and Z bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevents latching up.

8.3.2 Layout Example

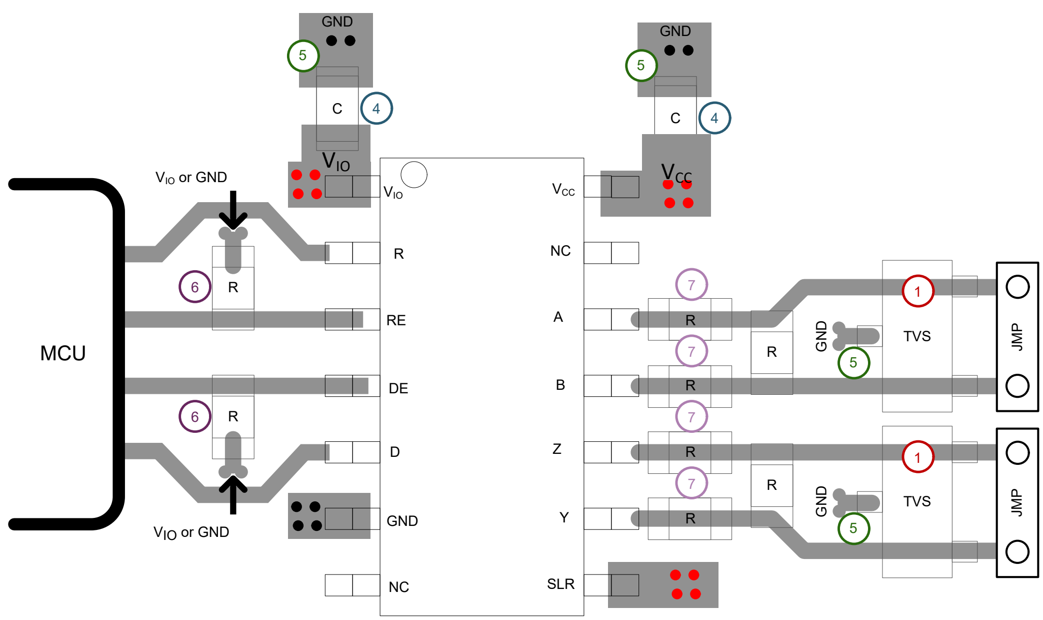


Figure 8-4. Full-Duplex Layout Example

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status[(1)]	Material type[(2)]	Package | Pins	Package qty | Carrier	RoHS [(3)]	Lead finish/Ball material[(4)]	MSL rating/Peak reflow[(5)]	Op temp (°C)	Part marking[(6)]
PTHVD9491DTSP	ACTIVE	Preproduction	SOIC (D) |14	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	PT9491SP

(1) **Status:** For more details on status, see our product life cycle.
(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

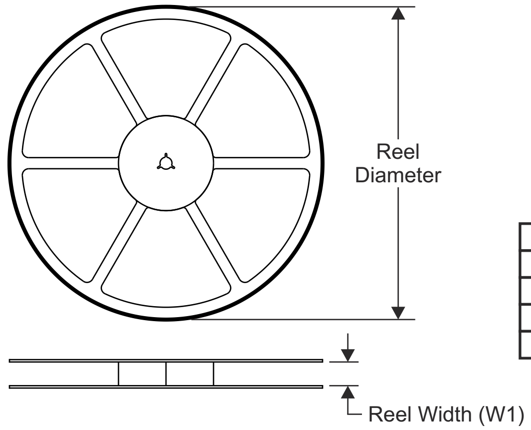
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

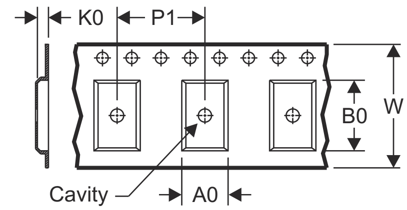
ADVANCE INFORMATION

11.1 Tape and Reel Information

REEL DIMENSIONS

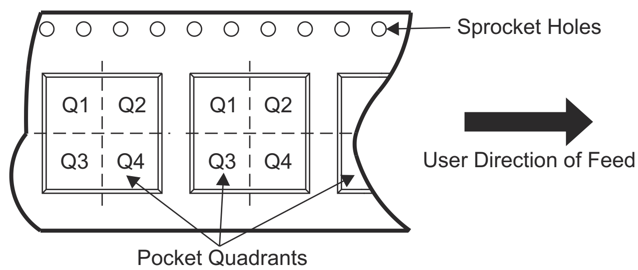


TAPE DIMENSIONS



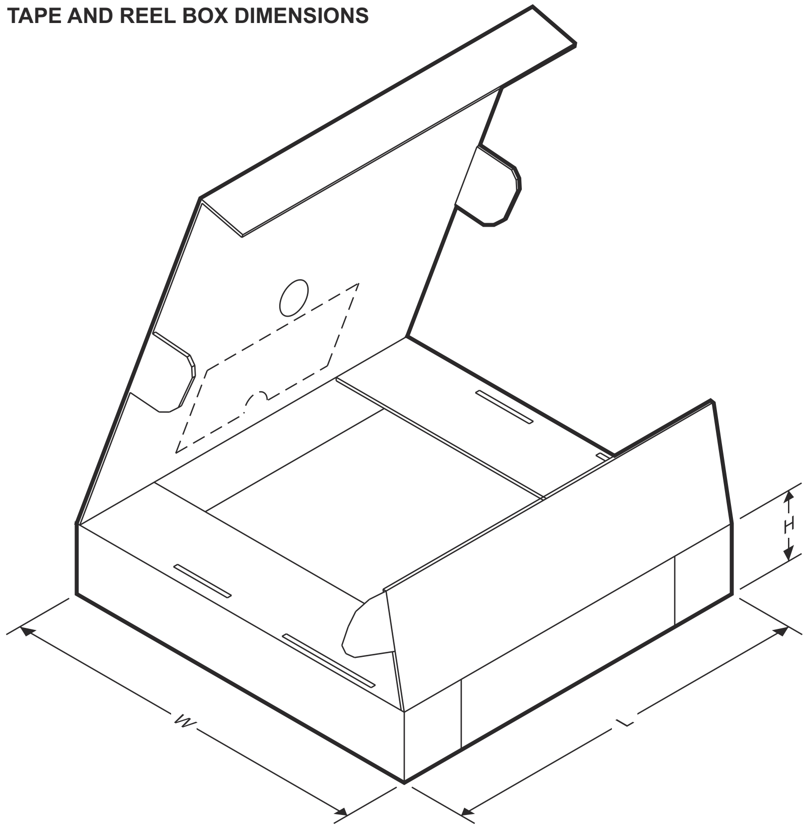
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTHVD9491DTSP	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTHVD9491DTSP	SOIC	D	14	250	353.0	353.0	32.0

ADVANCE INFORMATION

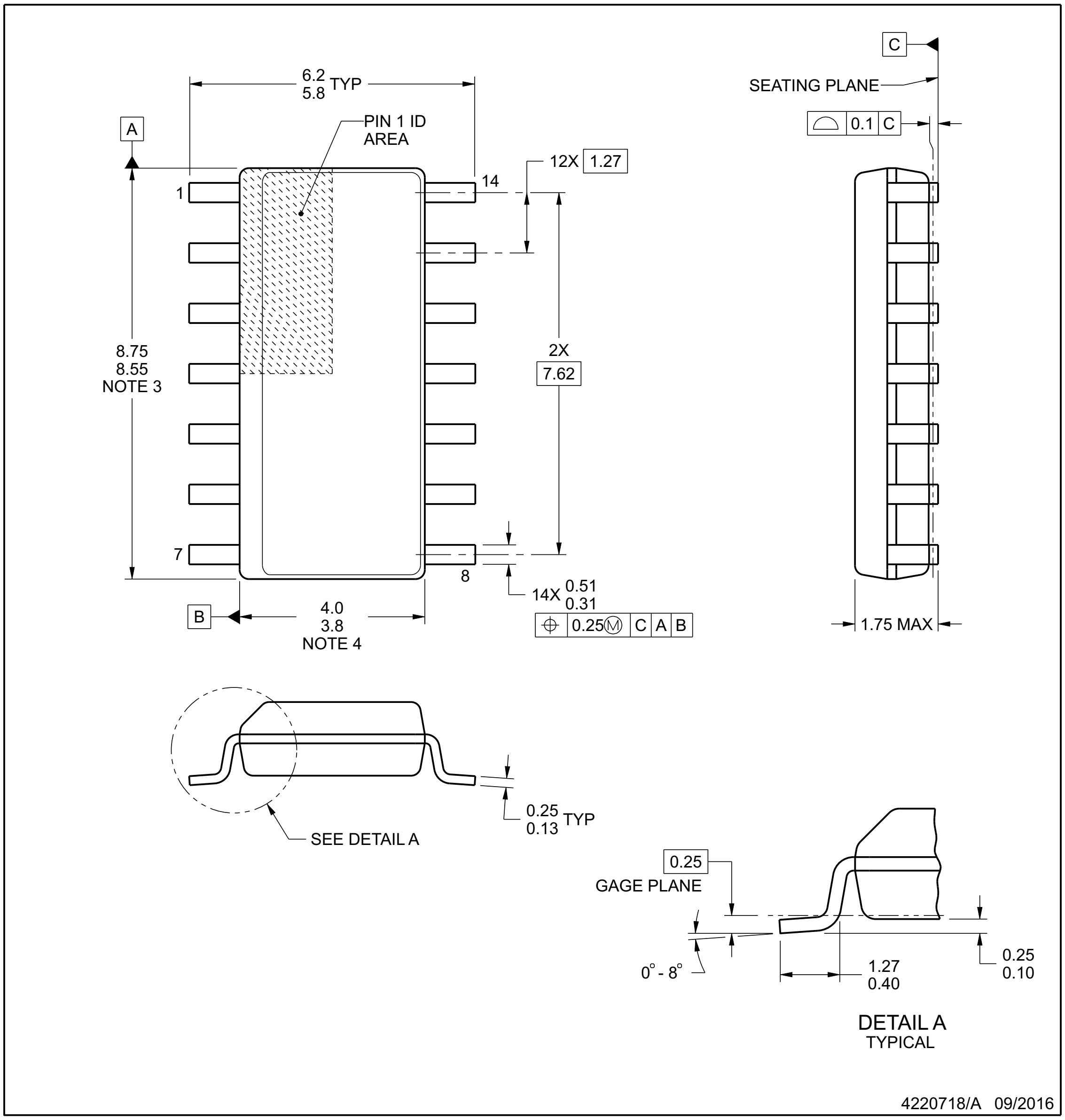
11.2 Mechanical Data

PACKAGE OUTLINE

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

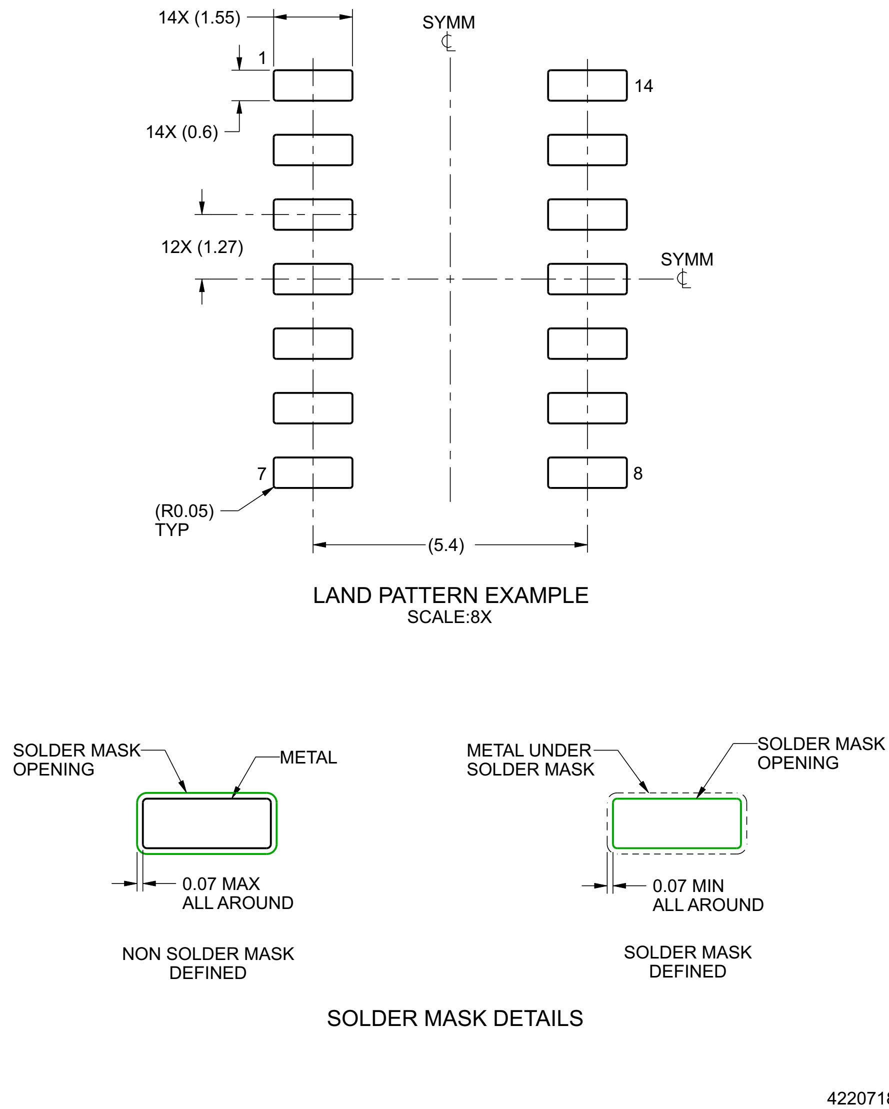
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

ADVANCE INFORMATION

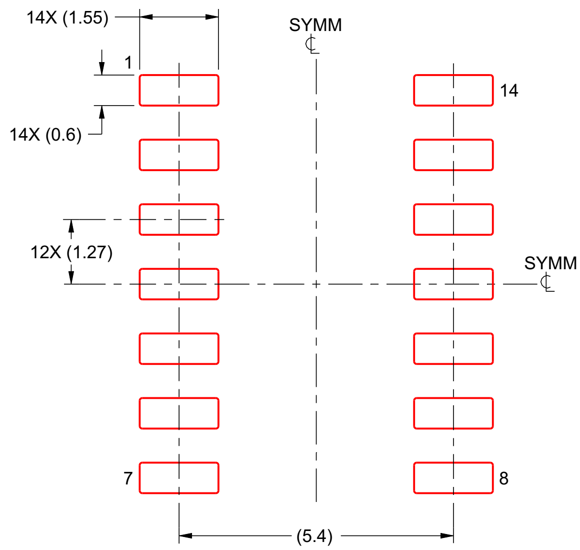
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.