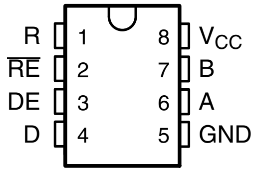
TL3695
DIFFERENTIAL BUS TRANSCEIVER

SLLS044D – NOVEMBER 1988 – REVISED DECEMBER 1999

- **Bidirectional Transceiver**
- **Meets or Exceeds the Requirements of TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendation V.11**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Low Skew . . . 6 ns Max**
- **Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply-Current Requirements . . . 30 mA Max**
- **Wide Positive and Negative Input/Output Bus-Voltage Ranges**
- **Driver Output Capacity . . . ±60 mA**
- **Thermal-Shutdown Protection**
- **Driver Positive and Negative Current Limiting**
- **Receiver Input Impedances . . . 12 kΩ Min**
- **Receiver Input Sensitivity . . . ±200 mV Max**
- **Receiver Input Hysteresis . . . 120 mV Typ**
- **Fail Safe . . . High Receiver Output With Inputs Open**
- **Operates From a Single 5-V Supply**
- **Glitch-Free Power-Up and Power-Down Protection**
- **Interchangeable With National DS3695 and DS3695A**

D OR P PACKAGE
(TOP VIEW)



description

The TL3695 differential bus transceiver is designed for bidirectional data communication on multipoint bus-transmission lines. It is designed for balanced transmission lines and meets TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendation V.11.

The TL3695 combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a directional control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0. This port features wide positive and negative common-mode voltage ranges, making the device suitable for party line applications.

The TL3695 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	TL3695D	TL3695P

The D package is available taped and reeled. Add the suffix R to device type (e.g., TL3695DR).

Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

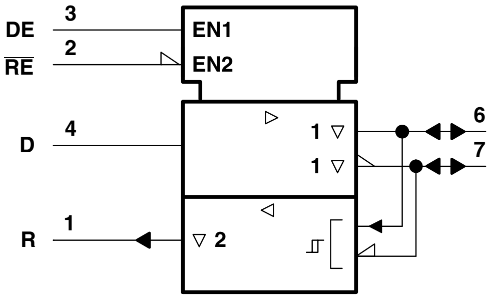
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

RECEIVER

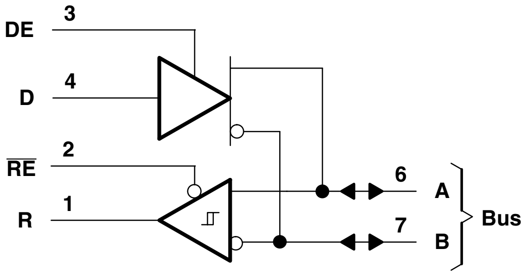
DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Inputs open	L	H

H = high level, L = low level, ? = indeterminate, X = irrelevant,
Z = high impedance (off)

logic symbol†



logic diagram (positive logic)



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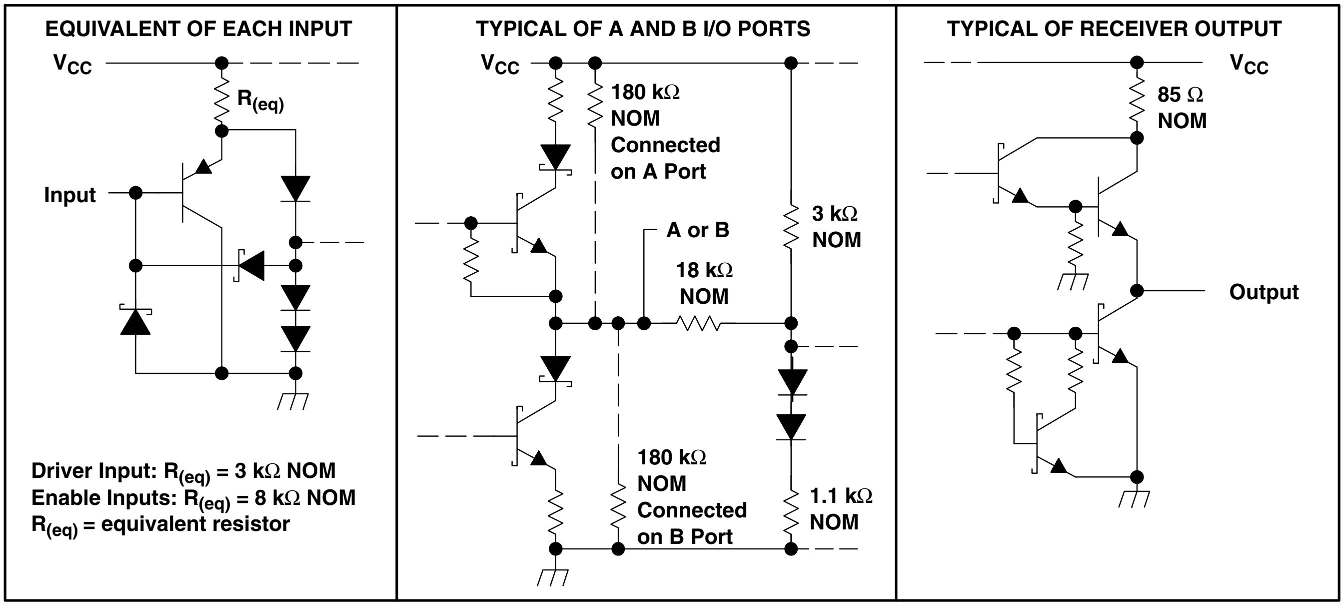
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematic of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)		7 V
Voltage range at any bus terminal		−10 V to 15 V
Enable input voltage, V_I		5.5 V
Operating free-air temperature range, T_A		0°C to 70°C
Package thermal impedance, θ_{JA} (see Note 2):	D package	97°C/W
	PW package	85°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C
Storage temperature range, T_{stg}		−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}				12	V
				−7	
High-level Input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level Input voltage, V_{IL}	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (see Note 3)				±12	V
High-level output current, I_{OH}	Driver			– 60	mA
	Receiver			– 400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

NOTE 3: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_O	Output voltage	$I_O = 0$		0		6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	$I_O = 0$		1.5		5	V
$\lvert V_{OD2} \rvert$	Differential output voltage	$R_L = 100\ \Omega$,	See Figure 1	1/2 V_{OD1} or 2§			V
		$R_L = 54\ \Omega$,	See Figure 1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	$V_{test} = -7$ V to 12 V,	See Figure 2	1.5		5	V
$\Delta \lvert V_{OD} \rvert$	Change in magnitude of differential output voltage¶	$R_L = 54\ \Omega$,	See Figure 1			±0.2	V
V_{OC}	Common-mode output voltage					3	V
$\Delta \lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage¶					±0.2	V
I_O	Output current	Output disabled, See Note 4	$V_O = 12$ V			1	mA
			$V_O = -7$ V			−0.8	
I_{IH}	High-level input current	$V_I = 2.4$ V				20	μA
I_{IL}	Low-level input current	$V_I = 0.4$ V				−200	μA
I_{OS}	Short-circuit output current#	$V_O = -6$ V				−250	mA
		$V_O = 0$				−150	
		$V_O = V_{CC}$				250	
		$V_O = 8$ V				250	
I_{CC}	Supply current	No load	Outputs enabled		23	50	mA
			Outputs disabled		19	35	

† The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.

‡ All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

§ The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.

¶ $\Delta \lvert V_{OD} \rvert$ and $\Delta \lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

Duration of the short circuit should not exceed one second for this test.

NOTE 4: This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	$C_{L1} = C_{L2} = 100$ pF,	$R_L = 60\ \Omega$,	See Figure 3		8	22	ns
	Skew ($\lvert t_{d(ODH)} - t_{d(ODL)} \rvert$)					1	8	ns
$t_{t(OD)}$	Differential output transition time					8	18	ns
t_{PZH}	Output enable time to high level	$C_L = 100$ pF,	$R_L = 500\ \Omega$,	See Figure 4			50	ns
t_{PZL}	Output enable time to low level	$C_L = 100$ pF,	$R_L = 500\ \Omega$,	See Figure 5			50	ns
t_{PHZ}	Output disable time from high level	$C_L = 15$ pF,	$R_L = 500\ \Omega$,	See Figure 4		8	30	ns
t_{PLZ}	Output disable time from low level	$C_L = 15$ pF,	$R_L = 500\ \Omega$,	See Figure 5		8	30	ns

‡ All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.

SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$\lvert V_{OD3} \rvert$		V_t (test termination measurement 2)
V_{test}		V_{tst}
$\Delta \lvert V_{OD} \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$	$\lvert \lvert V_t \rvert - \lvert \overline{V}_t \rvert \rvert$
V_{OC}	$\lvert V_{os} \rvert$	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	$\lvert I_{sa} \rvert$, $\lvert I_{sb} \rvert$	
I_O	$\lvert I_{xa} \rvert$, $\lvert I_{xb} \rvert$	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[†]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA	−0.2[‡]			V
V_{hys}	Hysteresis voltage (V_{IT+}–V_{IT-})	V_{OC} = 0			70		mV
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV or inputs open, I_{OH} = −400 µA, See Figure 6		2.4			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 6	I_{OL} = 16 mA			0.5	V
			I_{OL} = 8 mA			0.45	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	µA
I_I	Line input current	Other input = 0, See Note 5	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	µA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	µA
r_I	Input resistance			12			kΩ
I_{OS}	Short-circuit output current[§]	V_O = 0		−15		−85	mA
I_{CC}	Supply current	No load	Outputs enabled		23	50	mA
			Outputs disabled		19	35	

[†] All typical values are at V_{CC} = 5 V and T_A = 25°C.

[‡] The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

[§] Duration of the short circuit should not exceed one second for this test.

NOTE 5: This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range, C_L = 15 pF

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = –1.5 V to 1.5 V, See Figure 7		14	37	ns
t_{PHL}	Propagation delay time, high- to low-level output			14	37	ns
t_{PZH}	Output enable time to high level	See Figure 8		7	20	ns
t_{PZL}	Output enable time to low level			7	20	ns
t_{PHZ}	Output disable time from high level	See Figure 8		7	16	ns
t_{PLZ}	Output disable time from low level			8	16	ns

† All typical values are at V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

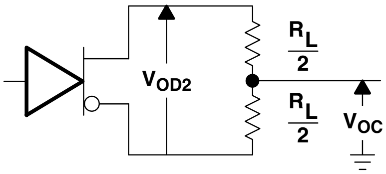


Figure 1. Driver V_{OD} and V_{OC}

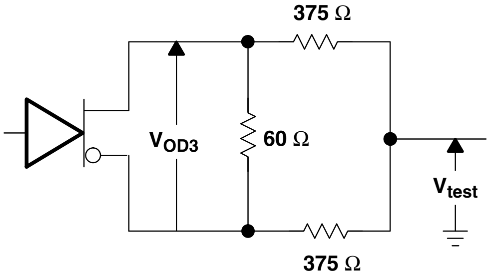
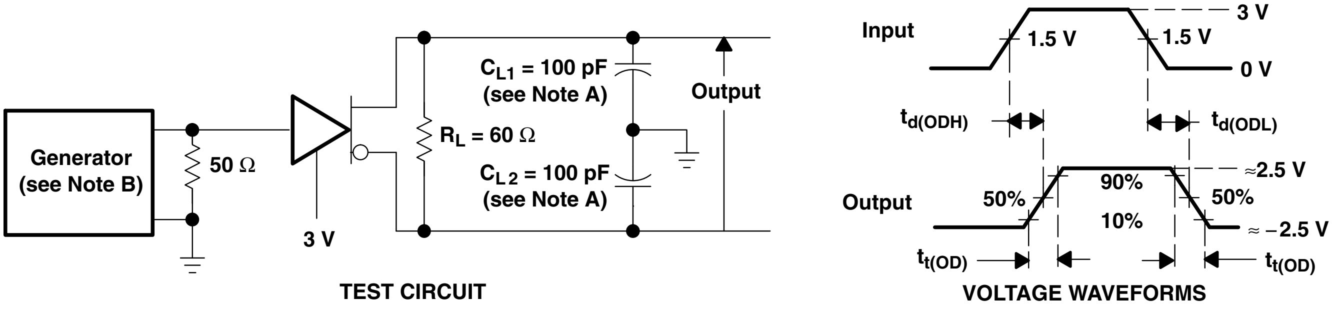


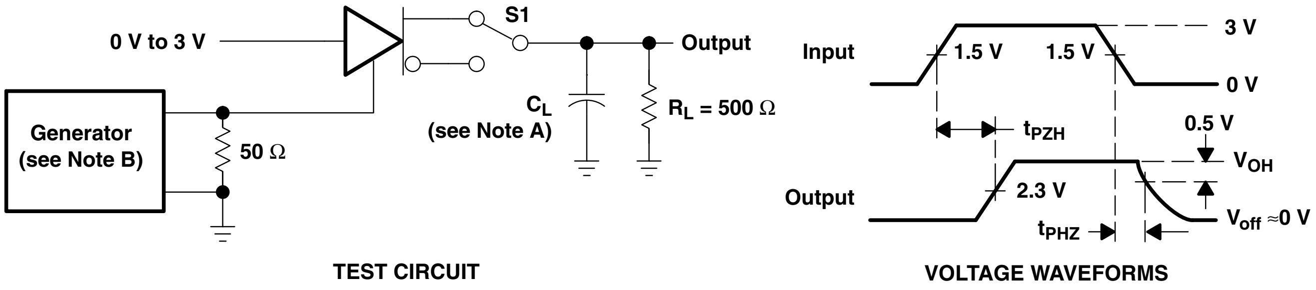
Figure 2. Driver V_{OD3}



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

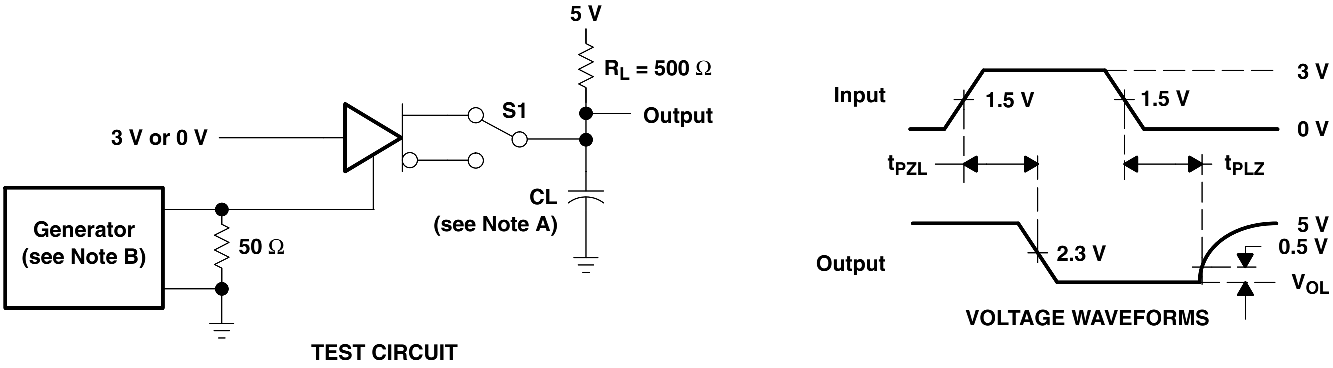
Figure 3. Driver Differential-Output Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_O = 50 Ω.

Figure 4. Driver Test Circuit and Voltage Waveforms



NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns, Z_O = 50 Ω..

Figure 5. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

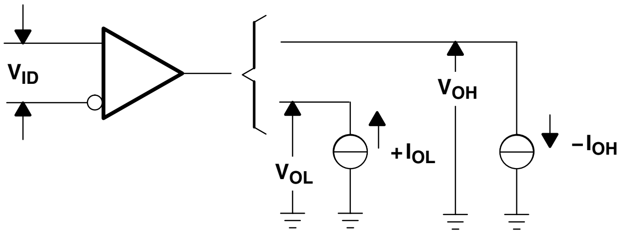
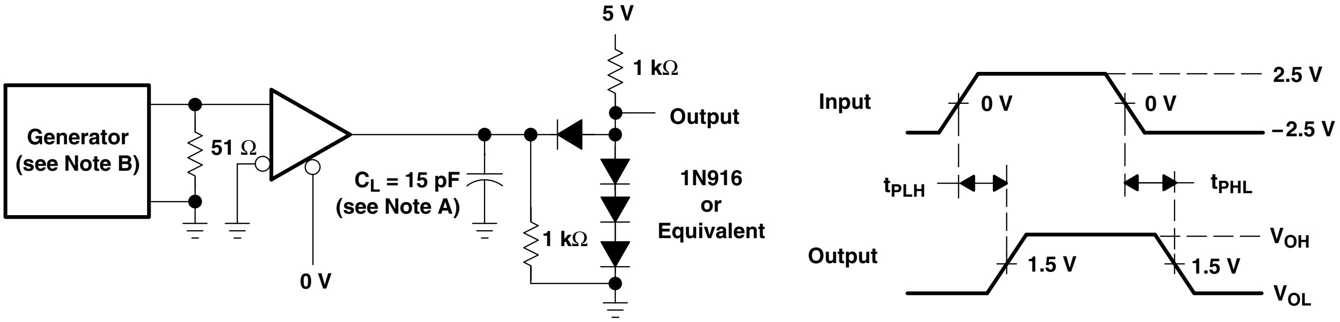


Figure 6. Receiver V_{OH} and V_{OL}



TEST CIRCUIT

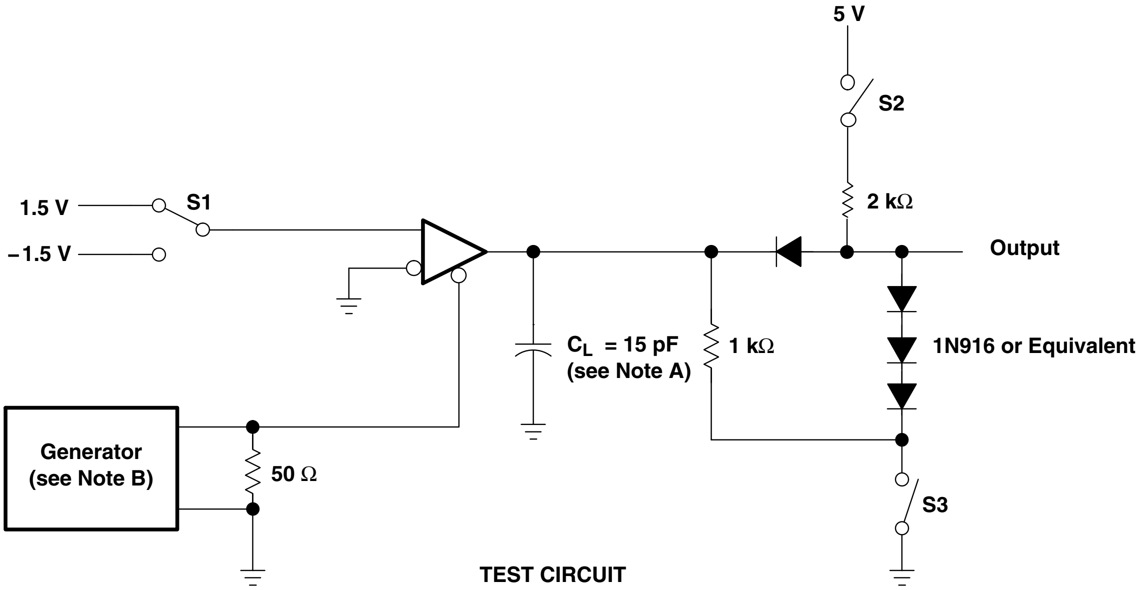
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.

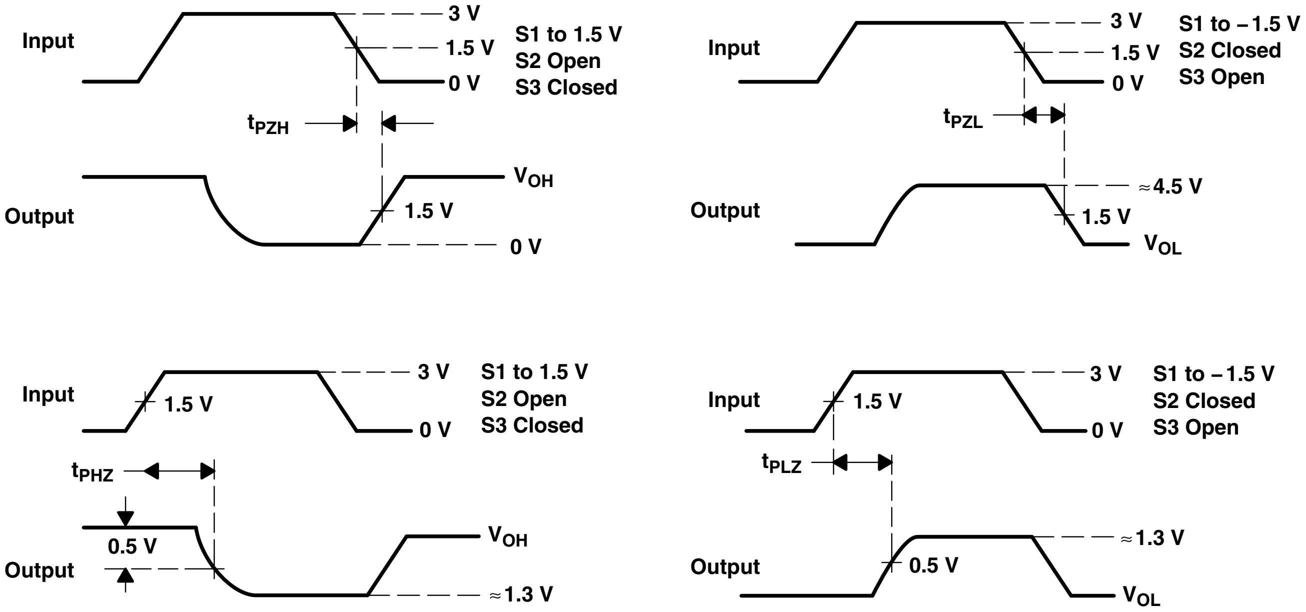
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns, $Z_O = 50\ \Omega$.

Figure 7. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50\ \Omega$.

Figure 8. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

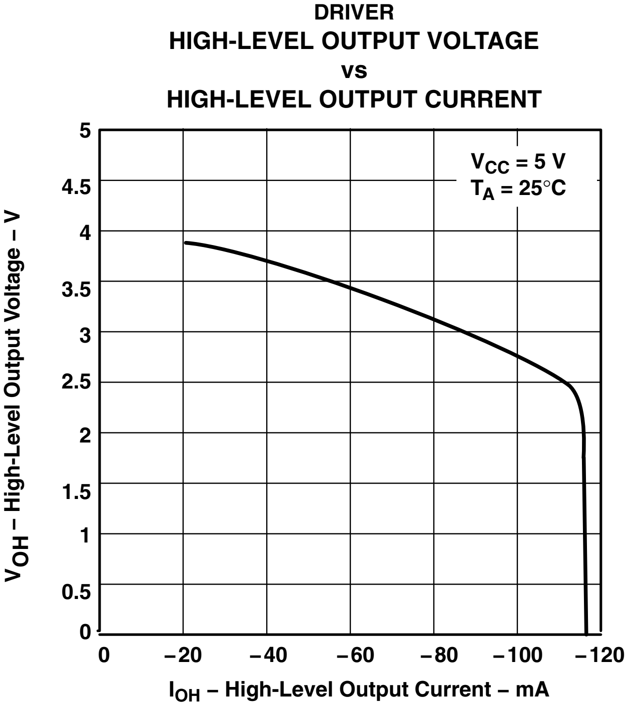


Figure 9

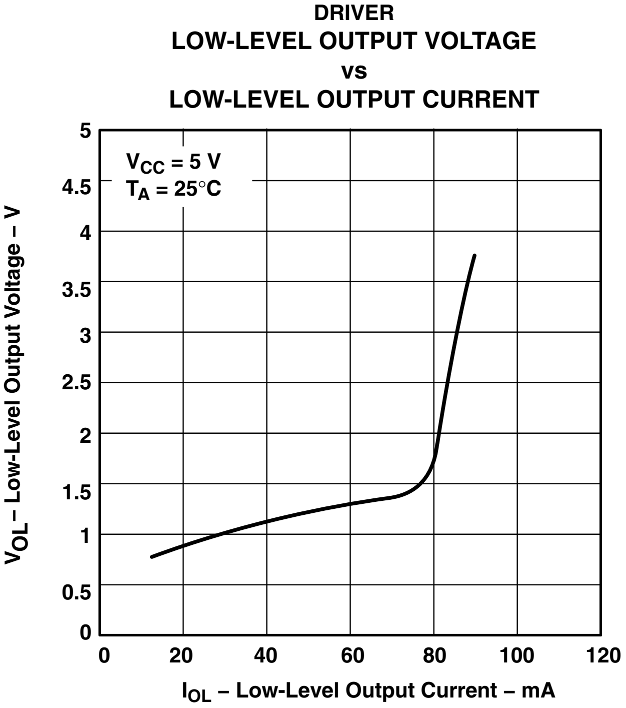


Figure 10

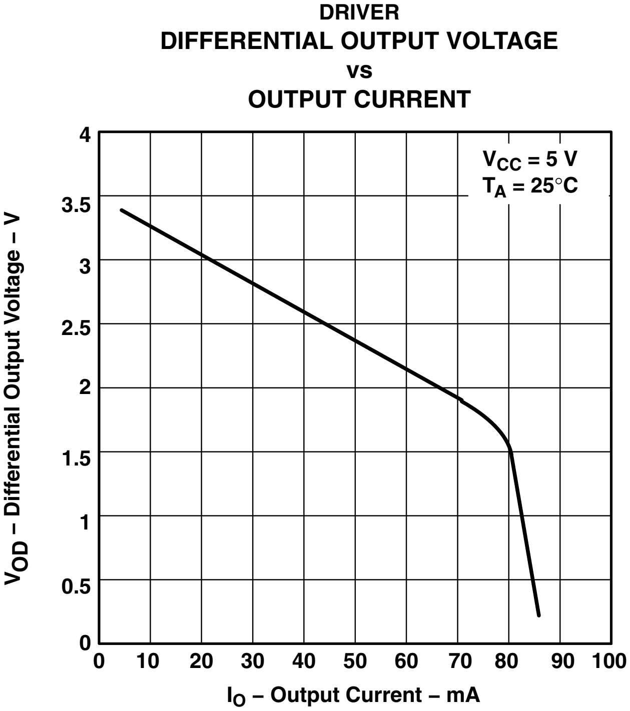


Figure 11

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† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

TYPICAL CHARACTERISTICS†

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

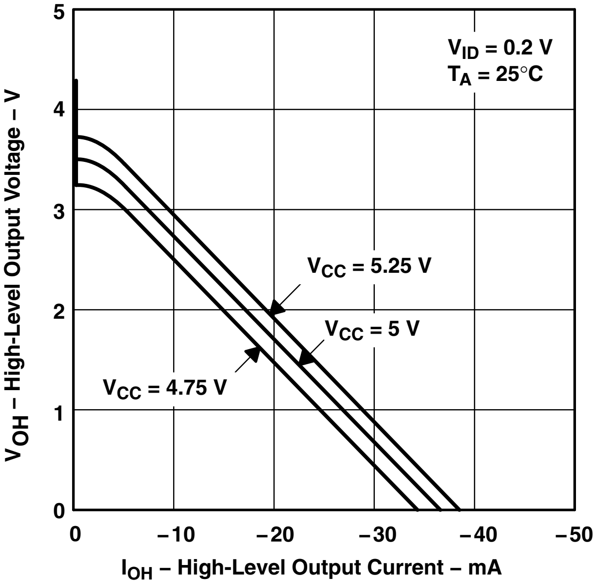

Figure 12

RECEIVER
HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

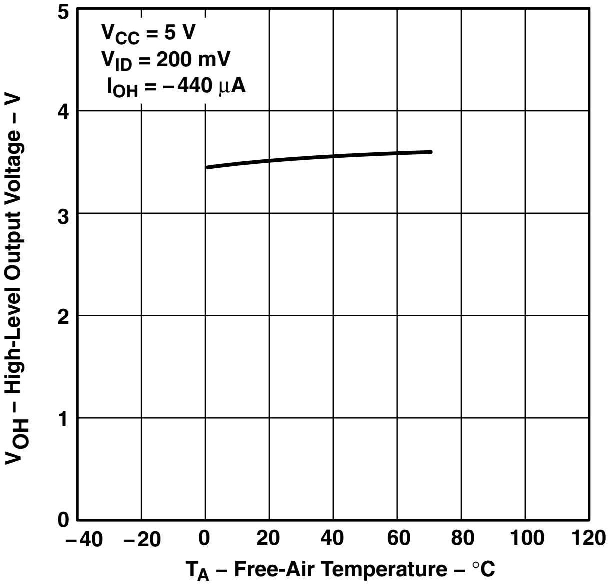

Figure 13

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

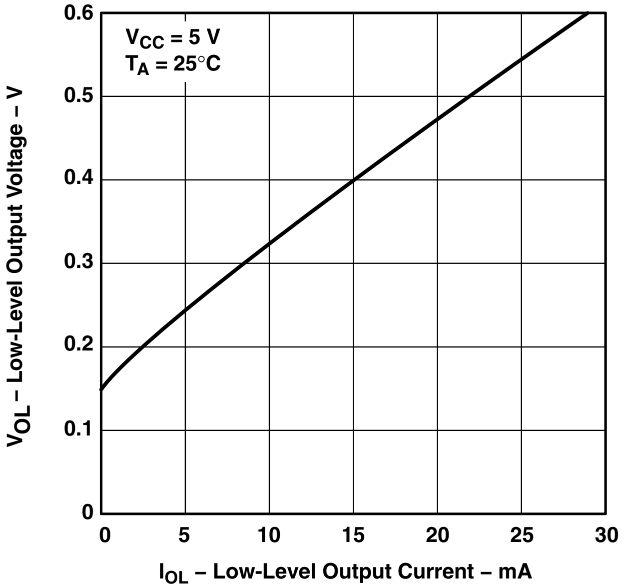

Figure 14

RECEIVER
LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

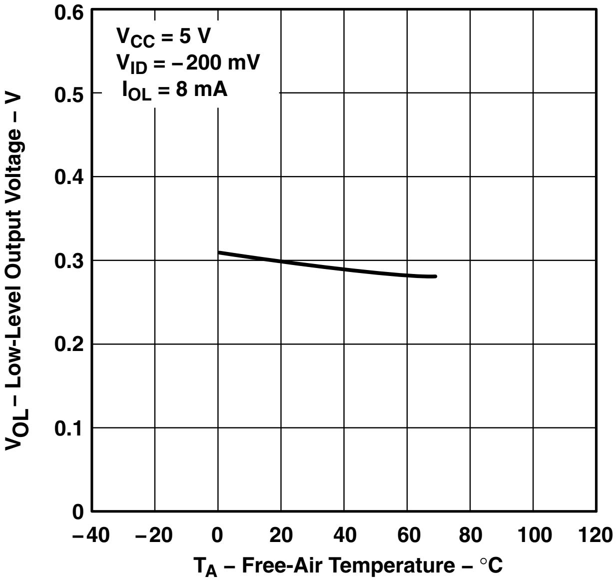

Figure 15

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† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

TYPICAL CHARACTERISTICS†

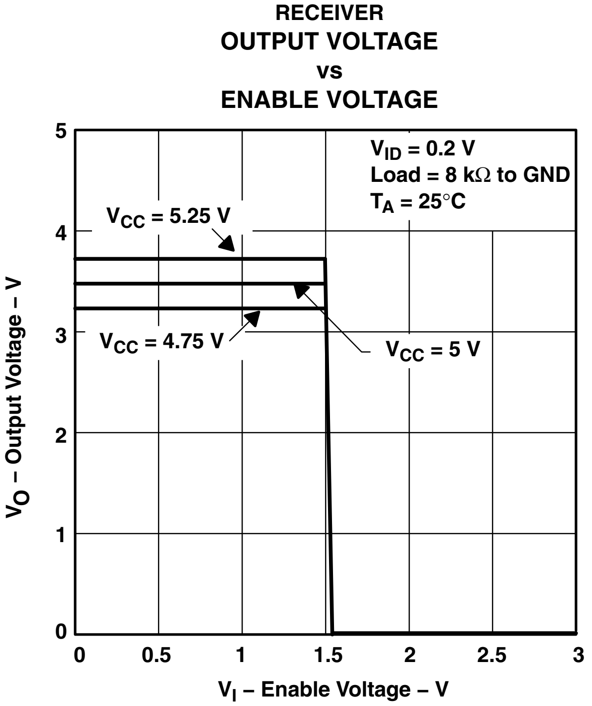


Figure 16

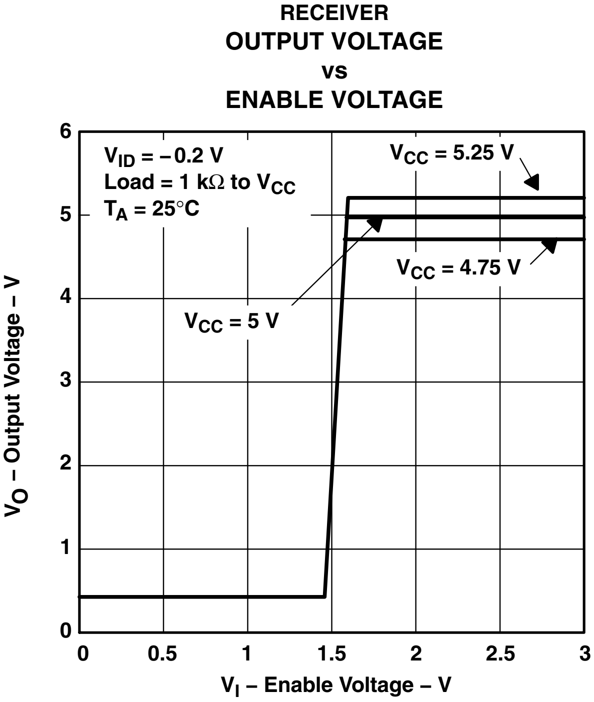
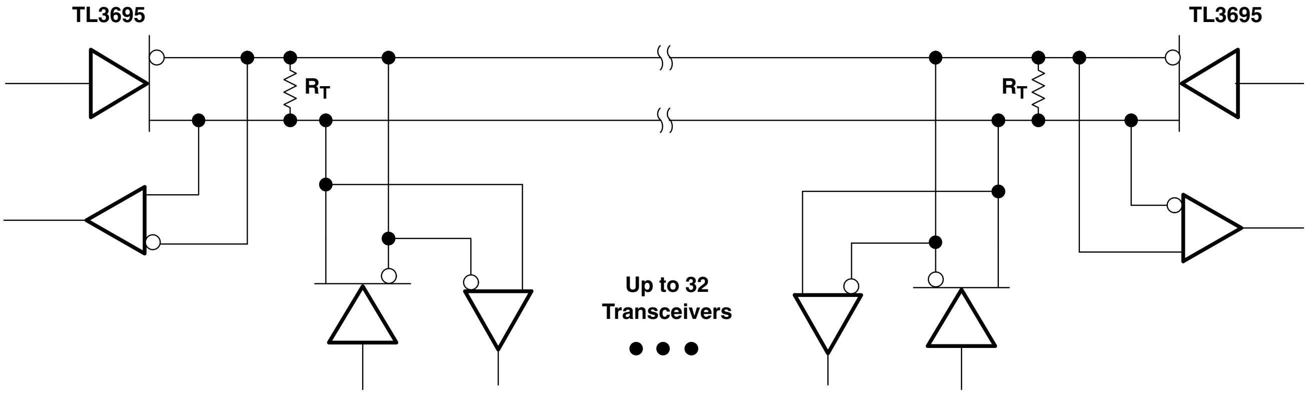


Figure 17

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 18. Typical Application Circuit

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL3695D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3695	Samples
TL3695DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3695	Samples
TL3695DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL3695	Samples
TL3695P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL3695P	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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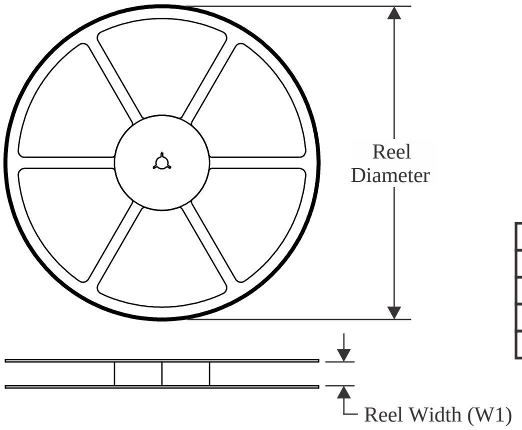
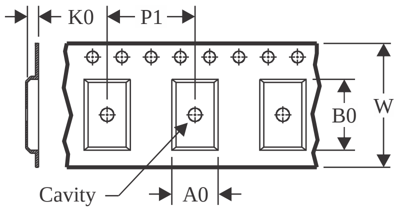
TAPE AND REEL INFORMATION

REEL DIMENSIONS

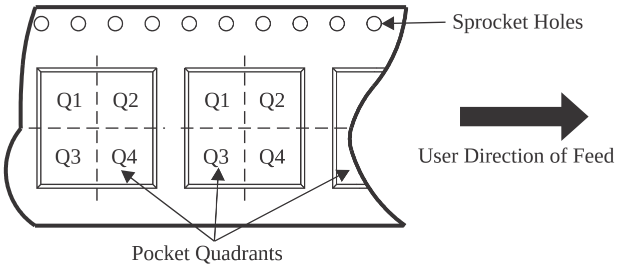


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

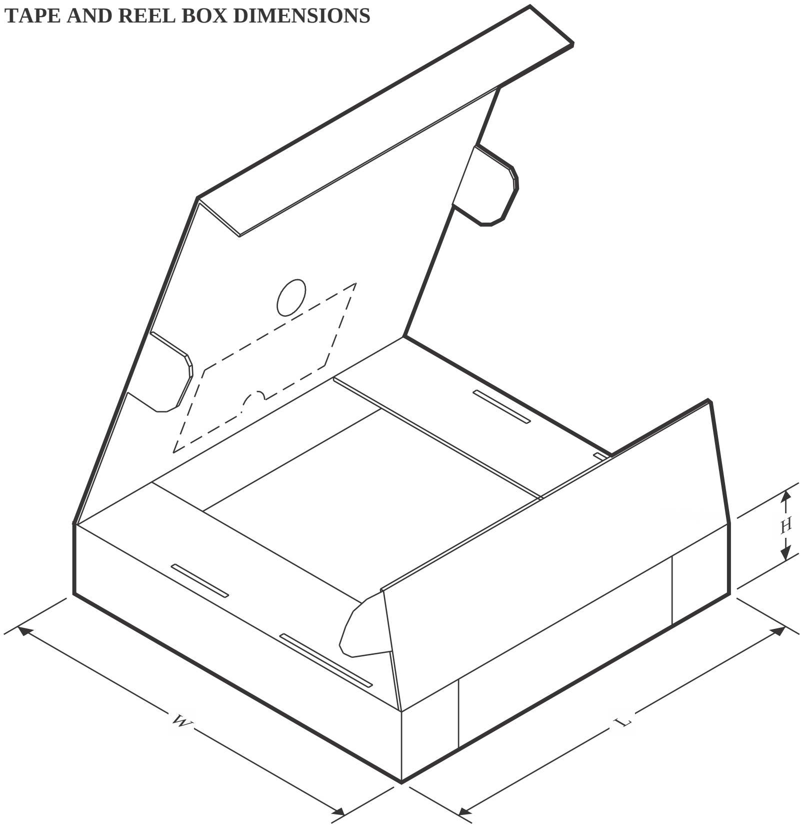
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL3695DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

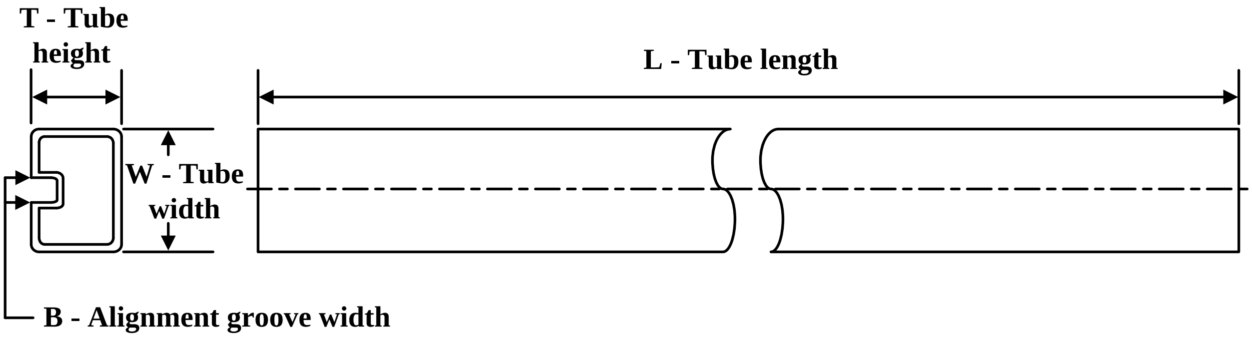
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

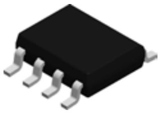
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL3695DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL3695D	D	SOIC	8	75	507	8	3940	4.32
TL3695P	P	PDIP	8	50	506	13.97	11230	4.32

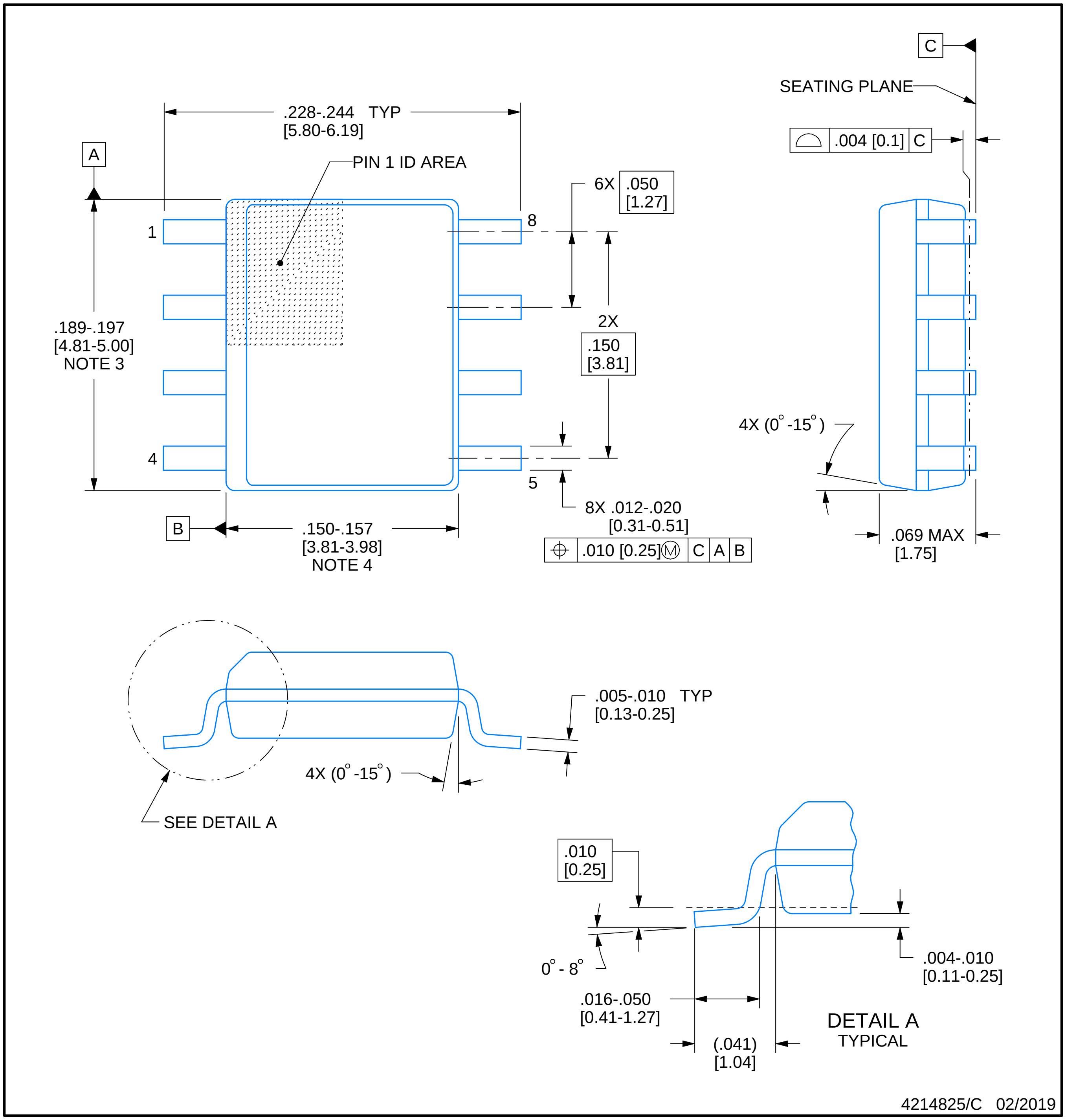


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



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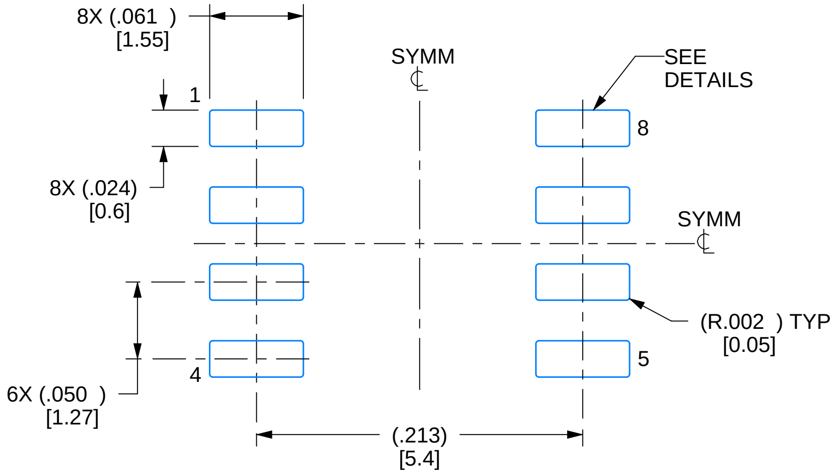
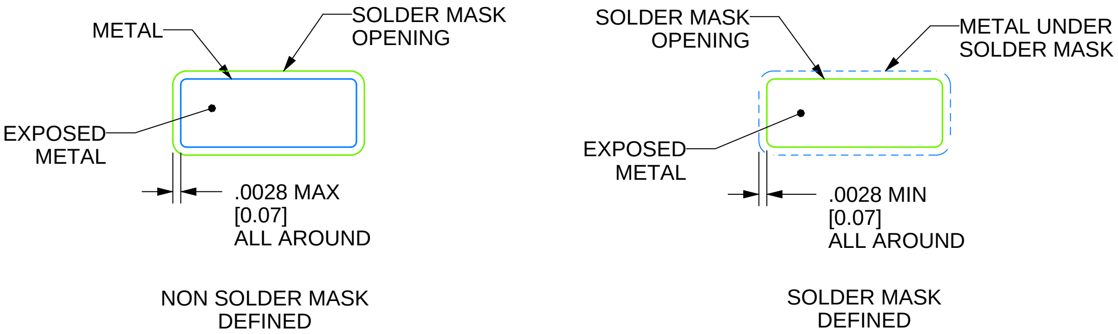
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



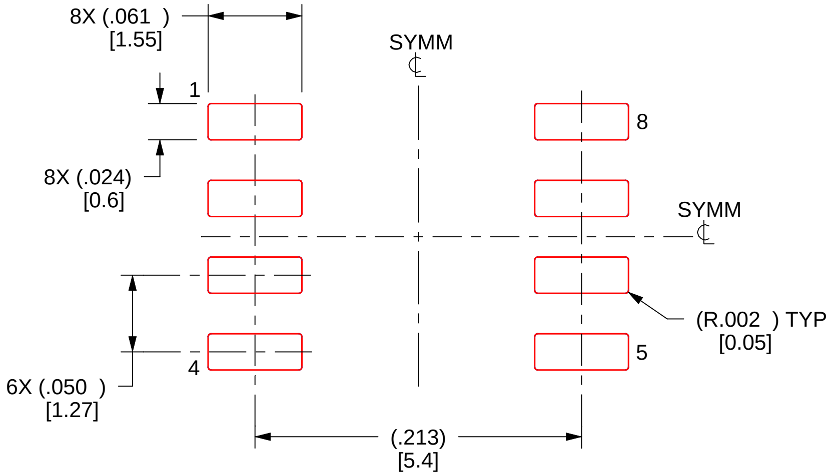
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

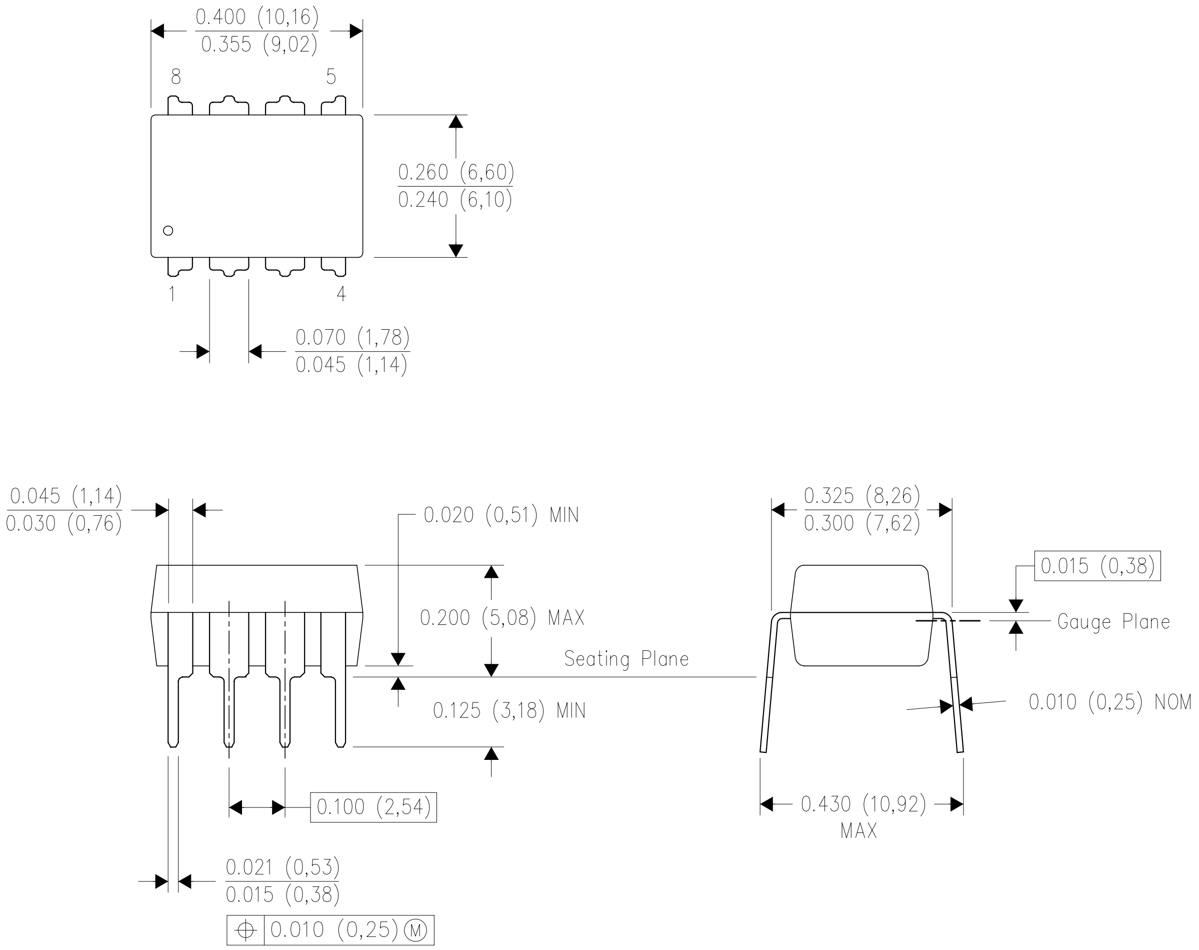


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



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NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001 variation BA.

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