TL594 Pulse-Width-Modulation Control Circuit

1 Features

- Complete PWM power-control circuitry
- Uncommitted outputs for 200mA sink or source current
- Output control selects single-ended or push-pull operation
- Internal circuitry prohibits double pulse at either output
- Variable dead time provides control over total range
- Internal regulator provides a stable 5V reference supply trimmed to 1%
- Circuit architecture allows easy synchronization
- Undervoltage lockout (UVLO) for low-V_{CC} conditions

2 Applications

- White goods
- Power supplies: AC/DC, isolated, with PFC, > 90W
- Server PSUs
- Solar micro-inverters
- Power supplies: AC/DC, isolated, no PFC, < 90W
- Power: telecom/server AC/DC supplies
- Solar power inverters

3 Description

The TL594 device incorporates all the functions required in the construction of a pulse width modulation (PWM) control circuit on a chip. Designed primarily for power-supply control, this device offers the systems engineer the flexibility to tailor the power-supply control circuitry to a specific application.

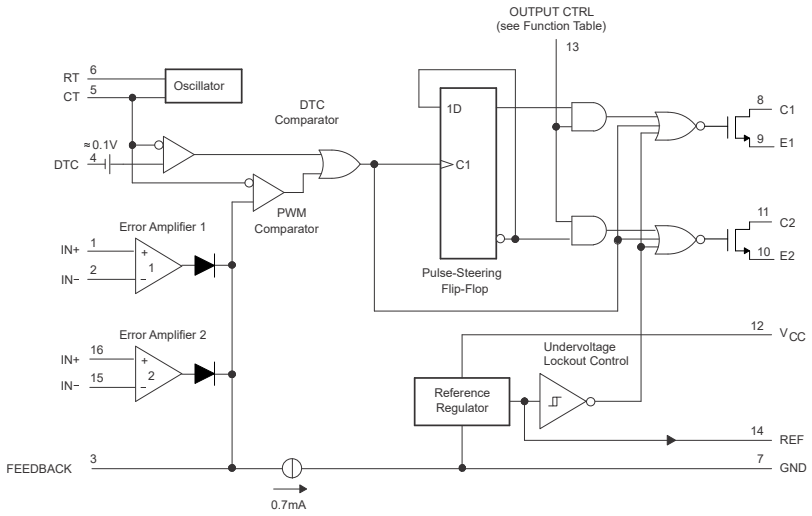
The TL594 device contains two error amplifiers, an on-chip adjustable oscillator, a dead-time control (DTC) comparator, a pulse-steering control flip-flop, a 5V regulator with a precision of 1%, an undervoltage lockout control circuit, and output control circuitry.

The uncommitted output transistors provide either common-source or source-follower output capability. Each device provides for push-pull or single-ended output operation, with selection by means of the output-control function. The architecture of these devices prohibits the possibility of either output pulsing twice during push-pull operation. The undervoltage lockout control circuit locks the outputs off until the internal circuitry is operational.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TL594D	SOIC (16)	9.90mm × 3.91mm
TL594NS	SO (16)	10.30mm × 5.30mm
TL594PW	TSSOP (16)	5.00mm × 4.40mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



For OUTPUT CTRL function, see Table 7-1.

Block Diagram

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4 Pin Configuration and Functions

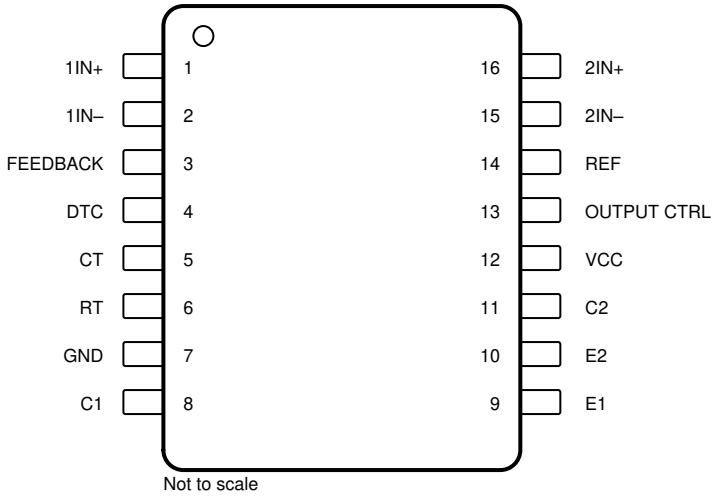


Figure 4-1. D, NS, or PW Package 16-Pin SOIC, SO, or TSSOP Top View

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
1IN–	2	I	Inverting input to error amplifier 1
1IN+	1	I	Noninverting input to error amplifier 1
2IN–	15	I	Inverting input to error amplifier 2
2IN+	16	I	Noninverting input to error amplifier 2
C1	8	O	Drain terminal of MOSFET output 1
C2	11	O	Drain terminal of MOSFET output 2
CT	5	—	Capacitor terminal used to set oscillator frequency
DTC	4	I	Dead-time control comparator input
E1	9	O	Source terminal of MOSFET output 1
E2	10	O	Source terminal of MOSFET output 2
FEEDBACK	3	I	Input pin for feedback
GND	7	—	Ground
OUTPUT CTRL	13	I	Selects single-ended, parallel output, or push-pull operation
REF	14	O	5V reference regulator output
RT	6	—	Resistor terminal used to set oscillator frequency
V_{CC}	12	—	Positive supply

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage, V_{CC} (2)		41	V
Amplifier input voltage		V_{CC} + 0.3	V
Collector output voltage		41	V
Collector output current		250	mA
Operating junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential voltages, are with respect to the network ground terminal.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		7	40	V
V_I	Amplifier input voltage		–0.3	V_{CC} – 2	V
V_O	Collector output voltage			40	V
	Collector output current (each transistor)			200	mA
	Current into FEEDBACK terminal			0.3	mA
C_T	Timing capacitor		0.47	10000	nF
R_T	Timing resistor		1.8	500	kΩ
f_{osc}	Oscillator frequency		1	300	kHz
T_A	Operating free-air temperature	TL594C	0	70	°C
		TL594I	–40	85	

5.4 Thermal Information

THERMAL METRIC(1)		TL594			UNIT
		D (SOIC)	NS (SO)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	88.0	95.3	114.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.4	56.8	53.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	50.6	62.0	71.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.5	19.6	7.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.1	61.3	71.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

V_{CC} = 15V, over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]	MIN	TYP[2]	MAX	UNIT
REFERENCE					
Output voltage (REF)	I_O = 1mA, T_A = 25°C	4.95	5	5.05	V
Input regulation	V_{CC} = 7V to 40V, T_A = 25°C		2	25	mV
Output regulation	I_O = 1mA to 10mA, T_A = 25°C		6	35	mV
Output-voltage change with temperature	ΔT_A = MIN to MAX		2	10	mV/V
Short-circuit output current[3]	V_{ref} = 0	10	35	50	mA
AMPLIFIER (see Figure 6-1)					
Input offset voltage, error amplifier	FEEDBACK = 2.5V		2	10	mV
Input offset current	FEEDBACK = 2.5V		25	250	nA
Input bias current	FEEDBACK = 2.5V		0.2	1	µA
Common mode input voltage, error amplifier	V_{CC} = 7V to 40V	0.3 to V_{CC} – 2			V
Open-loop voltage amplification, error amplifier	ΔV_O = 3V, R_L = 2kΩ, V_O = 0.5V to 3.5V	70	80		dB
Unity-gain bandwidth	V_O = 0.5V to 3.5V, R_L = 2kΩ		800		kHz
Common mode rejection ratio, error amplifier	V_{CC} = 40V, T_A = 25°C	65	100		dB
Output sink current, FEEDBACK	V_{ID} = –15mV to –5V, FEEDBACK = 0.5V	0.3	0.7		mA
Output source current, FEEDBACK	V_{ID} = 15mV to 5V, FEEDBACK = 3.5V	–2			mA
OSCILLATOR, C_T = 0.01µF, R_T = 12kΩ (see Figure 6-2)					
Frequency			10		kHz
Standard deviation of frequency[4]	All values of V_{CC}, C_T, R_T, and T_A constant		100		Hz/kHz
Frequency change with voltage	V_{CC} = 7V to 40V, T_A = 25°C		1		Hz/kHz
Frequency change with temperature[5]	ΔT_A = MIN to MAX			50	Hz/kHz
DEAD-TIME CONTROL (see Figure 6-2)					
Input bias current	V_I = 0 to 5.25V		–0.006	–10	µA
Maximum duty cycle, each output	DTC = 0V	0.45			
Input threshold voltage	Zero duty cycle		2.5	3.3	V
	Maximum duty cycle	0			
OUTPUT					
C1, C2 off-state current	V_C = 40V, V_E = 0V, V_{CC} = 40V		4	100	µA
	DTC and OUTPUT CTRL = 0V, V_C = 15 V, V_E = 0 V, V_{CC} = 1 V to 3 V		2	200	
E1, E2 off-state current	V_{CC} = V_C = 40V, V_E = 0			–100	µA
C1E1, C2E2 saturation voltage	Common Source, V_E = 0, I_C = 200mA		0.5	1.3	V
	Source follower, V_C = 15V, I_E = –200mA		1.65	2.5	
Output control input current	V_I = V_{ref}			3.5	mA
PWM COMPARATOR (see Figure 6-2)					
Input threshold voltage, FEEDBACK	Zero duty cycle		3.4	4.5	V
Input sink current, FEEDBACK	FEEDBACK = 0.5V	0.3	0.7		mA
UNDERVOLTAGE LOCKOUT (see Figure 6-2)					
Threshold voltage	T_A = 25°C			6	V
	ΔT_A = MIN to MAX	3.5		6.9	
Hysteresis[6]		100			mV

5.5 Electrical Characteristics (continued)

V_{CC} = 15V, over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
OVERALL DEVICE						
Standby supply current	R_T at V_{ref}, All other inputs and outputs open	V_{CC} = 15V		1.62	15	mA
		V_{CC} = 40V		1.68	18	
Average supply current	DTC = 2V, see Figure 6-2			2.2		mA

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(2) All typical values, except for parameter changes with temperature, are at T_A = 25°C.
(3) Duration of the short circuit must not exceed one second.
(4) Standard deviation is a measure of the statistical distribution about the mean, as derived from the formula:

$$\sigma = \sqrt{\frac{\sum_{n=1}^{N} [x_n - \bar{X}]^2}{N-1}} \quad (1)$$

(5) Temperature coefficient of timing capacitor and timing resistor is not taken into account.
(6) Hysteresis is the difference between the positive-going input threshold voltage and the negative-going input threshold voltage.

5.6 Switching Characteristics

V_{CC} = 15V, T_A = 25°C, over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output-voltage rise time	Common-source configuration (see Figure 6-3)		70	200	ns
Output-voltage fall time	Common-source configuration (see Figure 6-3)		20	100	ns
Output-voltage rise time	Source-follower configuration (see Figure 6-4)		85	400	ns
Output-voltage fall time	Source-follower configuration (see Figure 6-4)		35	100	ns

5.7 Typical Characteristics

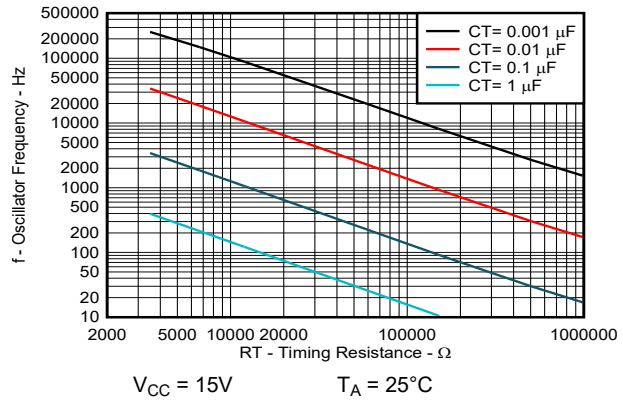


Figure 5-1. Oscillator Frequency vs Timing Resistance

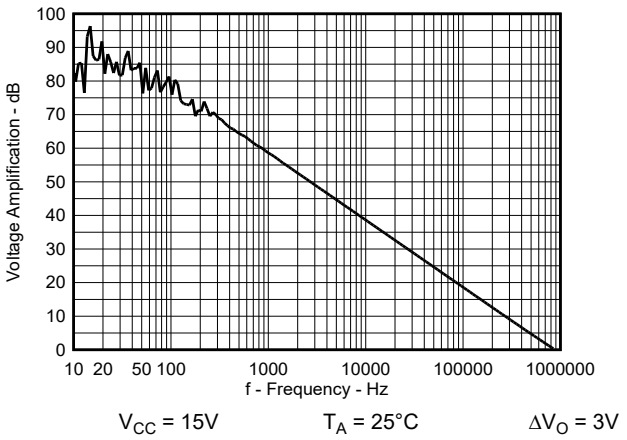


Figure 5-2. Amplifier Voltage Amplification vs Frequency

6 Parameter Measurement Information

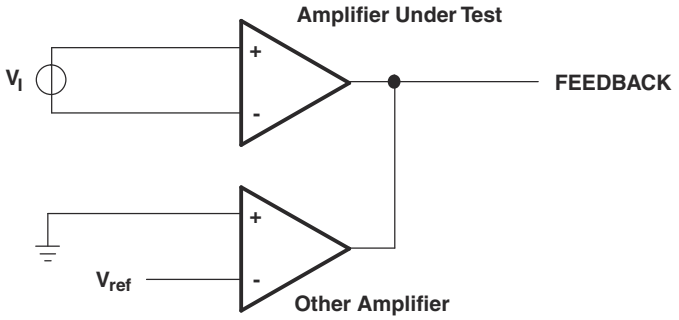


Figure 6-1. Amplifier-Characteristics Test Circuit

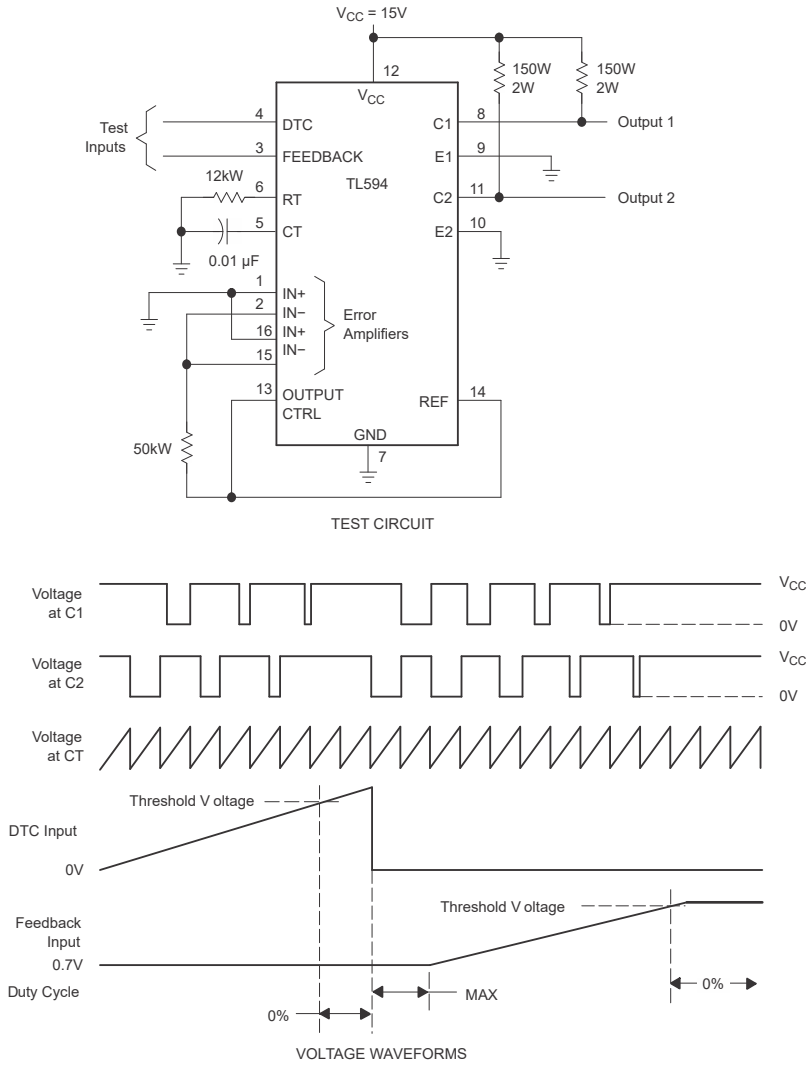


Figure 6-2. Operational Test Circuit and Waveforms

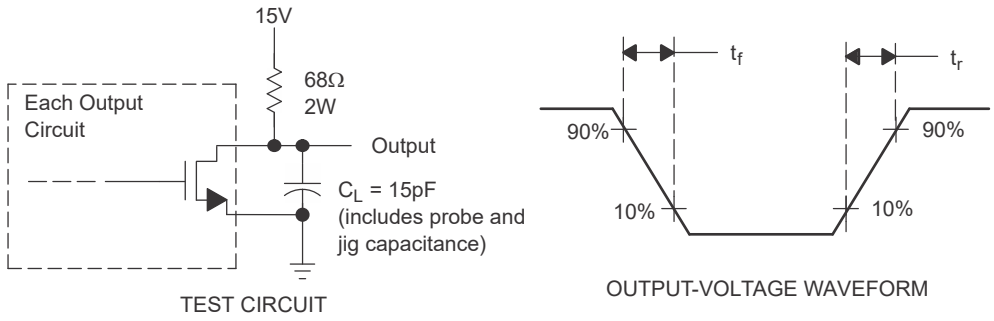


Figure 6-3. Common-Emitter Configuration

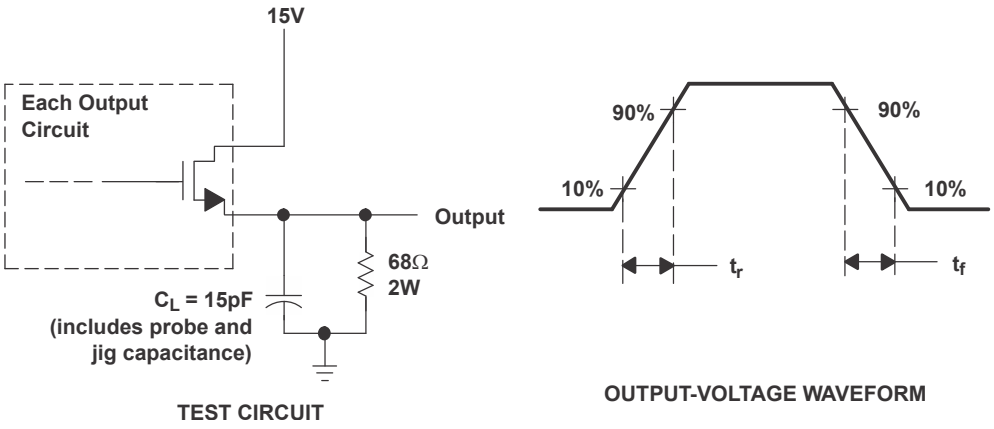


Figure 6-4. Emitter-Follower Configuration

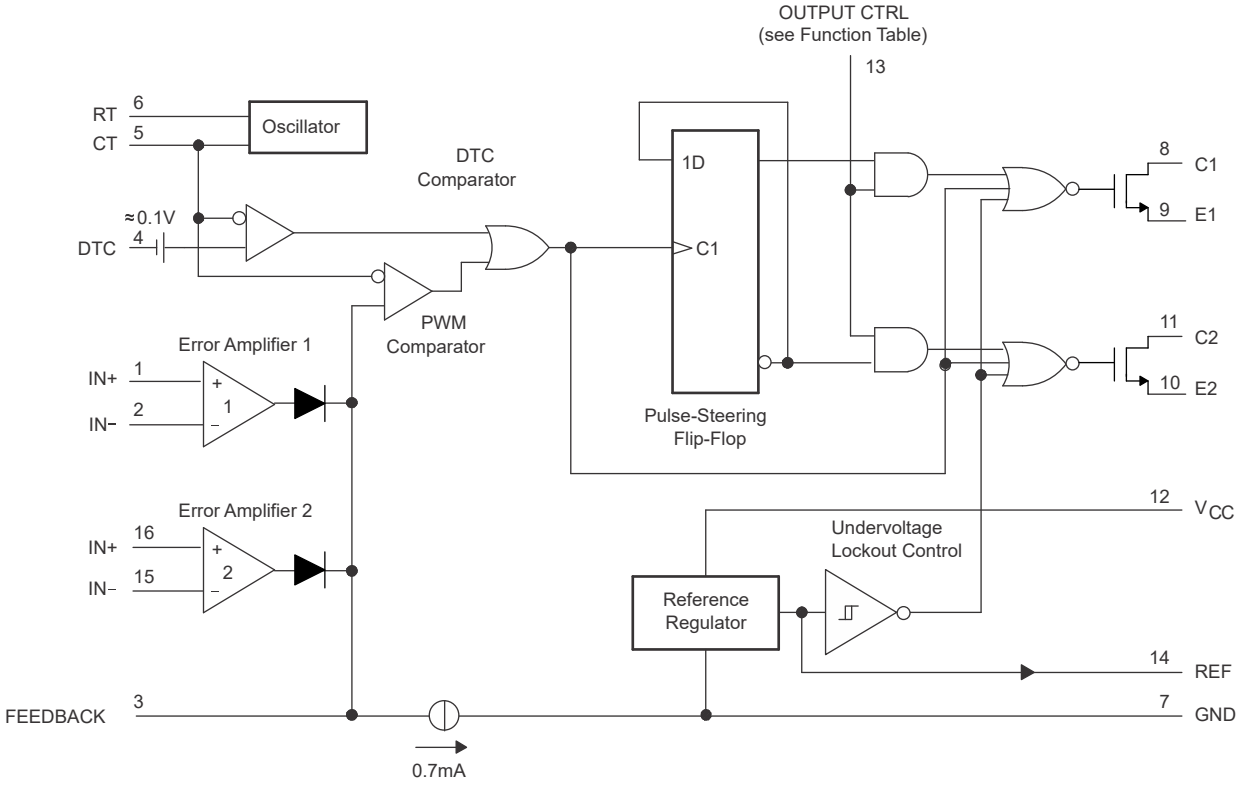
7 Detailed Description

7.1 Overview

The design of the TL594 incorporates the primary building blocks required to control a switching power supply and also addresses many basic problems and reduces the amount of additional circuitry required in the total design. The TL594 is a fixed-frequency pulse width modulation (PWM) control circuit. Modulation of output pulses is accomplished by comparing the sawtooth waveform created by the internal oscillator on the timing capacitor (CT) to either of two control signals. The output stage is enabled during the time when the sawtooth voltage is greater than the voltage control signals. As the control signal increases, the time during which the sawtooth input is greater decreases; therefore, the output pulse duration decreases. A pulse-steering flip-flop alternately directs the modulated pulse to each of the two output transistors.

The error amplifiers have a common-mode voltage range from –0.3 V to V_{CC} – 2 V. The DTC comparator has a fixed offset that provides approximately 5% dead time. Bypass the on-chip oscillator by terminating RT to the reference output and providing a sawtooth input to CT, or use the on-chip oscillator to drive the common circuitry in synchronous multiple-rail power supplies. For more information on the operation of the TL594, see *Designing Switching Voltage Regulators With the TL494*.

7.2 Functional Block Diagram



For OUTPUT CTRL function, see Table 7-1.

7.3 Feature Description

7.3.1 5V Reference Regulator

The TL594 internal 5V reference regulator output is the REF pin. In addition to providing a stable reference, it acts as a preregulator and establishes a stable supply from which the output-control logic, pulse-steering flip-flop, oscillator, dead-time control comparator, and PWM comparator are powered. The regulator employs a band-gap circuit as its primary reference to maintain thermal stability of less than 100mV variation over the operating free-air temperature range from 0°C to 70°C. Short-circuit protection is provided to protect the internal reference and preregulator; 10mA of load current is available for additional bias circuits. The reference

is internally programmed to an initial accuracy of ±1% and maintains a stability of less than 25mV variation over an input voltage range from 7V to 40V. For input voltages less than 7V, regulator output remains at 0V until the internal references reach a valid level, after which it transitions to 5V, resulting in more deterministic startup behavior, as Figure 8-9 shows.

7.3.2 Undervoltage Lockout

The TL594 has circuitry to provide an undervoltage-lockout functionality. A minimum recommended V_{CC} voltage of 7V is recommended for operation, but if the V_{CC} voltage drops below 6V during operation, then the device shuts off. See *Electrical Characteristics* for additional information regarding the undervoltage lockout circuitry.

7.3.3 Oscillator

The oscillator provides a positive sawtooth waveform to the dead-time and PWM comparators for comparison to the various control signals.

Select the timing components R_T and C_T to program the frequency of the oscillator. The oscillator charges the external timing capacitor, C_T, with a constant current. The external timing resistor, R_T determines the value of the constant current and produces a linear-ramp voltage waveform. When the voltage across C_T reaches 3V, the oscillator circuit discharges it, and the charging cycle is reinitiated. Equation 2 determines the charging current.

$$I_{CHARGE} = \frac{3V}{R_T} \tag{2}$$

The period of the sawtooth waveform is Equation 3.

$$T = \frac{3V \times C_T}{I_{CHARGE}} \tag{3}$$

The frequency of the oscillator becomes Equation 4.

$$f_{OSC} = \frac{1}{R_T \times C_T} \tag{4}$$

However, the oscillator frequency is equal to the output frequency only for single-ended applications. For push-pull applications, the output frequency is one-half the oscillator frequency.

Calculate single-ended applications with Equation 5.

$$f = \frac{1}{R_T \times C_T} \tag{5}$$

Calculate push-pull applications with Equation 6.

$$f = \frac{1}{2R_T \times C_T} \tag{6}$$

7.3.4 Dead-Time Control

The dead-time control input provides control of the minimum dead time (off time). The output of the comparator inhibits switching transistors Q1 and Q2 when the voltage at the input is greater than the ramp voltage of the oscillator. An internal offset of 110 mV confirms a minimum dead time of approximately 3% with the dead-time control input grounded. Applying a voltage to the dead-time control input can impose additional dead time. This provides a linear control of the dead time from its minimum of 3% to 100% as the input voltage varies from 0 V to 3.3 V, respectively. With full-range control, external sources can control the output without disrupting the error amplifiers. The dead-time control input is a relatively high-impedance input (I_I < 10 µA) and must be used where additional control of the output duty cycle is required. However, for proper control, the input must be terminated. An open circuit is an undefined condition.

7.3.5 Comparator

The comparator is biased from the 5V reference regulator and provides isolation from the input supply for improved stability. The input of the comparator does not exhibit hysteresis, so protection against false triggering near the threshold must be provided. The comparator has a response time of 400ns from either of the control-signal inputs to the output transistors, with only 100 mV of overdrive. This establishes positive control of the output within one-half cycle for operation within the recommended 300kHz range.

7.3.6 Pulse-Width Modulation (PWM)

The comparator also provides modulation control of the output pulse duration. For this, the ramp voltage across timing capacitor C_T is compared to the control signal present at the output of the error amplifiers. The timing capacitor input incorporates a series diode that is omitted from the control signal input. This requires the control signal (error amplifier output) to be approximately 0.7V greater than the voltage across C_T to inhibit the output logic, and specifies maximum duty cycle operation without requiring the control voltage to sink to a true ground potential. The output pulse duration varies from 97% of the period to 0 as the voltage present at the error amplifier output varies from 0.5V to 3.5V, respectively.

7.3.7 Error Amplifiers

Both high-gain error amplifiers receive bias from the V_I supply rail. This permits a common-mode input voltage range from –0.3V to 2V less than V_I. Both amplifiers behave characteristically of a single-ended single-supply amplifier, in that each output is active high only. This allows each amplifier to pull up independently for a decreasing output pulse-width demand. With both outputs ORed together at the inverting input node of the PWM comparator, the amplifier demanding the minimum pulse out dominates. The amplifier outputs are biased low by a current sink to provide maximum pulse duration out when both amplifiers are biased off.

7.3.8 Output-Control Input

The output-control input determines whether the output transistors operate in parallel or push-pull. This input is the supply source for the pulse-steering flip-flop. The output-control input is asynchronous and has direct control over the output, independent of the oscillator or pulse-steering flip-flop. The input condition is intended to be a fixed condition that the application defines. For parallel operation, ground the output-control input. This disables the pulse-steering flip-flop and inhibits its outputs. In this mode, both output transistors in parallel transmit the pulses seen at the output of the dead-time control or PWM comparator. For push-pull operation, connect the output-control input to the internal 5V reference regulator. Under this condition, each of the output transistors is enabled, alternately, by the pulse-steering flip-flop.

7.3.9 Output Transistors

Two output transistors are available on the TL594. The configuration of both transistors is as open drain/open source, and each can sink or source up to 200 mA. The transistors have a saturation voltage of less than 1.3 V in the common-source configuration and less than 2.5 V in the source-follower configuration. The outputs are protected against excessive power dissipation to prevent damage and employ sufficient current limiting to operate the outputs as current-source outputs.

7.4 Device Functional Modes

When the OUTPUT CTRL pin is tied to ground, the TL594 is operating in single-ended or parallel mode. When the OUTPUT CTRL pin is tied to V_{REF}, the TL594 is operating in normal push-pull operation (see Table 7-1).

Table 7-1. Function Table

INPUT OUTPUT CTRL	OUTPUT FUNCTION
V_I = 0	Single-ended or parallel output
V_I = V_{ref}	Normal push-pull operation

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TL594 device contains an adjustable oscillator, a dead-time control comparator, a pulse-steering flip-flop, two error amplifiers, and a 5V regulator. Use the TL594 device for a wide variety of switching converter applications over a frequency range from 1Hz to 300kHz, where the oscillation frequency is set by the RT and CT values. For additional information regarding designing switching voltage regulators with the TL594, see *Designing Switching Voltage Regulators With the TL494*.

8.2 Typical Application

This design example uses the TL594 to create a 5V, 10A power supply. This application is from *Designing Switching Voltage Regulators With the TL494*.

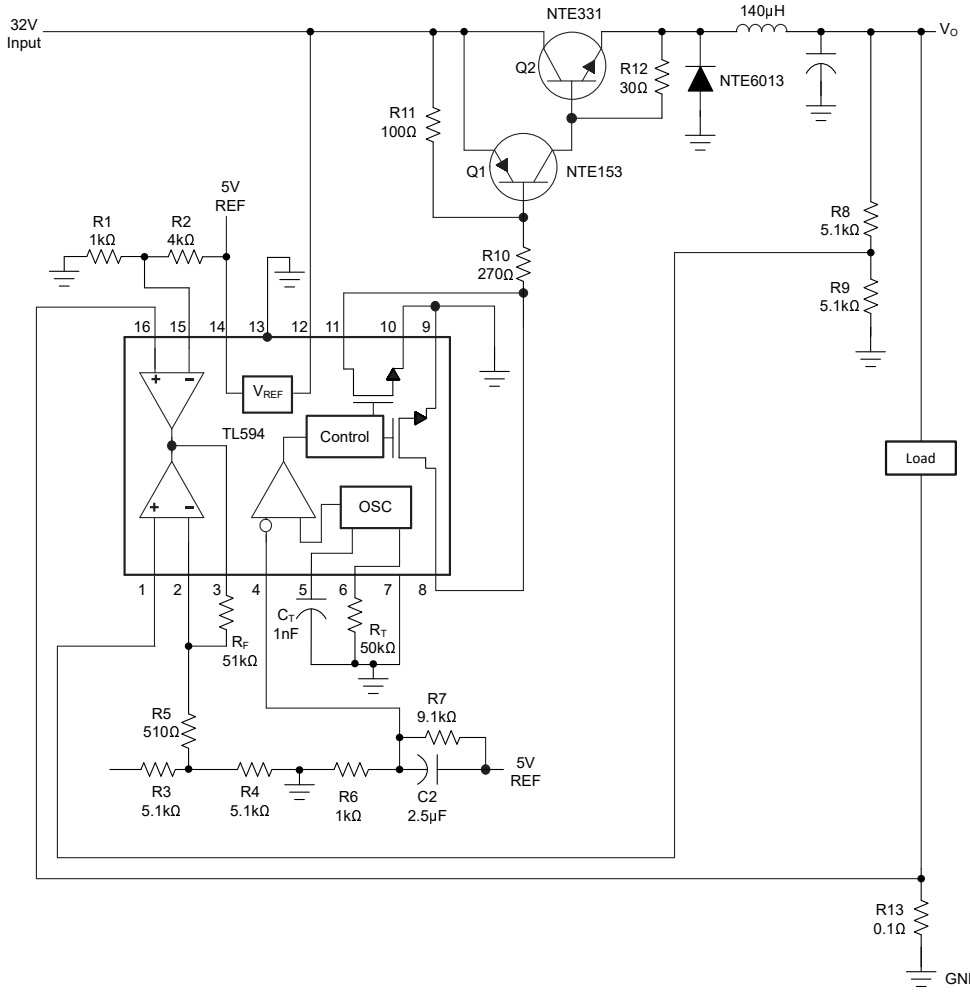


Figure 8-1. 32V to 5V, 10A Power Supply Application

8.2.1 Design Requirements

- V_I = 32V
- V_O = 5V
- I_O = 10A
- f_{OSC} = 20kHz switching frequency
- V_R = 20mV peak-to-peak (V_{RIPPLE})
- ΔI_L = 1.5A inductor current change

8.2.2 Detailed Design Procedure

8.2.2.1 Input Power Source

The 32V dc power source for this supply uses a 120V input, 24V output transformer rated at 75VA. The 24V secondary winding feeds a full-wave bridge rectifier, followed by a current-limiting resistor (0.3Ω) and two filter capacitors (see Figure 8-2).

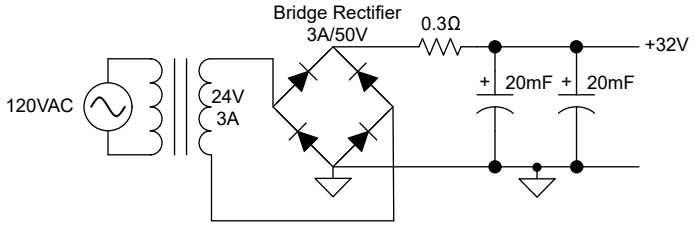


Figure 8-2. Input Power Source

Equation 7 and Equation 8 calculate the output voltage and current.

$$V_{RECTIFIER} = V_{SECONDARY} \times \sqrt{2} = 24V \times \sqrt{2} = 34V \quad (7)$$

$$I_{RECTIFIER[AVG]} \cong \frac{V_O}{V_I} \times I_O \cong \frac{5V}{32V} \times 10A = 1.6A \quad (8)$$

The 3A, 50V full-wave bridge rectifier meets these calculated conditions. Figure 8-1 shows the switching and control sections.

8.2.2.2 Control Circuits

8.2.2.2.1 Oscillator

Connecting an external capacitor and resistor to pins 5 and 6 controls the TL594 oscillator frequency. The oscillator is set to operate at 20kHz, using the component values calculated by Equation 4 and Equation 9.

Select C_T = 0.001µF and calculate R_T with Equation 9.

$$R_T = \frac{1}{f_{OSC} \times C_T} = \frac{1}{\left[20 \times 10^3\right] \times \left[0.001 \times 10^{-6}\right]} = 50k\Omega \quad (9)$$

8.2.2.2.2 Error Amplifier

The error amplifier compares a sample of the 5V output to the reference and adjusts the PWM to maintain a constant output current (see Figure 8-3).

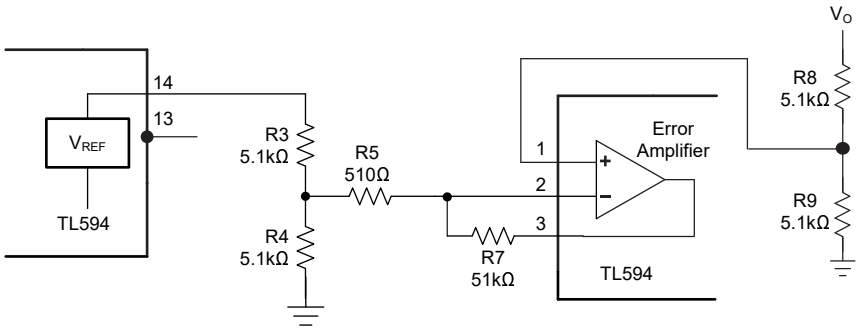


Figure 8-3. Error-Amplifier Section

The TL594 internal 5V reference is divided to 2.5 V by R3 and R4. The output-voltage error signal also is divided to 2.5 V by R8 and R9. If regulating the output to exactly 5V, use a 10kΩ potentiometer in place of R8 to provide an adjustment.

To increase the stability of the error-amplifier circuit, the output of the error amplifier is fed back to the inverting input through R_T, reducing the gain to 101.

8.2.2.2.3 Current-Limiting Amplifier

The design of the power supply is for a 10A load current and an I_L swing of 1.5 A; therefore, the calculate the short-circuit current using Equation 10.

$$I_{SC} = I_O + \frac{I_L}{2} = 10.75A \tag{10}$$

Figure 8-4 shows the current-limiting circuit.

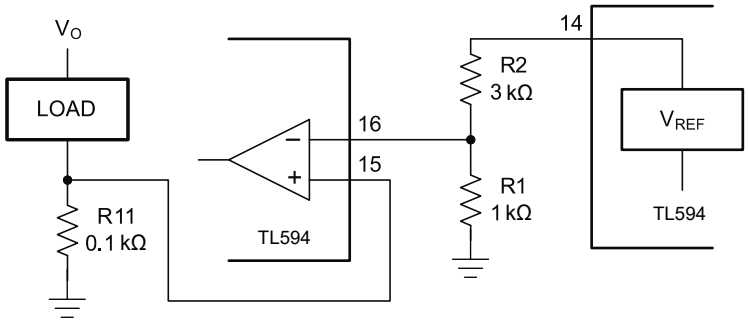


Figure 8-4. Current-Limiting Circuit

Resistors R1 and R2 set the reference of about 1 V on the inverting input of the current-limiting amplifier. Resistor R13, in series with the load, applies 1 V to the noninverting terminal of the current-limiting amplifier when the load current reaches 10 A. The output-pulse duration reduces accordingly. Calculate the value of R13 as Equation 11.

$$R13 = \frac{1V}{10A} = 0.1\Omega \tag{11}$$

8.2.2.2.4 Soft Start

To reduce stress on the switching transistors at start-up, reduce the start-up surge that occurs as the output filter capacitor charges. The availability of the dead-time control makes implementation of a soft-start circuit relatively simple (see Figure 8-5).

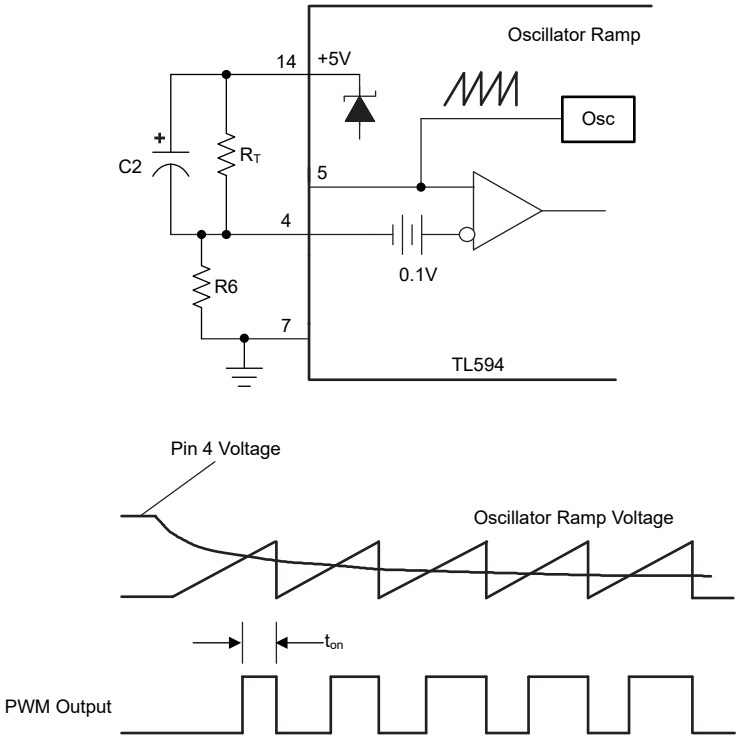


Figure 8-5. Soft-Start Circuit

The soft-start circuit allows the pulse duration at the output to increase slowly (see Figure 8-5) by applying a negative slope waveform to the dead-time control input (pin 4).

Initially, capacitor C2 forces the dead-time control input to follow the 5V regulator, which disables the outputs (100% dead time). As the capacitor charges through R6, the output pulse duration slowly increases until the control loop takes command. With a resistor ratio of 1:10 for R6 and R7, the voltage at pin 4 after start-up is 0.1 × 5 V, or 0.5 V.

The soft-start time generally is in the range from 25 to 100 clock cycles. If selecting 50 clock cycles at a 20kHz switching rate, calculate the soft-start time as Equation 12.

$$t = \frac{1}{f} = \frac{1}{20\text{kHz}} = 50\mu\text{s per clock cycle} \tag{12}$$

Calculate the value of the capacitor with Equation 13.

$$C2 = \frac{\text{soft} - \text{start time}}{R6} = \frac{50\mu\text{s} \times 50 \text{ cycles}}{1\text{k}\Omega} = 2.5\mu\text{F} \tag{13}$$

This helps eliminate any false signals that the control circuit creates as power is applied.

8.2.2.2.5 Setting the Dead Time

The primary function of the dead-time control is to control the minimum off time of the output of the TL594 device. The dead-time control input provides control from 5% to 100% dead time. Tailor the TL594 device to specific power transistor switches, to establish that the output transistors never experience a common on-time. Figure 8-6 shows the bias circuit for the basic function.

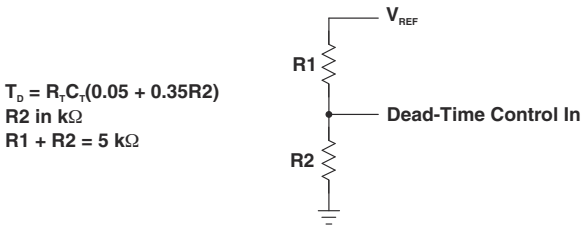


Figure 8-6. Setting Dead Time

8.2.2.3 Inductor Calculations

Figure 8-7 shows the switching circuit used.

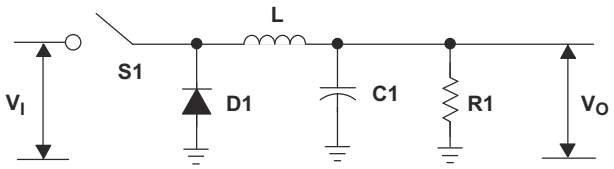


Figure 8-7. Switching Circuit

The size of the inductor (L) required is:

$$d = \text{duty cycle} = \frac{V_O}{V_I} = \frac{5V}{32V} = 0.156 \tag{14}$$

$$f = 20\text{kHz (design objective)} \tag{15}$$

$$t_{ON} = \text{time on (S1 closed)} = \left(\frac{1}{f}\right) \times d = 7.8\mu s \tag{16}$$

$$t_{OFF} = \text{time off (S1 open)} = \left(\frac{1}{f}\right) - \text{ton} = 42.2\mu s \tag{17}$$

$$\begin{aligned} L &\approx (V_I - V_O) \times \frac{t_{ON}}{\Delta I_L} \\ &\approx \frac{[(32V - 5V) \times 7.8\mu s]}{1.5A} \\ &\approx 140.4\mu H \end{aligned} \tag{18}$$

8.2.2.4 Output Capacitance Calculations

Once the filter inductor is calculated, calculate the value of the output filter capacitor to meet the output ripple requirements. Model an electrolytic capacitor as a series connection of an inductance, a resistance, and a capacitance. To provide good filtering, the ripple frequency must be far below the frequencies at which the series inductance becomes important. So, the two components of interest are the capacitance and the effective series resistance (ESR). Calculate the maximum ESR with Equation 19, according to the relation between the specified peak-to-peak ripple voltage and the peak-to-peak ripple current.

$$ESR[\max] = \frac{\Delta V_{O[ripple]}}{\Delta I_L} = \frac{V}{1.5A} \cong 0.067\Omega \tag{19}$$

Calculate the minimum capacitance of C3 necessary to maintain the V_O ripple voltage at less than the 100mV design objective according to Equation 20.

$$C3 = \frac{\Delta I_L}{8f\Delta V_O} = \frac{1.5A}{8 \times 20 \times 10^3 \times 0.1V} = 94\mu F \tag{20}$$

A 220mF, 60V capacitor is selected because it has a maximum ESR of 0.074 Ω and a maximum ripple current of 2.8A.

8.2.2.5 Transistor Power-Switch Calculations

The constructions of the transistor power switch is with an NTE153 pnp drive transistor and an NTE331 npn output transistor. These two power devices connect in a pnp hybrid Darlington circuit configuration (see Figure 8-8).

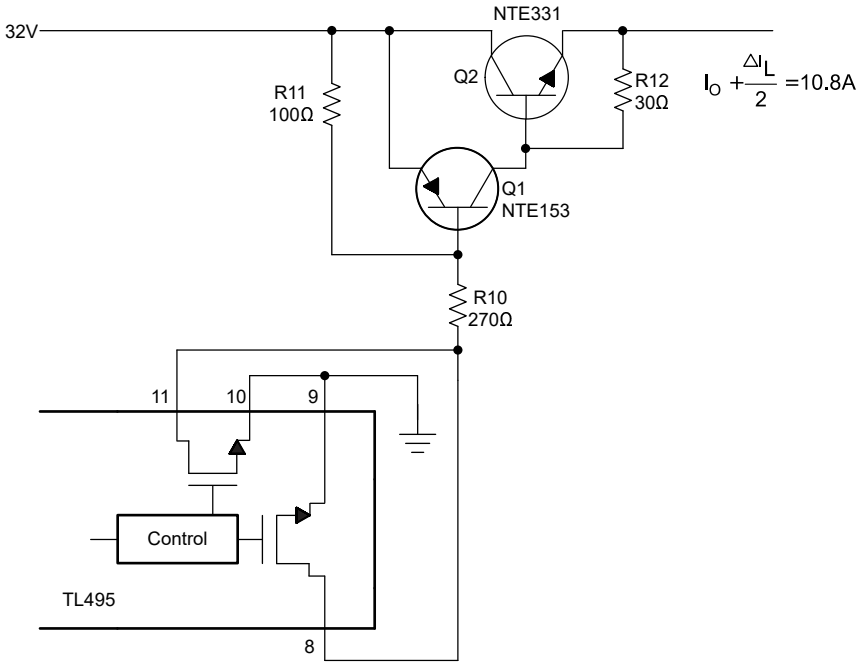


Figure 8-8. Power-Switch Section

Saturate the hybrid Darlington circuit at a maximum output current of I_O + ΔI_L/2, or 10.8 A. The Darlington h_{FE} at 10.8A must be high enough not to exceed the 250mA maximum output collector current of the TL594. Based on published NTE153 and NTE331 specifications, calculate the required power-switch minimum drive using Equation 21 through Equation 23, resulting in 144mA.

$$h_{FE}[Q1] \text{ at } I_C \text{ of } 3A = 15 \tag{21}$$

$$h_{FE}[Q2] \text{ at } I_C \text{ of } 10.0A = 5 \tag{22}$$

$$i_B \geq \frac{I_O + \frac{I_L}{2}}{h_{FE}[Q2] \times h_{FE}[Q1]} \geq 144mA \tag{23}$$

Use Equation 24 to calculate the value of R10.

$$R10 \leq \frac{V_I - [V_{BE}(Q1) + V_{CE}(TL494)]}{i_B} = \frac{32 - [1.5 + 0.7]}{0.144}$$
$$R10 \leq 207\Omega \tag{24}$$

Based on these calculations, the nearest standard resistor value of 220Ω is selected for R10. Resistors R11 and R12 permit the discharge of carriers in switching transistors when the resistors turn off.

The power supply described demonstrates the flexibility of the TL594 PWM control circuit. This power-supply design demonstrates many of the power-supply control methods the TL594 provides, as well as the versatility of the control circuit.

8.2.3 Application Curve

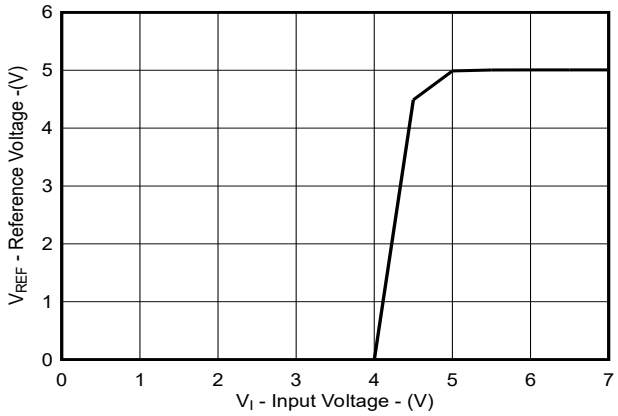


Figure 8-9. Reference Voltage vs Input Voltage

8.3 Power Supply Recommendations

The design of the TL594 is to operate from an input voltage supply range from 7V to 40V. This input supply must be well regulated. If the input supply is placed more than a few inches from the device, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. A tantalum capacitor with a value of 47µF is a typical choice; however this can vary depending upon the delivery of the output power.

8.4 Layout

8.4.1 Layout Guidelines

Always try to use a low EMI inductor with a ferrite type closed core. Some examples would be toroid and encased E core inductors. Use open cores if the open cores have low EMI characteristics and are placed a bit more away from the low-power traces and components. Make the poles perpendicular to the PCB as well if using an open core. Stick cores usually emit the most unwanted noise.

8.4.1.1 Feedback Traces

Try to run the feedback trace as far from the inductor and noisy power traces as possible. The feedback trace must be as direct as possible and wider to decrease impedance. These two sometimes involve a trade-off, but keeping it away from inductor EMI and other noise sources is the more critical of the two. Run the feedback trace on the side of the PCB opposite of the inductor, ideally with a ground plane separating the two.

8.4.1.2 Input or Output Capacitors

When using a low value ceramic input filter capacitor, place the capacitor as close to the VCC pin of the IC as possible. This eliminates as much trace inductance effects as possible and give the internal IC rail a cleaner voltage supply. Some designs require the use of a feed-forward capacitor connected from the output to the feedback pin as well, usually for stability reasons. In this case, position it as close to the IC as possible. Using surface-mount capacitors also reduces lead length and reduces the chance of noise coupling into the effective antenna created by through-hole components.

8.4.1.3 Compensation Components

Place external compensation components for stability close to the IC. Surface-mount components are recommended here as well for the same reasons discussed for the filter capacitors. Do not place surface-mount components very close to the inductor.

8.4.1.4 Traces and Ground Planes

Make all of the power (high current) traces as short and direct as possible, while trying to maximize trace width for the appropriate current carrying capability. It is good practice on a standard PCB board to make the traces an absolute minimum of 15mils (0.381mm) per ampere. The inductor, output capacitors, and output diode must be

as close to each other possible. This helps reduce the EMI the power traces radiate due to the high switching currents through the power traces. This also reduces lead inductance and resistance as well, which in turn reduces noise spikes, ringing, and resistive losses that produce voltage errors.

Closely connect together the grounds of the IC, input capacitors, output capacitors, and output diode (if applicable) directly to a ground plane. Have a ground plane on both sides of the PCB. This reduces noise as well by reducing ground loop errors as well as by absorbing more of the EMI the inductor radiates. For multi-layer boards with more than two layers, use a ground plane to separate the power plane (where the power traces and components are) and the signal plane (where the feedback and compensation and components are) for improved performance.

On multi-layer boards, using vias is required to connect traces and different planes. It is good practice to use one standard via per 200mA of current if the trace requires conduct to a significant amount of current from one plane to the other. Arrange the components so that the switching current loops curl in the same direction. Due to the way switching regulators operate, there are two power states. One state when the switch is on and one when the switch is off. During each state there is a current loop the power components make that are currently conducting. Place the power components so that during each of the two states the current loop is conducting in the same direction. This prevents magnetic field reversal the traces between the two half-cycles and reduces radiated EMI causes

8.4.2 Layout Example

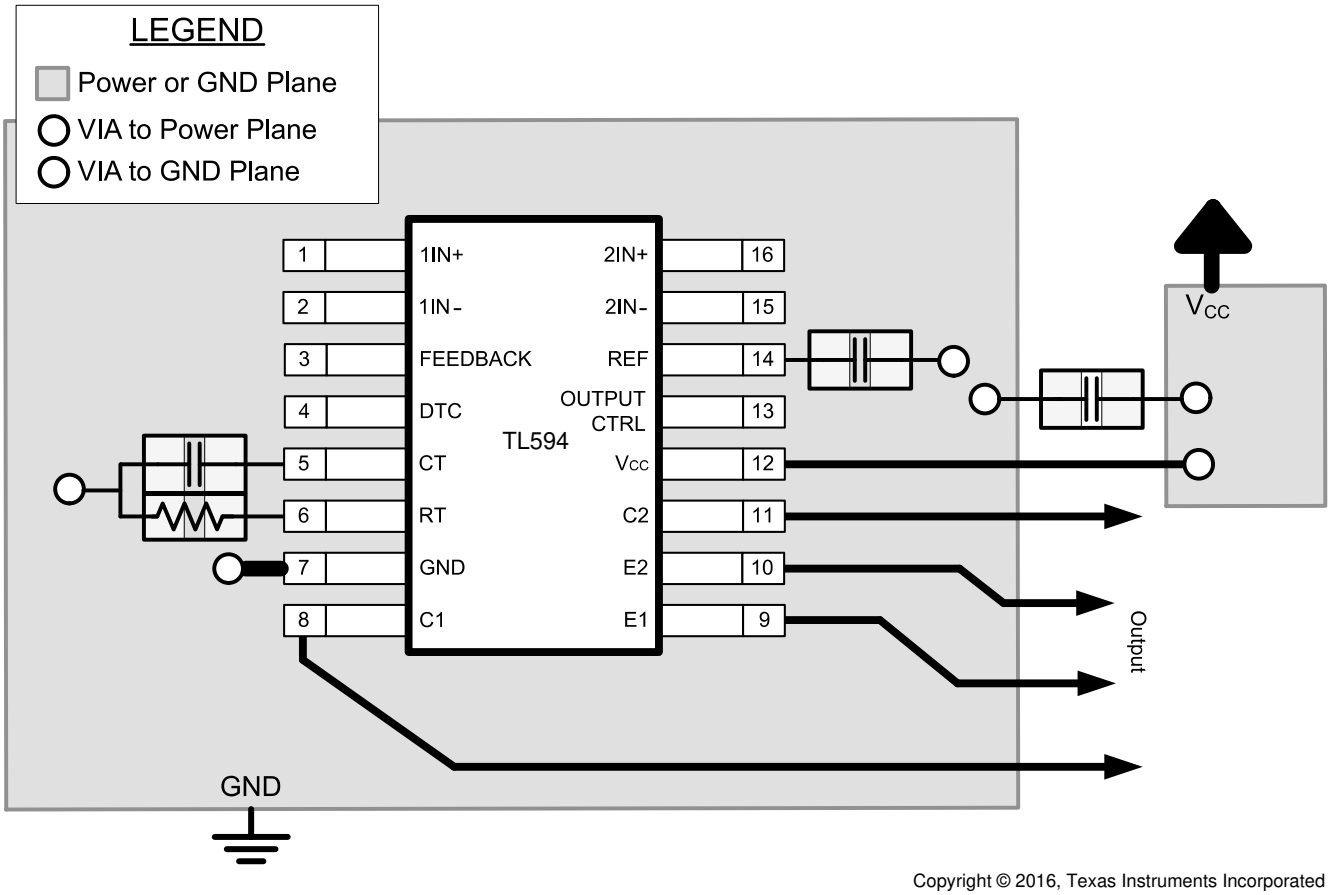


Figure 8-10. TL594 Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

Designing Switching Voltage Regulators With the TL494 (SLVA001)

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (September 2016) to Revision J (September 2026)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated output transistor description and symbols from BJT to MOSFET throughout the document	1
• Removed PDIP (16) package	1
• Updated values in the *Thermal Information* table for all packages	4
• Changed output regulation typical value from 14mV to 6mV	5
• Changed open-loop voltage amplification typical value from 95dB to 80dB	5
• Changed common-mode rejection ratio typical value from 80dB to 100dB	5
• Changed input bias current (DEAD-TIME CTRL) typical value from -2µA to -0.006µA	5
• Changed input threshold voltage (DEAD-TIME CTRL) typical value from 3V to 2.5V	5
• Changed output C1, C2 off-state current typical value from 2µA to 4µA, and 4µA to 2µA for other test condition	5
• Changed output C1E1, C2E2 saturation voltage in common source configuration typical value from 1.1V to 0.5V	5
• Changed output C1E1, C2E2 saturation voltage in source follower configuration typical value from 1.5V to 1.65V	5
• Changed input threshold voltage (FEEDBACK) typical value from 4V to 3.4V	5

- Changed standby supply current for VCC = 15V typical value from 9mA to 1.62mA....5
- Changed standby supply current for VCC = 40V typical value from 11mA to 1.68mA....5
- Changed average supply current typical value from 12.4mA to 2.2mA....5
- Changed rise time in common source configuration typical value from 100ns to 70ns....6
- Changed fall time in common source configuration typical value from 30ns to 20ns....6
- Changed rise time in source follower configuration typical value from 200ns to 85ns....6
- Changed fall time in source follower configuration typical value from 45ns to 35ns....6
- Updated Figure 5-1 and Amplifier Voltage Amplification vs Frequency....6
- Updated description to align VREF behavior changes for input voltages less than 7V....9
- Updated the formatting for inductor calculations....16
- Updated reference voltage vs input voltage application curve....18

Changes from Revision H (January 2014) to Revision I (September 2016) **Page**

- Added *Applications* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section....1
- Changed values in the *Thermal Information* table from 73 to 73.5 (D), from 67 to 43.5 (N), from 64 to 73.6 (NS), and from 108 to 101.5 (PW)....4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL594CD	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	TL594C
TL594CDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	TL594C
TL594CDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL594C
TL594CDRG4	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	0 to 70	TL594C
TL594CN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL594CN
TL594CN.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL594CN
TL594CNE4	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TL594CN
TL594CNSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL594
TL594CNSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL594
TL594CPW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	0 to 70	T594
TL594CPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T594
TL594CPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T594
TL594CPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	T594
TL594ID	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	TL594I
TL594IDR	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL594I
TL594IDR.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL594I
TL594IDRG4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL594I
TL594IN	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL594IN
TL594IN.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL594IN
TL594INSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL594I
TL594INSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL594I
TL594INSRG4	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL594I
TL594IPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z594
TL594IPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z594
TL594IPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z594

(1) **Status:** For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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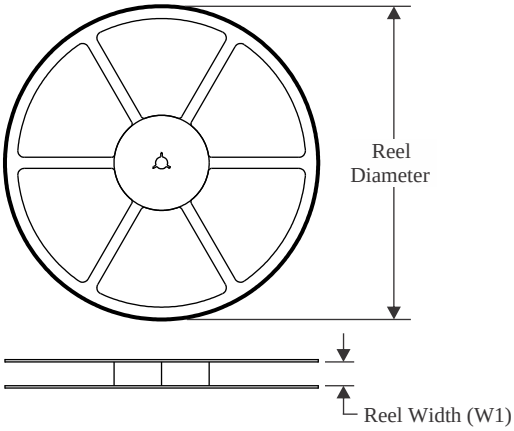
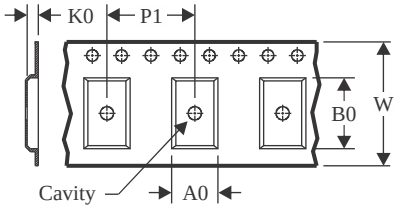
TAPE AND REEL INFORMATION

REEL DIMENSIONS

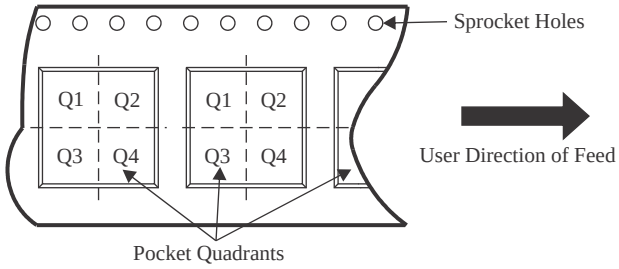


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

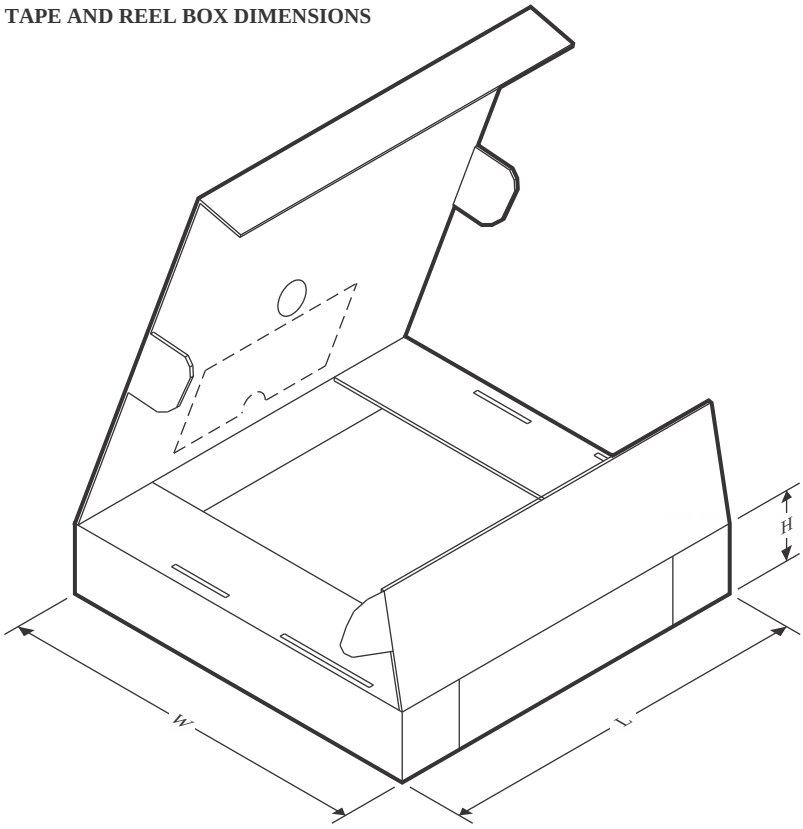
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL594CDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TL594CNSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
TL594CPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL594IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TL594INSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
TL594IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

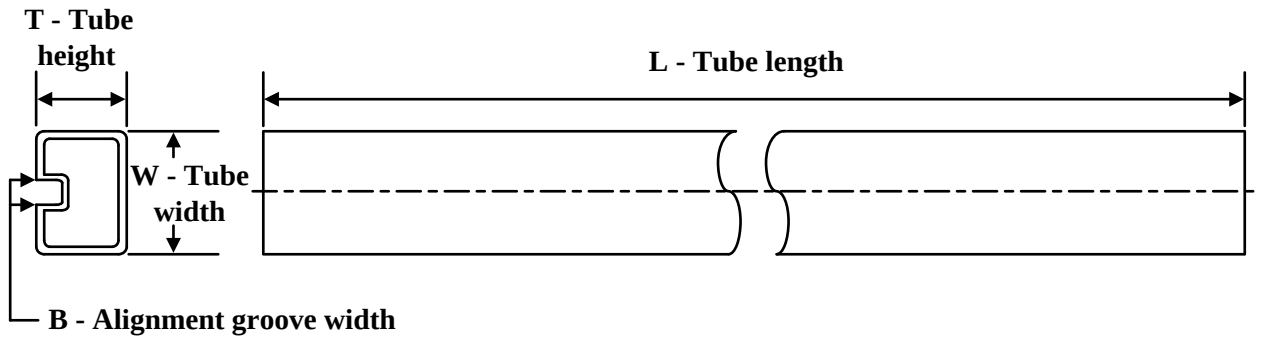
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

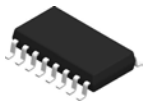
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL594CDR	SOIC	D	16	2500	353.0	353.0	32.0
TL594CNSR	SOP	NS	16	2000	353.0	353.0	32.0
TL594CPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TL594IDR	SOIC	D	16	2500	353.0	353.0	32.0
TL594INSR	SOP	NS	16	2000	353.0	353.0	32.0
TL594IPWR	TSSOP	PW	16	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL594CN	N	PDIP	16	25	506	13.97	11230	4.32
TL594CN	N	PDIP	16	25	506	13.97	11230	4.32
TL594CN.A	N	PDIP	16	25	506	13.97	11230	4.32
TL594CN.A	N	PDIP	16	25	506	13.97	11230	4.32
TL594CNE4	N	PDIP	16	25	506	13.97	11230	4.32
TL594CNE4	N	PDIP	16	25	506	13.97	11230	4.32
TL594IN	N	PDIP	16	25	506	13.97	11230	4.32
TL594IN.A	N	PDIP	16	25	506	13.97	11230	4.32

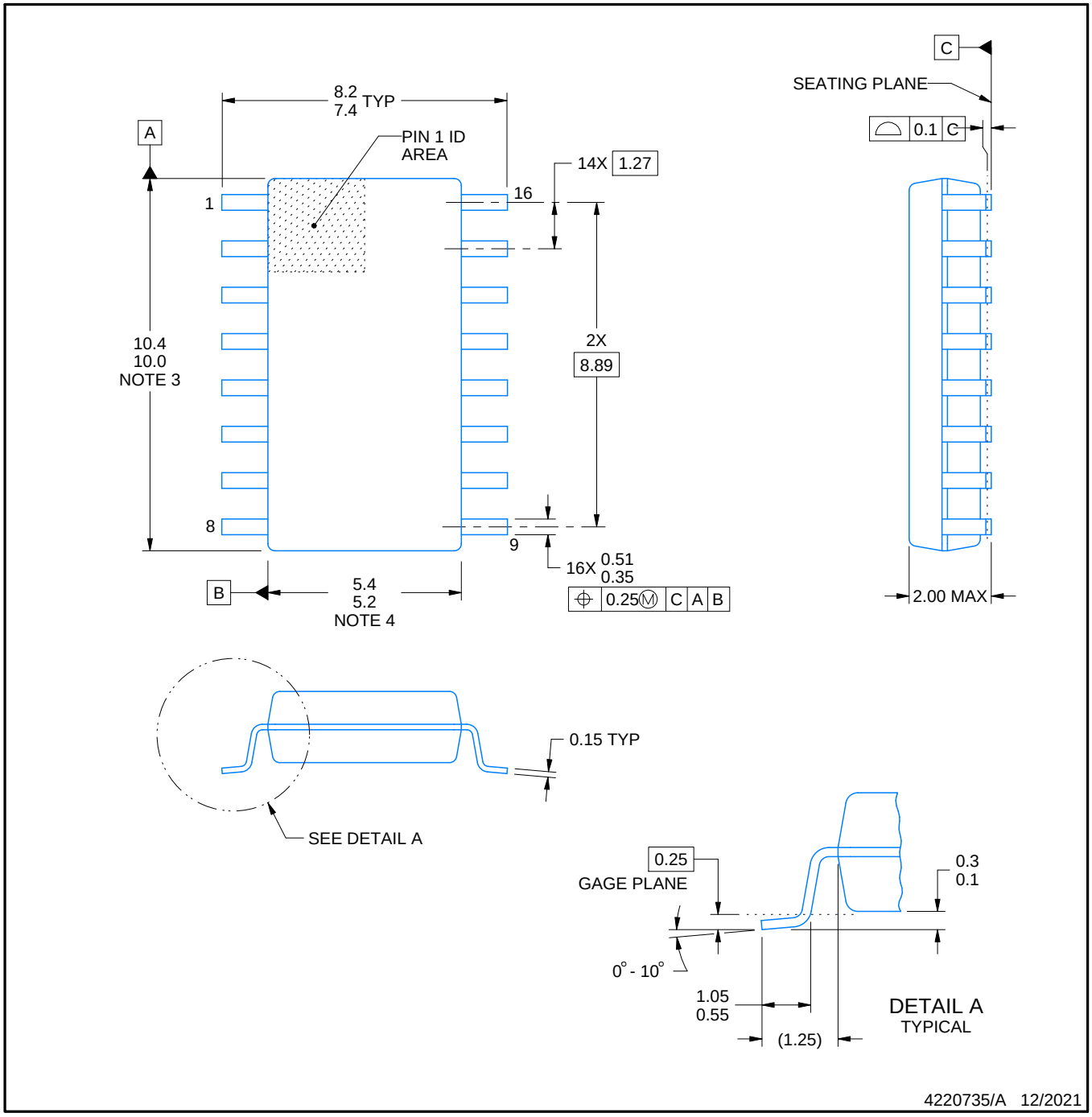


PACKAGE OUTLINE

NS0016A

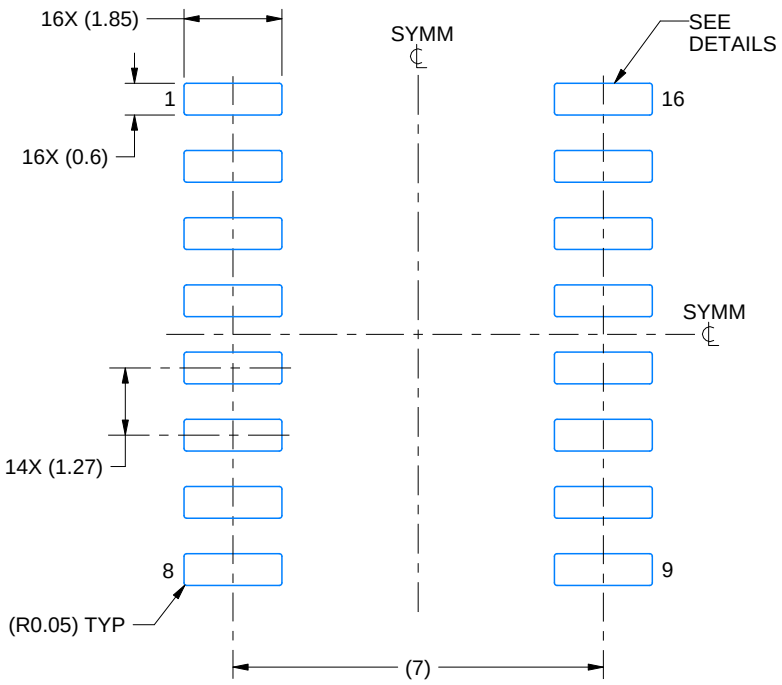
SOP - 2.00 mm max height

SOP

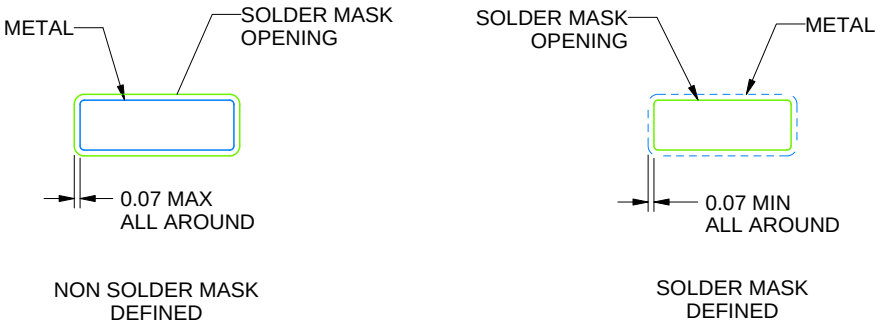


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

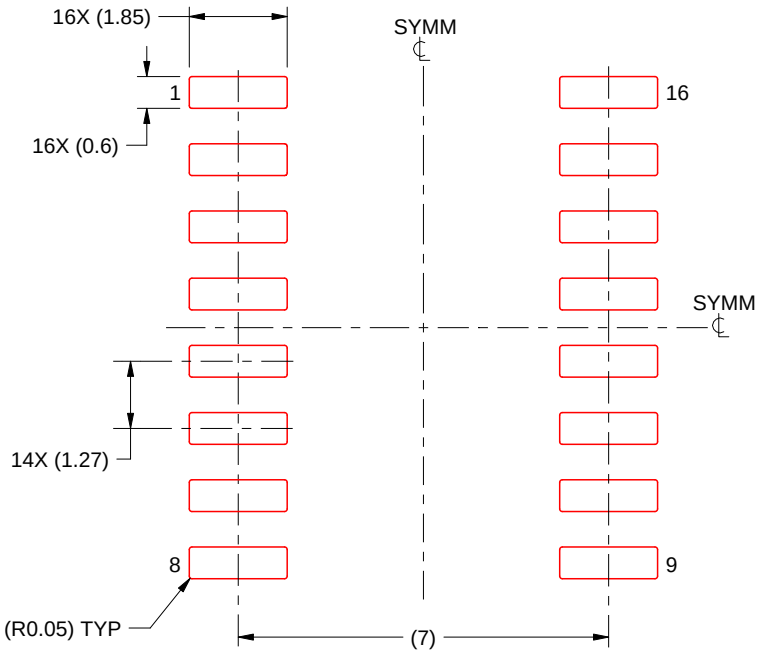
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



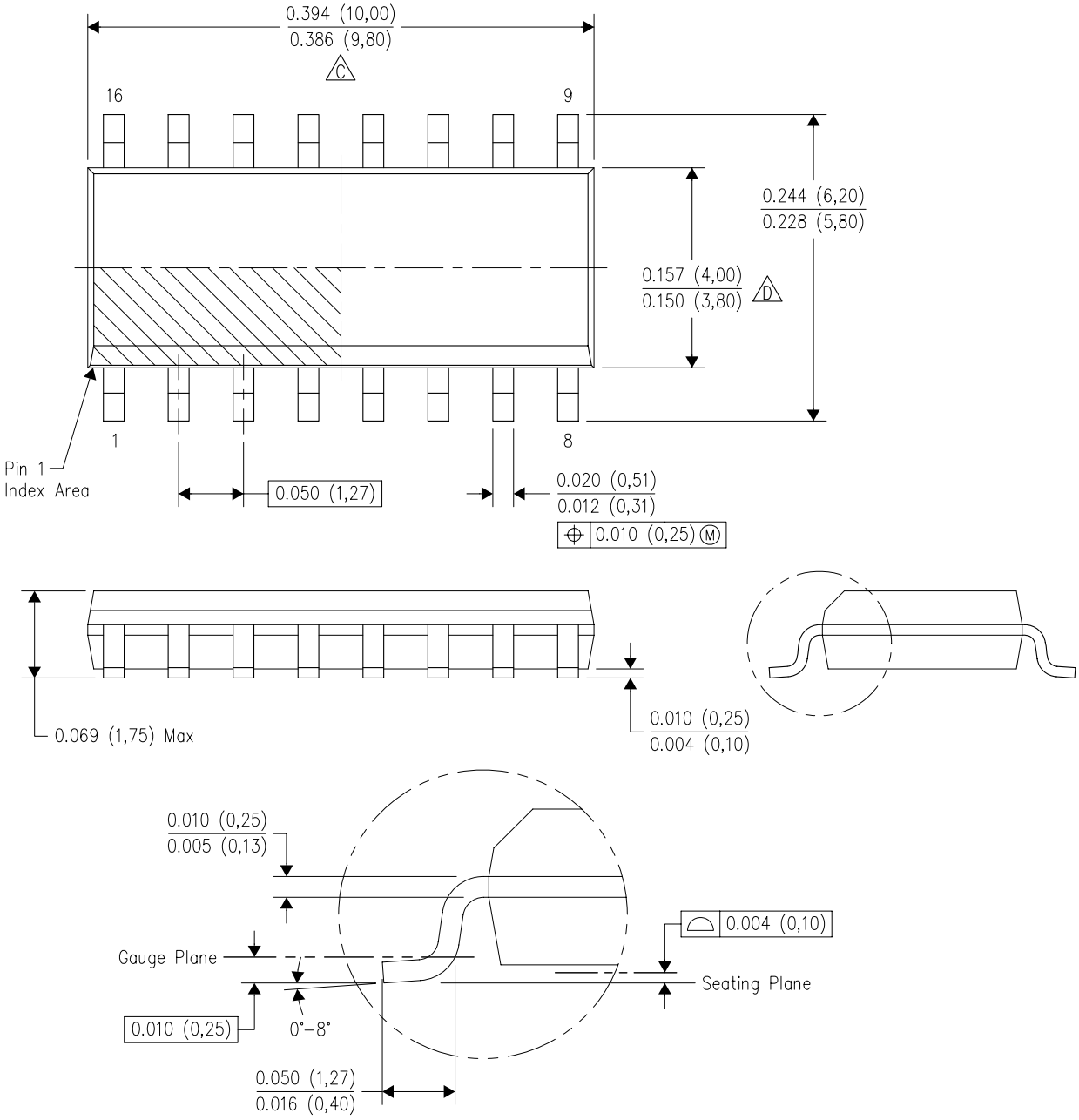
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



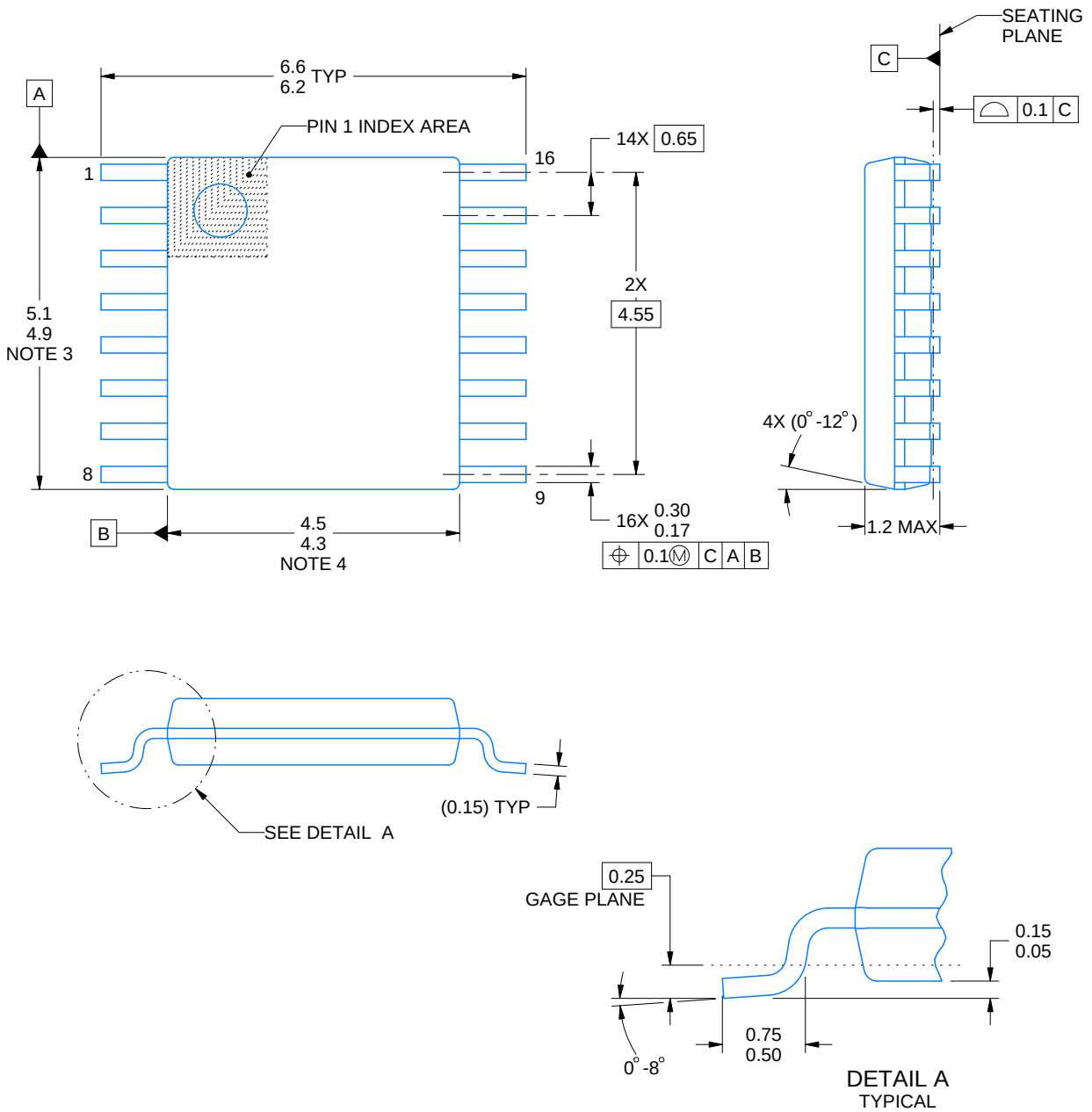
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

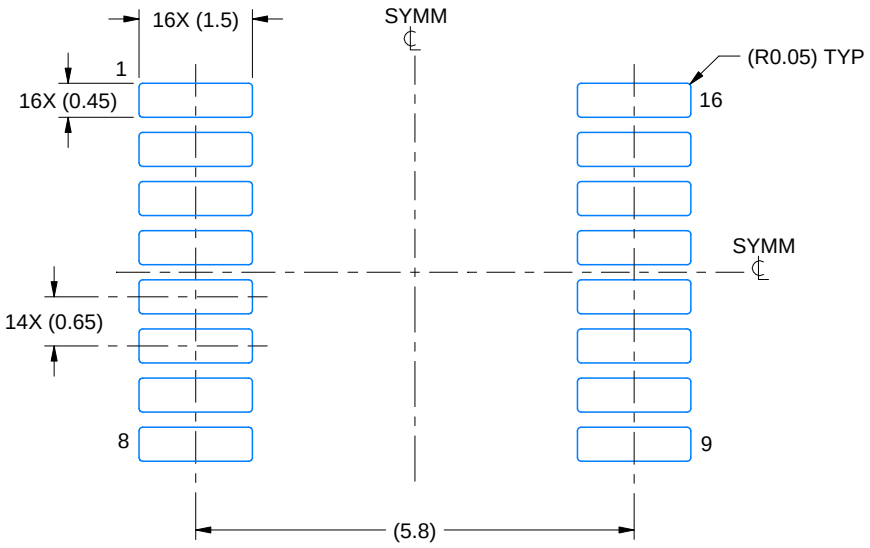
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



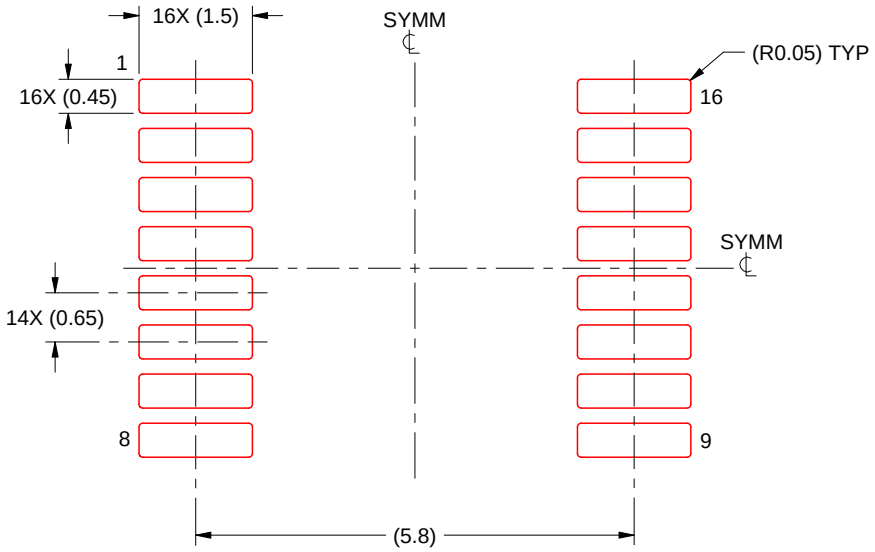
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

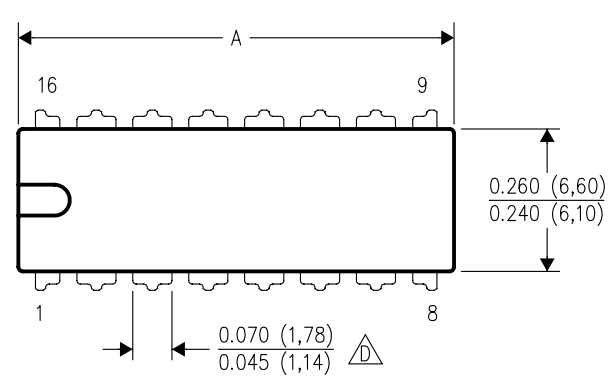
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

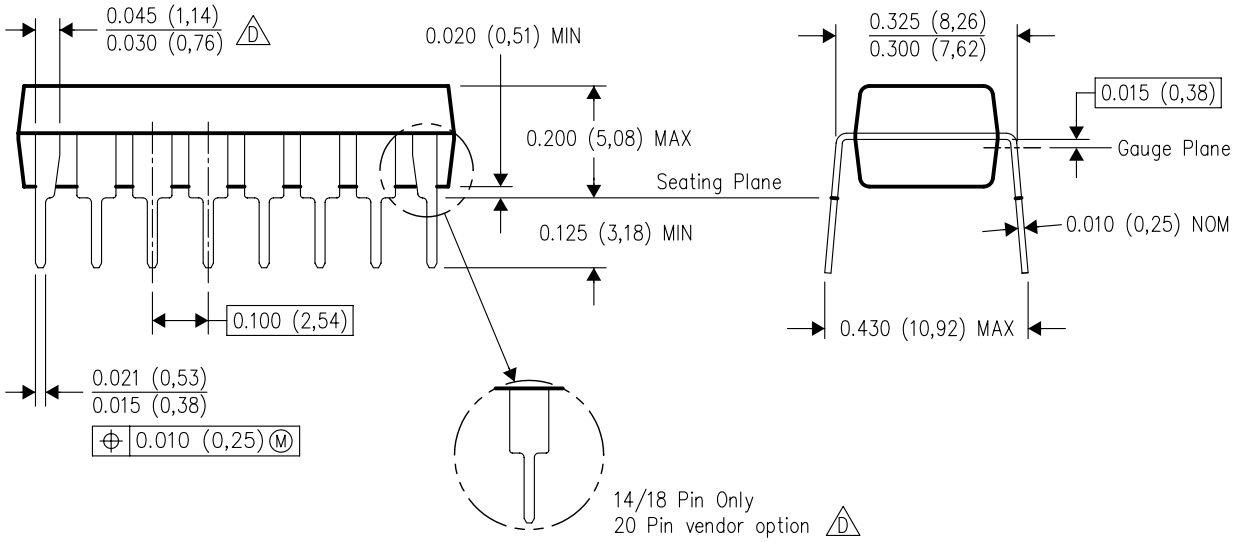
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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