TL7700 Supply-Voltage Supervisor

1 Features

- Adjustable Sense Voltage With Two External Resistors
- 1.0% Sense Voltage Tolerance (25°C)
- Adjustable Hysteresis of Sense Voltage
- Wide Operating Supply-Voltage Range: 1.8 V to 40 V
- Wide Operating Temperature Range: –40°C to 85°C
- Low Power Consumption: I_{CC} = 0.6 mA Typical, V_{CC} = 40 V

2 Applications

- Digital Signal Processors (DSPs)
- Microcontrollers (MCUs)
- FPGAs, ASICs
- Notebooks, Desktop Computers
- Set-Top Boxes
- Industrial Control Systems

3 Description

The TL7700 is a bipolar integrated circuit designed for use as a reset controller in microcomputer and microprocessor systems. The SENSE voltage can be set to any value greater than 0.5 V using two external resistors.

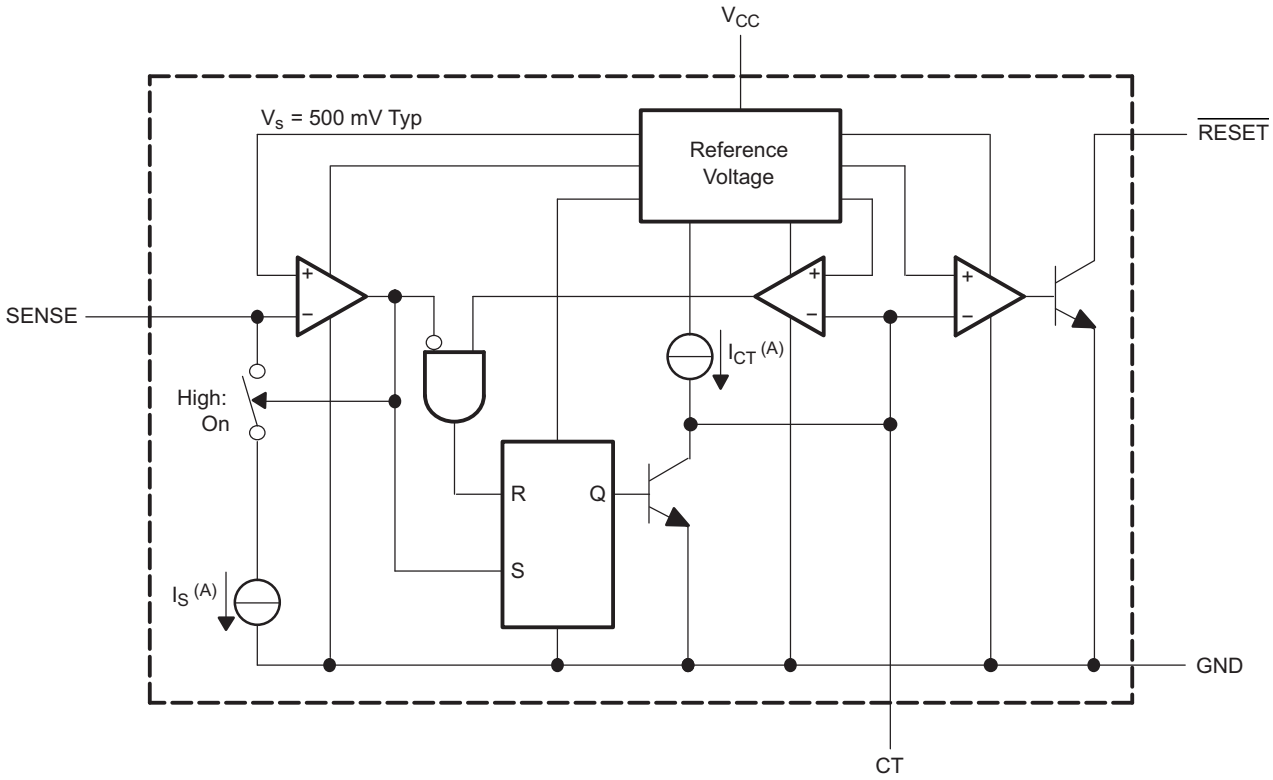
Circuit function is very stable, with supply voltage in the 1.8-V to 40-V range. Minimum supply current allows use with ac line operation, portable battery operation, and automotive applications. The TL7700 device is designed for operation from –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL7700DGK	VSSOP (8)	3.00 mm × 3.00 mm
TL7700P	PDIP (8)	9.81 mm × 6.35 mm
TL7700PS	SO (8)	6.20 mm × 5.30 mm
TL7700PW	TSSOP (8)	3.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (August 2011) to Revision G **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table, see POA at the end of the data sheet ... 1
- Changed values in the *Thermal Information* table to align with JEDEC standards ... 4

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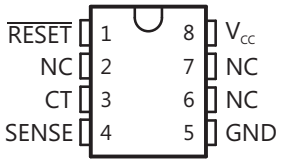
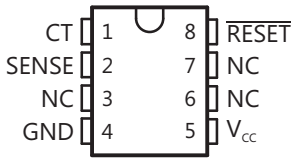
5 Pin Configuration and Functions

DGK Package
8-Pin VSSOP
Top View



P, PS, or PW Package
8-Pin PDIP, SO, TSSOP
Top View



NC – No internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	PDIP, SO, TSSOP	VSSOP		
CT	1	3	I/O	Timing capacitor connection. This terminal sets the RESET output pulse duration (t_{po}). It is connected internally to a 15-µA constant-current source. There is a limit on the switching speed of internal elements; even if CT is set to 0, response speeds remain at approximately 5 to 10 µs. If CT is open, the device can be used as an adjustable-threshold noninverting comparator. If CT is low, the internal output-stage comparator is active, and the $\overline{\text{RESET}}$ output transistor is on. An external voltage must not be applied to this terminal due to the internal structure of the device. Therefore, drive the device using an open-collector transistor, FET, or 3-state buffer (in the low-level or high-impedance state).
GND	4	5	—	Ground Keep this terminal as low impedance as possible to reduce circuit noise.
NC	3, 6, 7	2, 6, 7	—	No internal connection
$\overline{\text{RESET}}$	8	1	O	Reset output This terminal can be connected directly to a system that resets in the active-low state. A pullup resistor usually is required because the output is an npn open-collector transistor. An additional transistor should be connected when the active-high reset or higher output current is required.
SENSE	2	4	I	Voltage sense This terminal has a threshold level of 500 mV. The sense voltage and hysteresis can be set at the same time when the two voltage-dividing resistors are connected. The reference voltage is temperature compensated to inhibit temperature drift in the threshold voltage within the operating temperature range.
V_{CC}	5	8	—	Power supply This terminal is used in an operating-voltage range of 1.8 V to 40 V.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		41	V
V_s	Sense input voltage	–0.3	41	V
V_{OH}	Output voltage (off state)		41	V
I_{OL}	Output current (on state)		5	mA
T_J	Operating virtual-junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	1.8	40	V
I_{OL}	Low-level output current		3	mA
T_A	Operating free-air temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TL7700				UNIT
		DGK (VSSOP)	P (PDIP)	PS (SO)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	173.8	57.6	112.5	172.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.1	47.4	64.2	56.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	93.9	34.7	61.6	101.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.5	25	25.1	5.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	92.5	34.6	60.7	99.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

V_{CC} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_S	SENSE input voltage		25°C	495	500	505	mV
			–40°C to 85°C	490		510	
I_S	SENSE input current	V_S = 0.4 V	25°C	2	2.5	3	µA
			–40°C to 85°C	1.5		3.5	
I_{CC}	Supply current	V_{CC} = 40 V, V_S = 0.6 V, No load	25°C		0.6	1	mA
V_{OL}	Low-level output voltage	I_{OL} = 1.5 mA	25°C			0.4	V
		I_{OL} = 3 mA	25°C			0.8	
I_{OH}	High-level output current	V_{OH} = 40 V, V_S = 0.6 V	–40°C to 85°C			1	µA
I_{CT}	Timing-capacitor charge current	V_S = 0.6 V	25°C	11	15	19	µA

6.6 Switching Characteristics

V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pi}	SENSE pulse duration	C_T = 0.01 µF (See Figure 17)	2			µs
t_{po}	Output pulse duration	C_T = 0.01 µF (See Figure 17)	0.5	1	1.5	ms
t_r	Output rise time	C_T = 0.01 µF, R_L = 2.2 kΩ, C_L = 100 pF (See Figure 17)			15	µs
t_f	Output fall time	C_T = 0.01 µF, R_L = 2.2 kΩ, C_L = 100 pF (See Figure 17)			0.5	µs
t_{pd}	Propagation delay time, SENSE to output	C_T = 0.01 µF (See Figure 17)			10	µs

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6.7 Typical Characteristics

Data at high and low temperatures are applicable only within the recommended operating conditions.

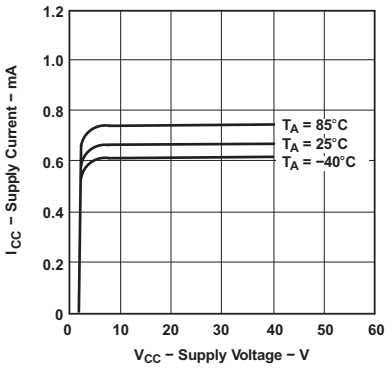

Figure 1. Supply Current vs Supply Voltage

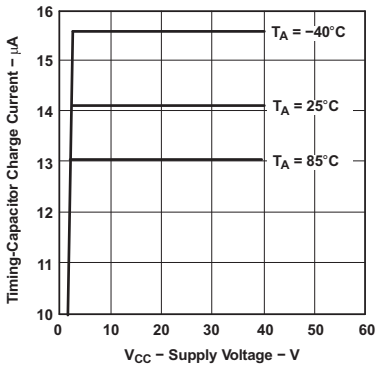

Figure 2. Timing Capacitor Charge Current vs Supply Voltage

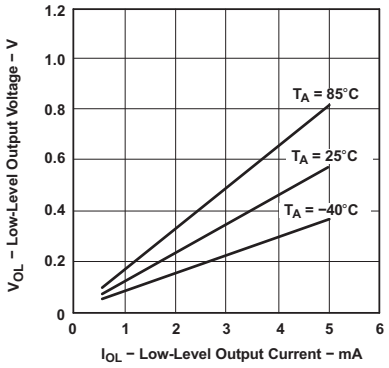

Figure 3. V_{OL} vs I_{OL}

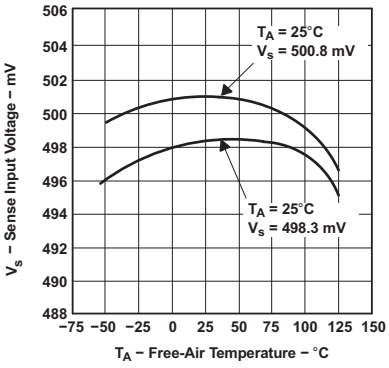

Figure 4. Sense Input Voltage vs Temperature

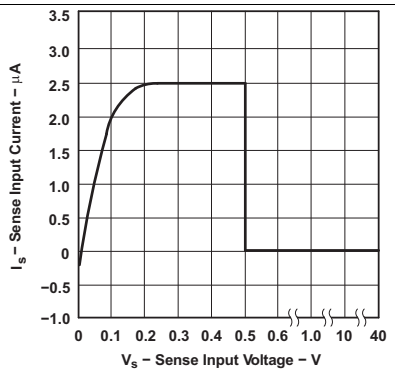

Figure 5. Sense Input Current vs Sense Input Voltage

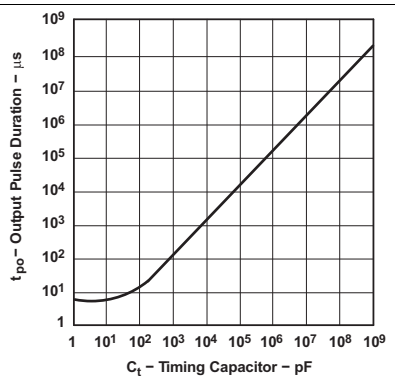

Figure 6. Output Pulse Duration vs Timing Capacitor

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Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the recommended operating conditions.

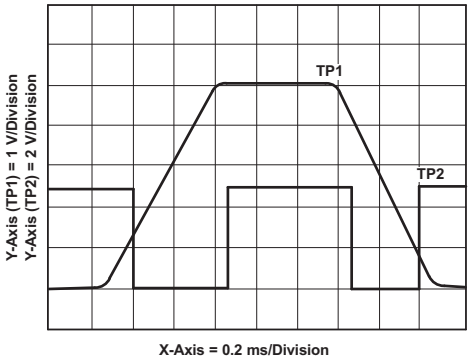

Figure 7. V_{CC} vs Output Waveform 1 - See Figure 8

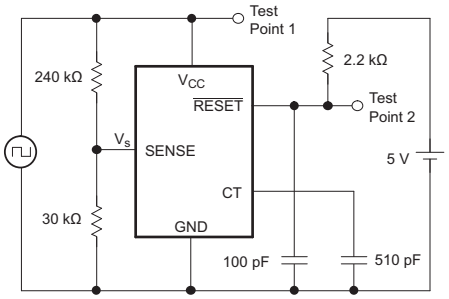

Figure 8. V_{CC} vs Output Test Circuit 1

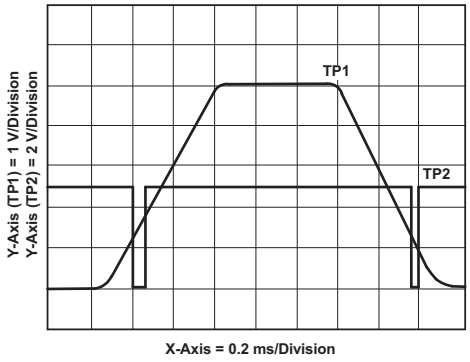

Figure 9. V_{CC} vs Output Waveform 2 - See Figure 10

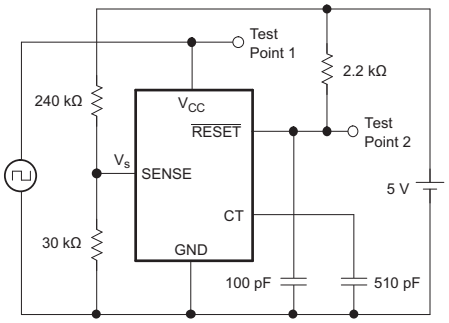

Figure 10. V_{CC} vs Output Test Circuit 2

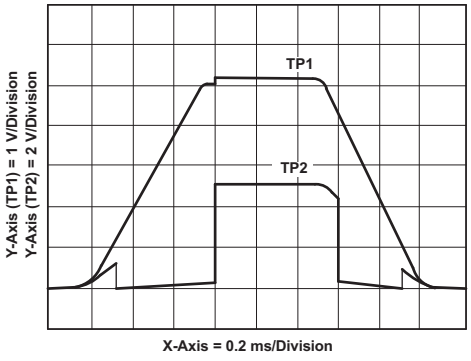

Figure 11. V_{CC} vs Output Waveform 3 - See Figure 12

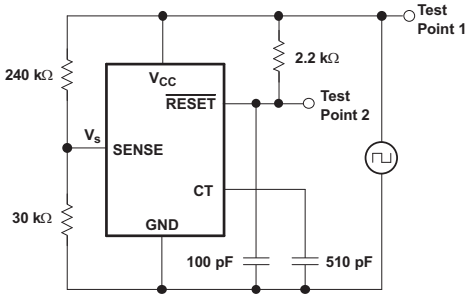

Figure 12. V_{CC} vs Output Test Circuit 3

7 Parameter Measurement Information

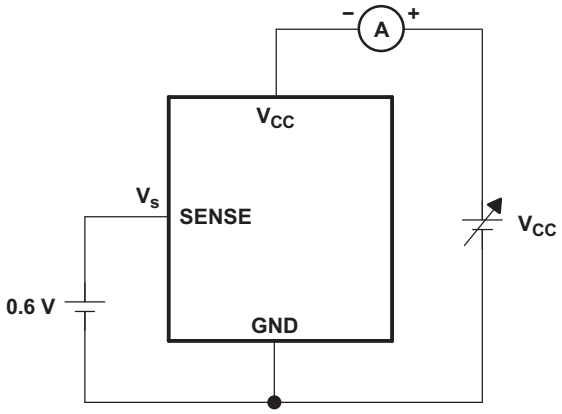

Figure 13. V_{CC} vs I_{CC} Measurement Circuit

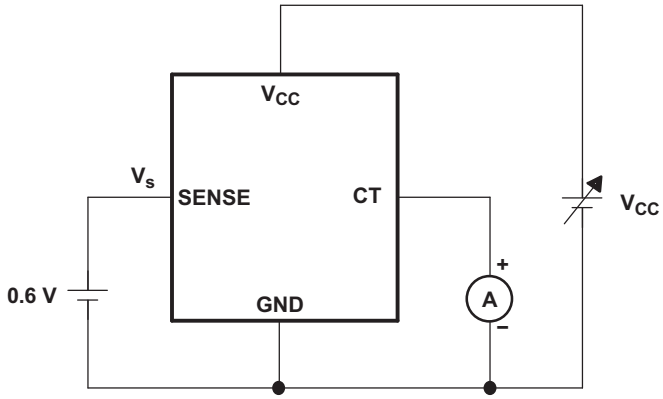

Figure 14. V_{CC} vs I_{CT} Measurement Circuit

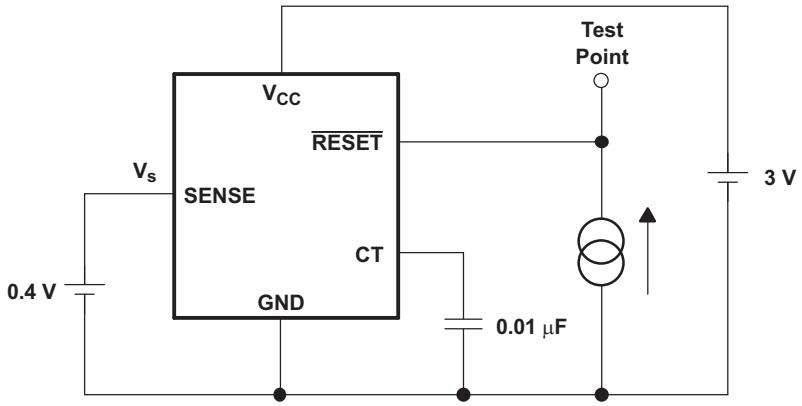

Figure 15. I_{OL} vs V_{OL} Measurement Circuit

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Parameter Measurement Information (continued)

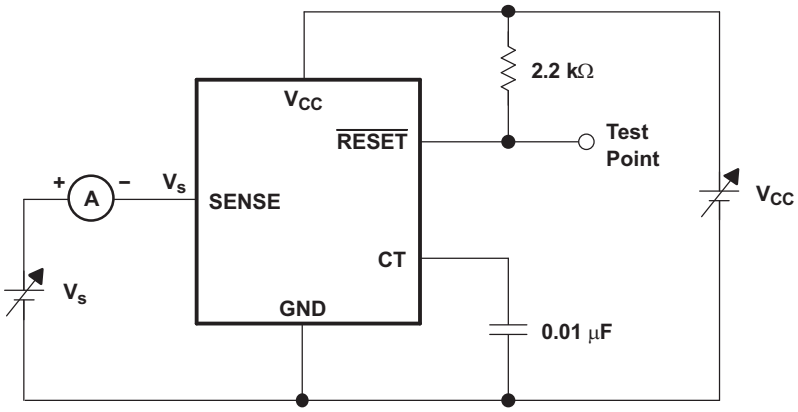


Figure 16. V_S, I_S Characteristics Measurement Circuit

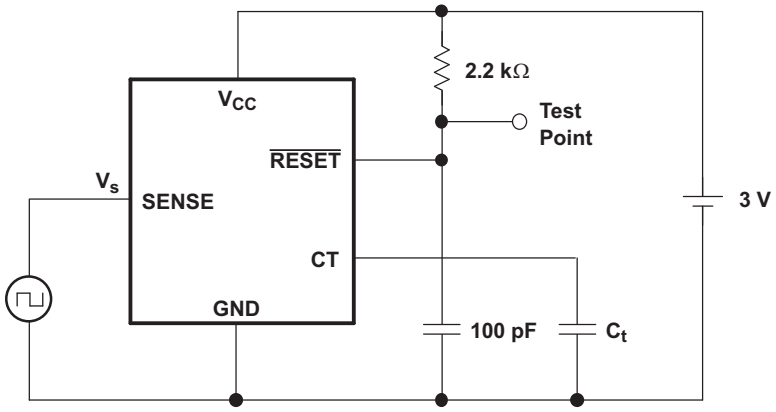


Figure 17. Switching Characteristics Measurement Circuit

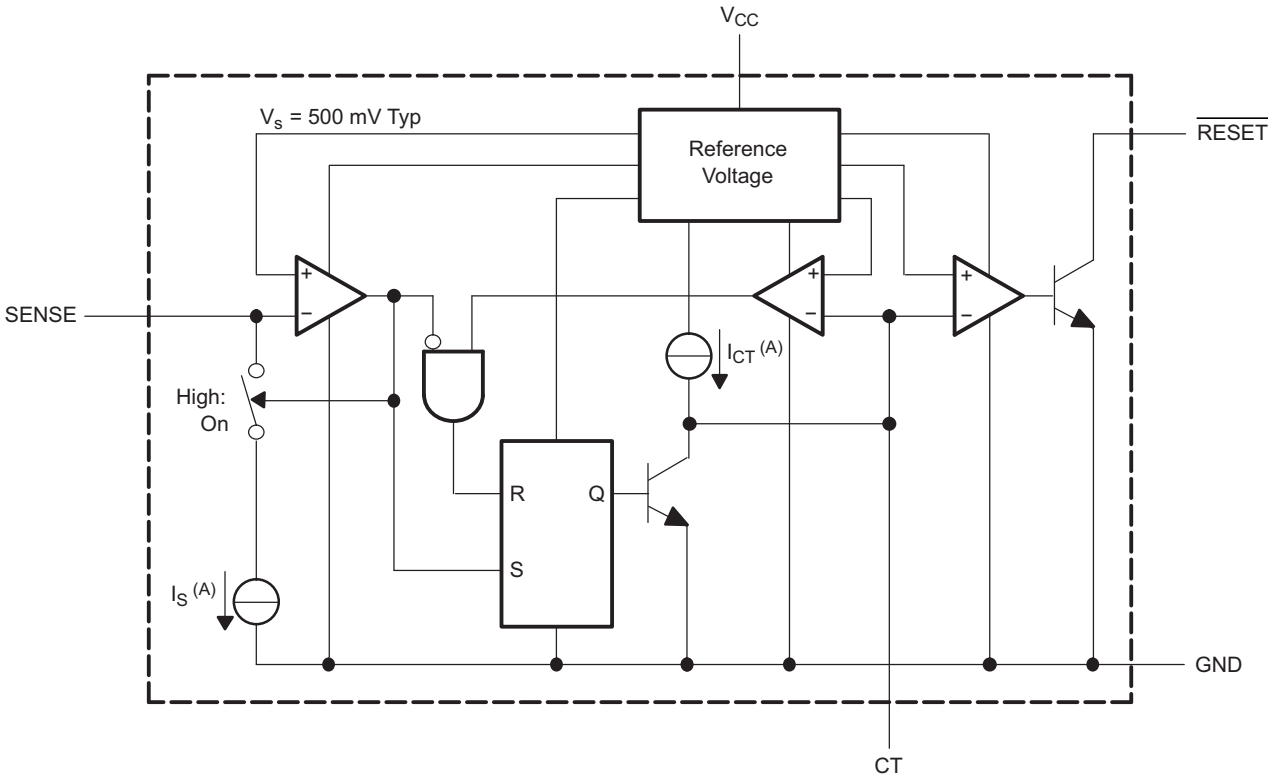
8 Detailed Description

8.1 Overview

The TL7700 is a bipolar integrated circuit designed for use as a reset controller in microcomputer and microprocessor systems. The SENSE voltage can be set to any value greater than 0.5 V using two external resistors. The hysteresis value of the sense voltage also can be set by the same resistors. The device includes a precision voltage reference, fast comparator, timing generator, and output driver, so it can generate a power-on reset signal in a digital system.

The TL7700 has an internal 1.5-V temperature-compensated voltage reference from which all function blocks are supplied. Circuit function is very stable, with supply voltage in the 1.8-V to 40-V range. Minimum supply current allows use with ac line operation, portable battery operation, and automotive applications.

8.2 Functional Block Diagram



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A. I_{CT} = 15 µA (Typ), I_s = 2.5 µA (Typ)

8.3 Feature Description

8.3.1 Sense-Voltage Setting

The SENSE terminal input voltage, Vs, of the TL7700 typically is 500 mV. By using two external resistors, the circuit designer can obtain any sense voltage over 500 mV. In Figure 18, the sensing voltage, Vs', is calculated as:

$$V_{s'} = V_s \times (R1 + R2)/R2 \quad (1)$$

where

- V_s = 500 mV typ at T_A = 25°C

At room temperature, V_S has a variation of 500 mV ± 5 mV. In the basic circuit shown in Figure 18, variations of [±5 ± (R1 + R2)/R2] mV are superimposed on V_S.

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Feature Description (continued)

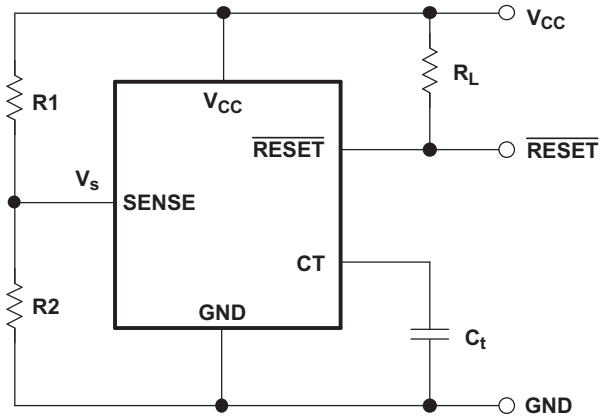


Figure 18. Setting the Sense Voltage

8.3.2 Sense-Voltage Hysteresis Setting

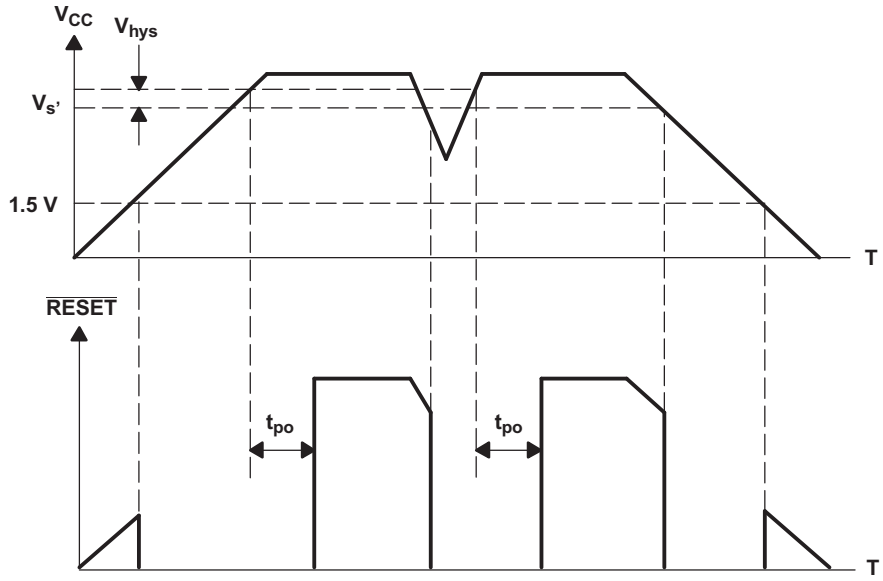
If the sense voltage ($V_{s'}$) does not have hysteresis in it, and the voltage on the sensing line contains ripples, the resetting of TL7700 is unstable. Hysteresis is added to the sense voltage to prevent such problems. As shown in Figure 19, the hysteresis (V_{hys}) is added, and the value is determined as:

$$V_{hys} = I_s \times R1$$

where

- I_s = 2.5 µA typ at T_A = 25°C (2)

At room temperature, I_s has variations of 2.5 µA ± 0.5 µA. Therefore, in the circuit shown in Figure 18, V_{hys} has variations of (±0.5 × R1) µV. In circuit design, it is necessary to consider the voltage-dividing resistor tolerance and temperature coefficient in addition to variations in V_s and V_{hys}.



The sense voltage, $V_{s'}$, is different from the SENSE terminal input voltage, V_s. V_s normally is 500 mV for triggering.

Figure 19. V_{CC}-RESET Timing Chart

Feature Description (continued)

8.3.3 Output Pulse-Duration Setting

Constant-current charging starts on the timing capacitor when the sensing-line voltage reaches the TL7700 sense voltage. When the capacitor voltage exceeds the threshold level of the output drive comparator, $\overline{\text{RESET}}$ changes from a low to a high level. The output pulse duration is the time between the point when the sense-pin voltage exceeds the threshold level and the point when the $\overline{\text{RESET}}$ output changes from a low level to a high level. When the TL7700 is used for system power-on reset, the output pulse duration, t_{po}, must be set longer than the power rise time. The value of t_{po} is:

$$t_{po} = C_t \times 10^5 \text{ seconds} \quad (3)$$

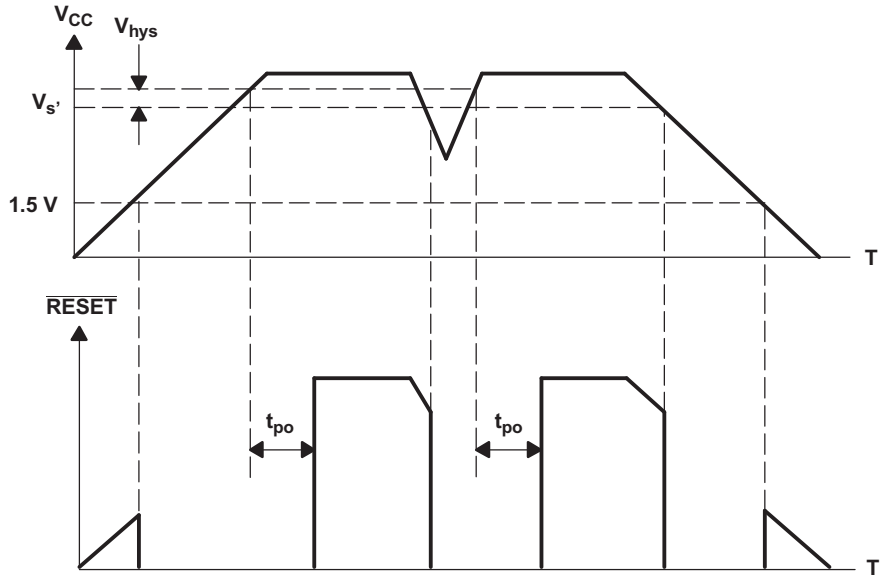
where

- C_t is the timing capacitor in farads

There is a limit on the device response speed. Even if C_t = 0, t_{po} is not 0, but approximately 5 µs to 10 µs. Therefore, when the TL7700 is used as a comparator with hysteresis without connecting C_t, switching speeds (t_r/t_f, t_{po}/t_{pd}, and so forth) must be considered.

8.4 Device Functional Modes

Figure 20 describes how the $\overline{\text{RESET}}$ output pin responds to a change in the voltage at the sense pin. When the sense pin drops below 500 mV, the $\overline{\text{RESET}}$ pin is pulled low.



The sense voltage, $V_{s'}$, is different from the SENSE terminal input voltage, V_s. V_s normally is 500 mV for triggering.

Figure 20. V_{CC} $\overline{\text{RESET}}$ Response and Timing

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TL7700 supply-voltage supervisor allows for any voltage greater than 500mV to be monitored. This flexibility allows it to be used in many applications from FPGAs and Microcontrollers to Industrial supply monitoring.

9.2 Typical Application

Figure 21 shows an application where the TL7700 device is being used to sense the voltage supply for a microcontroller that is supplied with 5 V. If the sense voltage drops below 4.5 V, the $\overline{\text{RESET}}$ pin is pulled LOW, signaling the microcontroller to reset.

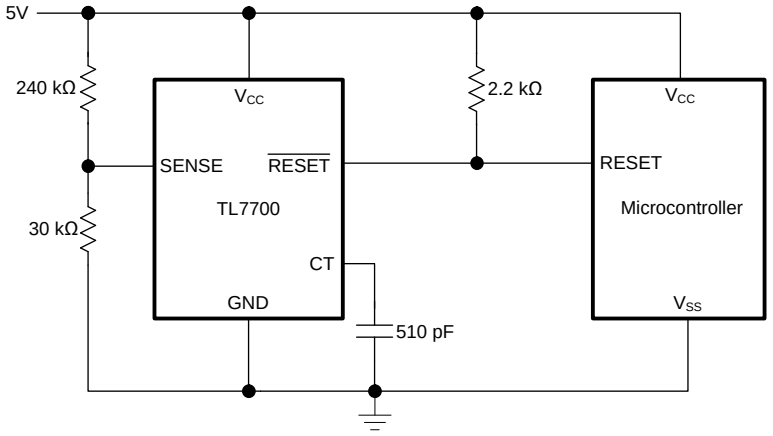

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Figure 21. 5-V Supply Voltage Supervision

9.2.1 Design Requirements

- When the TL7700 is used for system power-on reset, the output pulse duration, t_{po}, must be set longer than the power rise time. The value of t_{po} is: $t_{po} = C_t \times 10^5$ seconds
- The RESET output is an open-collector output, so a pullup resistor is required.

9.2.2 Detailed Design Procedure

The SENSE terminal input voltage, Vs, of the TL7700 typically is 500 mV. By using two external resistors, any sense voltage over 500 mV can be sensed.

Resistor R1 should be selected first to set the desired hysteresis. See *Sense-Voltage Hysteresis Setting* for detailed information on how to set the hysteresis.

Resistor R2 should then be selected based on the R1 value and the desired $V_{s'}$ voltage. In Figure 18, the sensing voltage, $V_{s'}$, is calculated as: $V_{s'} = V_s \times (R1 + R2)/R2$

Typical Application (continued)

9.2.3 Application Curve

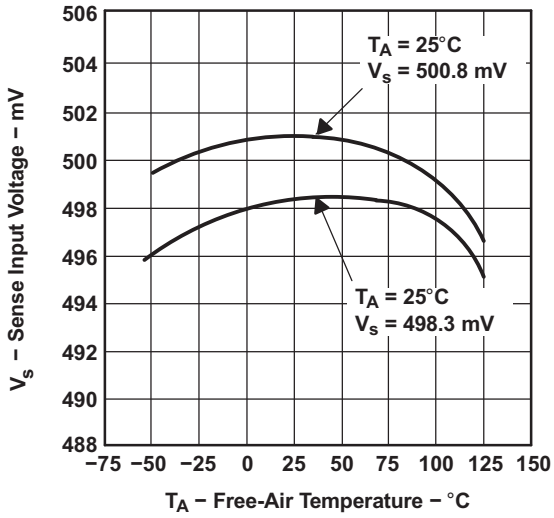

Figure 22. Sense Input Voltage vs Temperature

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10 Power Supply Recommendations

The TL7700 device will operate within the supply range specified in *Recommended Operating Conditions*. The device risks permanent damage over the voltage specified in *Absolute Maximum Ratings*.

11 Layout

11.1 Layout Guidelines

Figure 23 shows an example layout for the TL7700 device. As the $\overline{\text{RESET}}$ pin is an open collector output, a pullup resistor is required to ensure the output is high when the output transistor is off.

11.2 Layout Example

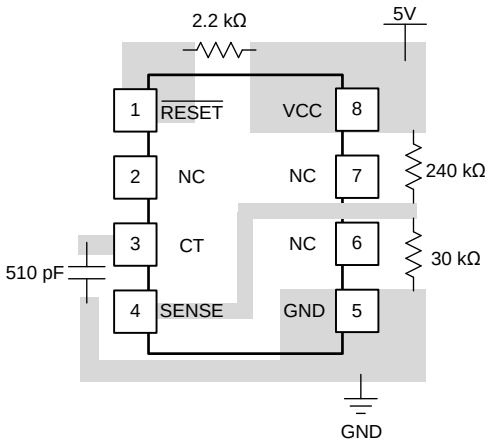

Figure 23. DGK Package Example Layout for 5 V Supply Supervision

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL7700CDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	9TS
TL7700CDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	9TS
TL7700CDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	9TS
TL7700CDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	9TS
TL7700CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL7700CP
TL7700CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TL7700CP
TL7700CPS	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	T7700
TL7700CPS.A	Active	Production	SO (PS) | 8	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	T7700
TL7700CPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	T7700
TL7700CPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	T7700
TL7700CPW	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	T7700
TL7700CPW.A	Active	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	T7700
TL7700CPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	T7700
TL7700CPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	T7700
TL7700CPWRG4	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	T7700
TL7700CPWRG4.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	T7700

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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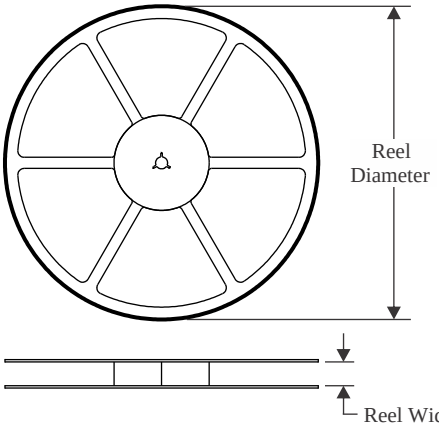
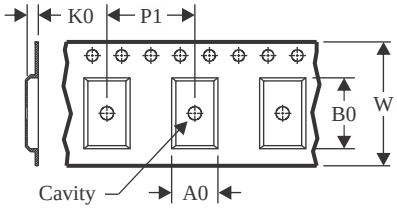
TAPE AND REEL INFORMATION

REEL DIMENSIONS

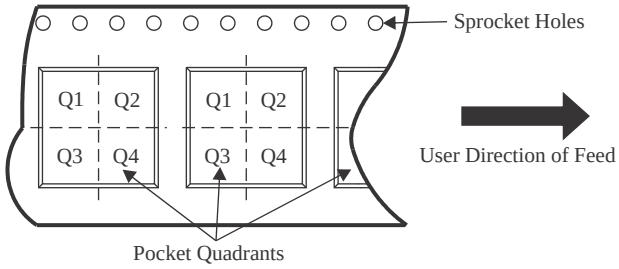


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

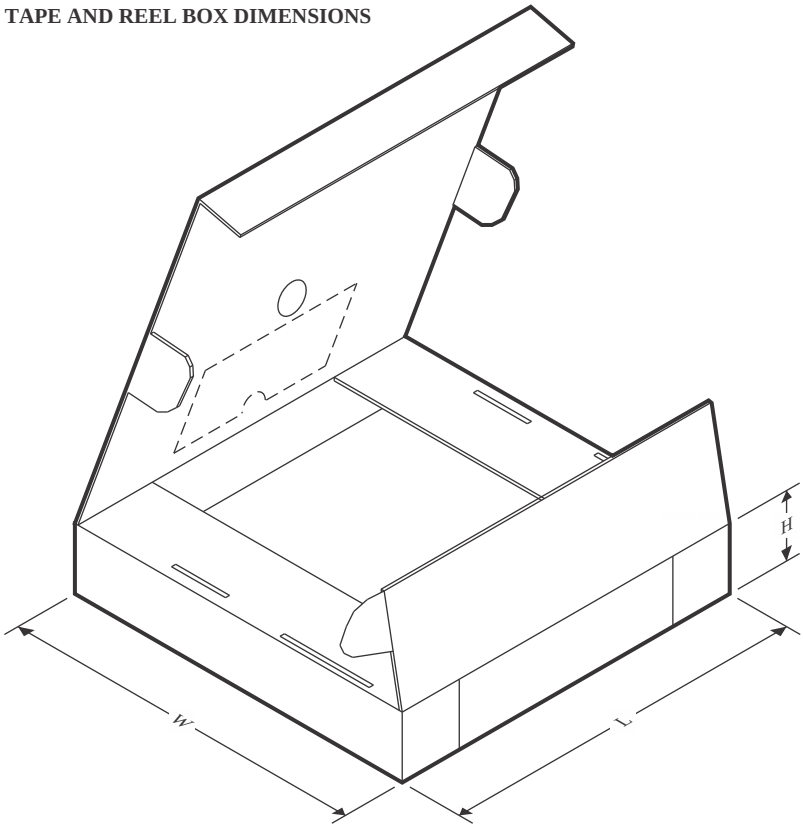
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL7700CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TL7700CDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TL7700CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL7700CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL7700CPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL7700CPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

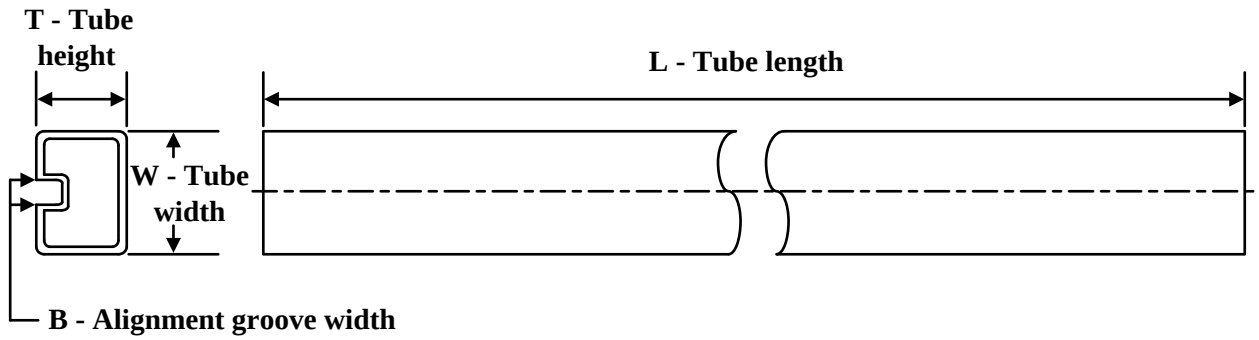
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL7700CDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TL7700CDGKT	VSSOP	DGK	8	250	358.0	335.0	35.0
TL7700CPSR	SO	PS	8	2000	353.0	353.0	32.0
TL7700CPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TL7700CPWRG4	TSSOP	PW	8	2000	353.0	353.0	32.0
TL7700CPWRG4	TSSOP	PW	8	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

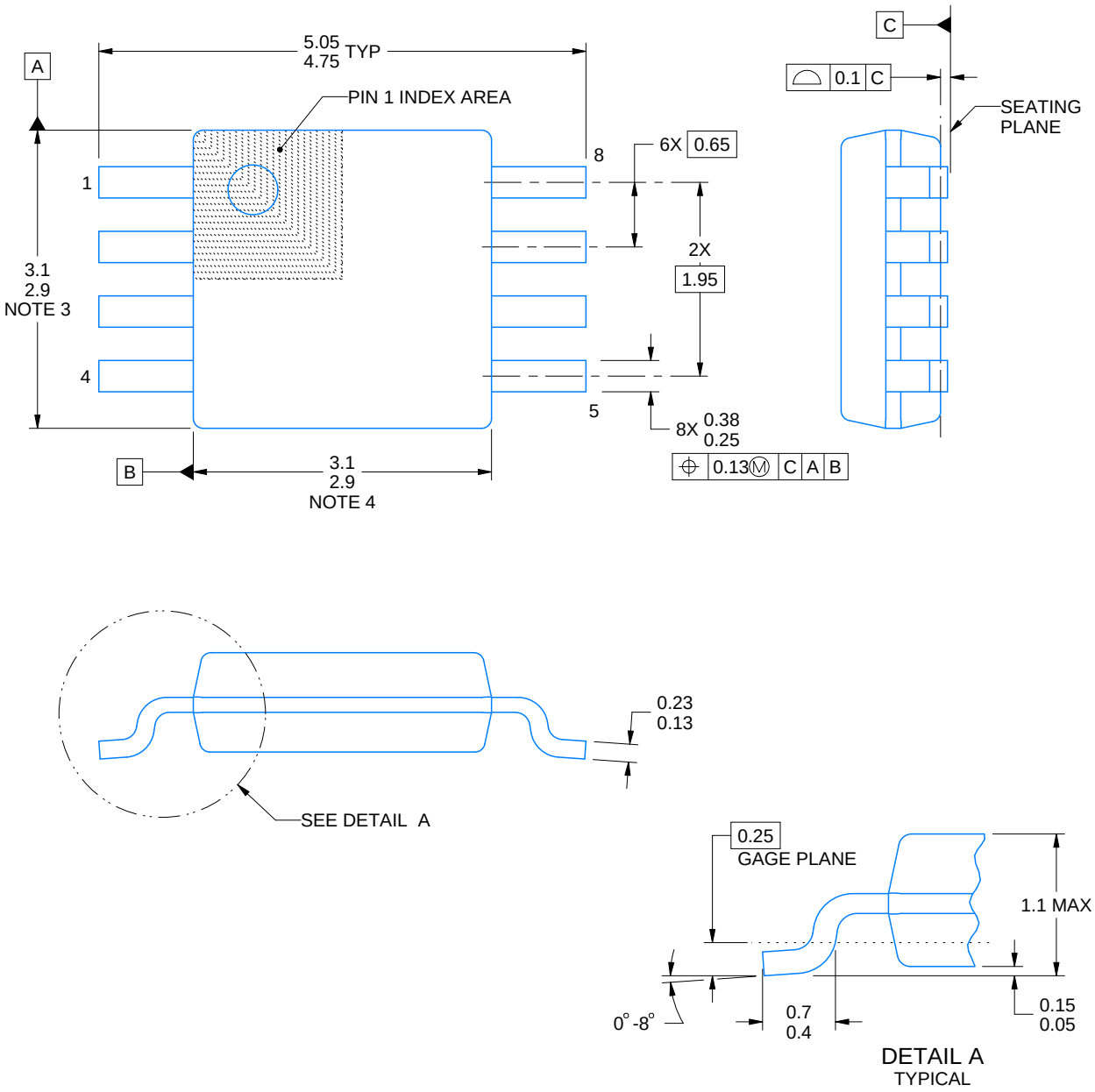
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL7700CP	P	PDIP	8	50	506	13.97	11230	4.32
TL7700CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TL7700CPS	PS	SOP	8	80	530	10.5	4000	4.1
TL7700CPS.A	PS	SOP	8	80	530	10.5	4000	4.1
TL7700CPW	PW	TSSOP	8	150	530	10.2	3600	3.5
TL7700CPW.A	PW	TSSOP	8	150	530	10.2	3600	3.5

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

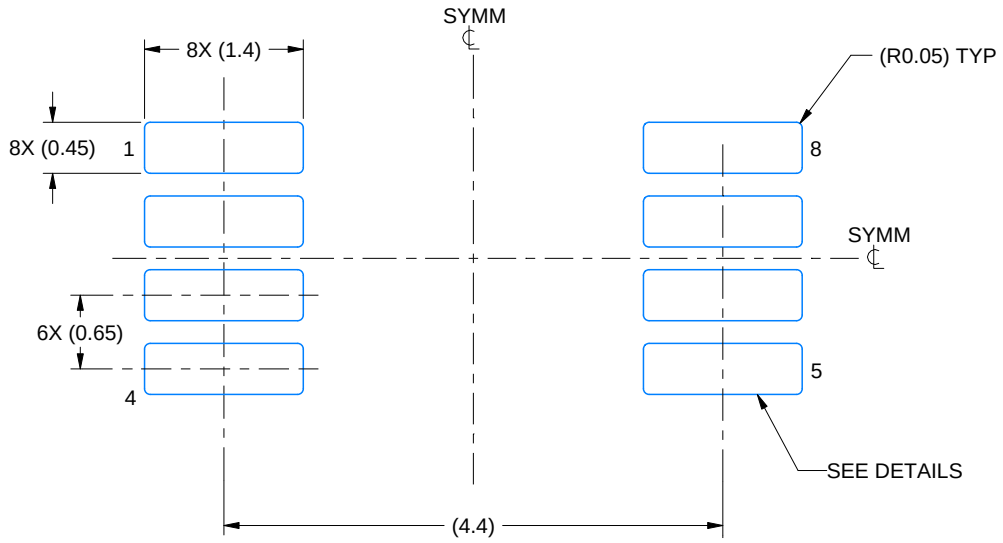
SMALL OUTLINE PACKAGE



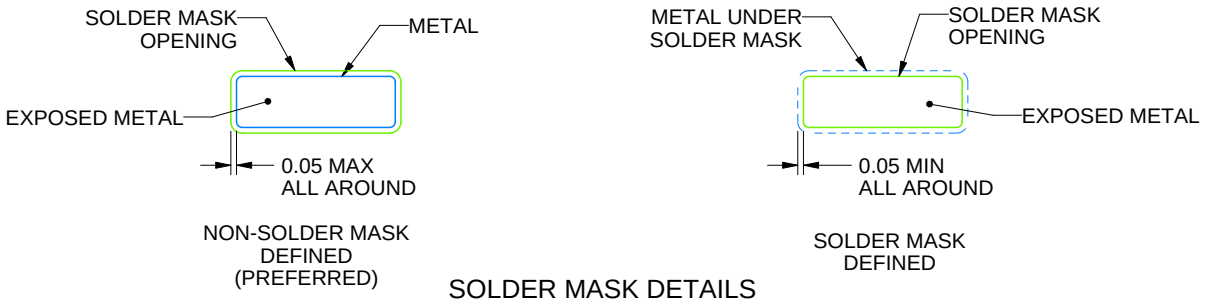
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

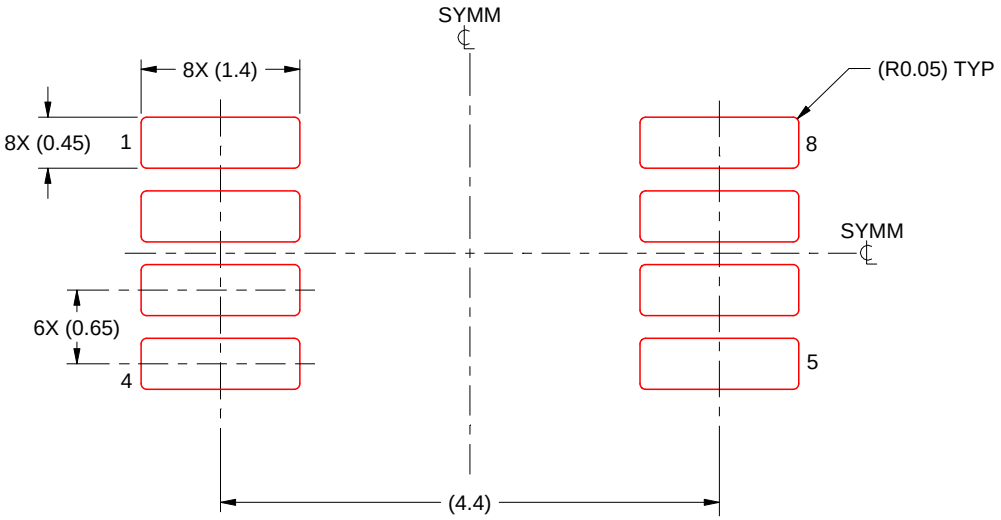


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

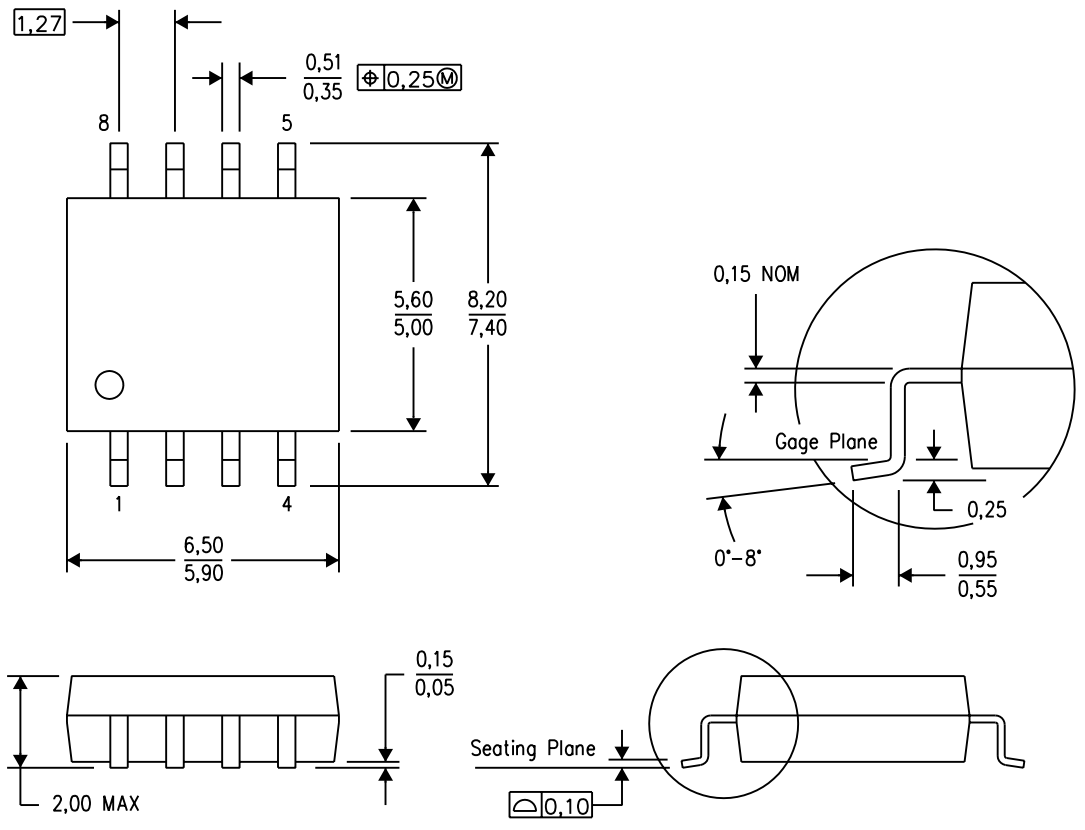
4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

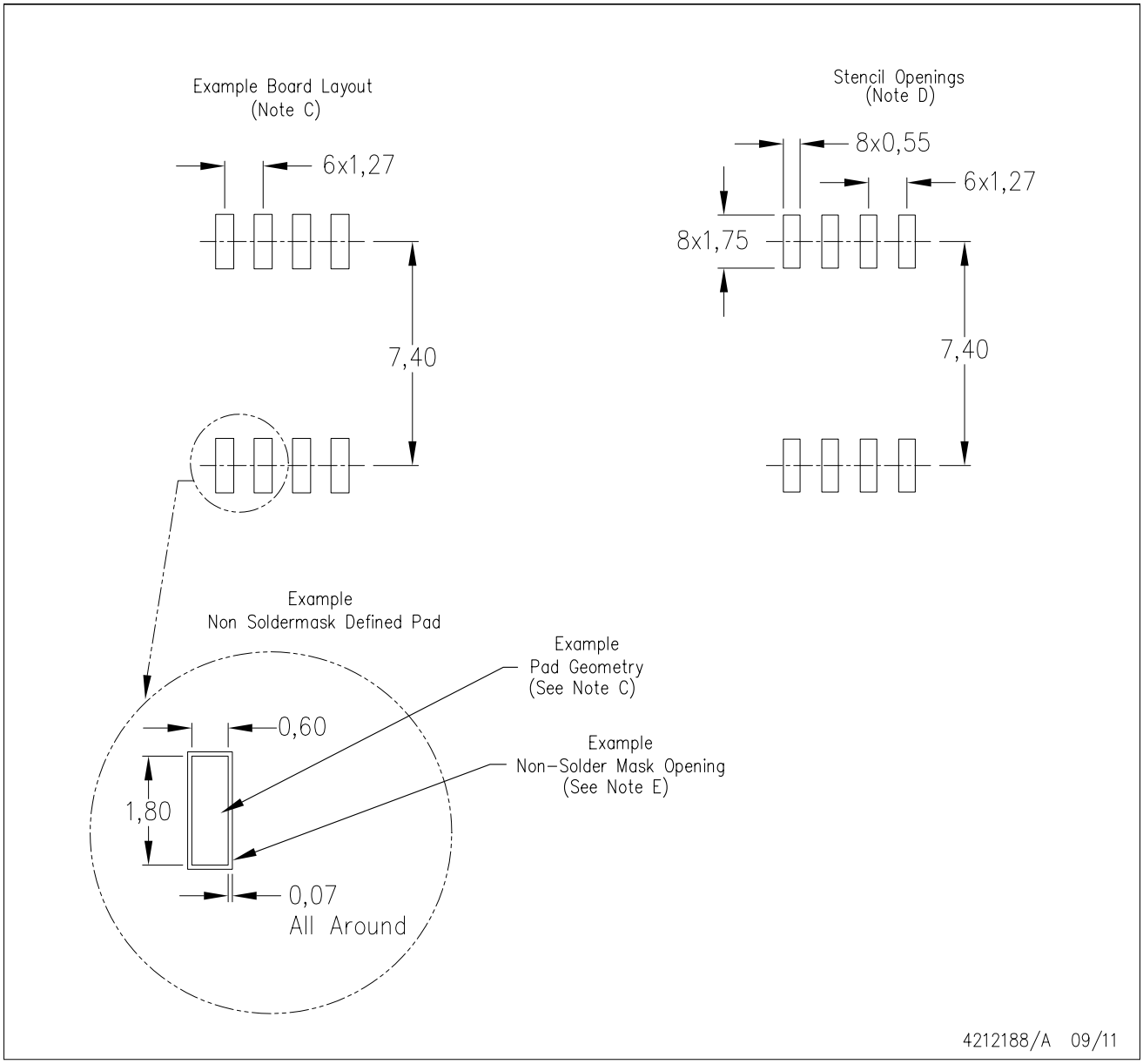
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

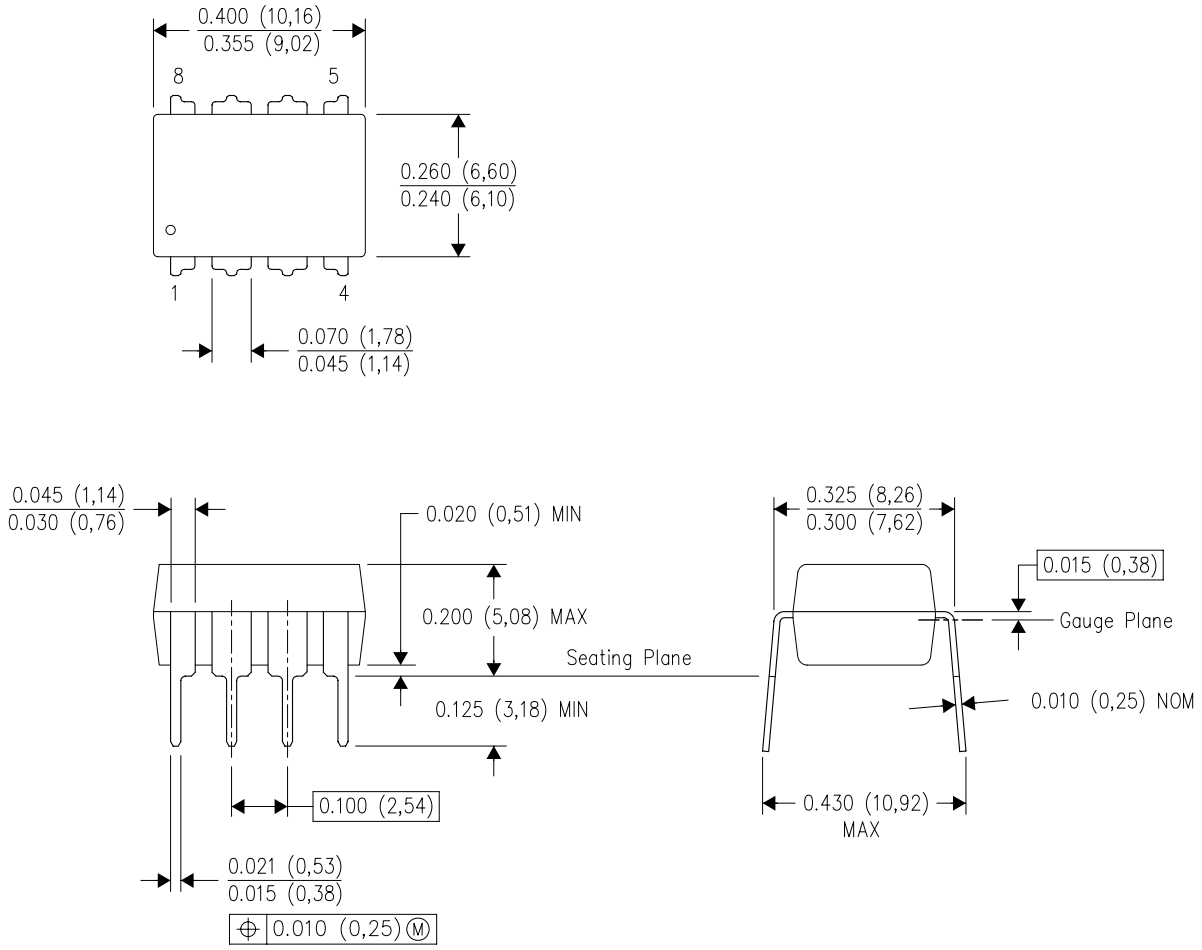
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



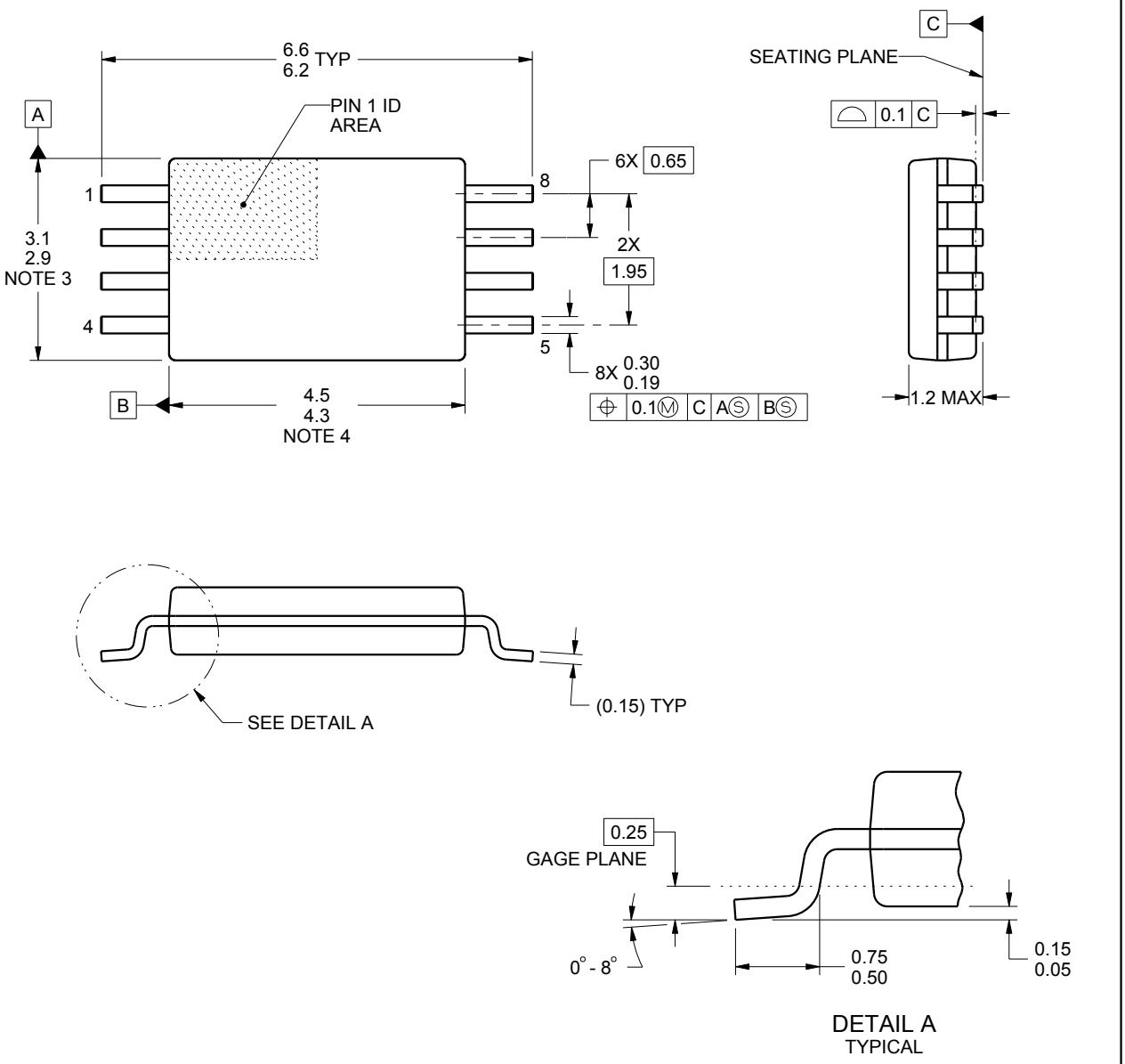
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

PW0008A

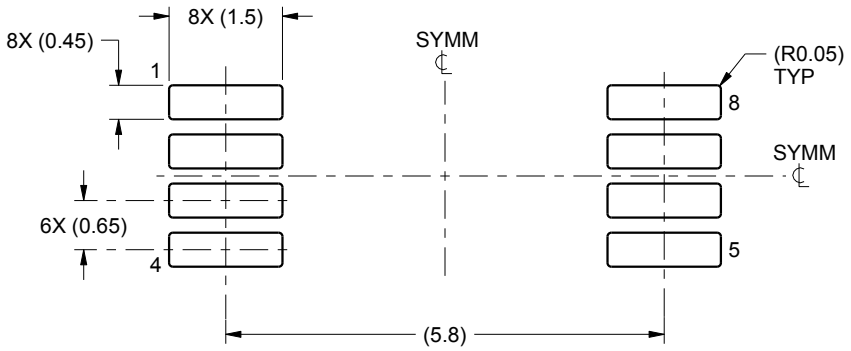
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

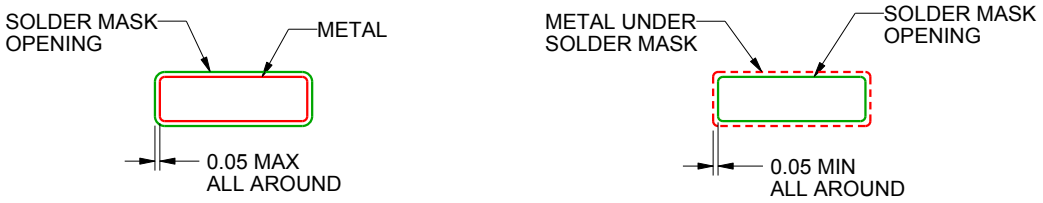


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

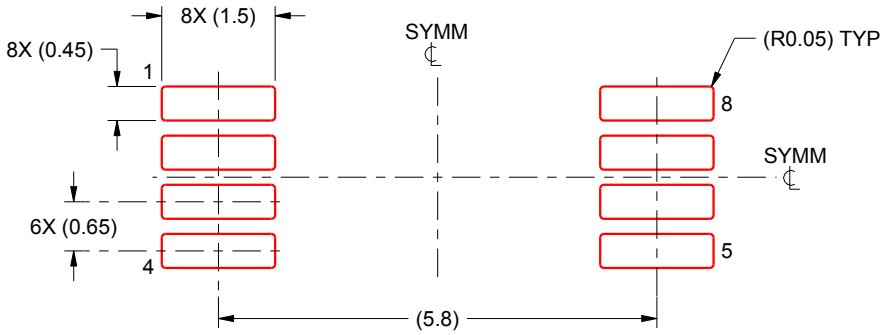


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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