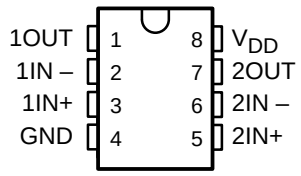
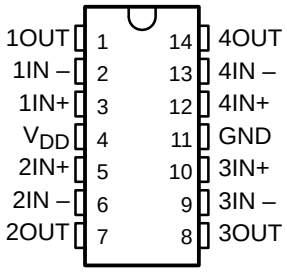
- **Power Dissipation as Low as 10 μW Typ Per Amplifier**
- **Operates on a Single Silver-Oxide Watch Battery, V_{DD} = 1.4 V Min**
- **V_{IO} . . . 450 μV/850 μV Max in DIP and Small-Outline Package (TLC1078/79)**
- **Input Offset Voltage Drift . . . 0.1 μV/Month Typ, Including the First 30 Days**
- **High-impedance LinCMOS™ Inputs**
  I_{IB} = 0.6 pA Typ
- **High Open-Loop Gain . . . 800 000 Typ**
- **Output Drive Capability > 20 mA**
- **Slew Rate . . . 47 V/ms Typ**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail**
- **Output Voltage Range Includes Negative Rail**
- **On-Chip ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**

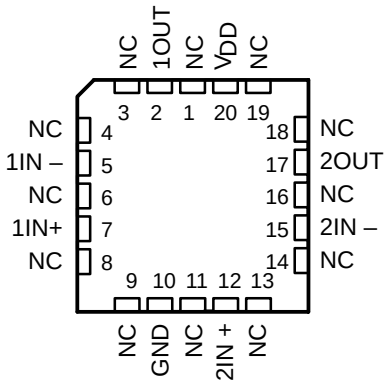
TLC1078
D, JG, OR P PACKAGE
(TOP VIEW)



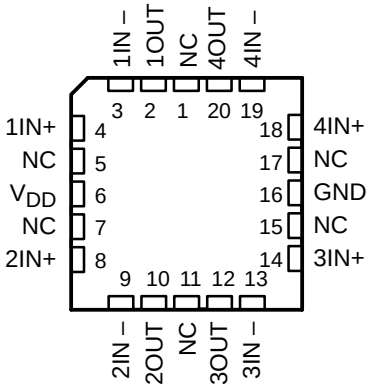
TLC1079
D, J, OR N PACKAGE
(TOP VIEW)



TLC1078
FK PACKAGE
(TOP VIEW)



TLC1079
FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TLC107x operational amplifiers offer ultra-low offset voltage, high gain, 110-kHz bandwidth, 47-V/ms slew rate, and just 150-μW power dissipation per amplifier.

With a supply voltage of 1.4 V, common-mode input to the negative rail, and output swing to the negative rail, the TLC107xC is an ideal solution for low-voltage battery-operated systems. The 20-mA output drive capability means that the TLC107x can easily drive small resistive and large capacitive loads when needed, while maintaining ultra-low standby power dissipation.

Since this device is functionally compatible as well as pin compatible with the TLC27L2/4 and TLC27L7/9, the TLC107x easily upgrades existing designs that can benefit from its improved performance.

description (continued)

The TLC107x incorporates internal ESD-protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-PRF-38535, Method 3015.2; however, care should be exercised when handling these devices as exposure to ESD may result in degradation of the device parametric performance. The TLC107x design also inhibits latch-up of the device inputs and outputs even with surge currents as large 100 mA.

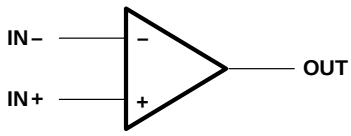
The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C. The wide range of packaging options includes small-outline and chip-carrier versions for high-density system applications.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES						CHIP FORM‡ (Y)
	SMALL OUTLINE† (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	CERAMIC DIP (JG)	PLASTIC DIP (N)	PLASTIC DIP (P)	
0°C to 70°C	TLC1078CD TLC1079CD	—	—	—	TLC1079CN	TLC1078CP	TLC1078Y TLC1079Y
–40°C to 85°C	TLC1078ID TLC1079ID	—	—	—	TLC1079IN	TLC1078IP	—
–55°C to 125°C	TLC1078MD TLC1079MD	TLC1078MFK TLC1079MFK	TLC1079MJ	TLC1078MJG	TLC1079MN	TLC1078MP	—

† The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC1078CDR).
‡ Chip forms are tested 25°C only.

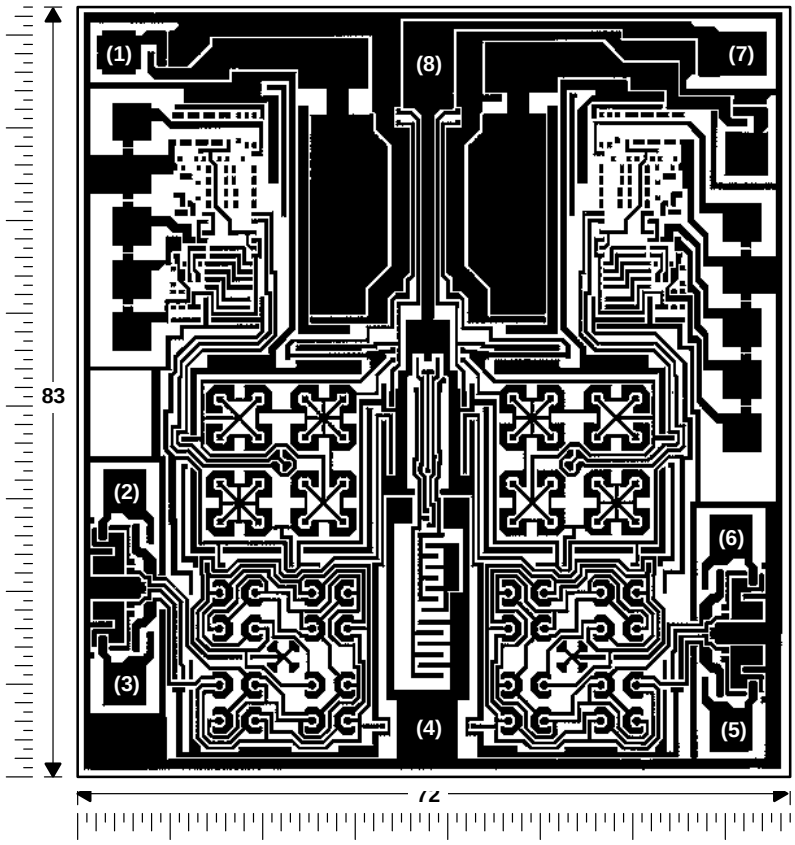
symbol (each amplifier)

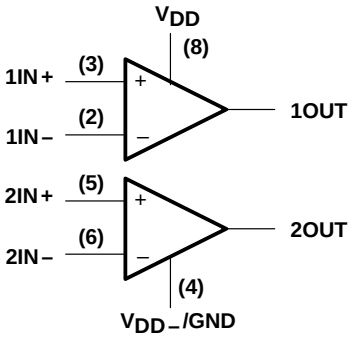


TLC1087Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC1078C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips can be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

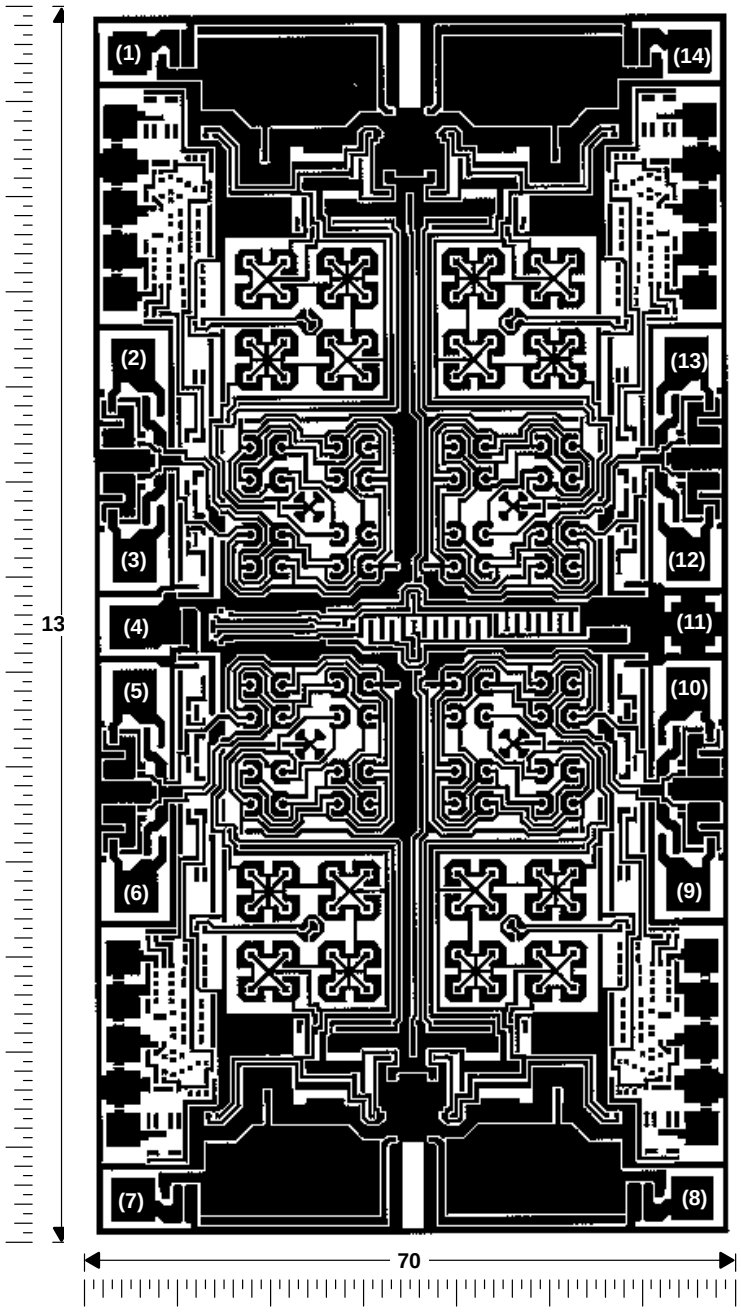
$T_J$max = 150°C

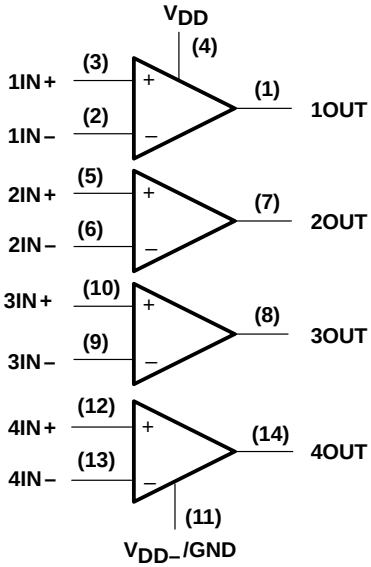
TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

TLC1079Y chip information

This chip, when properly assembled, display characteristics similar to the TLC1079C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips can be mounted with conductive epoxy or a gold-silicon preform.





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

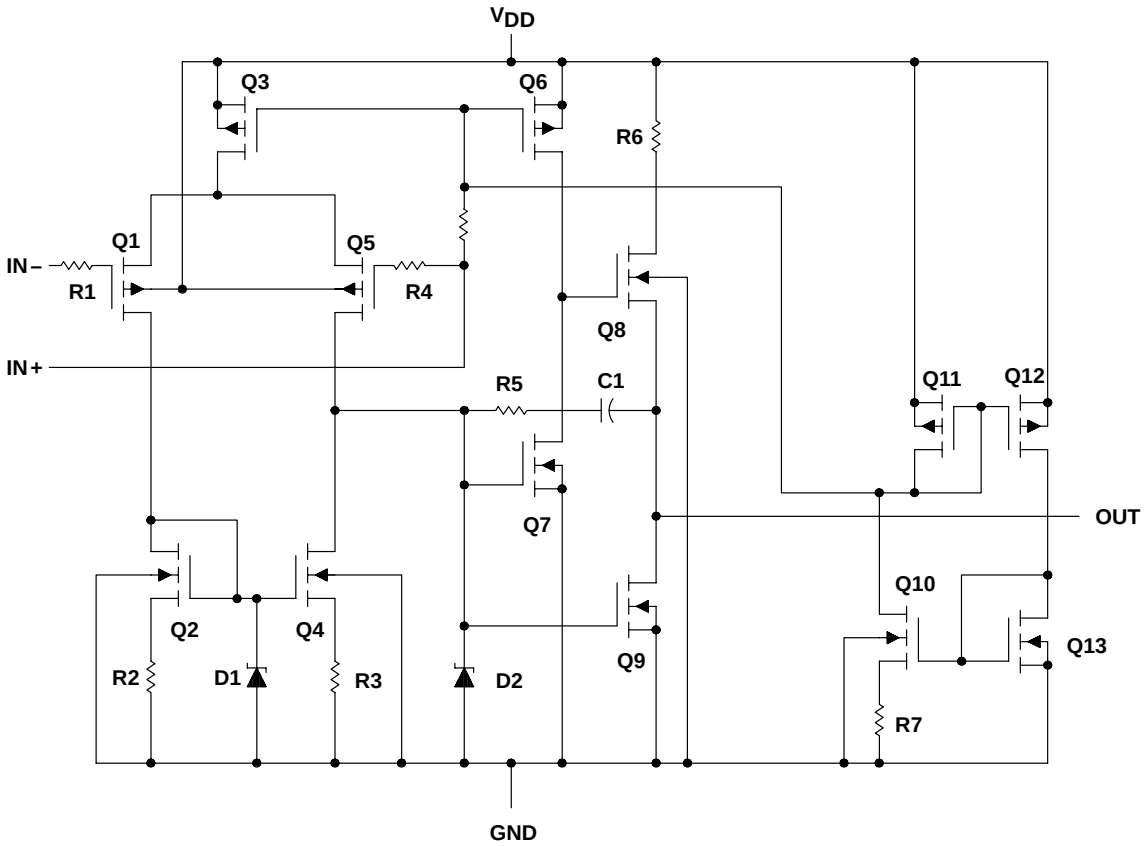
$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (11) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT		
COMPONENT	**TLC1078**	**TLC1079**
Transistors	38	76
Resistors	16	32
Diodes	12	24
Capacitors	2	4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Differential input voltage, V_{ID} (see Note 2) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input) . . . . . –0.3 V to V_{DD}
Input current, I_I (each input) . . . . . ± 5 mA
Output current, I_O (each output) . . . . . ± 30 mA
Total current into V_{DD} (see Note 3) . . . . . 45 mA
Duration of short-circuit at (or below) T_A = 25°C (see Note 3) . . . . . unlimited
Continuous total power dissipation . . . . . see Dissipation Rating Table
Operating free-air temperature range, T_A: C suffix . . . . . 0°C to 70°C
I suffix . . . . . –40°C to 85°C
M suffix . . . . . –55°C to 125°C
Storage temperature range . . . . . –65°C to 150°C
Case temperature for 60 seconds: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or P package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN–.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation ratings are not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D–8	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW
D–14	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW	230 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

recommended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{DD}		1.4	16	3	16	4	16	V
Common-mode input voltage, V_{IC}	V_{DD} = 5 V	–0.2	4	–0.2	4	0	4	V
	V_{DD} = 10 V	–0.2	9	–0.2	9	0	9	
Operating free-air temperature, T_A		0	70	–40	85	–55	125	°C

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLC1078C						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, R_S = 50 Ω, V_{IC} = 0, R_I = 1 MΩ	25°C		160	450		180	600	μV
			Full range			800			950	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2	25°C		0.1	60		0.1	60	pA
			70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		25°C		0.6	60		0.7	60	pA
			70°C		40	600		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	–0.2 to 4	–0.3 to 4.2		–0.2 to 9	–0.3 to 9.2		V
			Full range	–0.2 to 3.5			–0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L= 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			0°C	3.2	4.1		8.2	8.9		
			70°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = –100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			0°C		0	25		0	25	
			70°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L= 1 MΩ, See Note 6	25°C	250	525		500	850		V/mV
			0°C	250	680		500	1010		
			70°C	200	380		350	660		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	70	95		75	97		dB
			0°C	70	95		75	97		
			70°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_O = 1.4 V	25°C	75	98		75	98		dB
			0°C	75	98		75	98		
			70°C	75	98		75	98		
I_{DD}	Supply current (two amplifiers)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2, No load	25°C		20	34		29	46	μA
			0°C		24	42		36	66	
			70°C		16	28		22	40	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V. V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLC1079C						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_I = 1 MΩ	25°C		190	850		200	1150	μV
			Full range			1200			1500	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 70°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 4)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1	60		0.1	60	pA
			70°C		7	300		7	300	
I_{IB}	Input bias current (see Note 4)		25°C		0.6	60		0.7	60	pA
			70°C		40	600		50	600	
V_{ICR}	Common mode input voltage range (see Note 5)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			0°C	3.2	4.1		8.2	8.9		
			70°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = –100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			0°C		0	25		0	25	
			70°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 6	25°C	250	525		500	850		V/mV
			0°C	250	700		500	1010		
			70°C	200	380		350	660		
CMRR	Common mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C	70	95		75	97		dB
			0°C	70	95		75	97		
			70°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			0°C	75	98		75	98		
			70°C	75	98		75	98		
I_{DD}	Supply current (four amplifiers)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		40	68		57	92	μA
			0°C		48	84		72	132	
			70°C		31	56		44	80	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A	TLC1078C						UNIT
					V_{DD} = 5 V			V_{DD} = 10 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, $V_{I(PP)}$ = 1 V,	C_L = 20 pF, See Figure 1	25°C		32			47		V/ms
				0°C		35			51		
				70°C		27			38		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 20 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF,	See Figure 2	25°C		85			110		kHz
				0°C		100			125		
				70°C		65			90		
ϕ_m	Phase margin at unity gain	C_L = 20 pF,	See Figure 2	25°C		34°			38°		
				0°C		36°			40°		
				70°C		30°			34°		

operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A	TLC1079C						UNIT
					V_{DD} = 5 V			V_{DD} = 10 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, $V_{I(PP)}$ = 1 V,	C_L = 20 pF, See Figure 1	25°C		32			47		V/ms
				0°C		35			51		
				70°C		27			38		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 20 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF,	See Figure 2	25°C		85			110		kHz
				0°C		100			125		
				70°C		65			90		
ϕ_m	Phase margin at unity gain	C_L = 20 pF,	See Figure 2	25°C		34°			38°		
				0°C		36°			40°		
				70°C		30°			34°		

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLC1078I						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, R_S = 50 Ω, V_{IC} = 0, R_I = 1 MΩ	25°C		160	450		180	600	μV
			Full range			950			1100	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2	25°C		0.1	60		0.1	60	pA
			85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 4)		25°C		0.6	60		0.7	60	pA
			85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			−40°C	3.2	4.1		8.2	8.9		
			85°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = –100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			−40°C		0	25		0	25	
			85°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 6	25°C	250	525		500	850		V/mV
			−40°C	250	900		500	1550		
			85°C	150	300		250	585		
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min	25°C	70	95		75	97		dB
			−40°C	70	95		75	97		
			85°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_O = 1.4 V	25°C	75	98		75	98		dB
			−40°C	75	98		75	98		
			85°C	75	98		75	98		
I_{DD}	Supply current (two amplifiers)	V_O = V_{DD}/ 2, V_{IC} = V_{DD}/ 2, No load	25°C		20	34		29	46	μA
			−40°C		31	54		50	86	
			85°C		15	26		20	36	

† Full range is –40°C to 80°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLC1079I						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_I = 1 MΩ	25°C		190	850		200	1150	μV
			Full range			1350			1650	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 85°C		1.1			1		μV/°C
I_{IO}	Input offset current (see Note 4)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1	60		0.1	60	pA
			85°C		24	1000		26	1000	
I_{IB}	Input bias current (see Note 4)		25°C		0.6	60		0.7	60	pA
			85°C		200	2000		220	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			−40°C	3.2	4.1		8.2	8.9		
			85°C	3.2	4.2		8.2	8.9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			−40°C		0	25		0	25	
			85°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 6	25°C	250	525		500	850		V/mV
			−40°C	250	900		500	1550		
			85°C	150	330		250	585		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C	70	95		75	97		dB
			−40°C	70	95		75	97		
			85°C	70	95		75	97		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			−40°C	75	98		75	98		
			85°C	75	98		75	98		
I_{DD}	Supply current (four amplifiers)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		40	68		57	92	μA
			−40°C		62	108		98	172	
			85°C		29	52		40	72	

† Full range is −40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A	TLC1078I						UNIT
					V_{DD} = 5 V			V_{DD} = 10 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, $V_{I(PP)}$ = 1 V,	C_L = 20 pF, See Figure 1	25°C		32			47		V/ms
				–40°C		39			59		
				85°C		25			34		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 20 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF,	See Figure 2	25°C		85			110		kHz
				–40°C		130			155		
				85°C		55			80		
ϕ_m	Phase margin at unity gain	C_L = 20 pF,	See Figure 2	25°C		34°			38°		
				–40°C		38°			40°		
				85°C		28°			32°		

operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A	TLC1079I						UNIT
					V_{DD} = 5 V			V_{DD} = 10 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, $V_{I(PP)}$ = 1 V,	C_L = 20 pF, See Figure 1	25°C		32			47		V/ms
				–40°C		39			59		
				85°C		25			34		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 20 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF,	See Figure 2	25°C		85			110		kHz
				–40°C		130			155		
				85°C		55			80		
ϕ_m	Phase margin at unity gain	C_L = 20 pF,	See Figure 2	25°C		34°			38°		
				–40°C		38°			42°		
				85°C		28°			32°		

electrical characteristics at specified operating free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLC1078M						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_L = 1 MΩ	25°C		160	450		180	600	μV
			Full range			1250			1400	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		μV/°C
I_{IO}	Input offset current (see Note 4)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1	60		0.1	60	pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		25°C		0.6	60		0.7	60	pA
			125°C		9	35		10	35	nA
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			−55°C	3.2	4.1		8.2	8.8		
			125°C	3.2	4.2		8.2	9		
V_{OL}	Low-level output voltage	V_{ID} = −100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			−55°C		0	25		0	25	
			125°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 6	25°C	250	525		500	850		V/mV
			−55°C	250	950		500	1750		
			125°C	35	200		75	380		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C	70	95		75	97		dB
			−55°C	70	95		75	97		
			125°C	70	85		75	91		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_O = 1.4 V	25°C	75	98		75	98		dB
			−55°C	70	98		70	98		
			125°C	70	98		70	98		
I_{DD}	Supply current (two amplifiers)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		20	34		29	46	μA
			−55°C		35	60		56	96	
			125°C		14	24		18	30	

† Full range is −55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T_A†	TLC1079M						UNIT
				V_{DD} = 5 V			V_{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1.4 V, V_{IC} = 0, R_S = 50 Ω, R_I = 1 MΩ	25°C		190	850		200	1150	μV
			Full range			1600			1900	
α_{VIO}	Temperature coefficient of input offset voltage		25°C to 125°C		1.4			1.4		μV/°C
I_{IO}	Input offset current (see Note 4)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$	25°C		0.1	60		0.1	60	pA
			125°C		1.4	15		1.8	15	nA
I_{IB}	Input bias current (see Note 4)		25°C		0.6	60		0.7	60	pA
			125°C		9	35		10	35	nA
V_{ICR}	Common mode input voltage range (see Note 5)		25°C	0 to 4	−0.3 to 4.2		0 to 9	−0.3 to 9.2		V
			Full range	0 to 3.5			0 to 8.5			V
V_{OH}	High-level output voltage	V_{ID} = 100 mV, R_L = 1 MΩ	25°C	3.2	4.1		8.2	8.9		V
			−55°C	3.2	4.1		8.2	8.9		
			125°C	3.2	4.2		8.2	9		
V_{OL}	Low-level output voltage	V_{ID} = –100 mV, I_{OL} = 0	25°C		0	25		0	25	mV
			−55°C		0	25		0	25	
			125°C		0	25		0	25	
A_{VD}	Large-signal differential voltage amplification	R_L = 1 MΩ, See Note 6	25°C	250	525		500	850		V/mV
			−55°C	250	950		500	1750		
			125°C	35	200		75	380		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min	25°C	70	95		75	97		dB
			−55°C	70	95		75	97		
			125°C	70	85		75	91		
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 5 V to 10 V, V_O = 1.4 V	25°C	75	98		75	98		dB
			−55°C	70	98		70	98		
			125°C	70	98		70	98		
I_{DD}	Supply current (four amplifiers)	$V_O = V_{DD}/2$, $V_{IC} = V_{DD}/2$, No load	25°C		40	68		57	92	μA
			−55°C		69	120		111	192	
			125°C		27	48		35	60	

† Full range is –55°C to 125°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

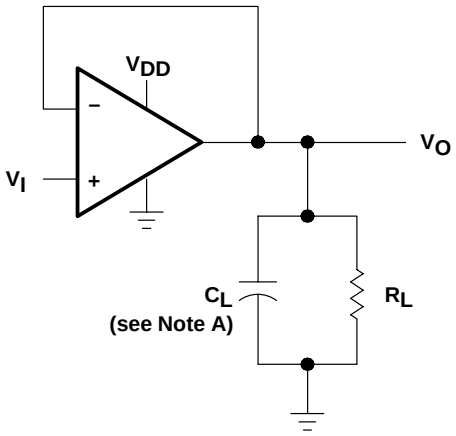
operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A	TLC1078M						UNIT
					V_{DD} = 5 V			V_{DD} = 10 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, $V_{I(PP)}$ = 1 V,	C_L = 20 pF, See Figure 1	25°C		32			47		V/ms
				–55°C		41			63		
				125°C		20			27		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 20 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF,	See Figure 2	25°C		85			110		kHz
				–55°C		140			165		
				125°C		45			70		
ϕ_m	Phase margin at unity gain	C_L = 20 pF,	See Figure 2	25°C		34°			38°		
				–55°C		39°			43°		
				125°C		25°			29°		

operating characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS		T_A	TLC1079M						UNIT
					V_{DD} = 5 V			V_{DD} = 10 V			
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	R_L = 1 MΩ, $V_{I(PP)}$ = 1 V,	C_L = 20 pF, See Figure 1	25°C		32			47		V/ms
				–55°C		41			63		
				125°C		20			27		
V_n	Equivalent input noise voltage	f = 1 kHz,	R_S = 20 Ω	25°C		68			68		nV/√Hz
B_1	Unity-gain bandwidth	C_L = 20 pF,	See Figure 2	25°C		85			110		kHz
				–55°C		140			165		
				125°C		45			70		
ϕ_m	Phase margin at unity gain	C_L = 20 pF,	See Figure 2	25°C		34°			38°		
				–55°C		39°			43°		
				125°C		25°			29°		

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate Test Circuit

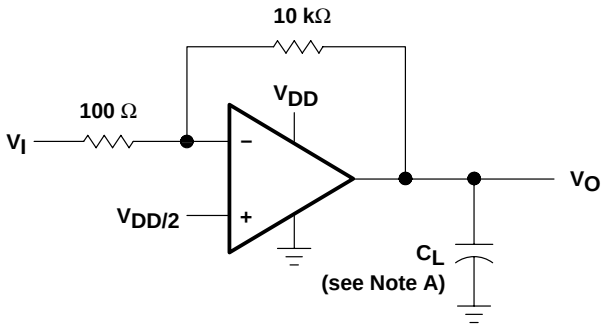


Figure 2. Unity-Gain Bandwidth and Phase-Margin Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
α_{VIO}	Temperature coefficient of input offset voltage	Distribution	3 – 6
I_{IB}	Input bias current	vs Free-air temperature	7
I_{IO}	Input offset current	vs Free-air temperature	7
V_{IC}	Common-mode input voltage	vs Supply voltage	8
V_{OH}	High-level output voltage	vs High-level output current vs Supply voltage vs Free-air temperature	9, 10 11 12
V_{OL}	Low-level output voltage	vs Common-mode input voltage vs Differential input voltage vs Free-air temperature vs Low-level output current	13, 14 15 16 17, 18
A_{VD}	Large-signal differential voltage amplification	vs Supply voltage vs Free-air temperature vs Frequency	19 20 21, 22
V_{OM}	Maximum peak output voltage	vs Frequency	23
I_{DD}	Supply current	vs Supply voltage vs Free-air temperature	24 25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
	Normalized slew rate	vs Free-air temperature	28
V_n	Equivalent input noise voltage	vs Frequency	29
B_1	Unity-gain bandwidth	vs Supply voltage vs Free-air temperature	30 31
ϕ_m	Phase margin	vs Supply voltage vs Free-air temperature vs Capacitive load	32 33 34
	Phase shift	vs Frequency	21, 22

TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLC1078
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

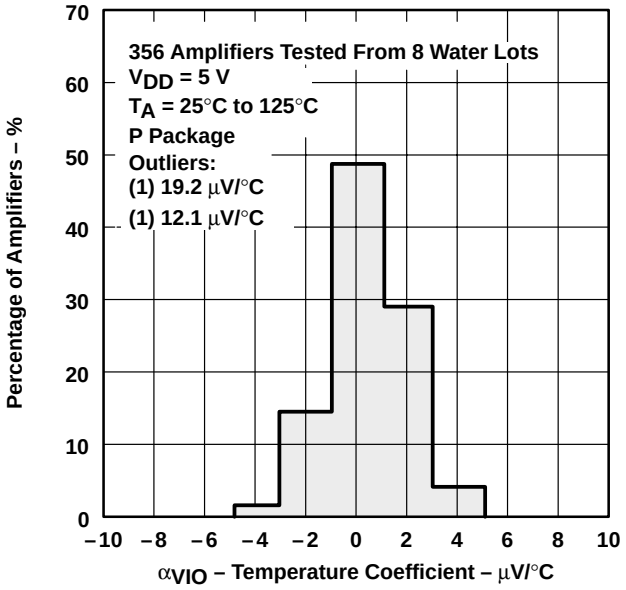


Figure 3

**DISTRIBUTION OF TLC1078
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

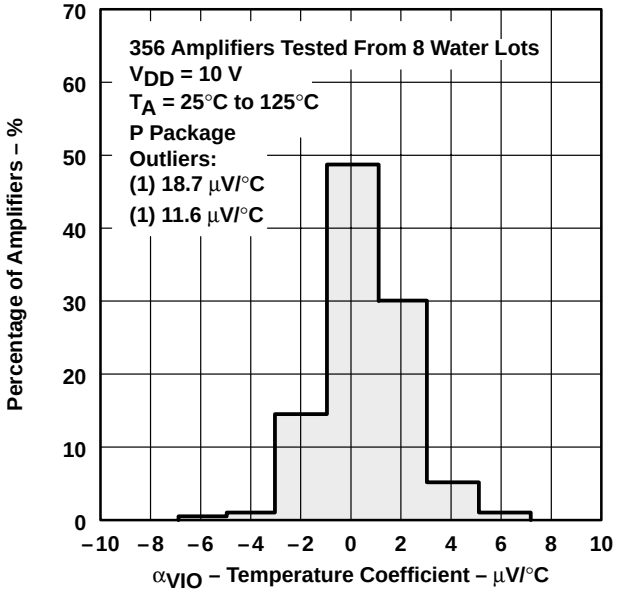


Figure 4

**DISTRIBUTION OF TLC1079
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

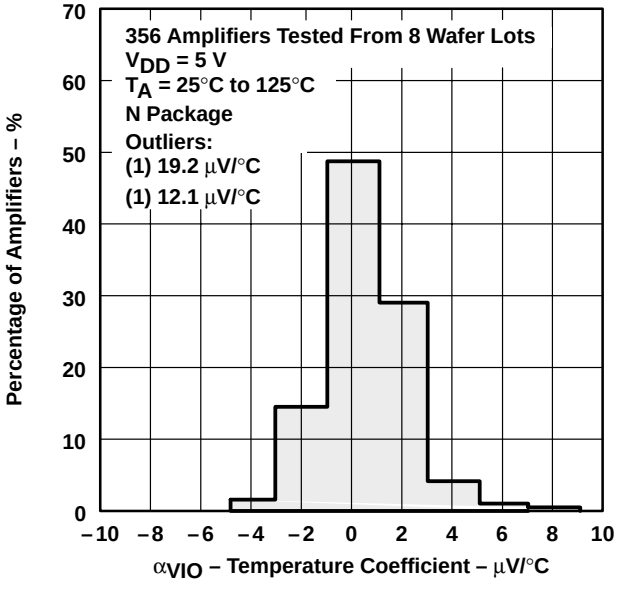


Figure 5

**DISTRIBUTION OF TLC1079
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT**

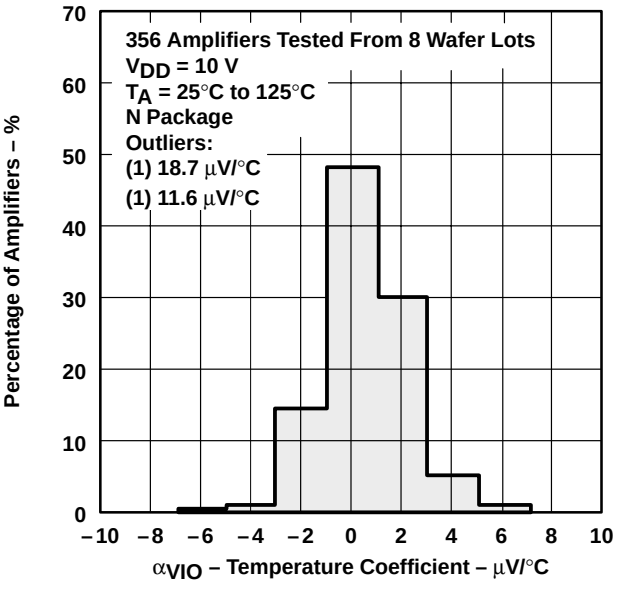
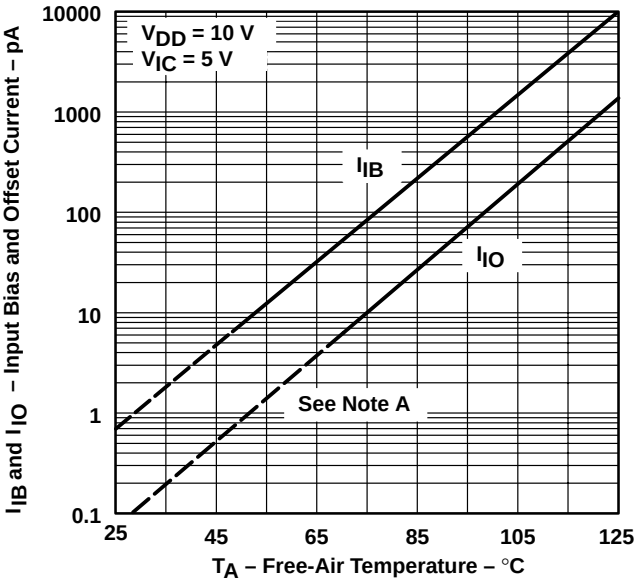


Figure 6

TYPICAL CHARACTERISTICS

INPUT BIAS AND OFFSET CURRENT† vs FREE-AIR TEMPERATURE



NOTE A: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

Figure 7

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT vs SUPPLY VOLTAGE

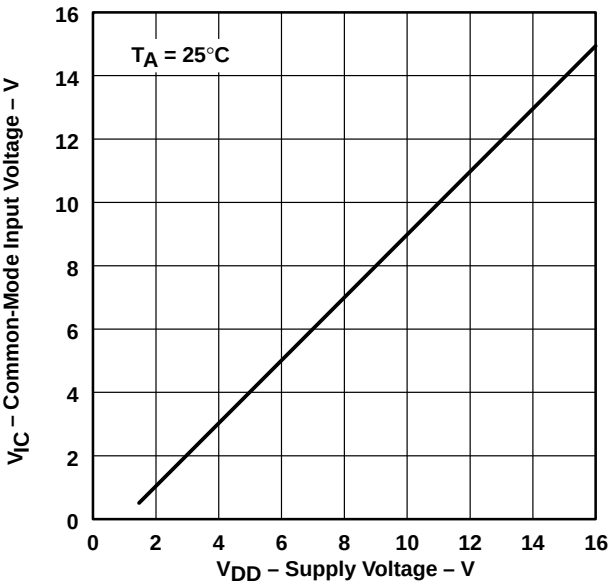


Figure 8

HIGH-LEVEL OUTPUT VOLTAGE†‡ vs HIGH-LEVEL OUTPUT CURRENT

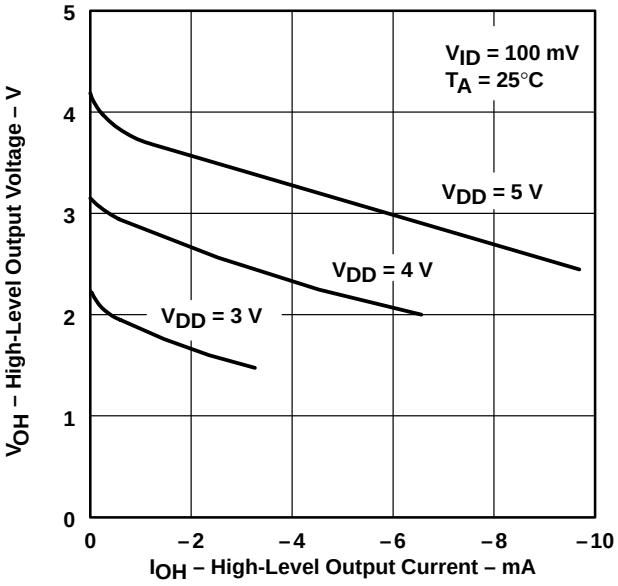


Figure 9

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

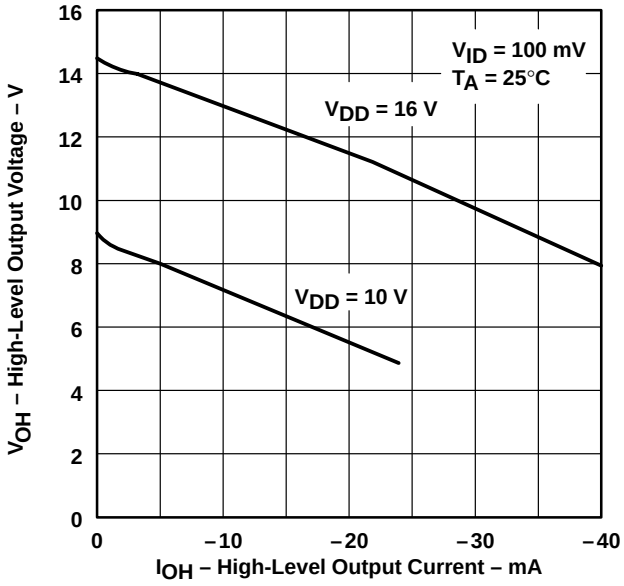


Figure 10

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
† The V_{DD} = 3 V curve does not apply to the TLC107xM.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs SUPPLY VOLTAGE

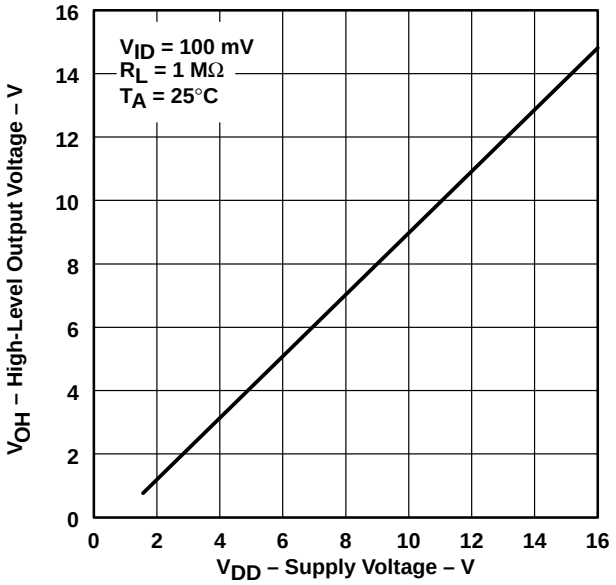


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE† vs FREE-AIR TEMPERATURE

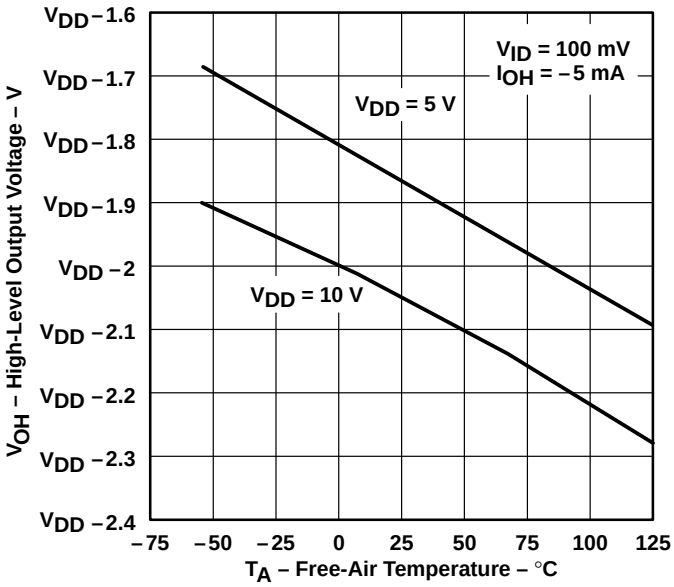


Figure 12

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

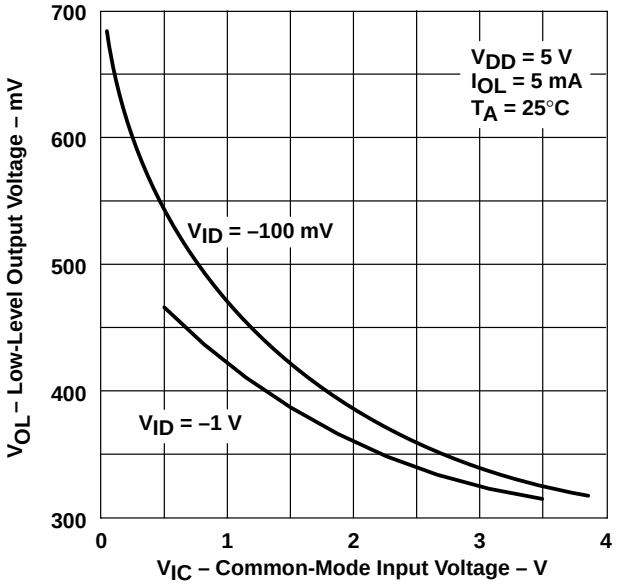


Figure 13

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

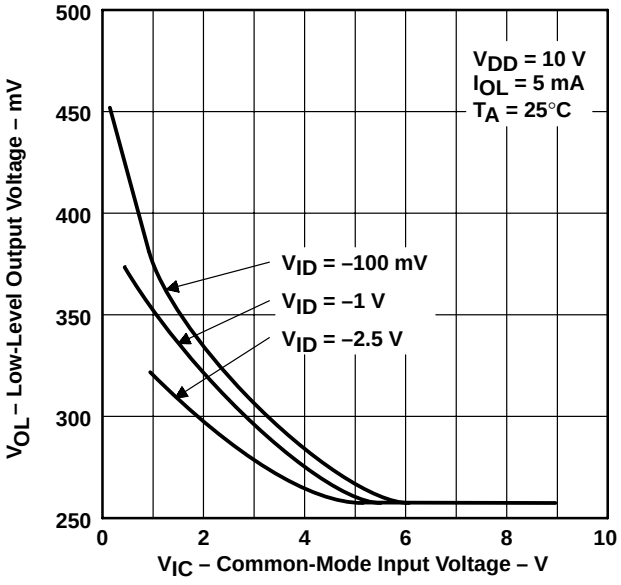


Figure 14

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs DIFFERENTIAL INPUT VOLTAGE

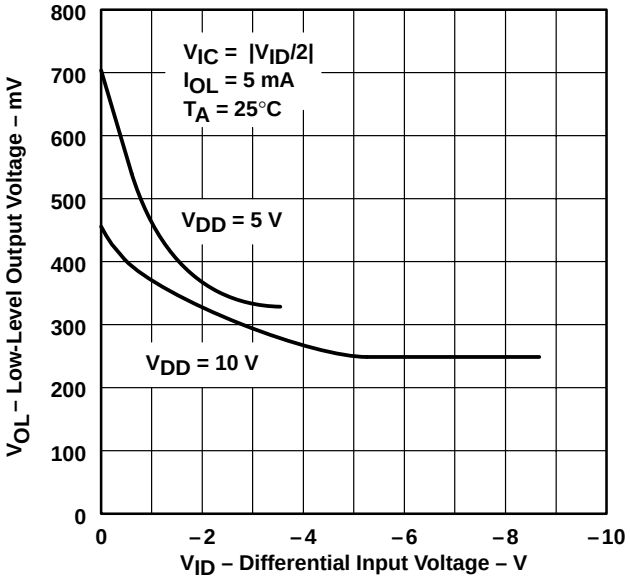


Figure 15

LOW-LEVEL OUTPUT VOLTAGE† vs FREE-AIR TEMPERATURE

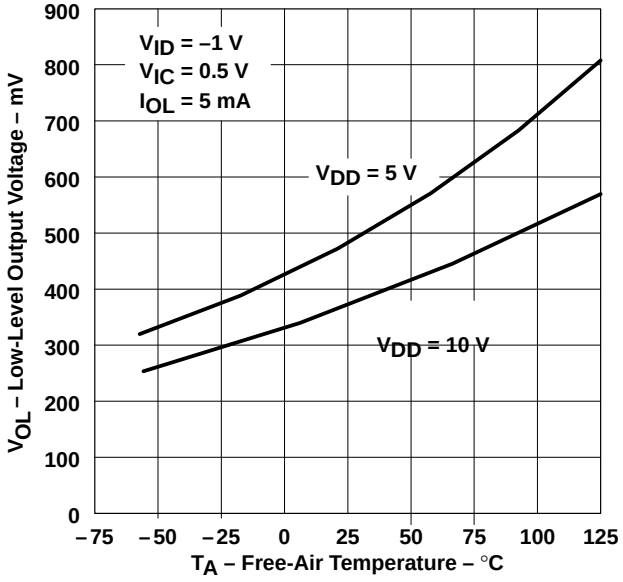


Figure 16

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

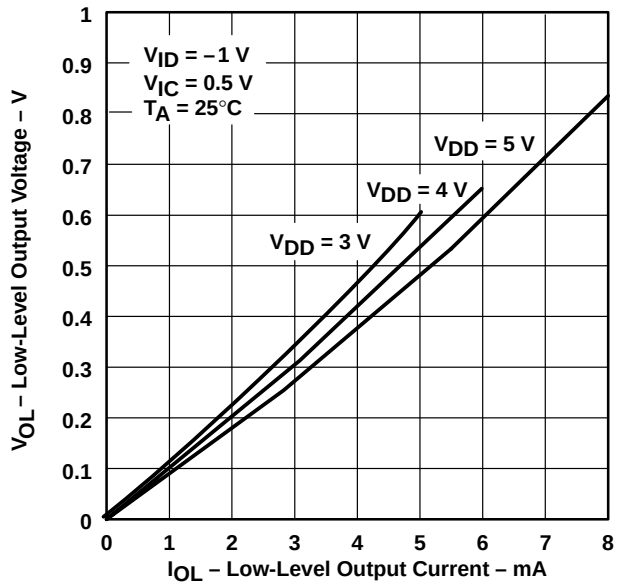


Figure 17

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

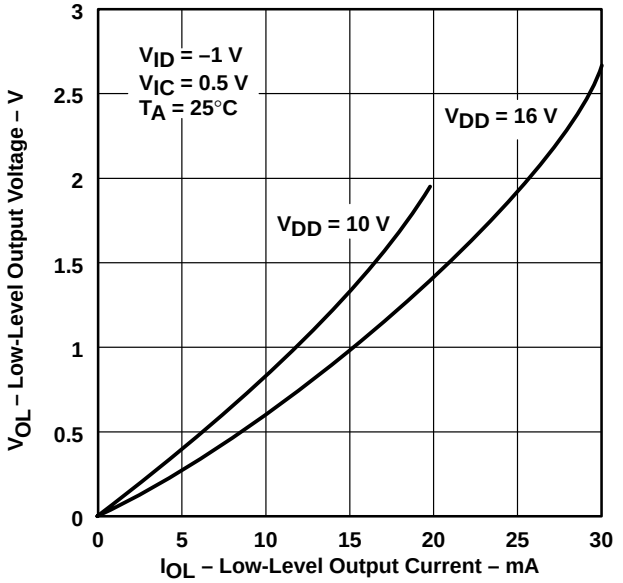


Figure 18

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION† vs SUPPLY VOLTAGE

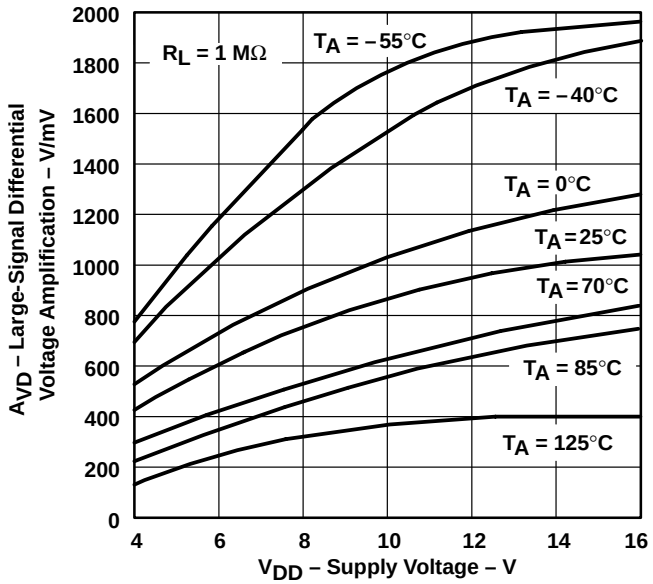


Figure 19

LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION† vs FREE-AIR TEMPERATURE

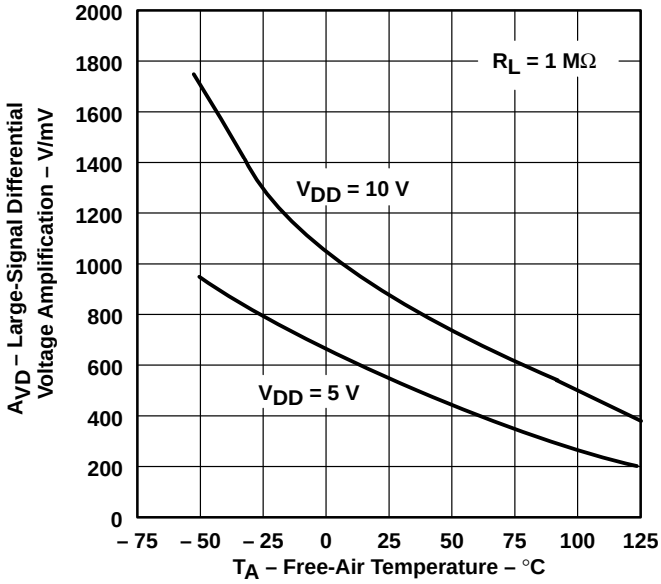


Figure 20

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

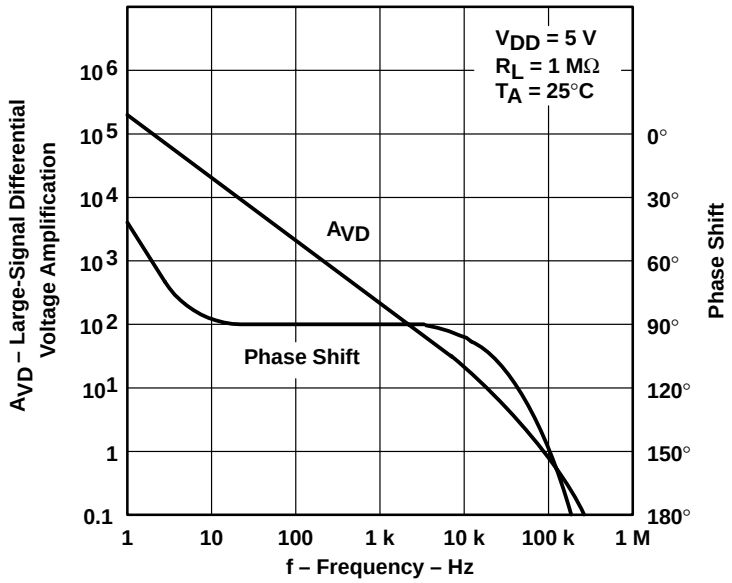


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

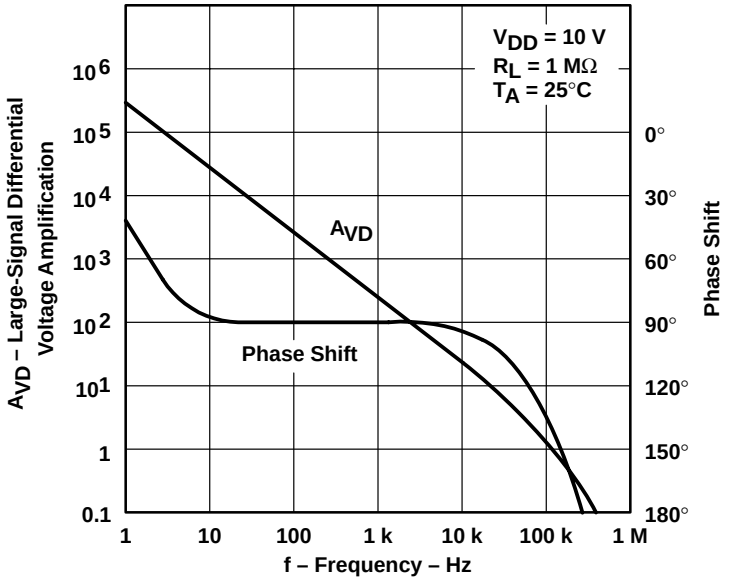


Figure 22

MAXIMUM PEAK OUTPUT VOLTAGE vs FREQUENCY

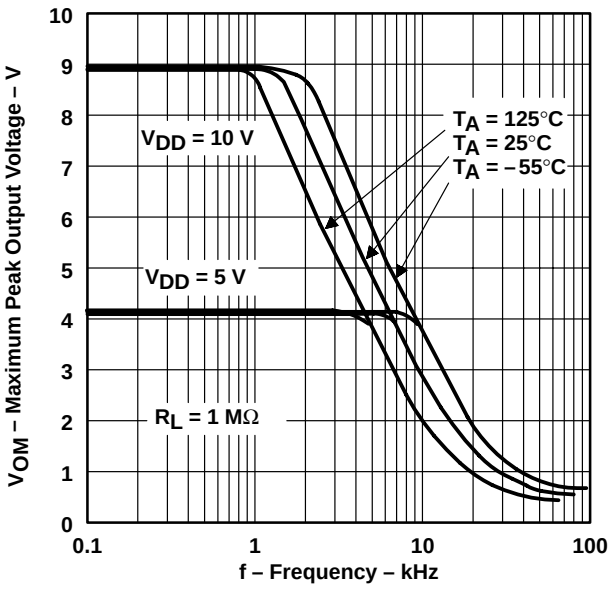


Figure 23

SUPPLY CURRENT† vs SUPPLY VOLTAGE

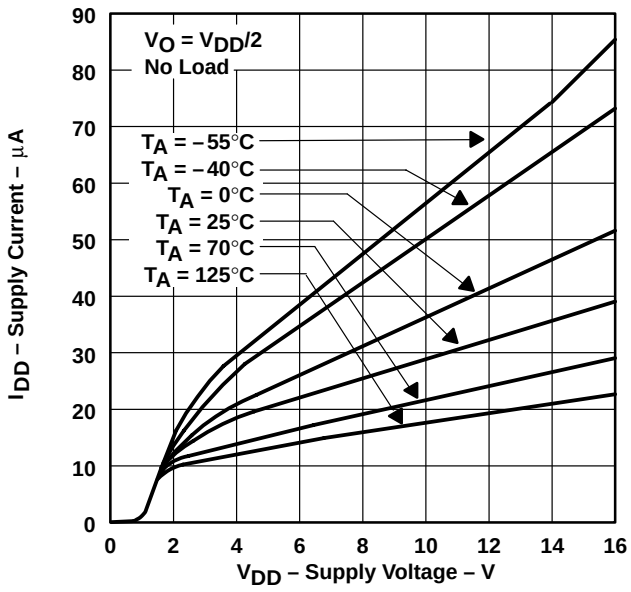


Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT† vs FREE-AIR TEMPERATURE

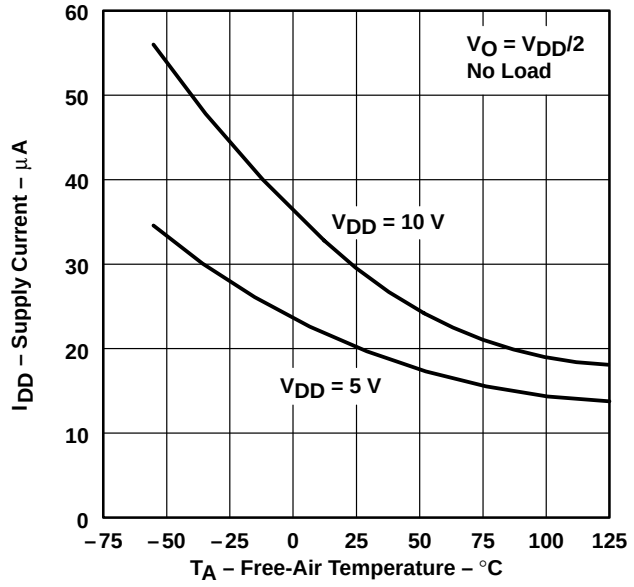


Figure 25

SLEW RATE vs SUPPLY VOLTAGE

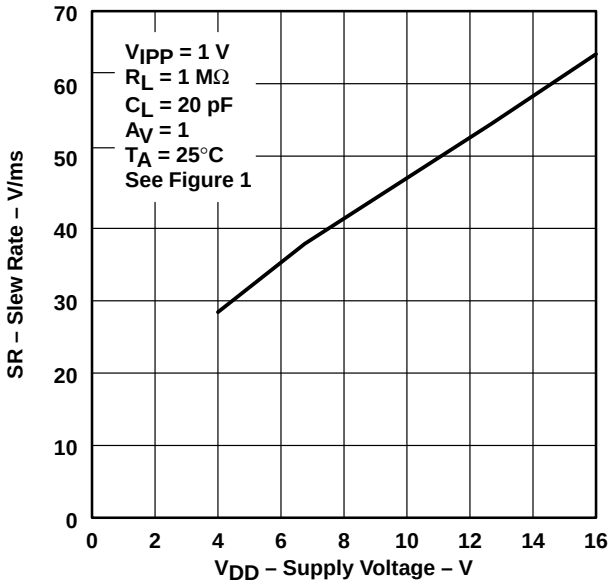


Figure 26

SLEW RATE† vs FREE-AIR TEMPERATURE

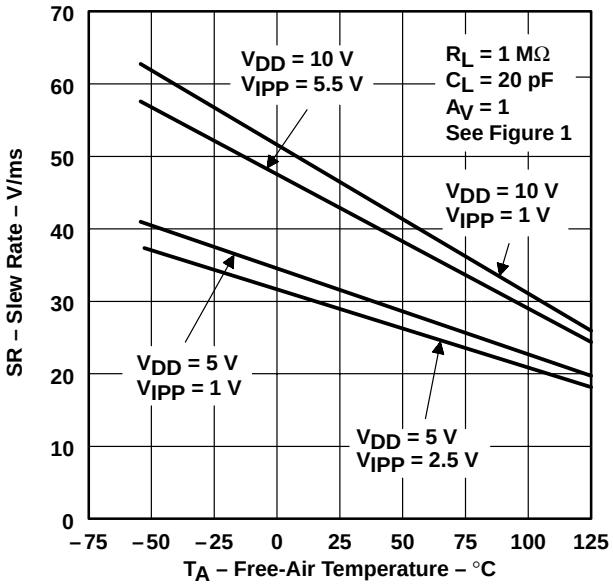


Figure 27

NORMALIZED SLEW RATE† vs FREE-AIR TEMPERATURE

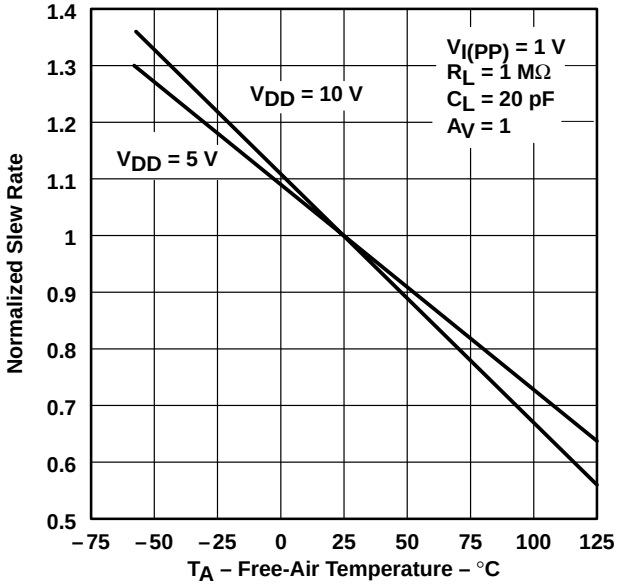


Figure 28

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

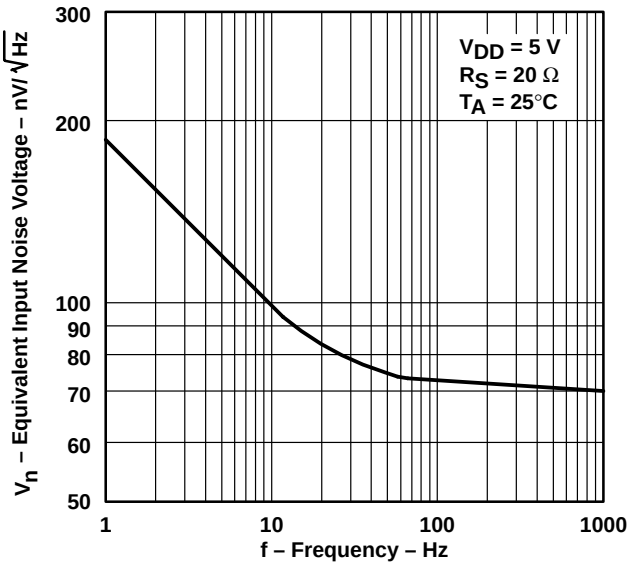


Figure 29

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

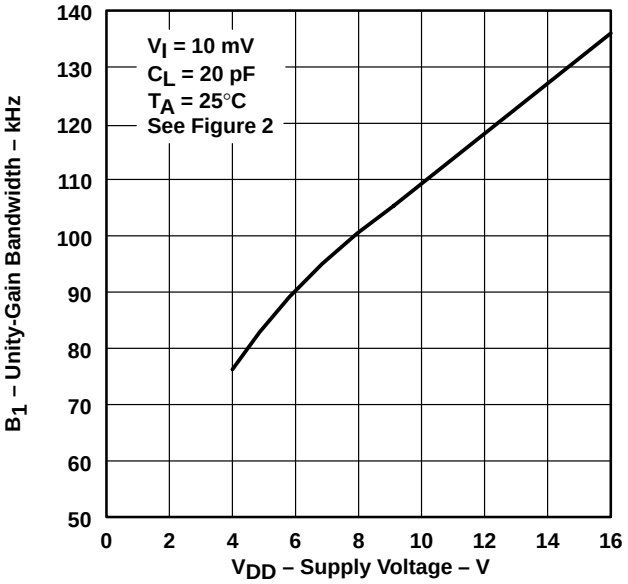


Figure 30

UNITY-GAIN BANDWIDTH†
vs
FREE-AIR TEMPERATURE

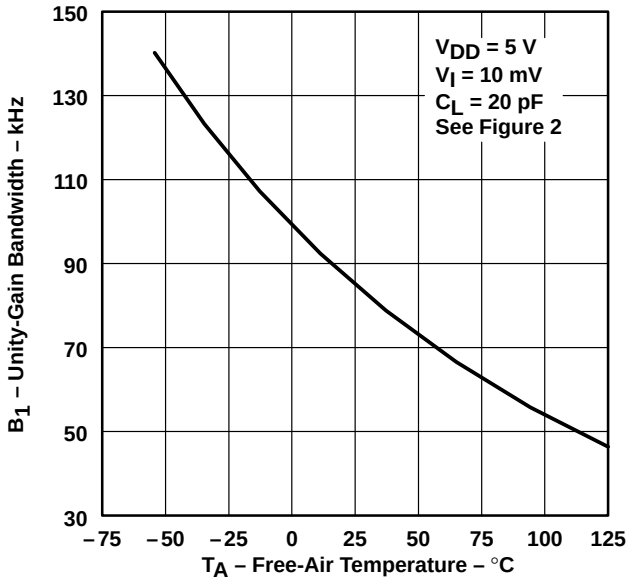


Figure 31

PHASE MARGIN
vs
SUPPLY VOLTAGE

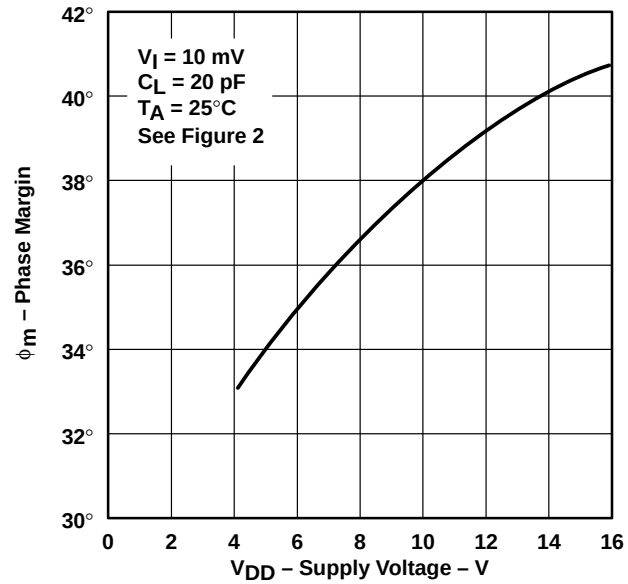


Figure 32

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

PHASE MARGIN† vs FREE-AIR TEMPERATURE

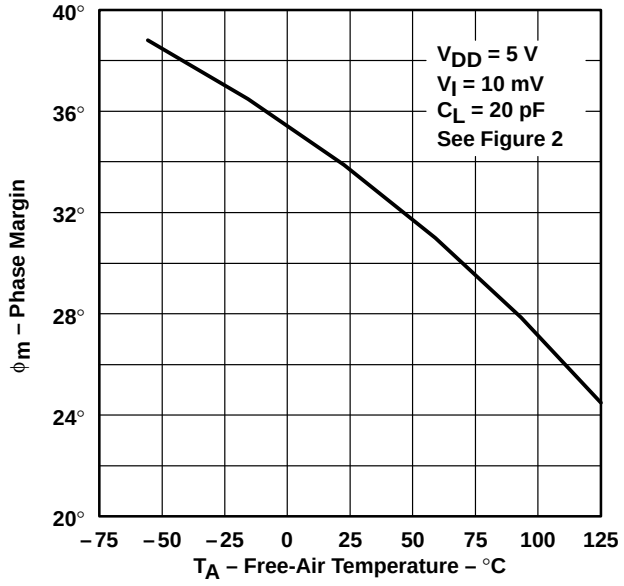


Figure 33

PHASE MARGIN vs CAPACITIVE LOAD

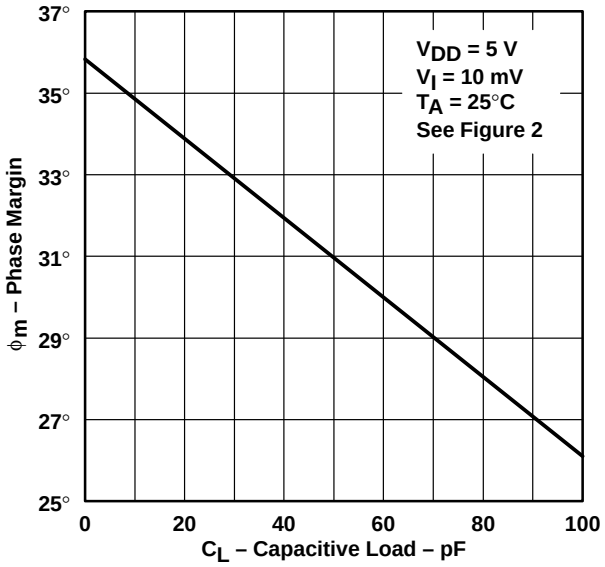


Figure 34

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLC1078CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1078C
TLC1078CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1078C
TLC1078CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1078C
TLC1078CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	1078C
TLC1078CP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC1078CP
TLC1078CP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC1078CP
TLC1078ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1078I
TLC1078ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1078I
TLC1078IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1078I
TLC1078IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1078I
TLC1078IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC1078IP
TLC1078IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	TLC1078IP
TLC1079CD	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC1079C
TLC1079CD.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC1079C
TLC1079CDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	TLC1079C
TLC1079CDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC1079C
TLC1079CN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLC1079CN
TLC1079CN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC1079CN
TLC1079ID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-	TLC1079I
TLC1079ID.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC1079I
TLC1079IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	TLC1079I
TLC1079IDR.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC1079I
TLC1079IN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-	TLC1079IN
TLC1079IN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	TLC1079IN

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

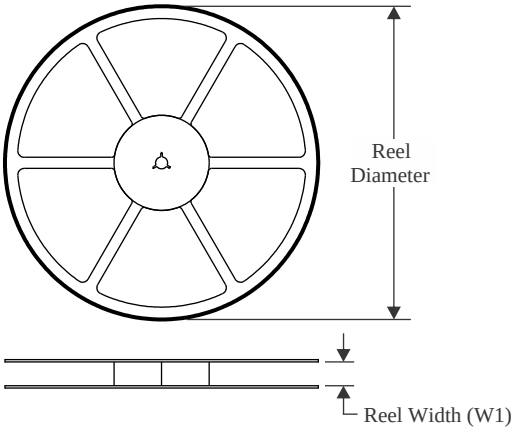
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

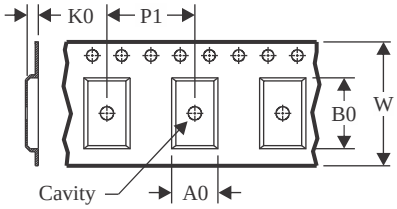
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

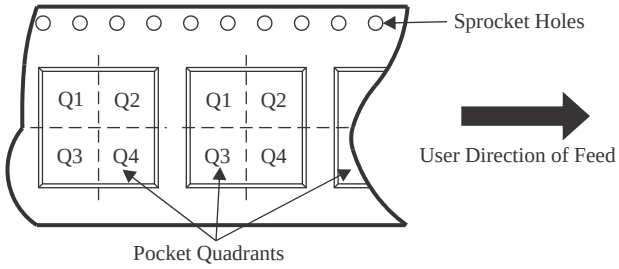


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

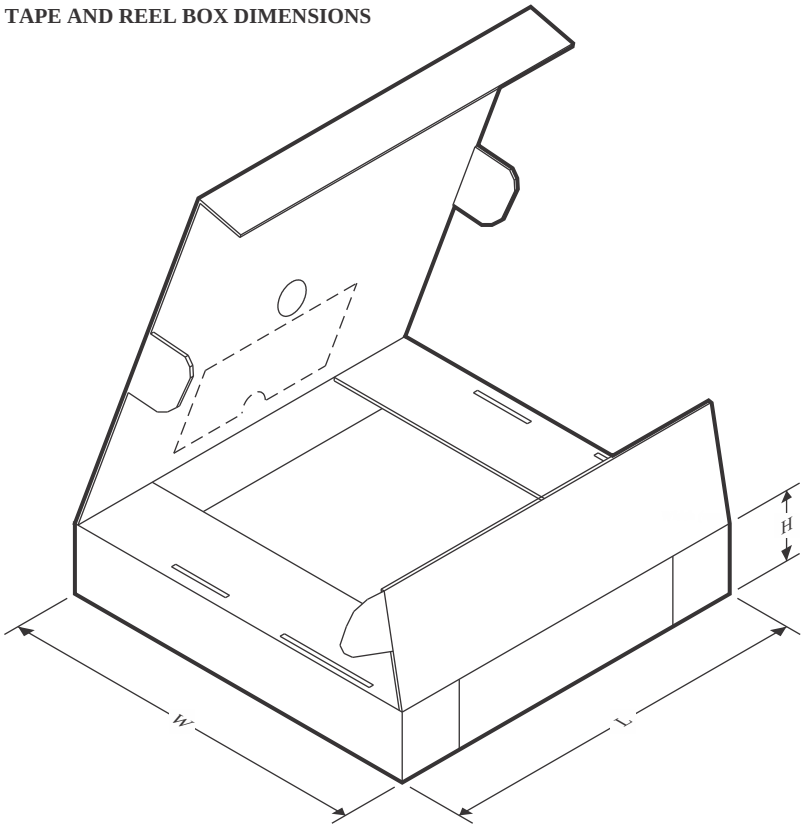
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC1078CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC1078IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC1079CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC1079IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

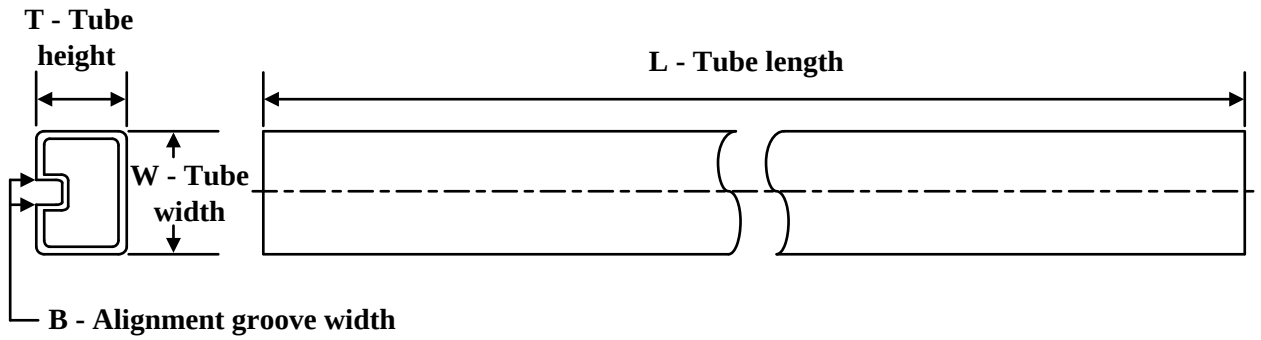
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

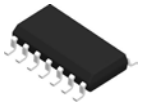
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC1078CDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC1078IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLC1079CDR	SOIC	D	14	2500	350.0	350.0	43.0
TLC1079IDR	SOIC	D	14	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC1078CD	D	SOIC	8	75	507	8	3940	4.32
TLC1078CD	D	SOIC	8	75	505.46	6.76	3810	4
TLC1078CD.A	D	SOIC	8	75	507	8	3940	4.32
TLC1078CD.A	D	SOIC	8	75	505.46	6.76	3810	4
TLC1078CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC1078CP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC1078ID	D	SOIC	8	75	505.46	6.76	3810	4
TLC1078ID	D	SOIC	8	75	507	8	3940	4.32
TLC1078ID.A	D	SOIC	8	75	505.46	6.76	3810	4
TLC1078ID.A	D	SOIC	8	75	507	8	3940	4.32
TLC1078IP	P	PDIP	8	50	506	13.97	11230	4.32
TLC1078IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLC1079CD	D	SOIC	14	50	505.46	6.76	3810	4
TLC1079CD.A	D	SOIC	14	50	505.46	6.76	3810	4
TLC1079CN	N	PDIP	14	25	506	13.97	11230	4.32
TLC1079CN.A	N	PDIP	14	25	506	13.97	11230	4.32
TLC1079ID	D	SOIC	14	50	505.46	6.76	3810	4
TLC1079ID.A	D	SOIC	14	50	505.46	6.76	3810	4
TLC1079IN	N	PDIP	14	25	506	13.97	11230	4.32
TLC1079IN.A	N	PDIP	14	25	506	13.97	11230	4.32

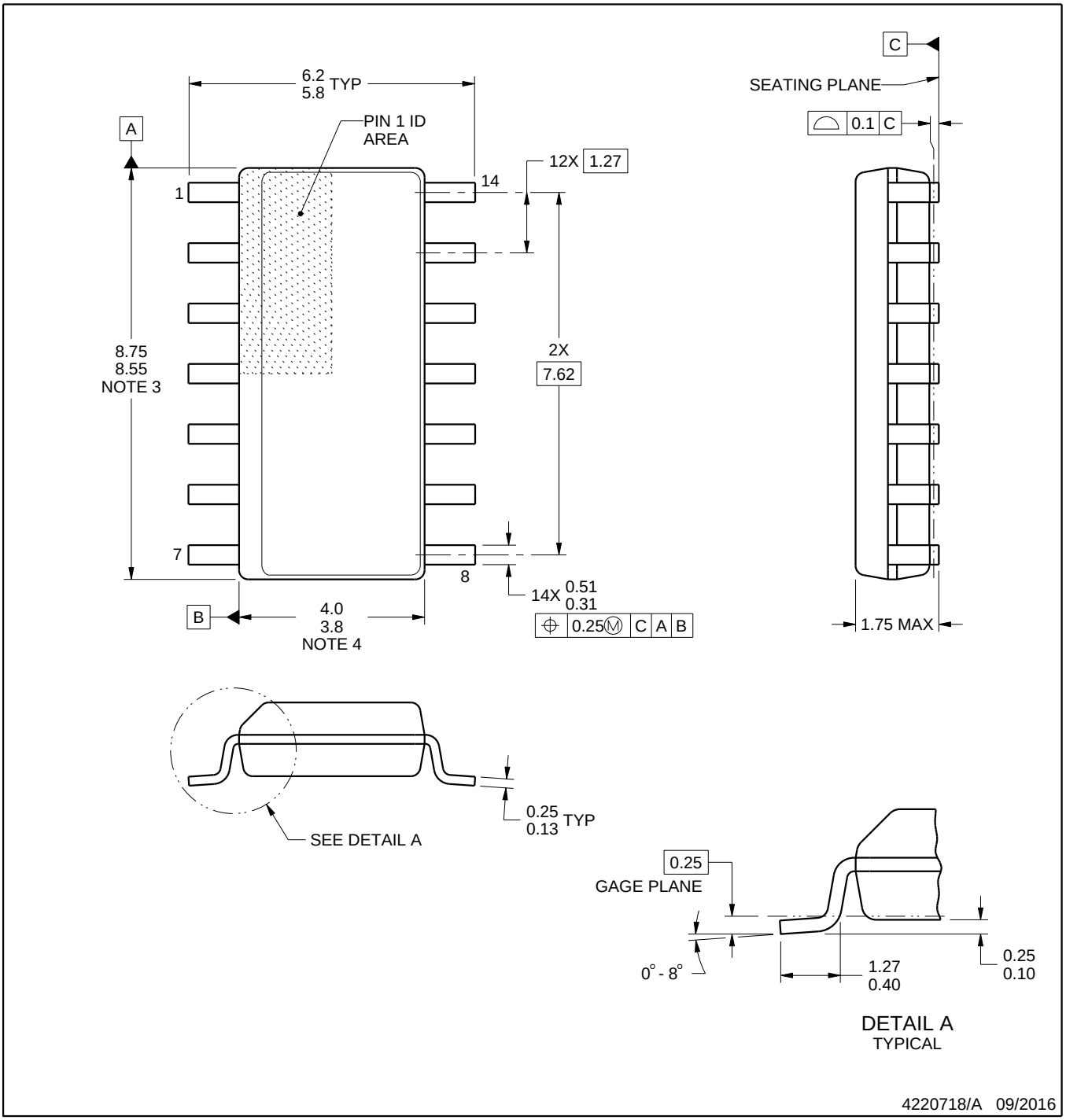


PACKAGE OUTLINE

D0014A

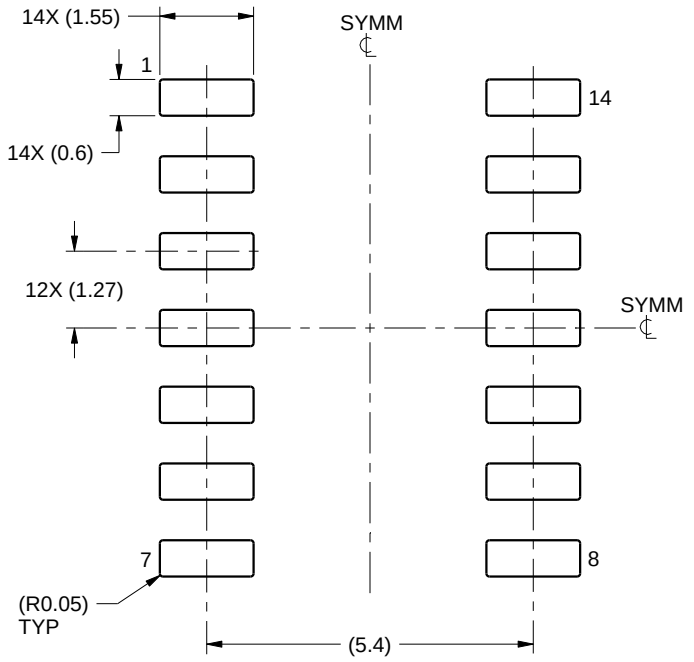
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

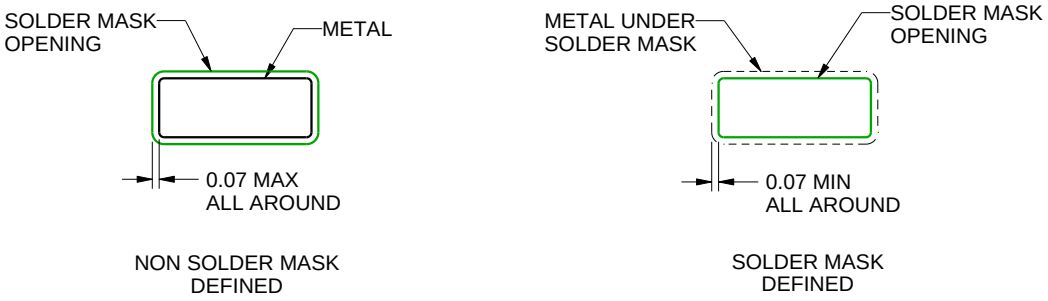


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

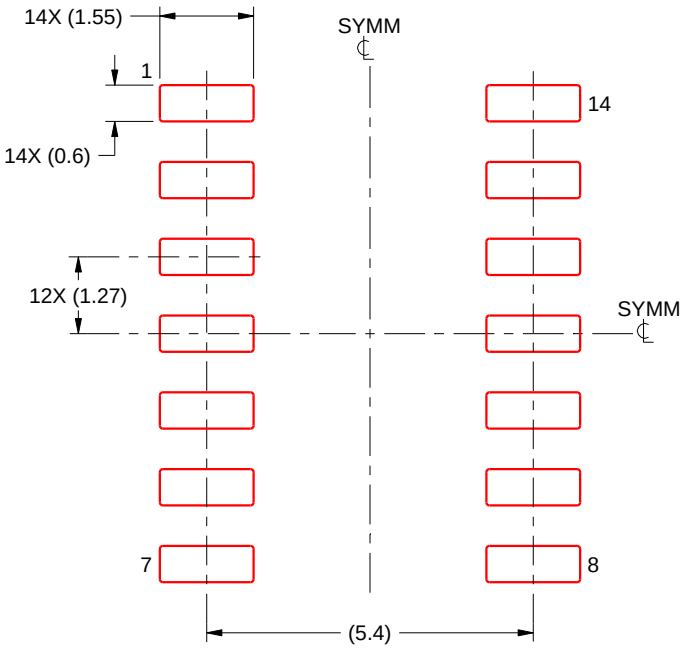
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

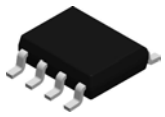


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

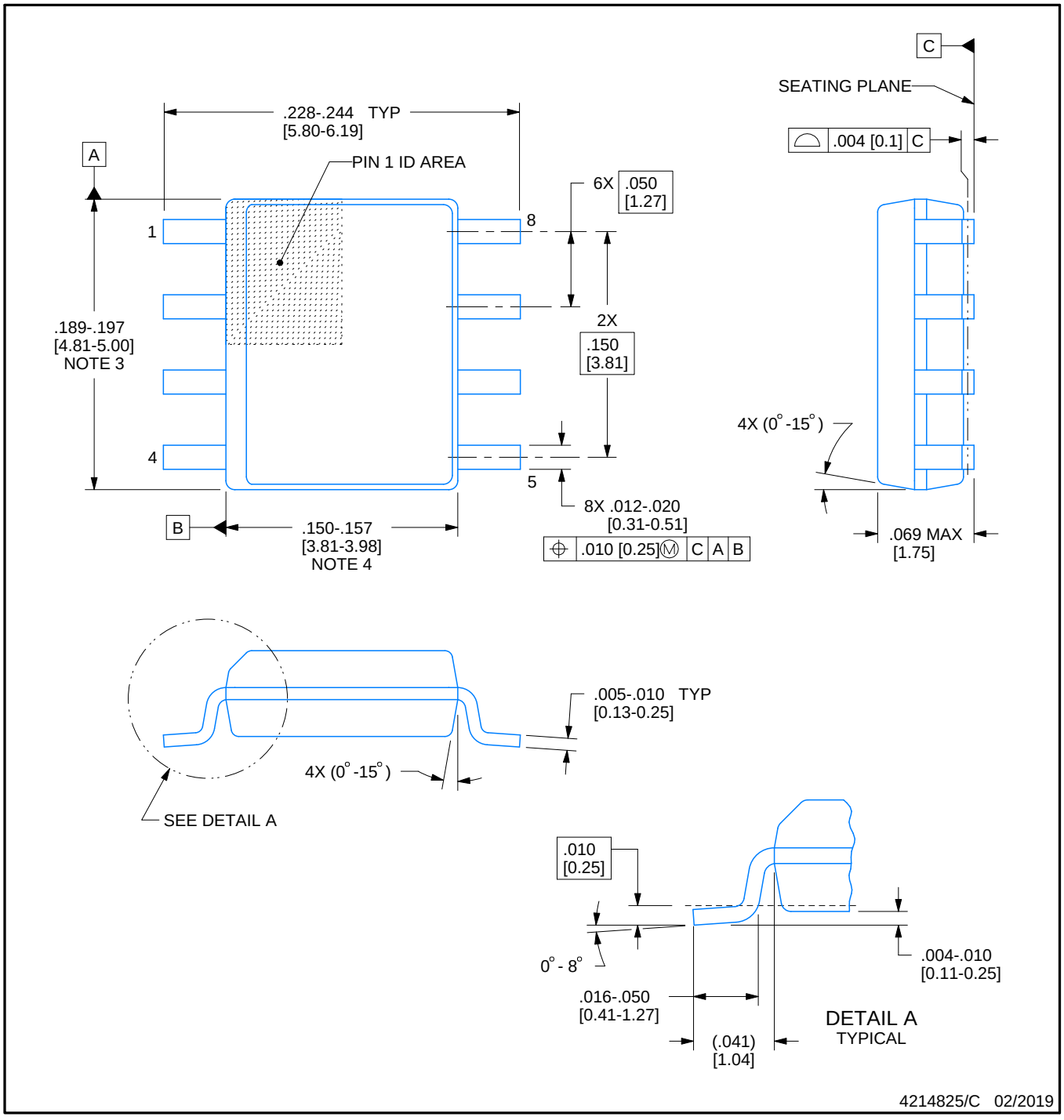


PACKAGE OUTLINE

D0008A

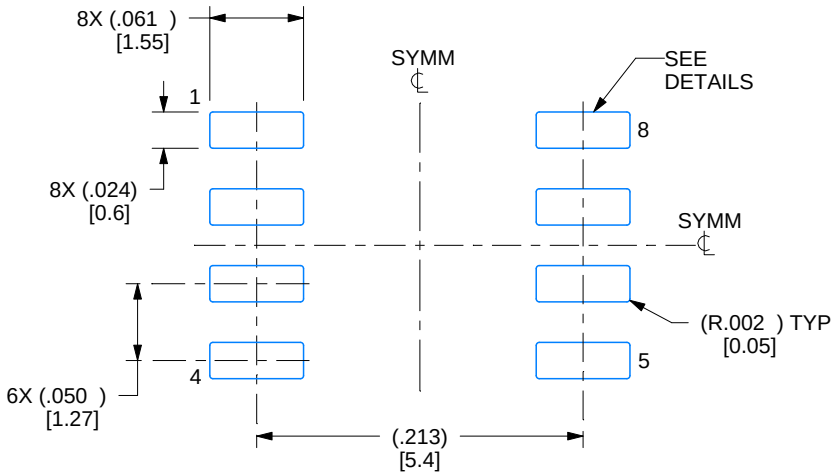
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

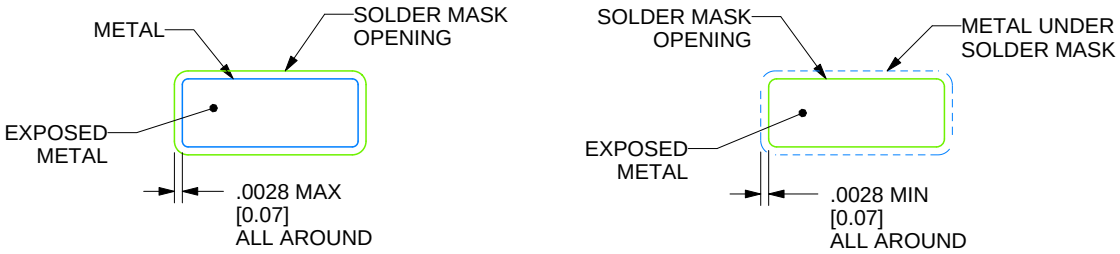


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

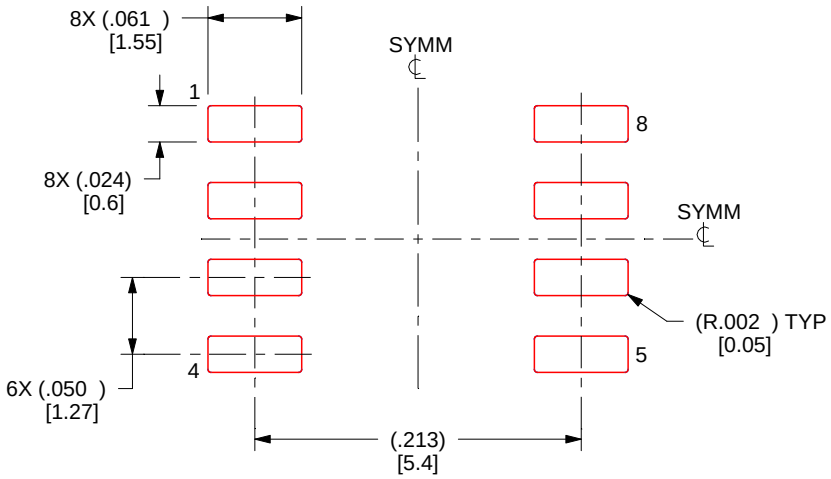
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



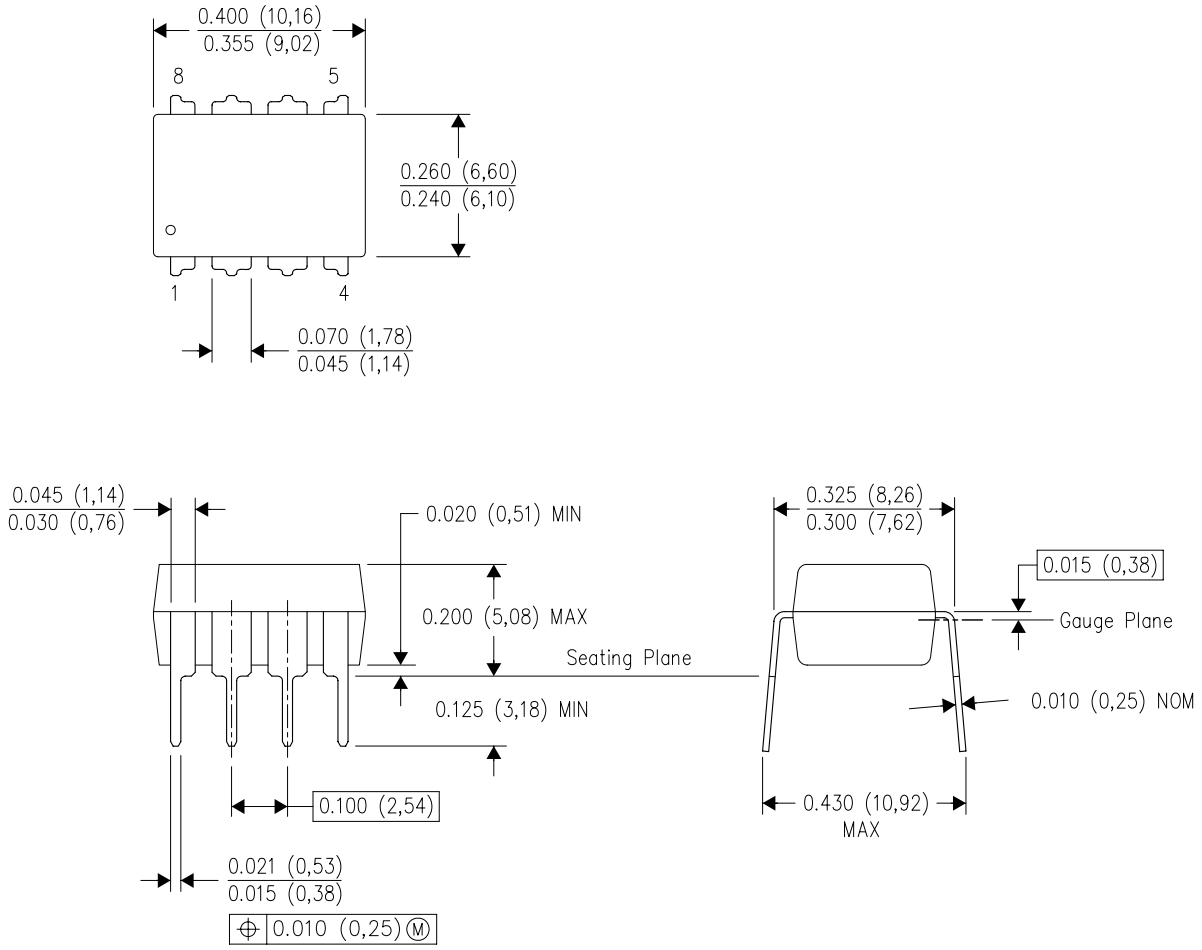
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

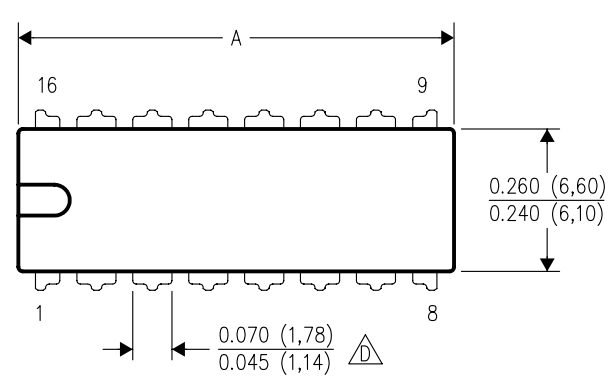


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

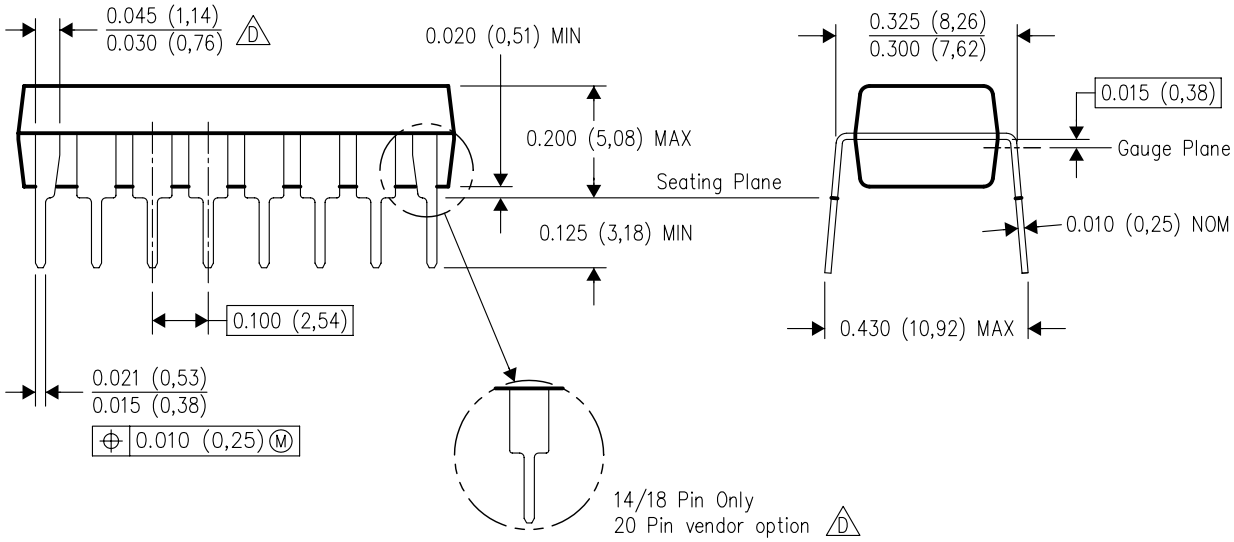
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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