

## TLC69699 SPI-Compatible Connectivity for TLC696xx Device Family

### 1 Features

- Operating voltage  $V_{CC}$  range: 2.5V to 5.5V
- SPI peripheral
  - Data transfer rate up to 20MHz
  - Support multiple peripherals with one controller
- Continuous Clock Serial Interface (CCSI) Controller and Peripheral
  - Data transfer rate up to 20MHz
  - Programmable clock jitter for EMI enhancement
- Diagnostics
  - Open-drain FAULT pin
  - SPI communication loss detection
  - CRC for SPI communication
  - Continuous clock watchdog
  - CCSI data integrity
- Data ready interrupt for availability of data

### 2 Applications

- SPI compatible connectivity for TLC696x0/1/2/4/8

### 3 Description

The TLC69699 SPI-compatible connectivity enables TLC696xx device family to be controlled using a standard SPI controller. The device features an internal oscillator to generate the continuous clock required by the TLC696xx device family. Jitter can be added to the continuous clock for EMI enhancement. The transmitted data is aligned to the continuous clock to maintain the timing requirements of the CCSI interface.

TLC69699 incorporates reporting of faults in both the TLC696xx daisy chain and TLC69699 internal. Data transmission of register and brightness to the TLC696xx daisy chain is CRC protected by TLC69699. In addition, both the data and continuous clock lines are guarded by TLC69699 for stuck-at faults.

#### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
TLC69699	SOT-23-THN (14)	4.20mm x 2.00mm
	WSON (12)	3.00mm x 3.00mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.  
 (2) The package size (length × width) is a nominal value.

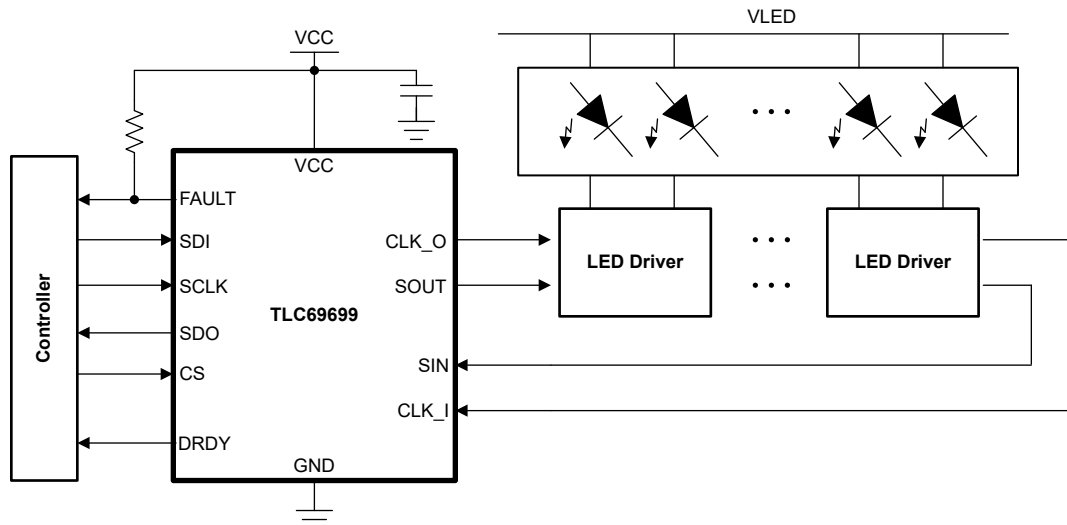


Figure 3-1. Typical Application Diagram



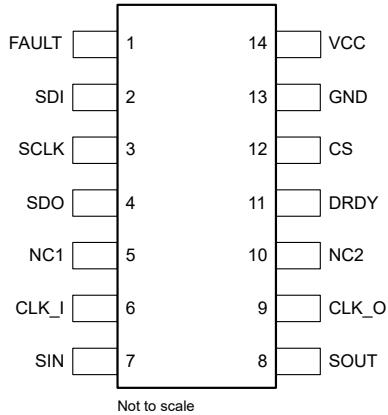
## Table of Contents

<b>1 Features</b> .....	1	6.4 Support Resources.....	4
<b>2 Applications</b> .....	1	6.5 Trademarks.....	4
<b>3 Description</b> .....	1	6.6 Electrostatic Discharge Caution.....	4
<b>4 Device Comparison</b> .....	3	6.7 Glossary.....	4
<b>5 Pin Configuration and Functions</b> .....	3	<b>7 Revision History</b> .....	4
<b>6 Device and Documentation Support</b> .....	4	<b>8 Mechanical, Packaging, and Orderable Information</b> ....	4
6.1 Device Support.....	4	8.1 Tape and Reel Information.....	5
6.2 Documentation Support.....	4	8.2 Mechanical Data.....	7
6.3 Receiving Notification of Documentation Updates.....	4		

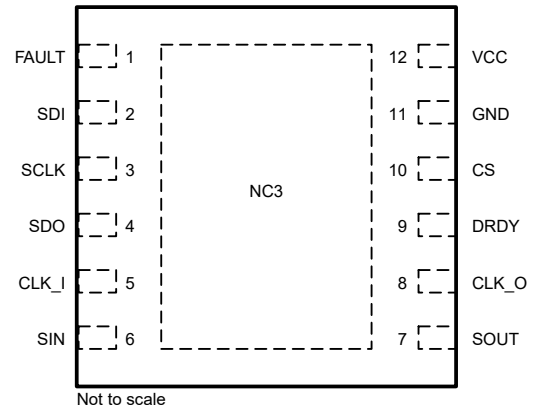
## 4 Device Comparison

PART NUMBER	MATERIAL	PACKAGE
TLC69699	TLC69699DYR	SOT-23-THN (14)
	TLC69699DRRR	WSON (12)

## 5 Pin Configuration and Functions



**Figure 5-1. TLC69699 DYY Package 14-pin SOT-23-THN Top View**



**Figure 5-2. TLC69699 DRR Package 12-pin WSON with Exposed Thermal Pad Top View**

**Table 5-1. Pin Functions**

NAME	PIN		TYPE <sup>(1)</sup>	DESCRIPTION
	DYY NO.	DRR NO.		
FAULT	1	1	O	Fault indicator pin
SDI	2	2	I	SPI Serial Data Input
SCLK	3	3	I	SPI Serial Clock Input
SDO	4	4	O	SPI Serial Data Output
NC1	5	-	NC	No connection. Can be used for signal routing.
CLK_I	6	5	I	CCSI continuous clock input
SIN	7	6	I	CCSI Serial Data Input
SOUT	8	7	O	CCSI Serial Data Output
CLK_O	9	8	O	CCSI Serial Clock Output
NC2	10	-	NC	No connection. Can be used for signal routing.
DRDY	11	9	O	Data ready interrupt.
CS	12	10	I	SPI Chip Select
GND	13	11	G	Ground pin (must connect to Ground)
VCC	14	12	P	VCC Power Supply Input
NC3	-	Exposed Pad	NC	No connection. Need to be electrically isolated from any signal except Ground.

(1) I = Input, O = Output, G = Ground, P = Power, NC = Not Connected.

## 6 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 6.1 Device Support

### 6.2 Documentation Support

#### 6.2.1 Related Documentation

### 6.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 6.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 6.5 Trademarks

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### 6.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 6.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 7 Revision History

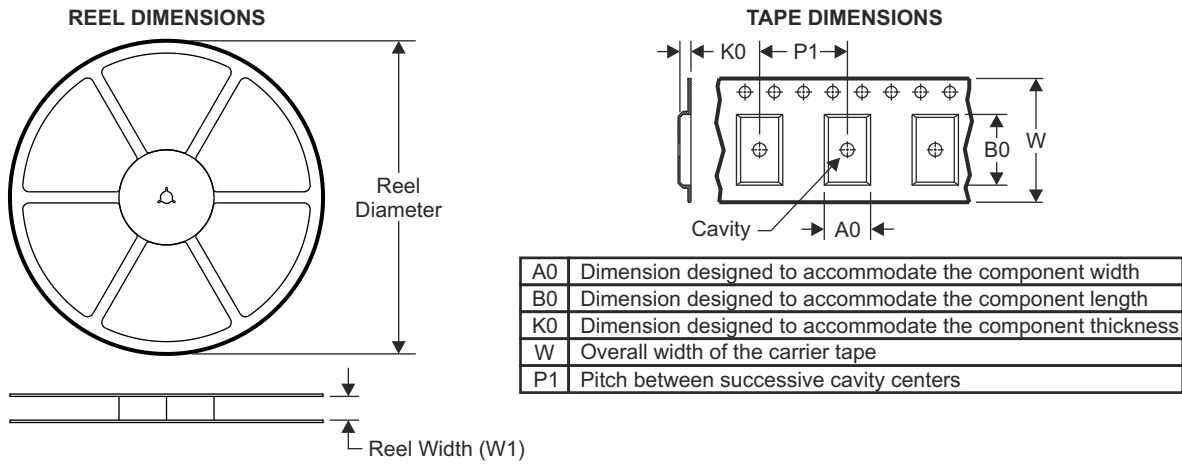
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2024	*	Initial Release

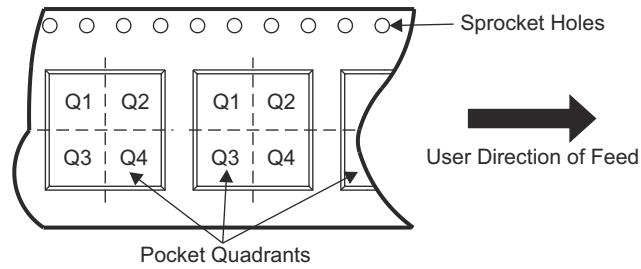
## 8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 8.1 Tape and Reel Information

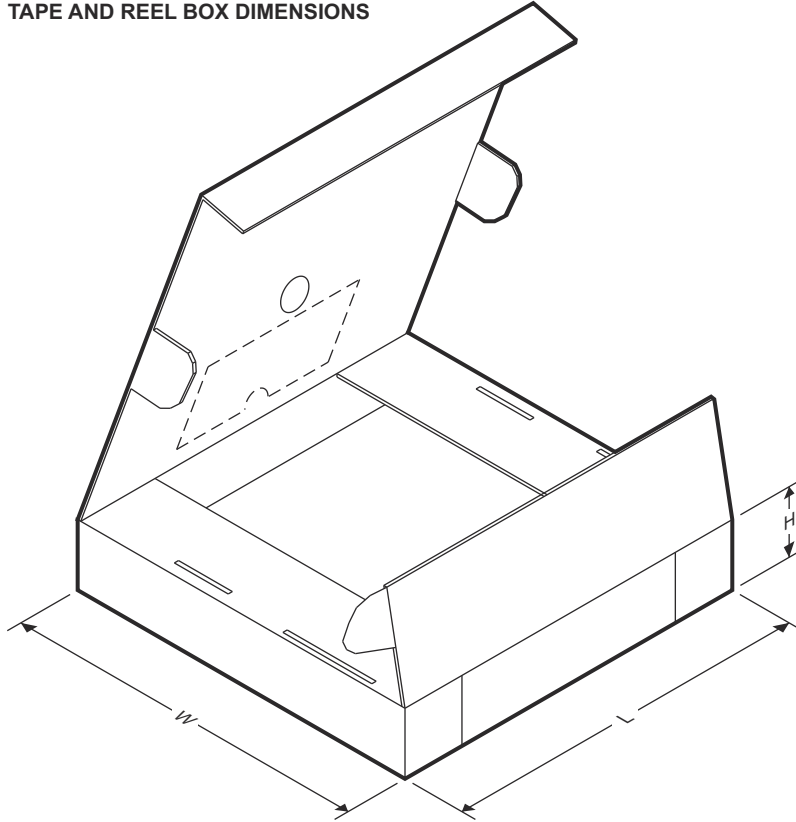


### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC69699DYYR	SOT-23-THN	DYY	14									
TLC69699DRRR	WSO	DRR	12									

**TAPE AND REEL BOX DIMENSIONS**



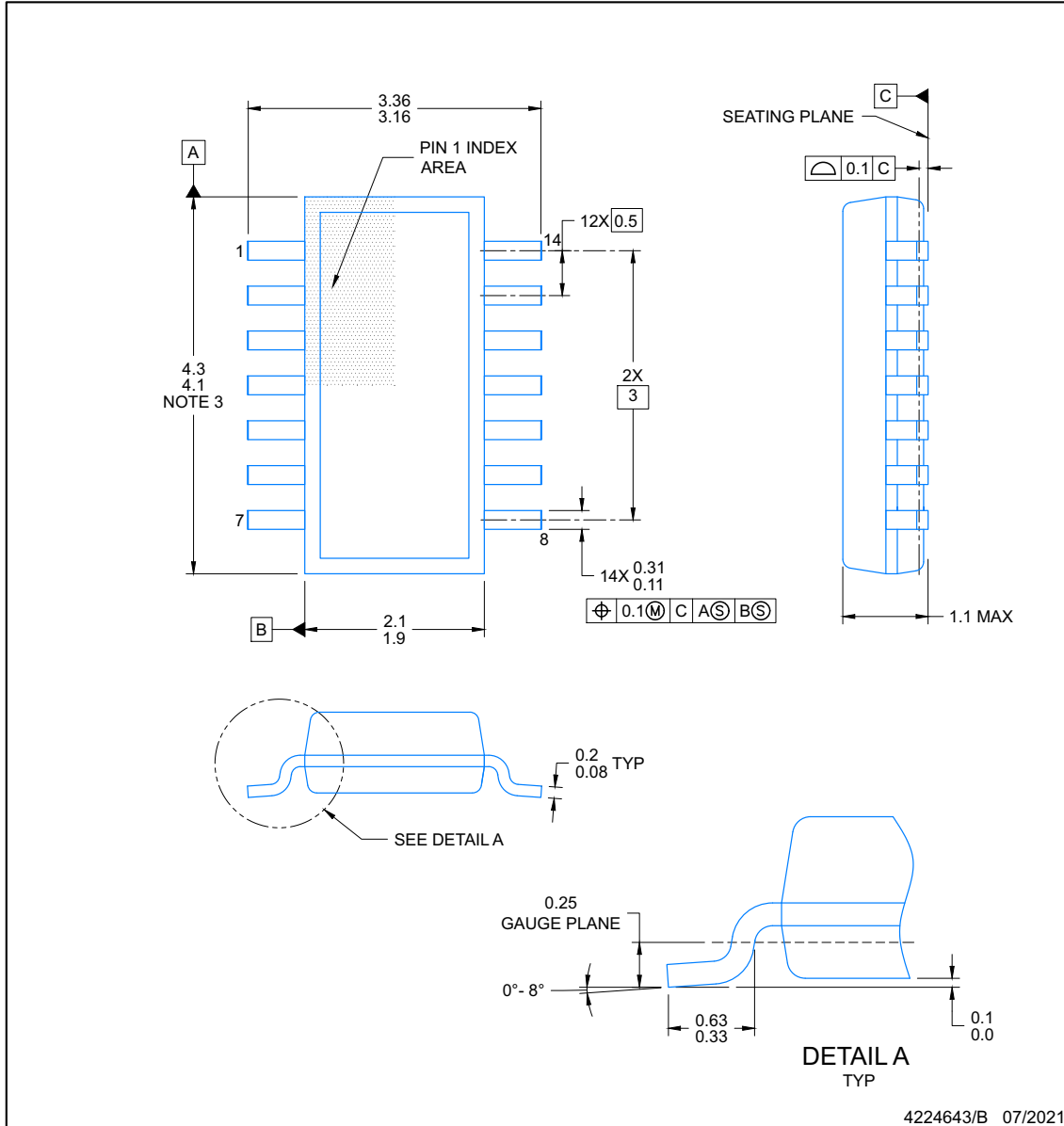
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC69699DYYR	SOT-23-THN	DYY	14				
TLC69699DRRR	WSON	DRR	12				

**8.2 Mechanical Data**

**DYY0014A**

**PACKAGE OUTLINE**  
**SOT-23-THIN - 1.1 mm max height**

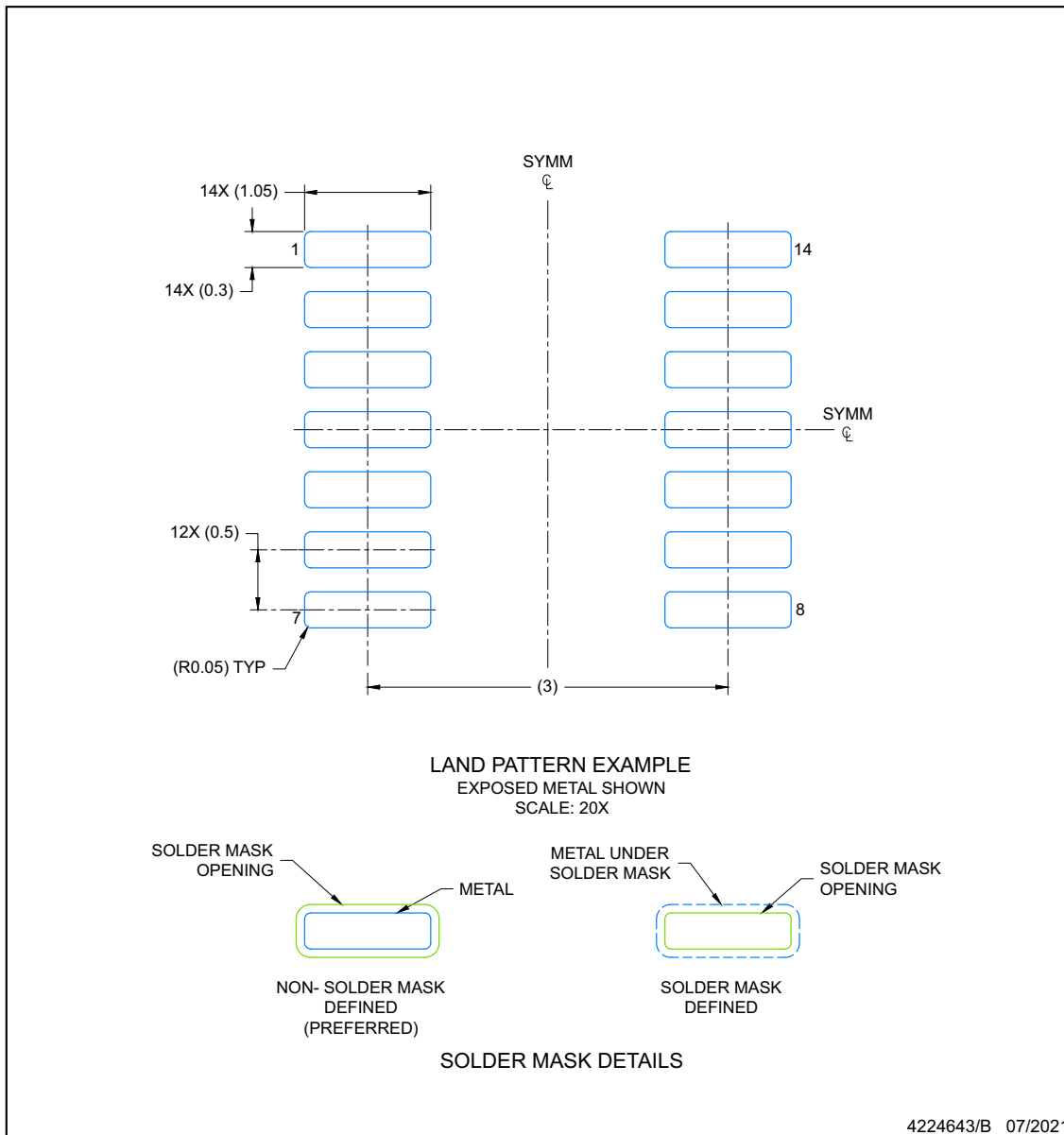
PLASTIC SMALL OUTLINE



**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB

**DYY0014A** **EXAMPLE BOARD LAYOUT**  
**SOT-23-THIN - 1.1 mm max height**  
 PLASTIC SMALL OUTLINE



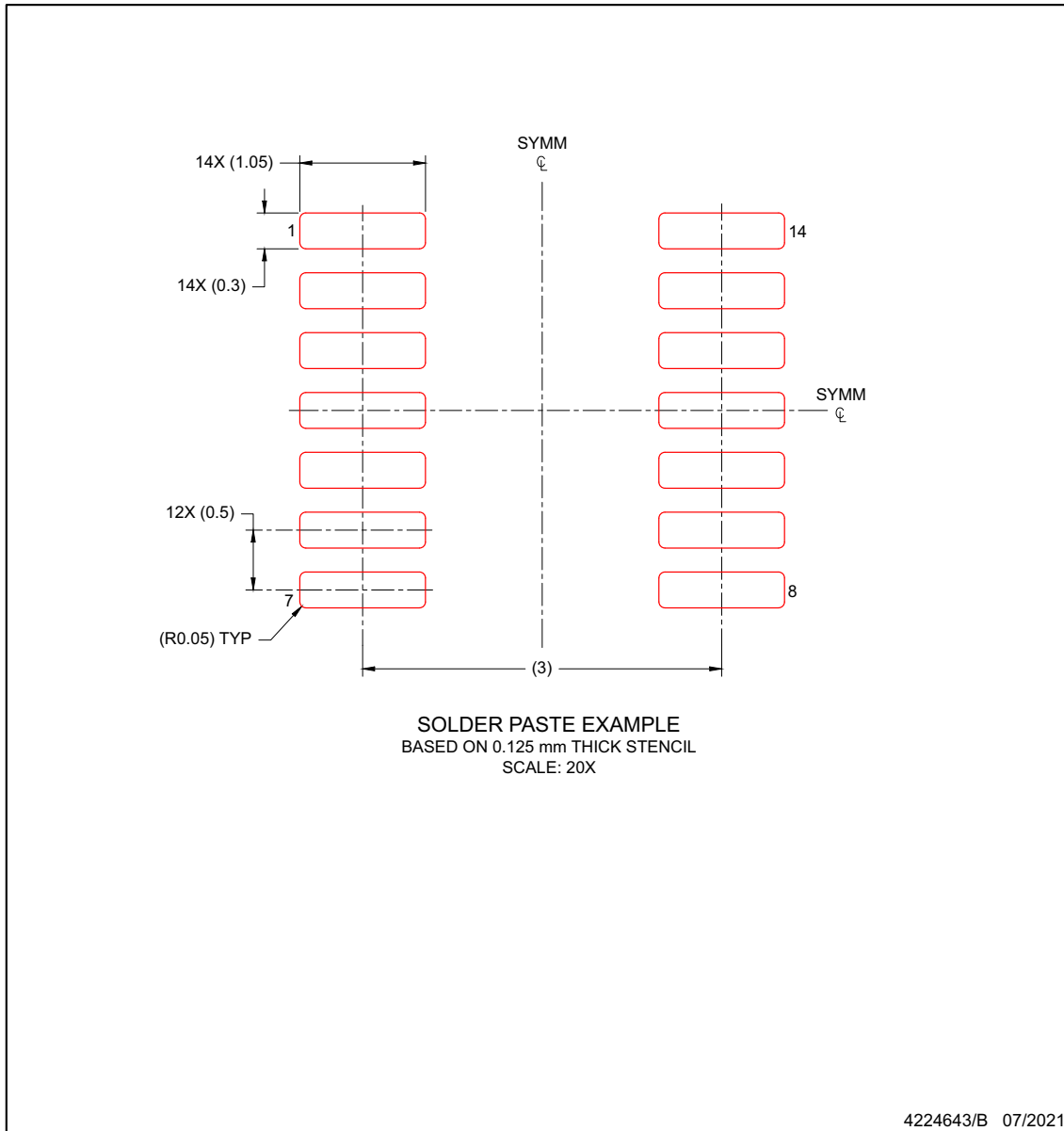
NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**EXAMPLE STENCIL DESIGN**  
**SOT-23-THIN - 1.1 mm max height**

**DYY0014A**

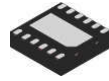
PLASTIC SMALL OUTLINE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

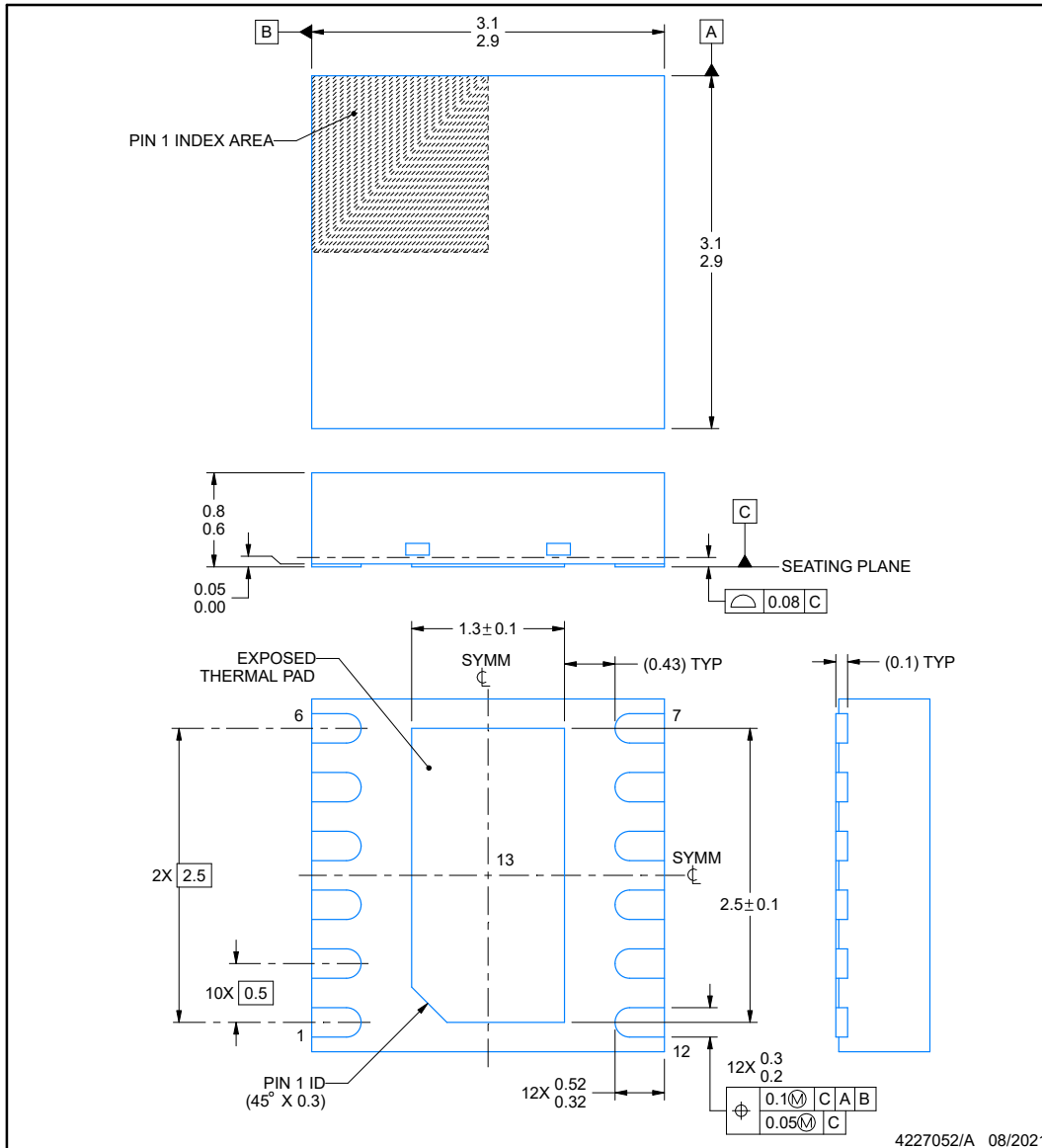
**DRR0012G**



**PACKAGE OUTLINE**

**WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



**NOTES:**

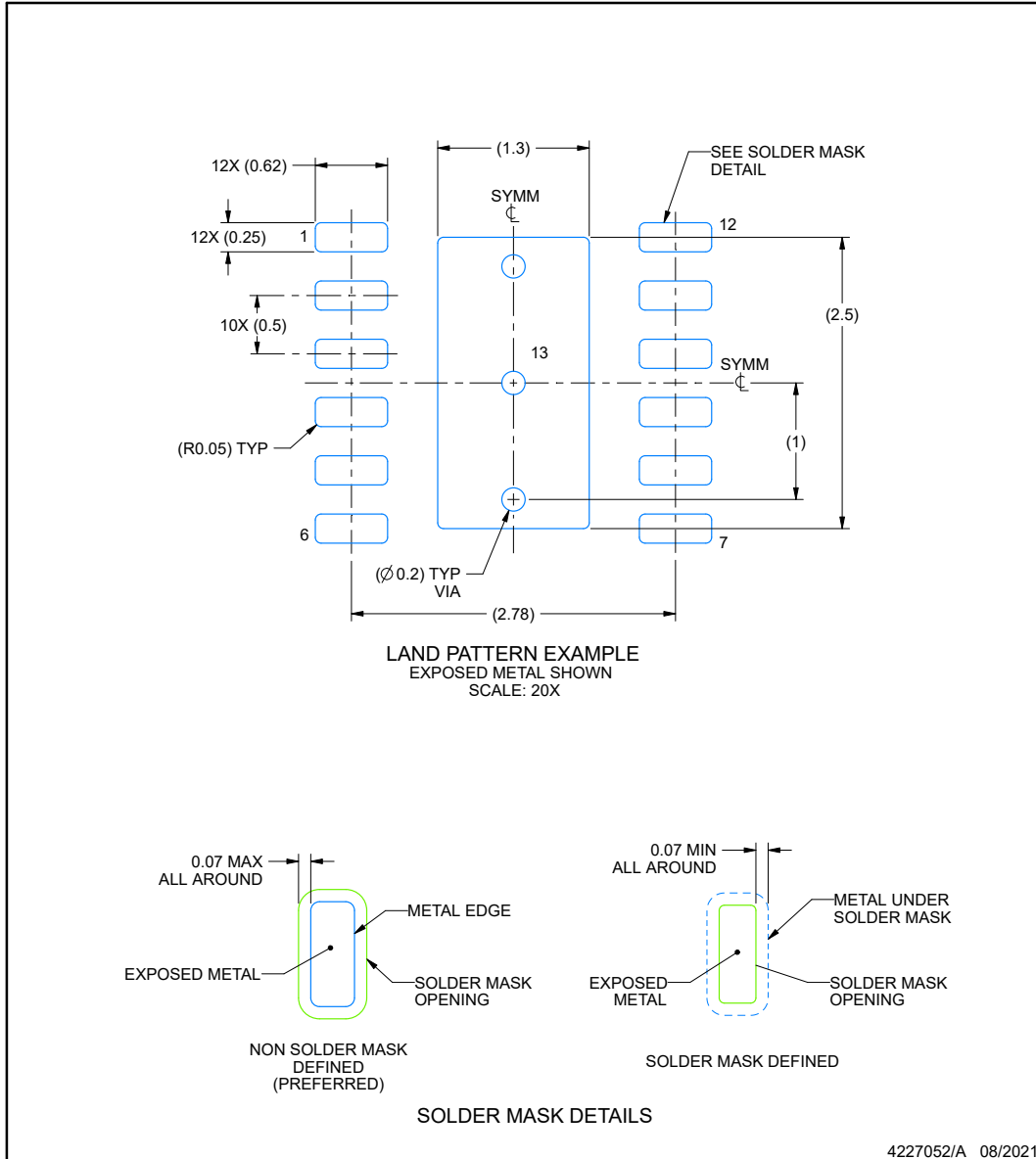
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

**EXAMPLE BOARD LAYOUT**

**DRR0012G**

**WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

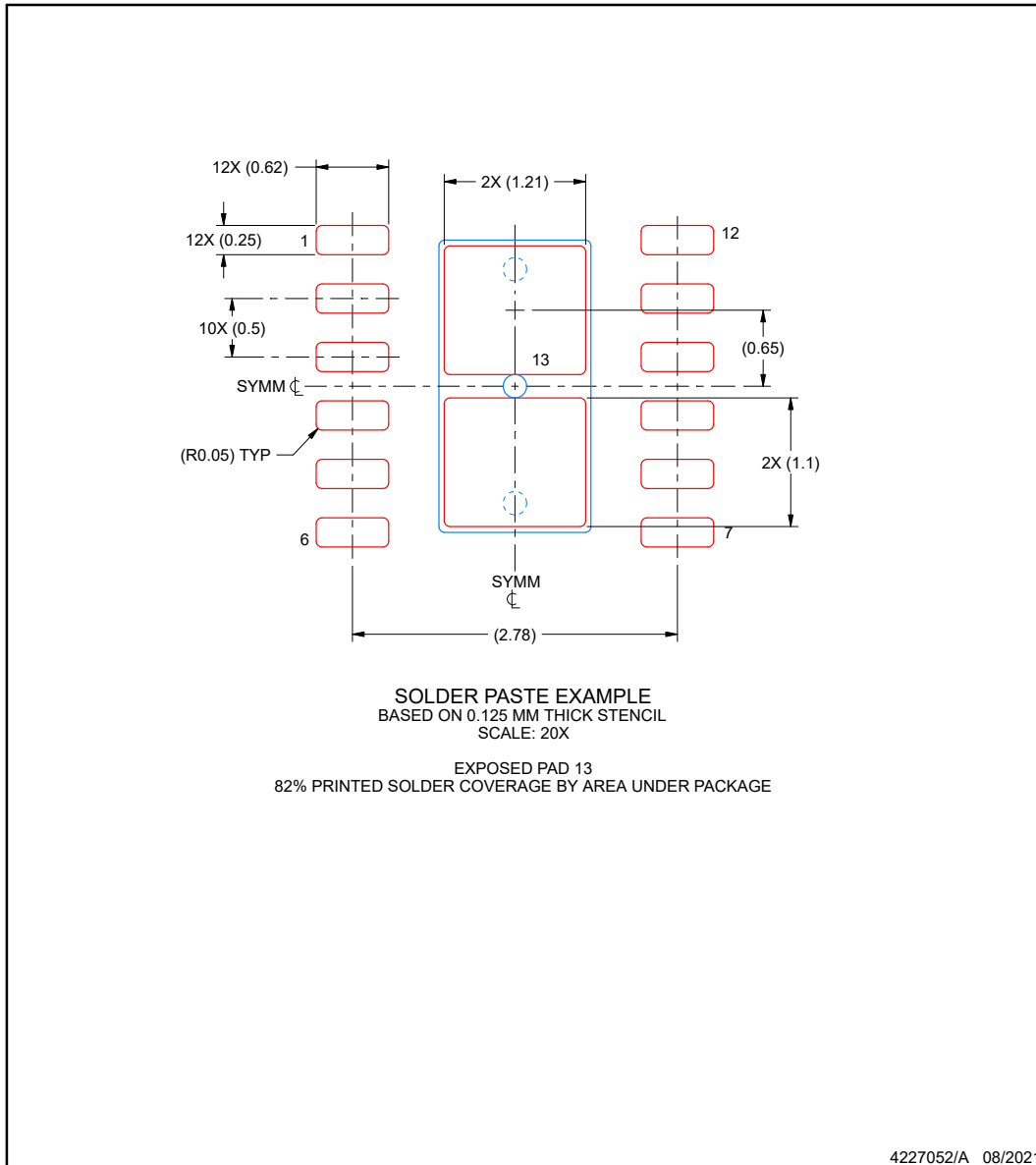
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

## EXAMPLE STENCIL DESIGN

**DRR0012G**

**WSON - 0.8 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TLC69699DRRR</a>	Active	Production	WSON (DRR)   12	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	69699N
TLC69699DRRR.A	Active	Production	WSON (DRR)   12	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	69699N
<a href="#">TLC69699DYYR</a>	Active	Production	SOT-23-THIN (DYY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	69699T
TLC69699DYYR.A	Active	Production	SOT-23-THIN (DYY)   14	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	69699T

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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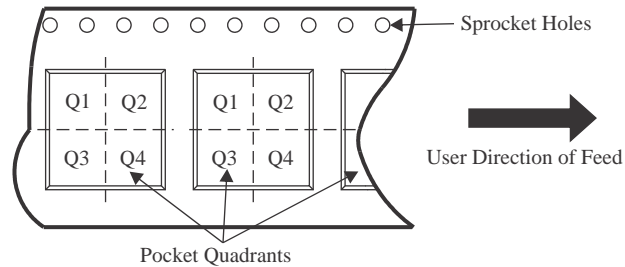
**OTHER QUALIFIED VERSIONS OF TLC69699 :**

- Automotive : [TLC69699-Q1](#)

## NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC69699DRRR	WSON	DRR	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLC69699DYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC69699DRRR	WSON	DRR	12	3000	367.0	367.0	35.0
TLC69699DYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8

## GENERIC PACKAGE VIEW

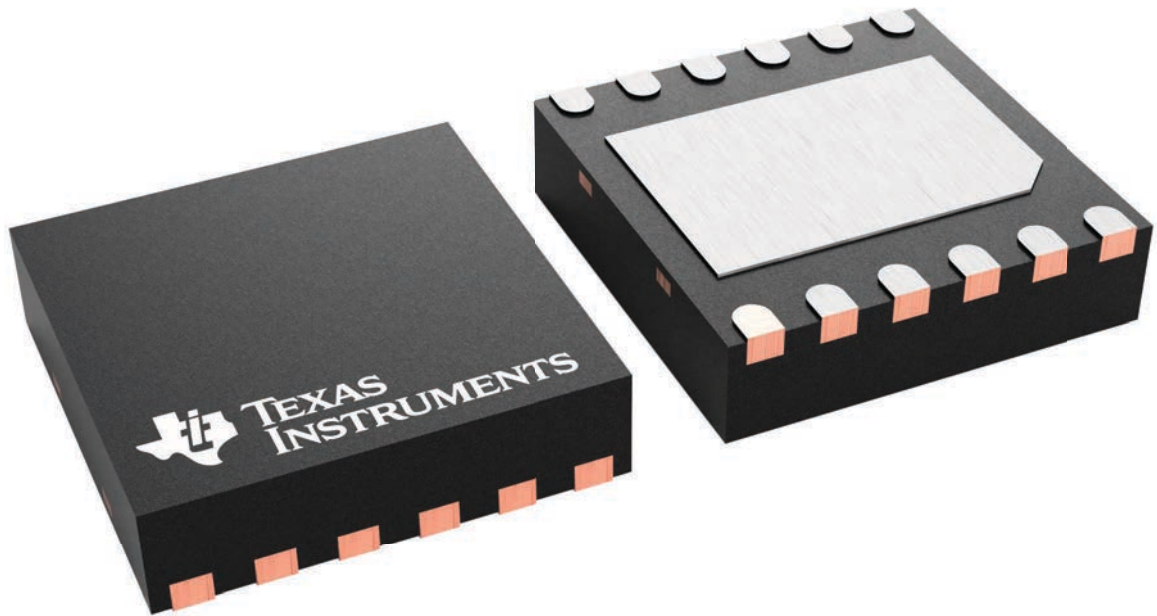
**DRR 12**

**WSON - 0.8 mm max height**

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4223490/B

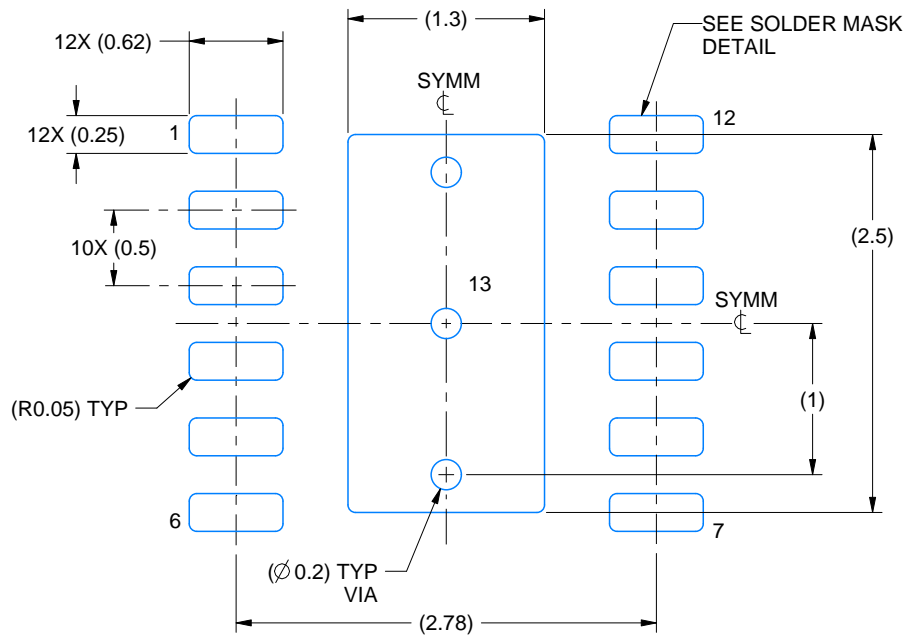


# EXAMPLE BOARD LAYOUT

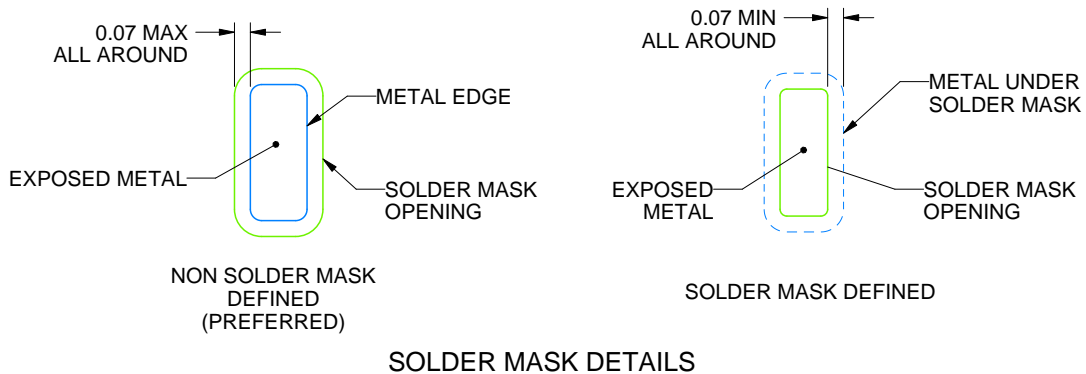
DRR0012G

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X

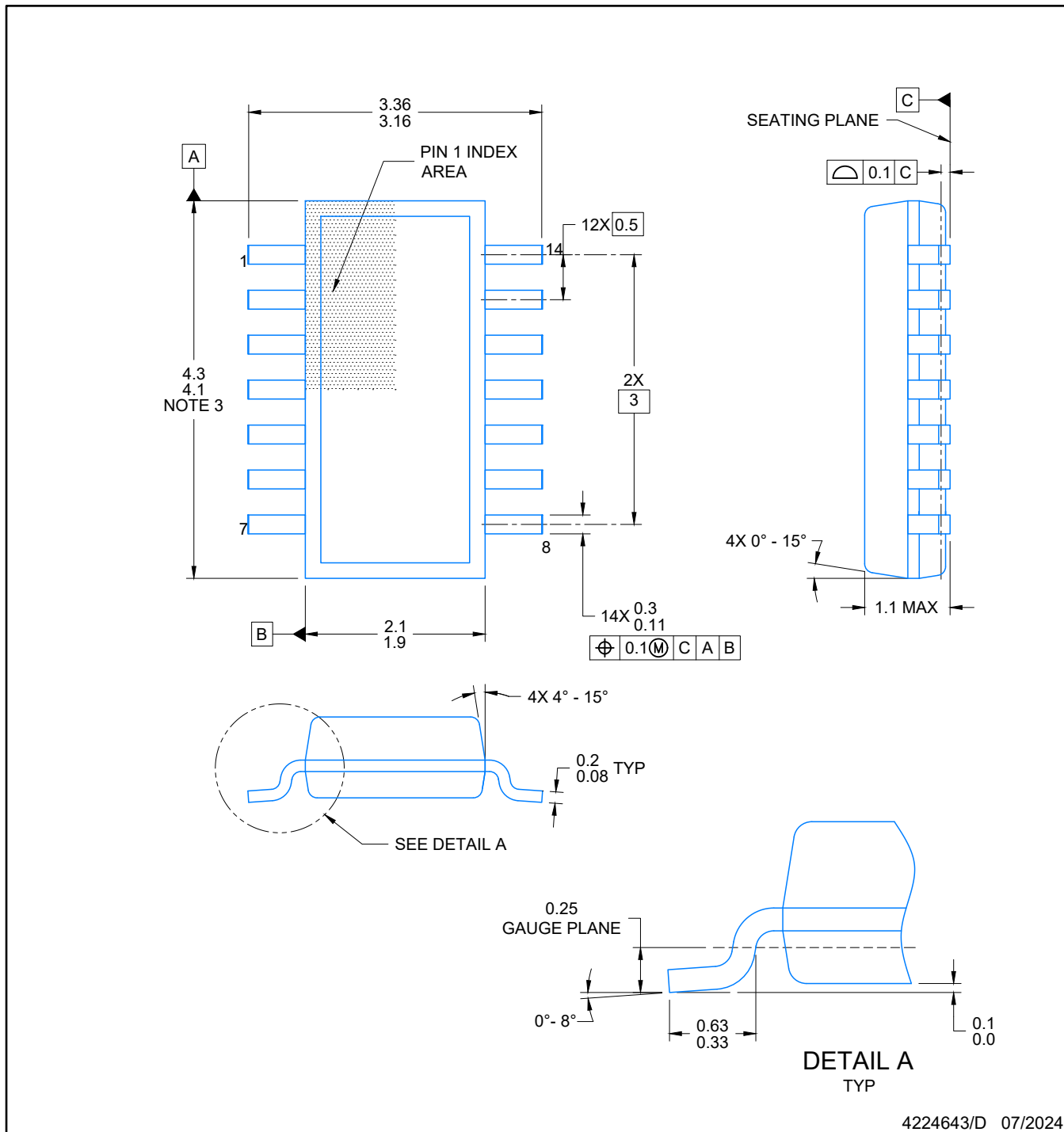


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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

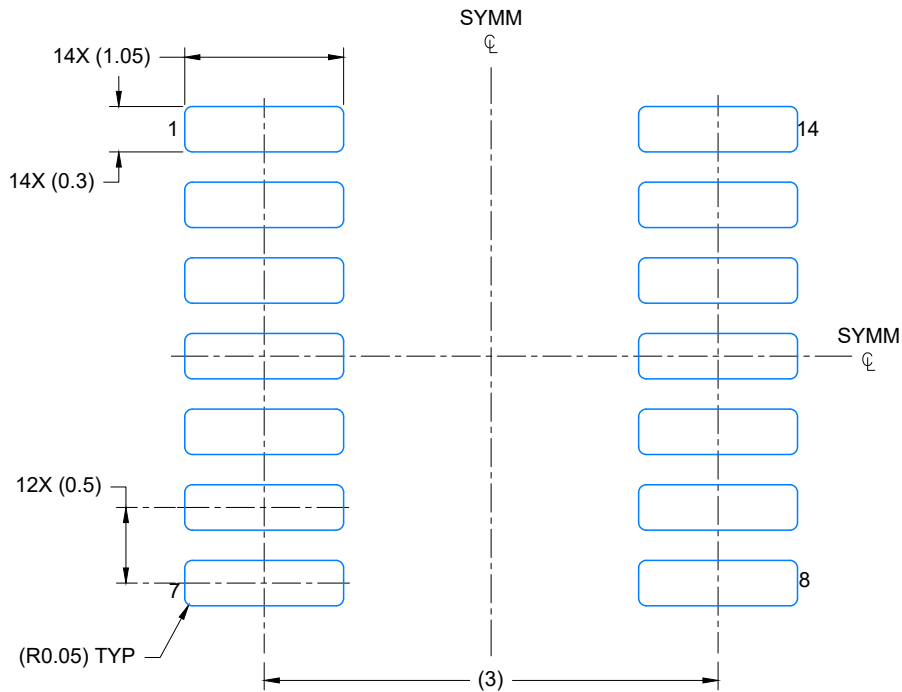




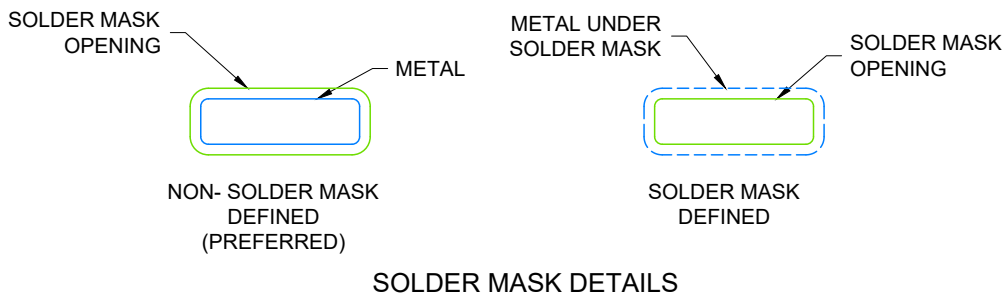
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



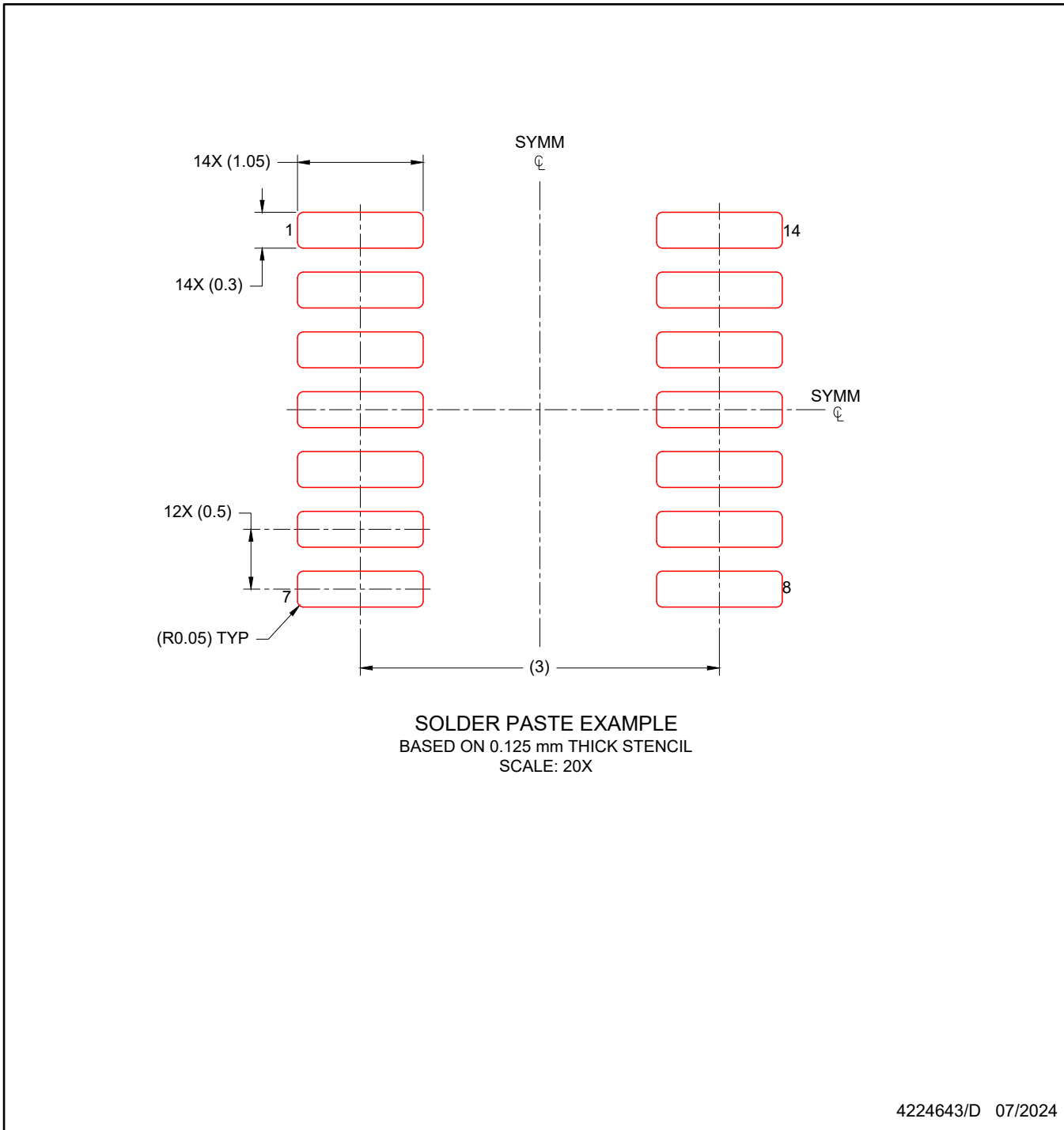
LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224643/D 07/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

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