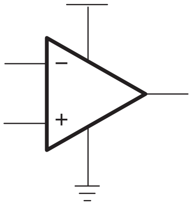
TLV2450, TLV2451, TLV2452, TLV2453, TLV2454, TLV2455, TLV245xA FAMILY OF 23-μA 220-kHz RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS218F − DECEMBER 1998 − REVISED JANUARY 2005

- **Supply Current . . . 23 μA/Channel**
- **Gain-Bandwidth Product . . . 220 kHz**
- **Output Drive Capability . . . ±10 mA**
- **Input Offset Voltage . . . 20 μV (typ)**
- **V_{DD} Range . . . 2.7 V to 6 V**
- **Power Supply Rejection Ratio . . . 106 dB**
- **Ultralow-Power Shutdown Mode**
  I_{DD} . . . 16 nA/ch
- **Rail-To-Rail Input/Output (RRIO)**
- **Ultrasmall Packaging**
  - **5 or 6 Pin SOT-23 (TLV2450/1)**
  - **8 or 10 Pin MSOP (TLV2452/3)**

Operational Amplifier



description

The TLV245x is a family of rail-to-rail input/output operational amplifiers that sets a new performance point for supply current and ac performance. These devices consume a mere 23 μA/channel while offering 220 kHz of gain-bandwidth product, much higher than competitive devices with similar supply current levels. Along with increased ac performance, the amplifier provides high output drive capability, solving a major shortcoming of older micropower rail-to-rail input/output operational amplifiers. The TLV245x can swing to within 250 mV of each supply rail while driving a 2.5-mA load. Both the inputs and outputs swing rail-to-rail for increased dynamic range in low-voltage applications. This performance makes the TLV245x family ideal for portable medical equipment, patient monitoring systems, and data acquisition circuits.

FAMILY PACKAGE TABLE

DEVICE	NUMBER OF CHANNELS	PACKAGE TYPES					SHUTDOWN	UNIVERSAL EVM BOARD
		PDIP	SOIC	SOT-23	TSSOP	MSOP		
TLV2450	1	8	8	6	—	—	Yes	Refer to the EVM Selection Guide (Lit# SLOU060)
TLV2451	1	8	8	5	—	—	—	
TLV2452	2	8	8	—	—	8	—	
TLV2453	2	14	14	—	—	10	Yes	
TLV2454	4	14	14	—	14	—	—	
TLV2455	4	16	16	—	16	—	Yes	

A SELECTION OF SINGLE-SUPPLY OPERATIONAL AMPLIFIER PRODUCTS†

DEVICE	V_{DD} (V)	BW (MHz)	SLEW RATE (V/μs)	I_{DD} (per channel) (μA)	RAIL-TO-RAIL
TLV245X	2.7 − 6.0	0.22	0.11	23	I/O
TLV247X	2.7 − 6.0	2.8	1.5	600	I/O
TLV246X	2.7 − 6.0	6.4	1.6	550	I/O
TLV277X	2.5 − 6.0	5.1	10.5	1000	O

† All specifications measured at 5 V.

description (continued)

Three members of the family (TLV2450/3/5) offer a shutdown terminal for conserving battery life in portable applications. During shutdown, the outputs are placed in a high-impedance state and the amplifier consumes only 16 nA/channel. The family is fully specified at 3 V and 5 V across an expanded industrial temperature range (−40°C to 125°C). The singles and duals are available in the SOT23 and MSOP packages, while the quads are available in TSSOP. The TLV2450 offers an amplifier with shutdown functionality all in a 6-pin SOT23 package, making it perfect for high density circuits.

TLV2450 and TLV2451 AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			
	SMALL OUTLINE (D)†	SOT-23		PLASTIC DIP (P)
		(DBV)	SYMBOL	
0°C to 70°C	TLV2450CD TLV2451CD	TLV2450CDBV TLV2451CDBV	VAQC VARC	TLV2450CP TLV2451CP
−40°C to 125°C	TLV2450ID TLV2451ID	TLV2450IDBV TLV2451IDBV	VAQI VARI	TLV2450IP TLV2451IP
	TLV2450AID TLV2451AID	— —	— —	TLV2450AIP TLV2451AIP

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2450CDR).

TLV2452 and TLV2453 AVAILABLE OPTIONS

T_A	PACKAGED DEVICES						
	SMALL OUTLINE (D)†	MSOP				PLASTIC DIP (N)	PLASTIC DIP (P)
		(DGK)†	SYMBOL‡	(DGS)†	SYMBOL‡		
0°C to 70°C	TLV2452CD TLV2453CD	TLV2452CDGK —	xxTIABI —	— TLV2453CDGS	— xxTIABK	— TLV2453CN	TLV2452CP —
−40°C to 125°C	TLV2452ID TLV2453ID	TLV2452IDGK —	xxTIABJ —	— TLV2453IDGS	— xxTIABL	— TLV2453IN	TLV2452IP —
	TLV2452AID TLV2453AID	— —	— —	— —	— —	— TLV2453AIN	TLV2452AIP —

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2452CDR).
‡ xx represents the device date code.

TLV2454 and TLV2455 AVAILABLE OPTIONS

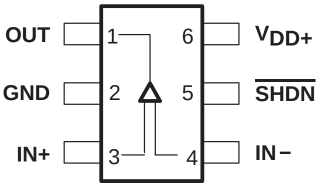
T_A	PACKAGED DEVICES		
	SMALL OUTLINE (D)†	PLASTIC DIP (N)	TSSOP (PW)†
0°C to 70°C	TLV2454CD TLV2455CD	TLV2454CN TLV2455CN	TLV2454CPW TLV2455CPW
−40°C to 125°C	TLV2454ID TLV2455ID	TLV2454IN TLV2455IN	TLV2454IPW TLV2455IPW
	TLV2454AID TLV2455AID	TLV2454AIN TLV2455AIN	TLV2454AIPW TLV2455AIPW

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2454CDR).

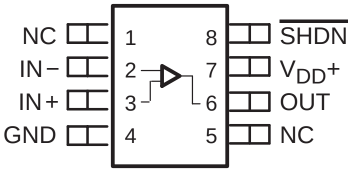
NOTE: For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or refer to our web site at www.ti.com.

TLV245x PACKAGE PINOUTS(1)

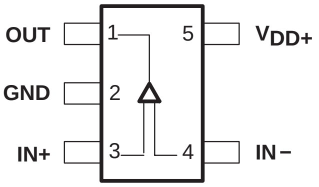
TLV2450
DBV PACKAGE
(TOP VIEW)



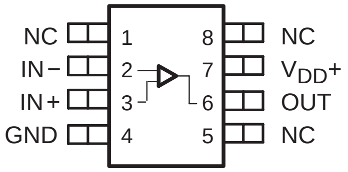
TLV2450
D OR P PACKAGE
(TOP VIEW)



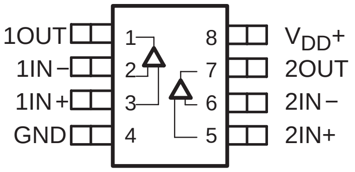
TLV2451
DBV PACKAGE
(TOP VIEW)



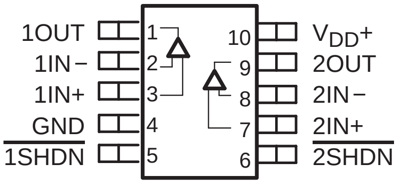
TLV2451
D OR P PACKAGE
(TOP VIEW)



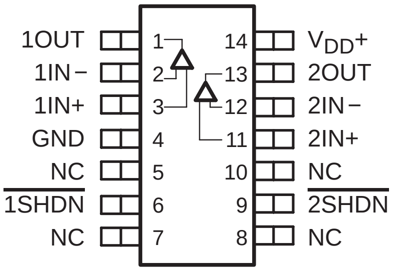
TLV2452
D, DGK, OR P PACKAGE
(TOP VIEW)



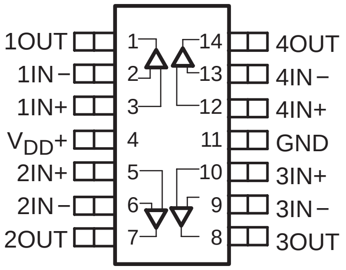
TLV2453
DGS PACKAGE
(TOP VIEW)



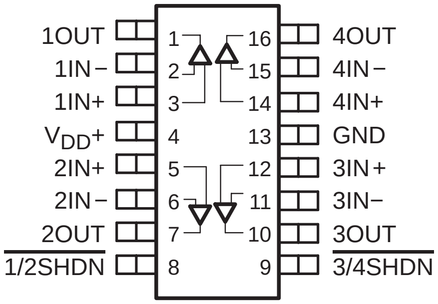
TLV2453
D OR N PACKAGE
(TOP VIEW)



TLV2454
D, N, OR PW PACKAGE
(TOP VIEW)

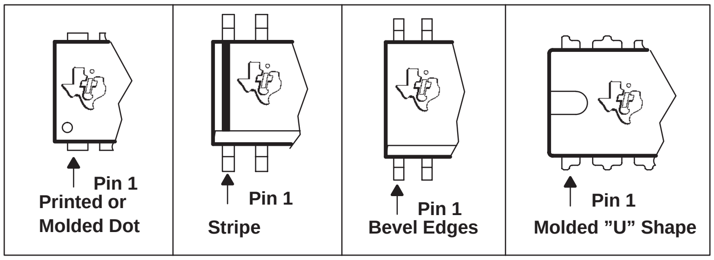


TLV2455
D, N, OR PW PACKAGE
(TOP VIEW)



NC − No internal connection
(1) SOT−23 may or may not be indicated

TYPICAL PIN 1 INDICATORS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1)		7 V
Differential input voltage, V_{ID}		$\pm V_{DD}$
Continuous total power dissipation		See Dissipation Rating Table
Operating free-air temperature range, T_A:	C suffix	0°C to 70°C
	I suffix	−40°C to 125°C
Maximum junction temperature, T_J		150°C
Storage temperature range, T_{stg}		−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltage values, except differential voltages, are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	$T_A \leq 25°C$ POWER RATING
D (8)	38.3	176	710 mW
D (14)	26.9	122.3	1022 mW
D (16)	25.7	114.7	1090 mW
DBV (5)	55	324.1	385 mW
DBV (6)	55	294.3	425 mW
DGK (8)	54.2	259.9	481 mW
DGS (10)	54.1	257.7	485 mW
N (14, 16)	32	78	1600 mW
P (8)	41	104	1200 mW
PW (14)	29.3	173.6	720 mW
PW (16)	28.7	161.4	774 mW

recommended operating conditions

			MIN	MAX	UNIT
Supply voltage, V_{DD}	Single supply		2.7	6	V
	Split supply		±1.35	±3	
Common-mode input voltage range, V_{ICR}			0	V_{DD}	V
Operating free-air temperature, T_A	C-suffix		0	70	°C
	I-suffix		−40	125	
Shutdown on/off voltage level[‡]	V_{IH}		2		V
	V_{IL}	V_{DD} = 5V		0.8	
		V_{DD} = 3V		0.5	V

[‡] Relative to voltage on the GND terminal of the device.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS			T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLV245x	V_{DD} = ±1.5 V V_{IC} = 0,	V_O = 0, R_S = 50 Ω		25°C		300	1500	µV
						Full range			2000	
		TLV245xA				25°C		300	1000	
						Full range			1300	
α_{VIO}	Temperature coefficient of input offset voltage							0.3		µV/°C
I_{IO}	Input offset current					25°C		0.3	4.5	nA
						Full range			5.5	
I_{IB}	Input bias current					25°C		0.9	5	nA
						Full range			7	
V_{OH}	High-level output voltage		V_{IC} = 1.5 V,	I_{OH} = −500 µA		25°C	2.85	2.95		V
						Full range	2.83			
V_{OL}	Low-level output voltage		V_{IC} = 1.5 V,	I_{OL} = 500 µA		25°C		0.09	0.16	V
						Full range			0.2	
I_{OS}	Short-circuit output current		Sourcing			25°C	4	12		mA
						Full range	3			
			Sinking			25°C	2	7		
						Full range	1			
I_O	Output current		V_O = 0.5 V from rail			25°C		±4		mA
A_{VD}	Large-signal differential voltage amplification		$V_{O(PP)}$ = 1 V,	R_L = 10 kΩ		25°C	96	110		dB
						Full range	91			
$r_{i(d)}$	Differential input resistance					25°C		10^9		Ω
C_{IC}	Common-mode input capacitance		f = 10 kHz			25°C		4.5		pF
z_o	Closed-loop output impedance		f = 10 kHz,	A_V = 10		25°C		80		Ω
CMRR	Common-mode rejection ratio		V_{IC} = 0 to 3 V, R_S = 50 Ω			25°C	70	80		dB
					TLV245xC	Full range	66			dB
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})		V_{DD} = 2.7 V to 6 V, No load	V_{IC} = V_{DD}/2,		25°C	76	89		dB
						Full range	74			
			V_{DD} = 3 V to 5 V, No load	V_{IC} = V_{DD}/2,		25°C	88	106		
						Full range	84			
I_{DD}	Supply current (per channel)		V_O = 1.5 V, No load			25°C		23	35	µA
					TLV245xC	Full range			40	
					TLV245xI	Full range			45	
$I_{DD(SHDN)}$	Supply current in shutdown mode (TLV2450, TLV2453, TLV2455) (per channel)		$\overline{SHDN}$ = $-V_{DD}$			25°C		12	65	nA
					TLV245xC	Full range			70	
					TLV245xI	Full range			80	

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix.

operating characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, R_L = 10 kΩ	C_L = 150 pF,	25°C	0.05	0.11		V/µs
				Full range	0.02			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		49		nV/√Hz
		f = 1 kHz		25°C		51		
I_n	Equivalent input noise current	f = 1 kHz		25°C		3.5		pA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 1.5 V, R_L = 10 kΩ, f = 1 kHz	A_V = 1	25°C		0.04%		
			A_V = 10			0.3%		
			A_V = 100			1.5%		
$t_{(on)}$	Amplifier turnon time	A_V = 5, Measured at 50% point	R_L = OPEN,	25°C		59		µs
$t_{(off)}$	Amplifier turnoff time			25°C		836		ns
	Gain-bandwidth product	f = 10 kHz,	R_L = 10 kΩ	25°C		200		kHz
t_s	Settling time	$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		26		µs
			0.01%			31		
		$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 56 pF, R_L = 10 kΩ	0.1%			26		
			0.01%			31		
ϕ_m	Phase margin	R_L = 10 kΩ,	C_L = 1000 pF	25°C		56°		
	Gain margin	R_L = 10 kΩ,	C_L = 1000 pF	25°C		7		dB

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TLV245x	V_{DD} = ±2.5 V V_{IC} = 0,	V_O = 0, R_S = 50 Ω	25°C		300	1500	µV
					Full range			2000	
		TLV245xA			25°C		300	1000	
					Full range			1300	
α_{VIO}	Temperature coefficient of input offset voltage						0.3		µV/°C
I_{IO}	Input offset current				25°C		0.3	4.5	nA
					Full range			5.5	
I_{IB}	Input bias current				25°C		0.5	5	nA
					Full range			7	
V_{OH}	High-level output voltage		V_{IC} = 2.5 V,	I_{OH} = −500 µA	25°C	4.87	4.97		V
					Full range	4.85			
V_{OL}	Low-level output voltage		V_{IC} = 2.5 V,	I_{OL} = 500 µA	25°C		0.07	0.15	V
					Full range			0.16	
I_{OS}	Short-circuit output current		Sourcing		25°C	20	32		mA
					Full range	18			
			Sinking		25°C	12	18		
					Full range	10			
I_O	Output current		V_O = 0.5 V from rail		25°C		±10		mA
A_{VD}	Large-signal differential voltage amplification		$V_{O(PP)}$ = 3 V,	R_L = 10 kΩ	25°C	96	103		dB
					Full range	91			
$r_{i(d)}$	Differential input resistance				25°C		10^9		Ω
C_{IC}	Common-mode input capacitance		f = 10 kHz		25°C		4.5		pF
z_o	Closed-loop output impedance		f = 10 kHz,	A_V = 10	25°C		45		Ω
CMRR	Common-mode rejection ratio		V_{IC} = 0 to 5 V, R_S = 50 Ω		25°C	70	80		dB
				TLV245xC	Full range	68			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} /ΔV_{IO})		V_{DD} = 2.7 V to 6 V, No load	V_{IC} = V_{DD}/2,	25°C	76	89		dB
					Full range	74			
			V_{DD} = 3 V to 5 V, No load	V_{IC} = V_{DD}/2,	25°C	88	106		
					Full range	84			
I_{DD}	Supply current (per channel)		V_O = 2.5 V, No load		25°C		23	42	µA
				TLV245xC	Full range			44	
				TLV245xI	Full range			46	
$I_{DD(SHDN)}$	Supply current in shutdown mode (TLV2450, TLV2453, TLV2455) (per channel)		$\overline{\text{SHDN}}$ = $-V_{DD}$		25°C		16	70	nA
				TLV245xC	Full range			70	
				TLV245xI	Full range			80	

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix.

operating characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$V_{O(PP)}$ = 2 V, C_L = 150 pF, R_L = 10 kΩ		25°C	0.05	0.11		V/µs
				Full range	0.02			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		49		nV/√Hz
		f = 1 kHz		25°C		52		
I_n	Equivalent input noise current	f = 1 kHz		25°C		3.5		pA/√Hz
THD + N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 3 V, R_L = 10 kΩ, f = 1 kHz	A_V = 1	25°C		0.02%		
			A_V = 10			0.18%		
			A_V = 100			0.9%		
$t_{(on)}$	Amplifier turnon time	A_V = 5, R_L = OPEN, Measured at 50% point		25°C		59		µs
$t_{(off)}$	Amplifier turnoff time			25°C		836		ns
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ		25°C		220		kHz
t_s	Settling time	$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		24		µs
			0.01%			30		
		$V_{(STEP)PP}$ = 2 V, A_V = −1, C_L = 56 pF, R_L = 10 kΩ	0.1%			25		
			0.01%			30		
ϕ_m	Phase margin	R_L = 10 kΩ, C_L = 1000 pF		25°C		56°		
	Gain margin	R_L = 10 kΩ, C_L = 1000 pF		25°C		7		dB

† Full range is 0°C to 70°C for C suffix and −40°C to 125°C for I suffix.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	1, 2
I_{IO}	Input offset current	vs Common-mode input voltage vs Free-air temperature	3, 4 7, 8
I_{IB}	Input bias current	vs Common-mode input voltage vs Free-air temperature	5, 6 7, 8
A_{VD}	Differential voltage amplification	vs Frequency	9, 10
	Phase	vs Frequency	9, 10
V_{OL}	Low-level output voltage	vs Low-level output current	11, 13
V_{OH}	High-level output voltage	vs High-level output current	12, 14
Z_o	Output impedance	vs Frequency	15, 16
CMRR	Common-mode rejection ratio	vs Frequency	17
PSRR	Power supply rejection ratio	vs Frequency	18
I_{DD}	Supply current	vs Supply voltage	19
I_{DD}	Supply current	vs Free-air temperature	20
V_n	Equivalent input noise voltage	vs Frequency	21
THD + N	Total harmonic distortion plus noise	vs Frequency	22, 23
ϕ_m	Phase margin	vs Load capacitance	24
	Gain-bandwidth product	vs Supply voltage	25
SR	Slew rate	vs Supply voltage vs Free-air temperature	26 27
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	28
	Crosstalk	vs Frequency	29, 30
	Small-signal follower pulse response	vs Time	31, 33
	Large-signal follower pulse response	vs Time	32, 34
	Shutdown on supply current	vs Time	35
	Shutdown off supply current	vs Time	36
	Shutdown supply current	vs Free-air temperature	37
	Shutdown supply current	vs Time	38 − 41
	Shutdown pulse	vs Time	38 − 41
	Shutdown off pulse response	vs Time	42, 43
	Shutdown on pulse response	vs Time	44, 45
	Shutdown reverse isolation	vs Frequency	46
	Shutdown forward isolation	vs Frequency	47

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

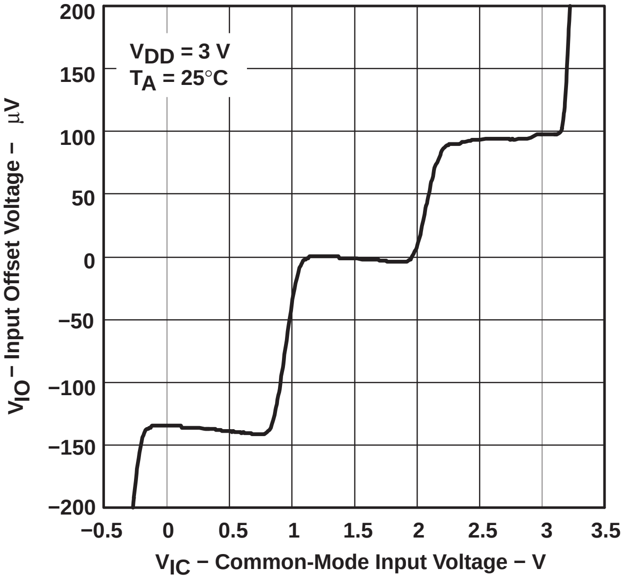


Figure 1

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

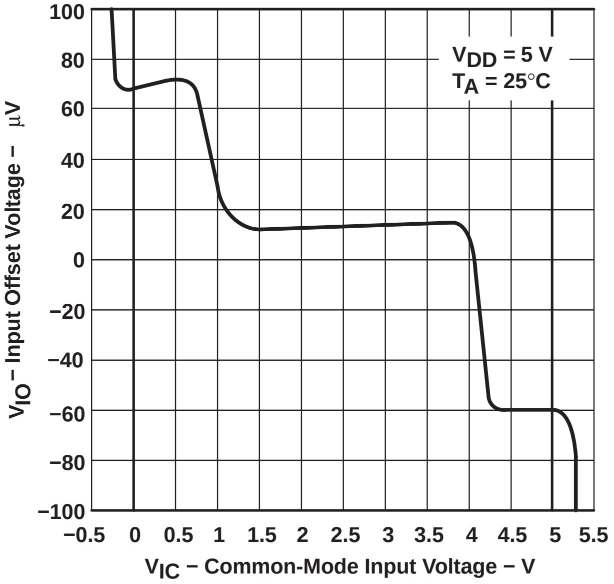


Figure 2

INPUT OFFSET CURRENT
vs
COMMON-MODE INPUT VOLTAGE

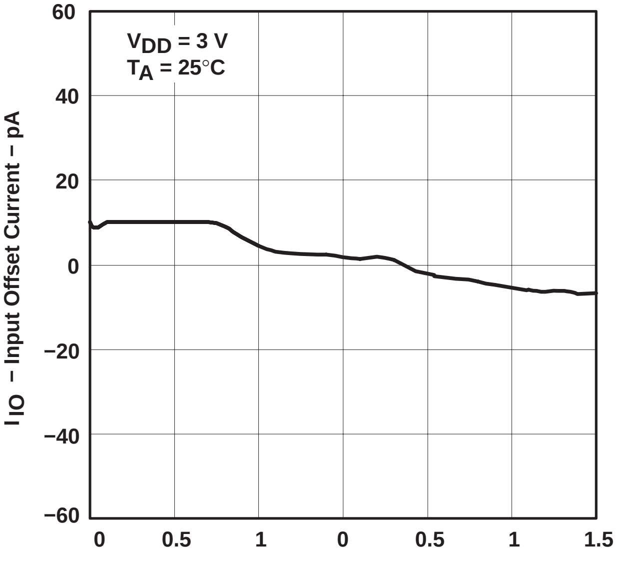


Figure 3

INPUT OFFSET CURRENT
vs
COMMON-MODE INPUT VOLTAGE

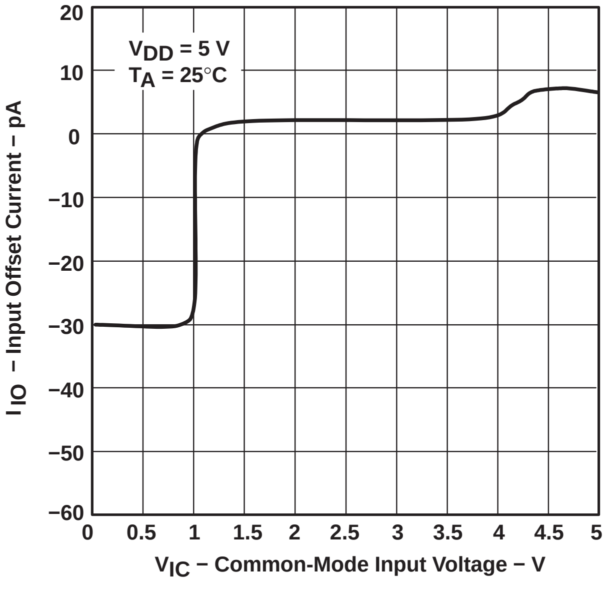


Figure 4

TYPICAL CHARACTERISTICS

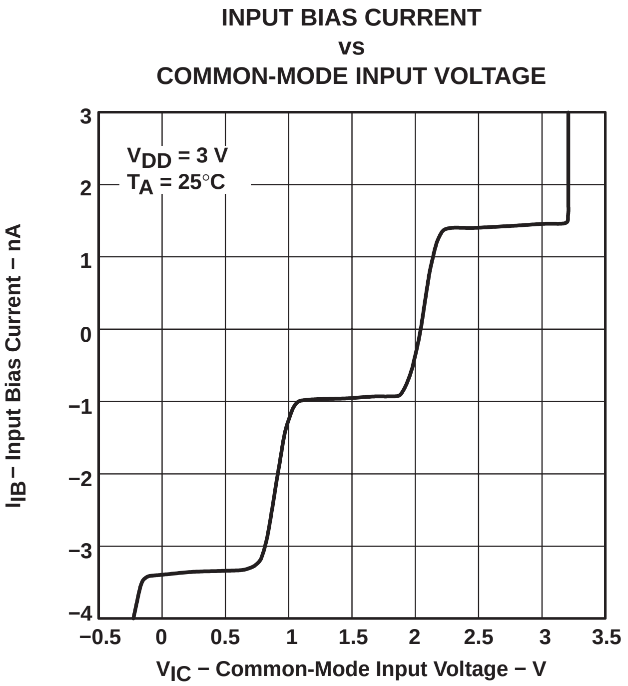

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

Figure 5

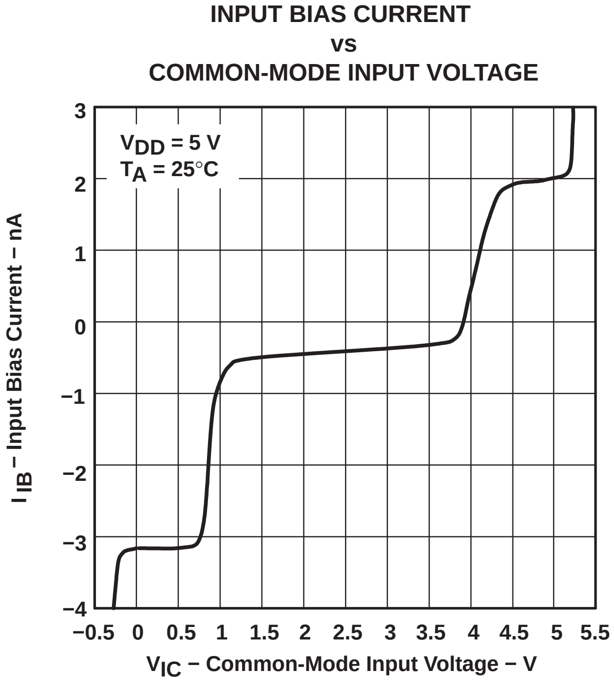

INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

Figure 6

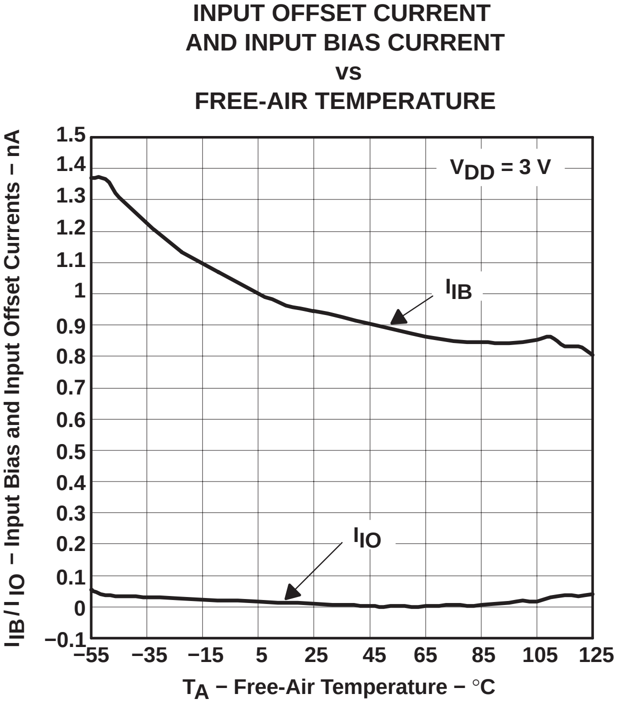

INPUT OFFSET CURRENT
AND INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

Figure 7

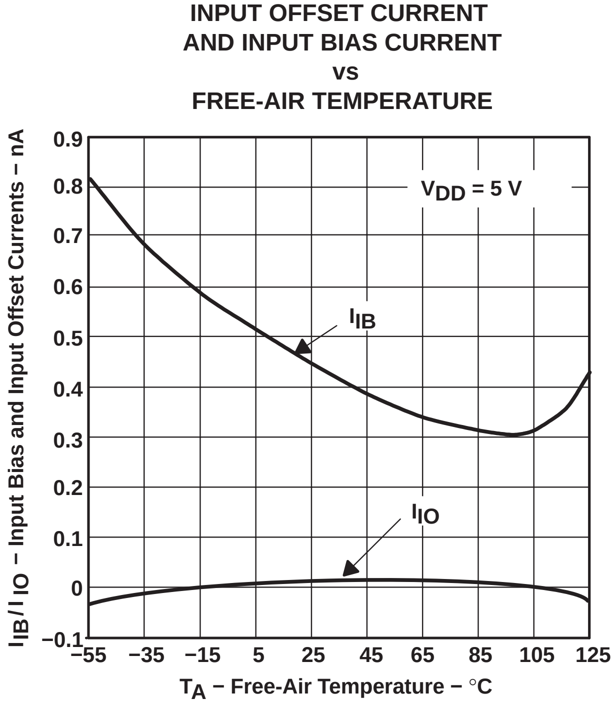

INPUT OFFSET CURRENT
AND INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

Figure 8

TYPICAL CHARACTERISTICS

DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE vs FREQUENCY

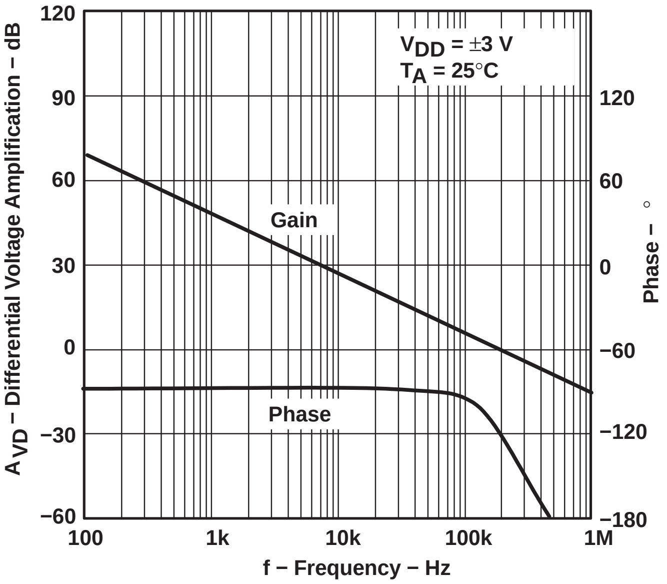


Figure 9

DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE vs FREQUENCY

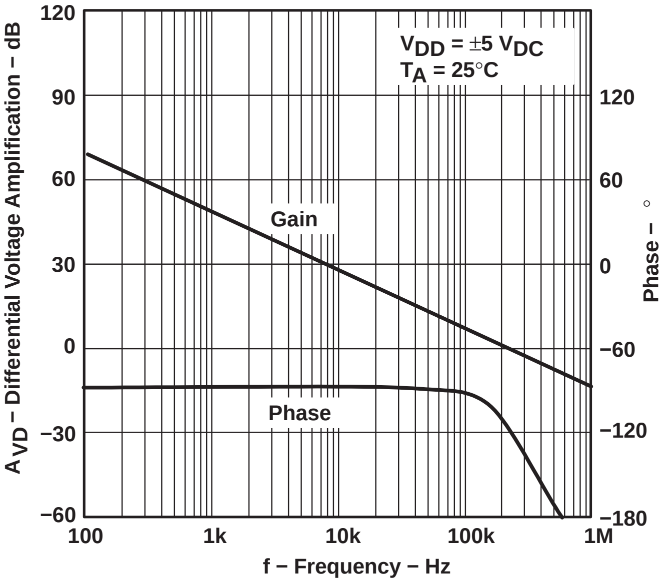


Figure 10

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

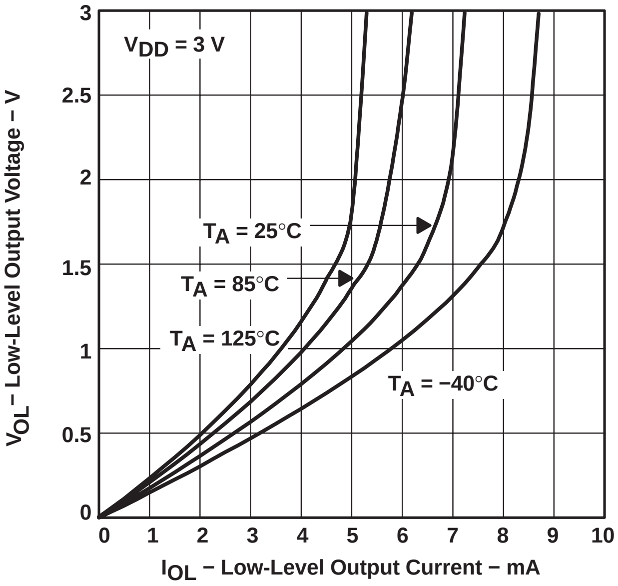


Figure 11

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

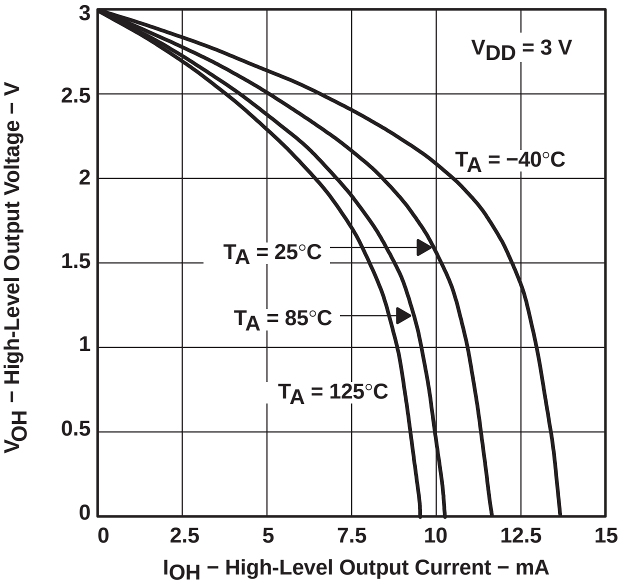


Figure 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

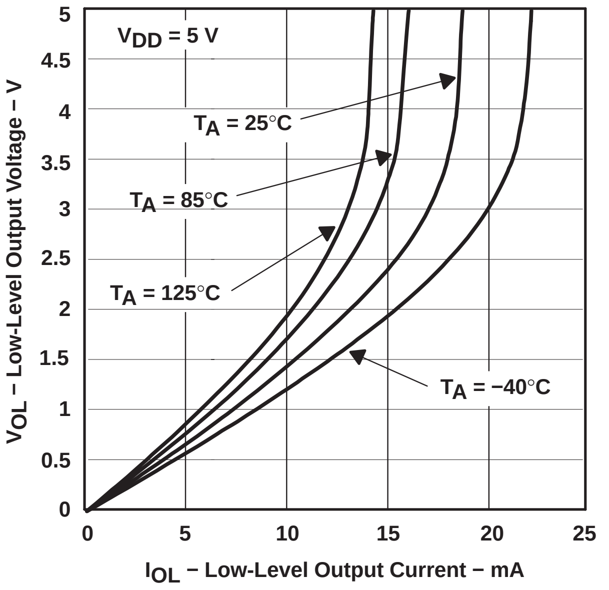


Figure 13

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

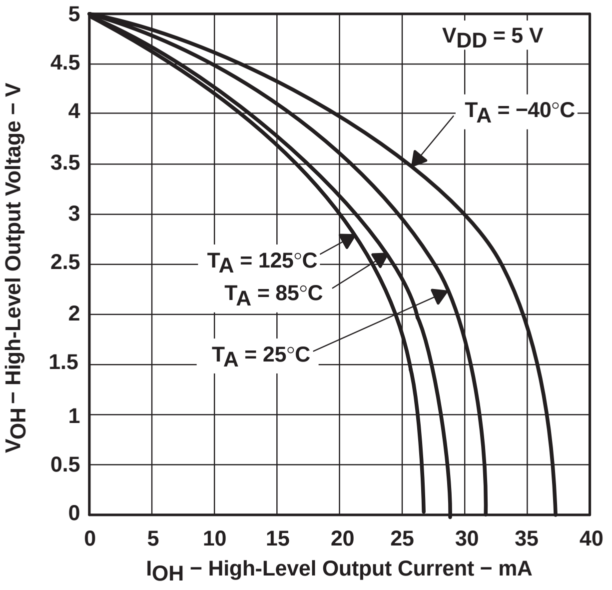


Figure 14

TYPICAL CHARACTERISTICS

OUTPUT IMPEDANCE vs FREQUENCY

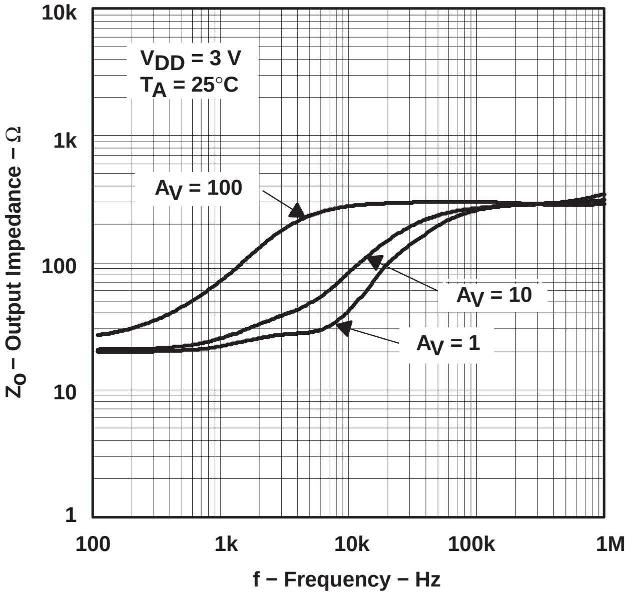


Figure 15

OUTPUT IMPEDANCE vs FREQUENCY

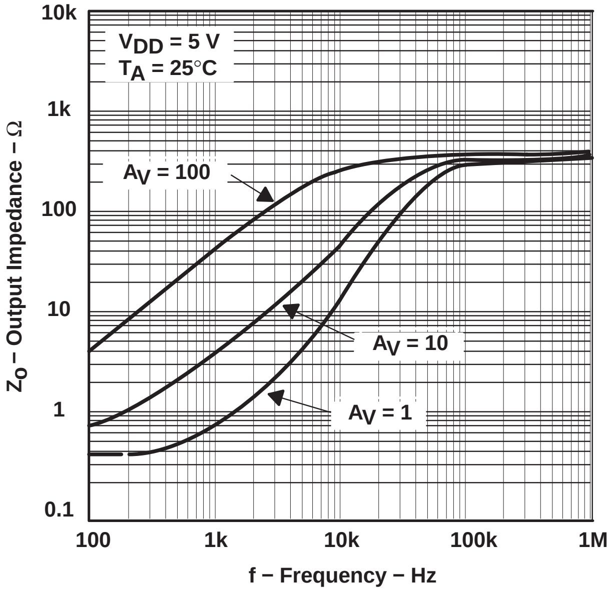


Figure 16

COMMON-MODE REJECTION RATIO vs FREQUENCY

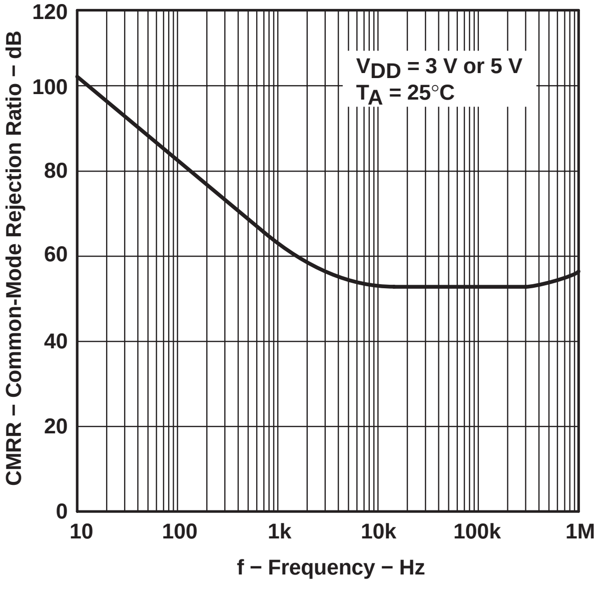


Figure 17

TYPICAL CHARACTERISTICS

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

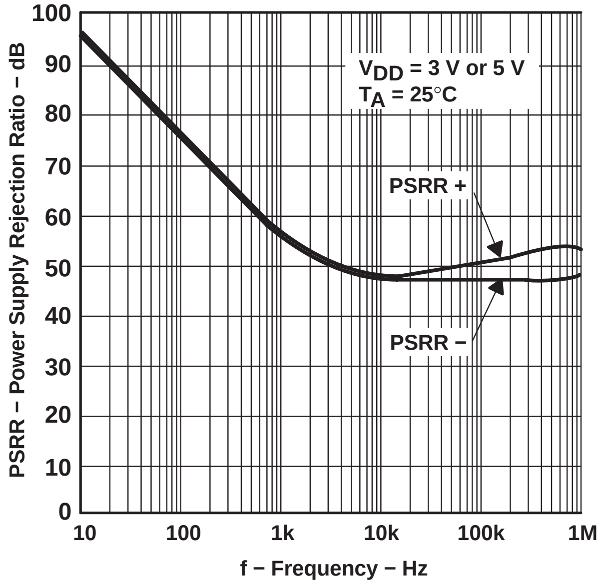


Figure 18

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

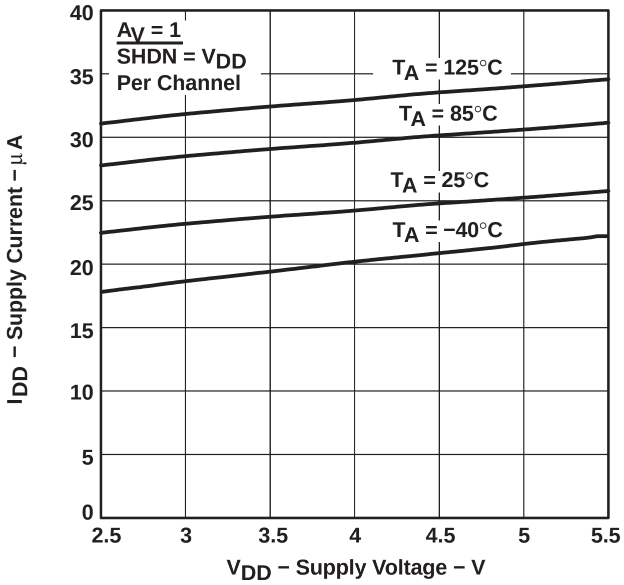


Figure 19

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

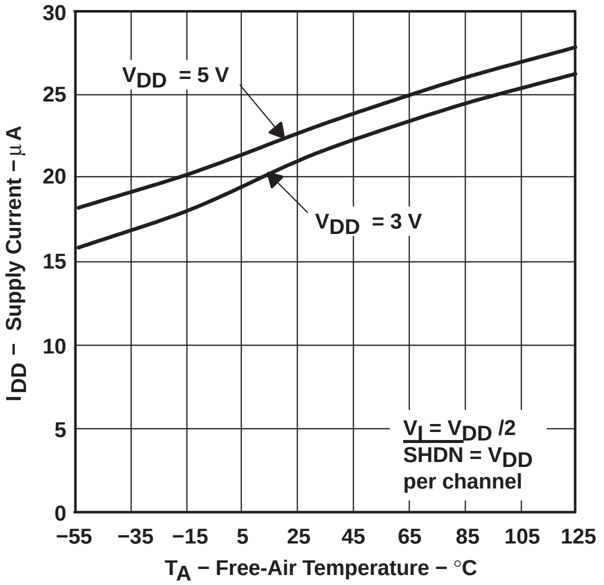


Figure 20

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

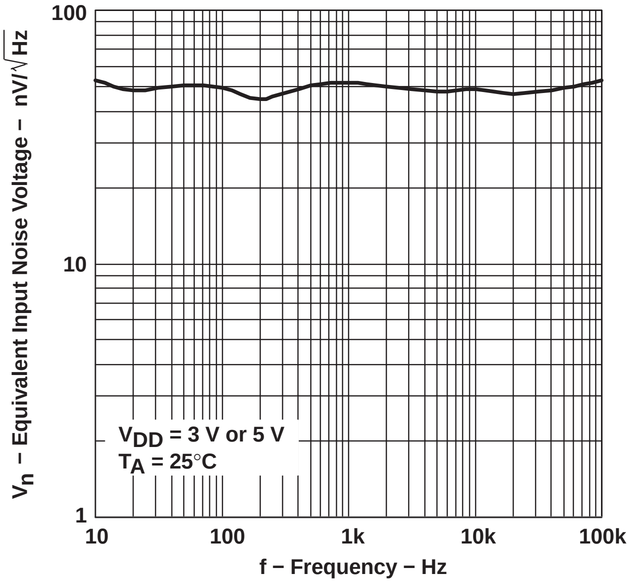


Figure 21

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

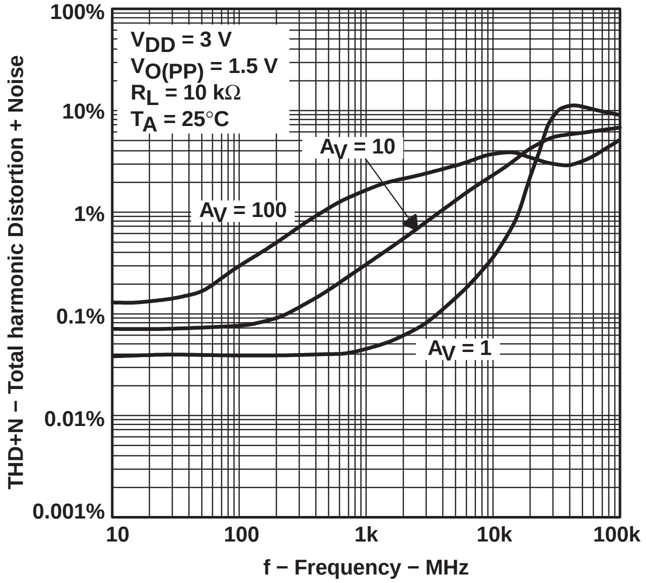


Figure 22

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

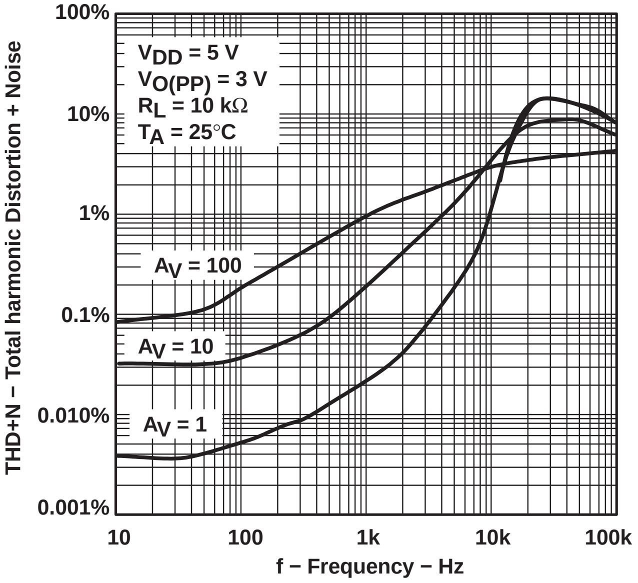


Figure 23

PHASE MARGIN
vs
LOAD CAPACITANCE

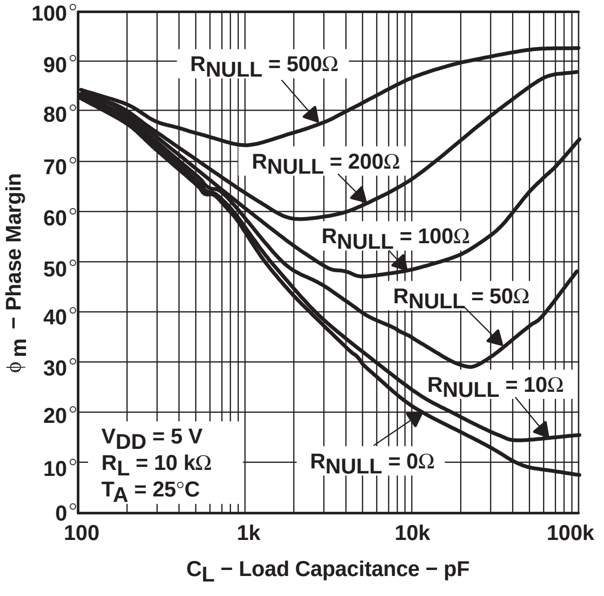


Figure 24

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

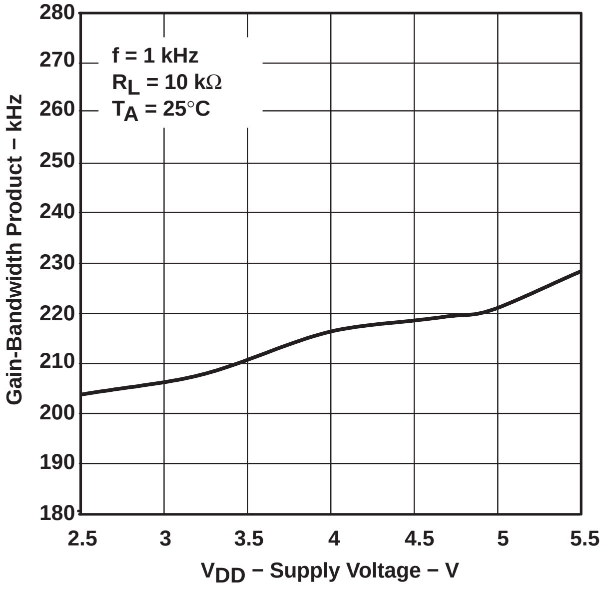


Figure 25

TYPICAL CHARACTERISTICS

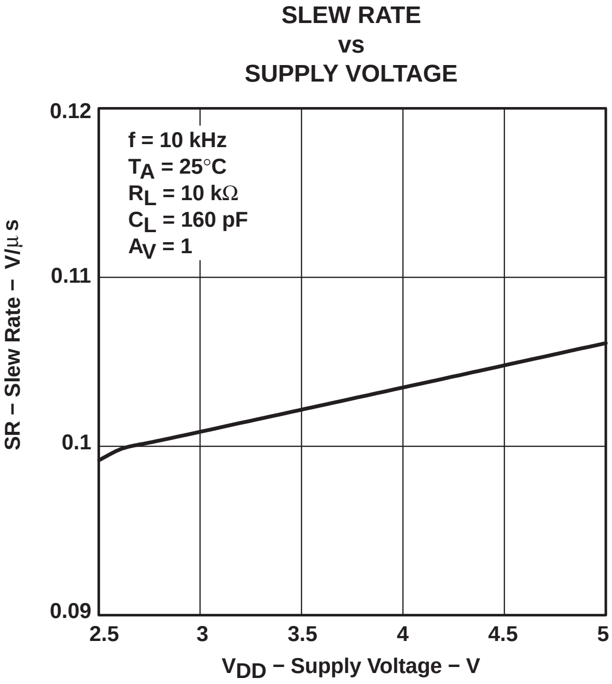


Figure 26

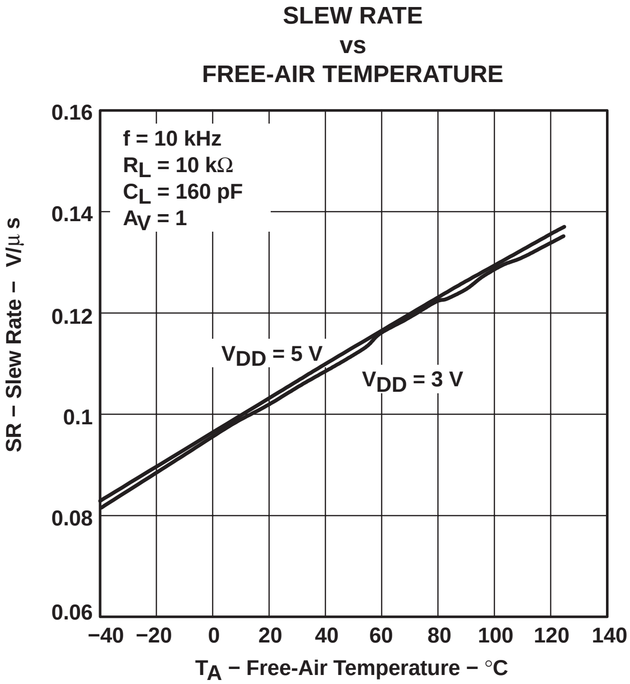


Figure 27

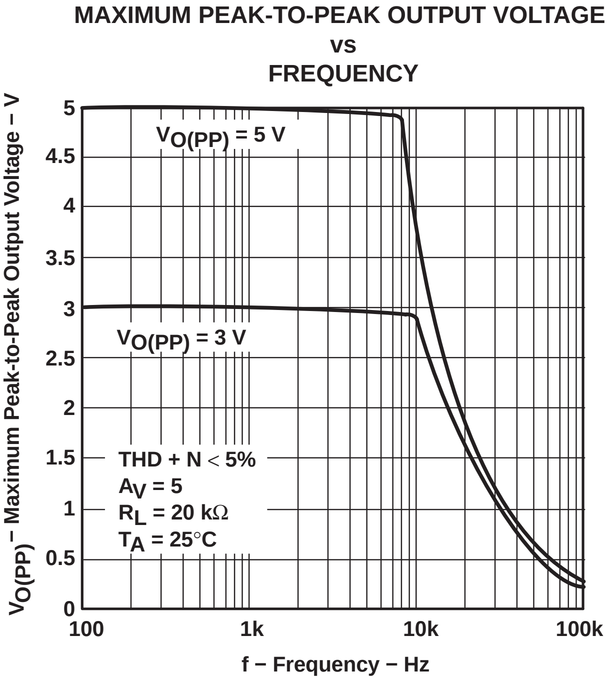


Figure 28

TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

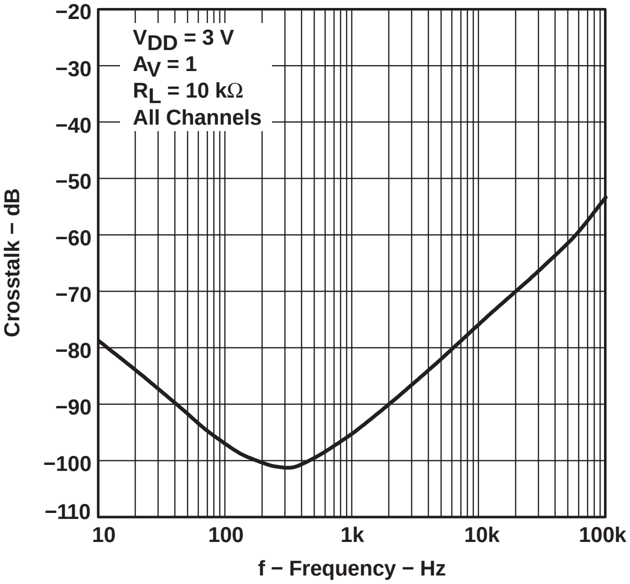


Figure 29

CROSSTALK
vs
FREQUENCY

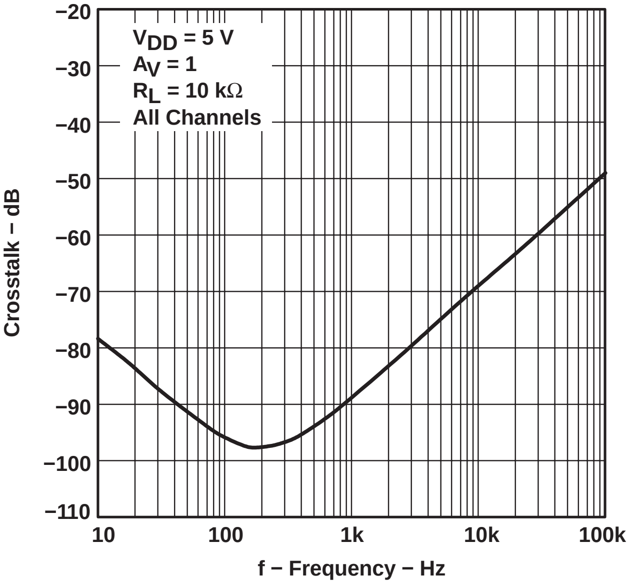


Figure 30

SMALL-SIGNAL FOLLOWER PULSE RESPONSE
vs
TIME

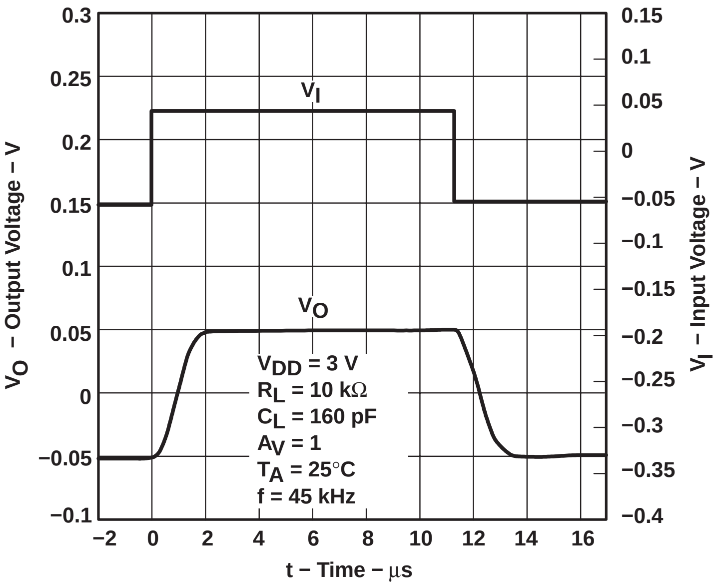


Figure 31

TYPICAL CHARACTERISTICS

LARGE-SIGNAL FOLLOWER PULSE RESPONSE
vs
TIME

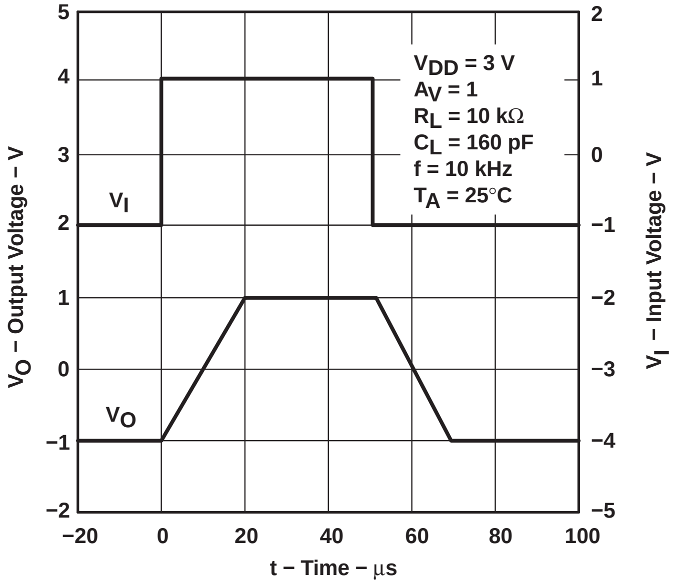


Figure 32

SMALL-SIGNAL FOLLOWER PULSE RESPONSE
vs
TIME

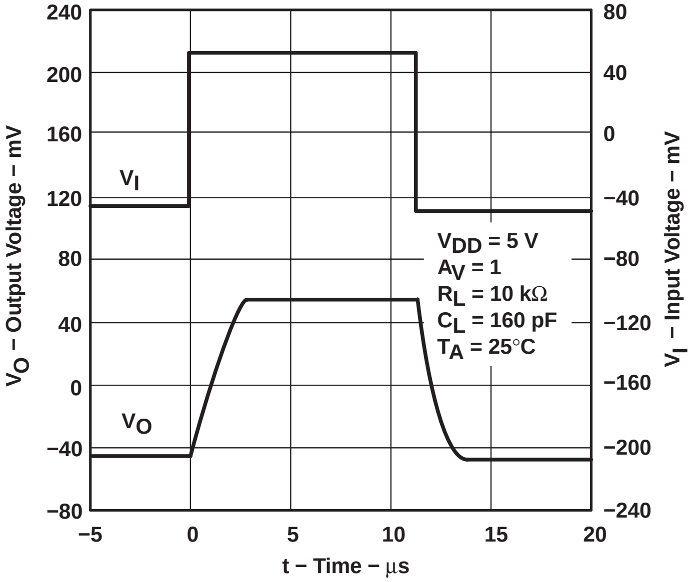


Figure 33

TYPICAL CHARACTERISTICS

LARGE-SIGNAL FOLLOWER PULSE RESPONSE vs TIME

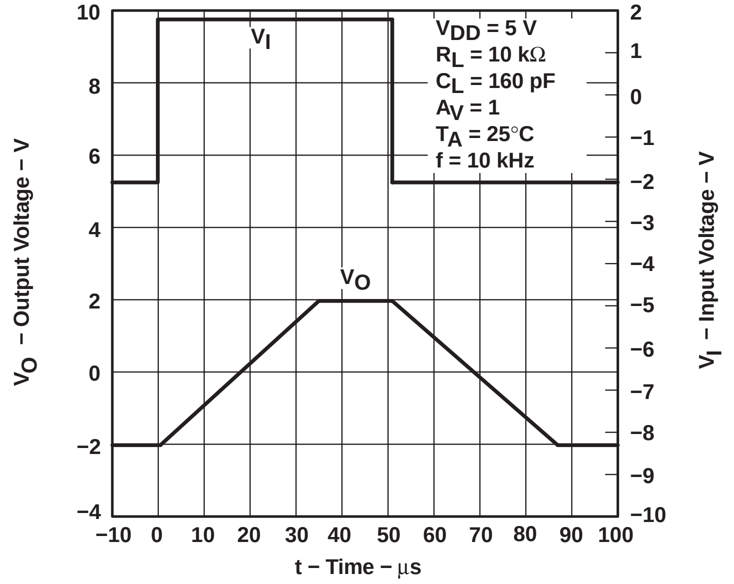


Figure 34

SHUTDOWN ON SUPPLY CURRENT vs TIME

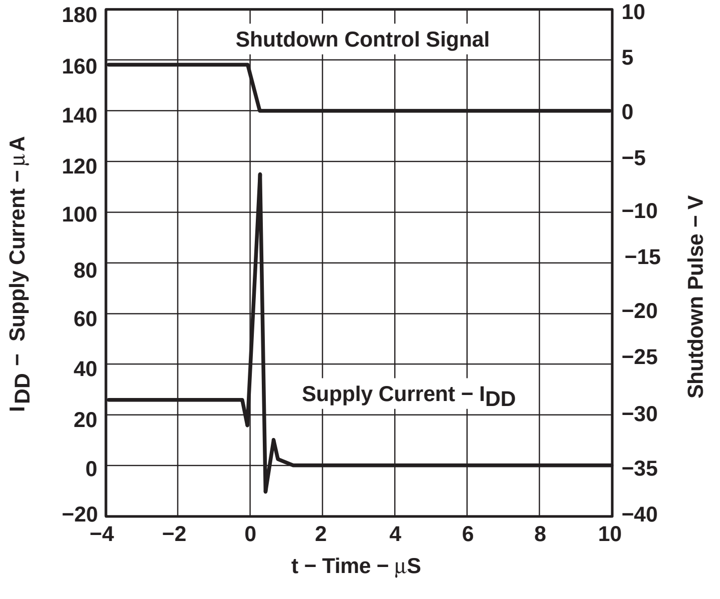


Figure 35

TYPICAL CHARACTERISTICS

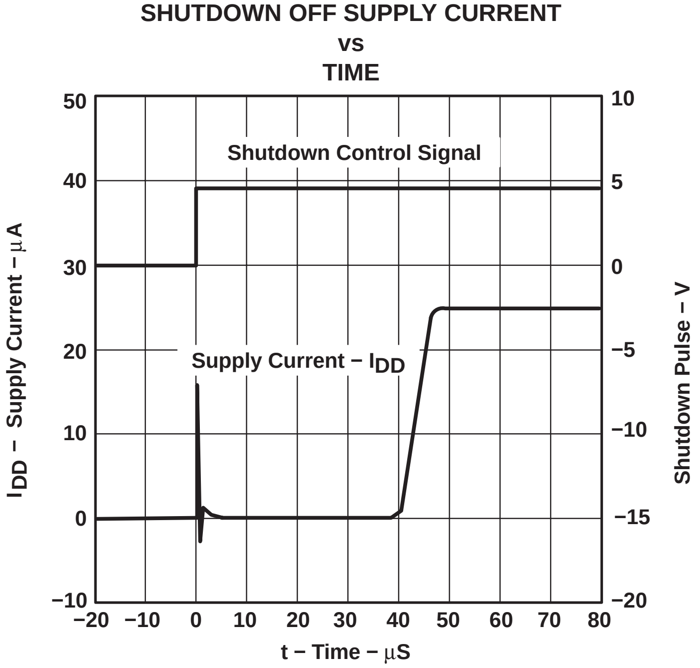


Figure 36

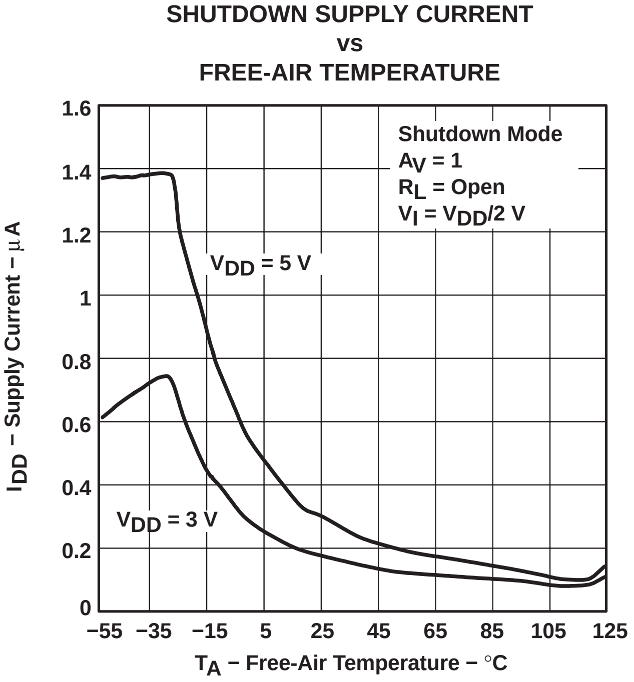


Figure 37

TYPICAL CHARACTERISTICS

SHUTDOWN SUPPLY CURRENT AND SHUTDOWN PULSE
vs
TIME

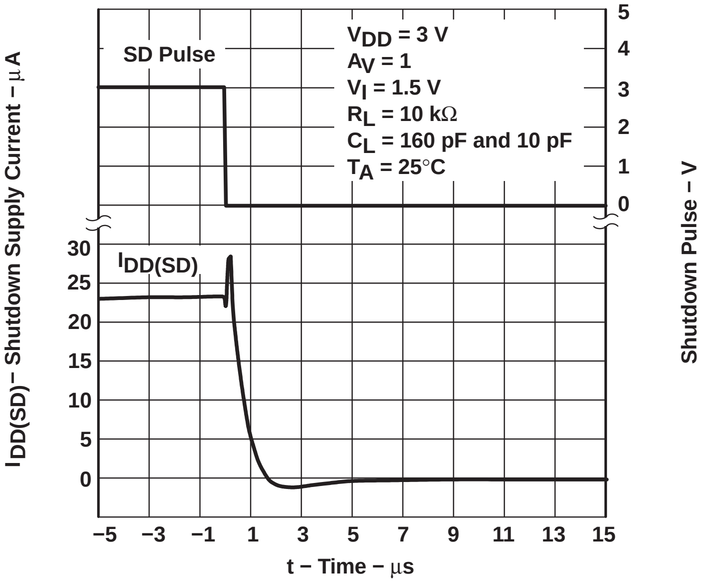


Figure 38

SHUTDOWN SUPPLY CURRENT AND SHUTDOWN PULSE
vs
TIME

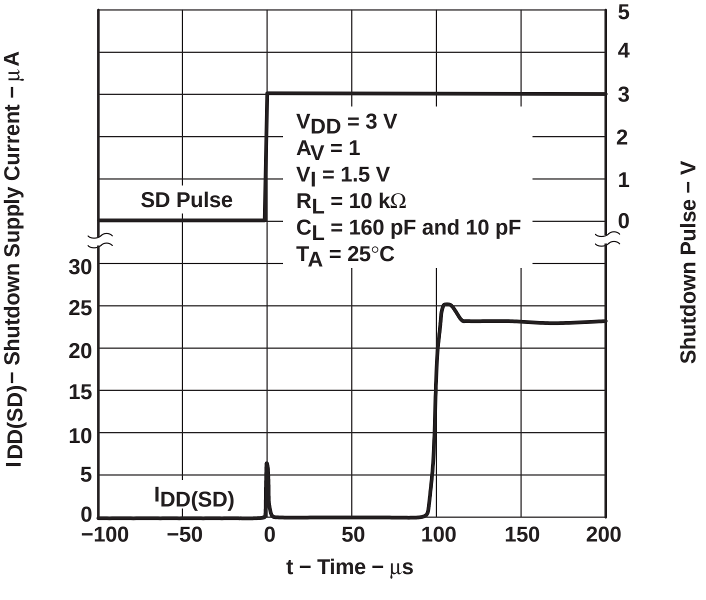


Figure 39

TYPICAL CHARACTERISTICS

SHUTDOWN SUPPLY CURRENT AND SHUTDOWN PULSE vs TIME

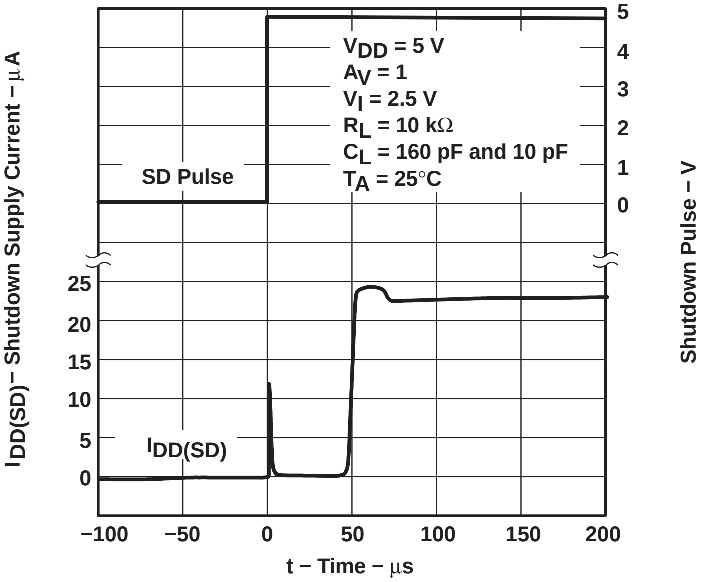


Figure 40

SHUTDOWN SUPPLY CURRENT AND SHUTDOWN PULSE vs TIME

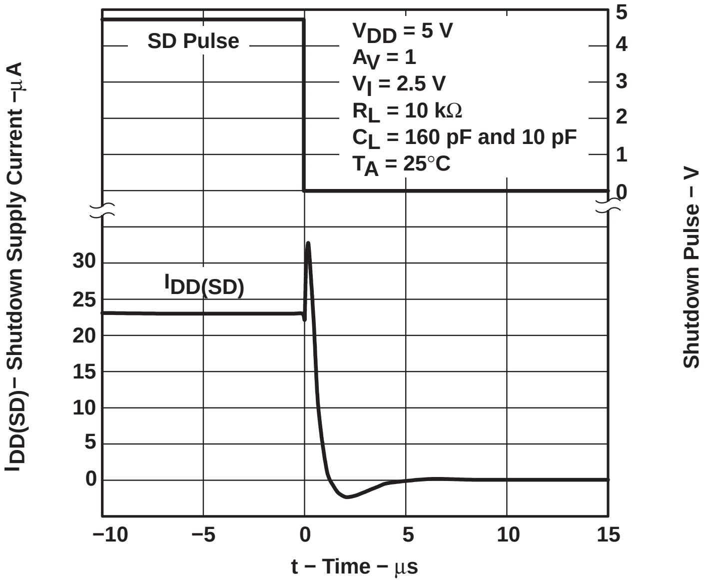


Figure 41

TYPICAL CHARACTERISTICS

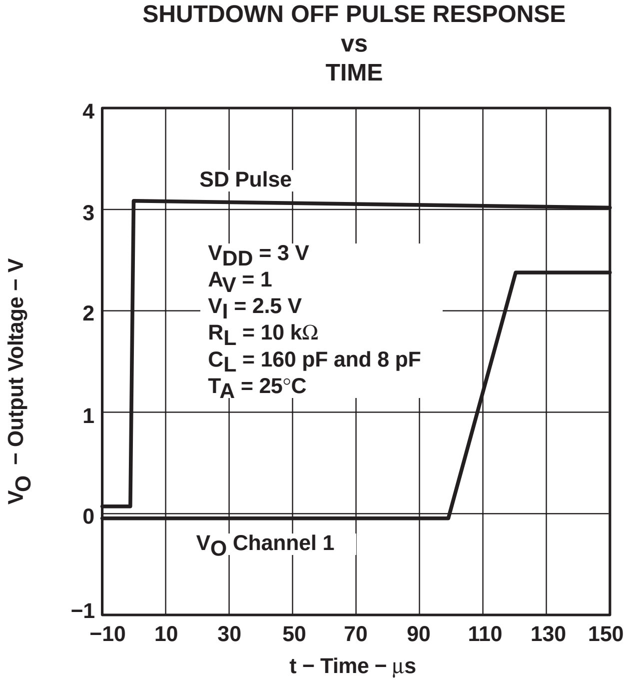


Figure 42

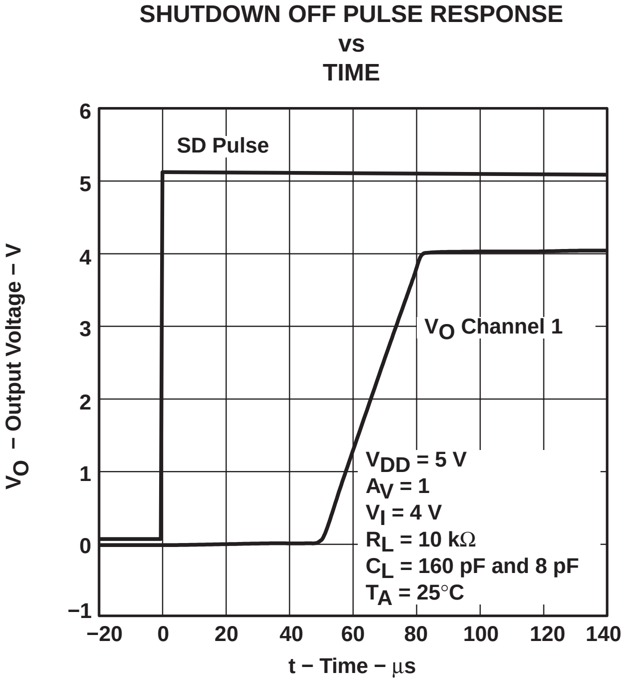


Figure 43

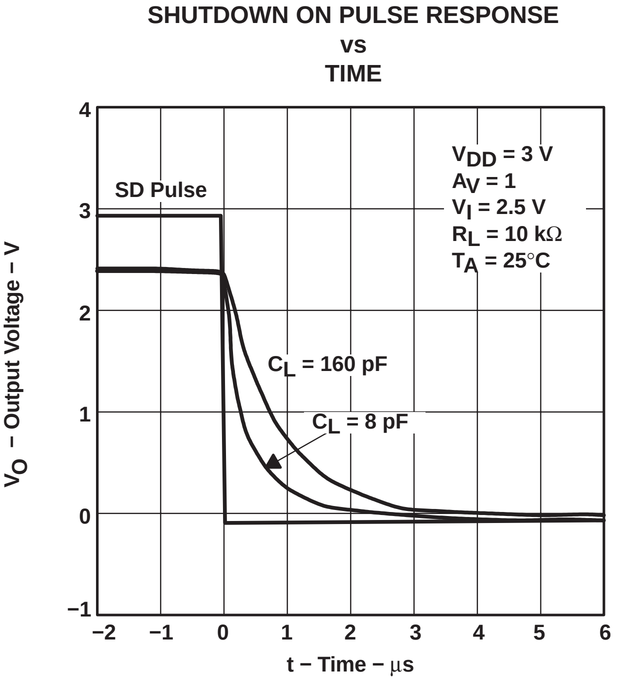


Figure 44

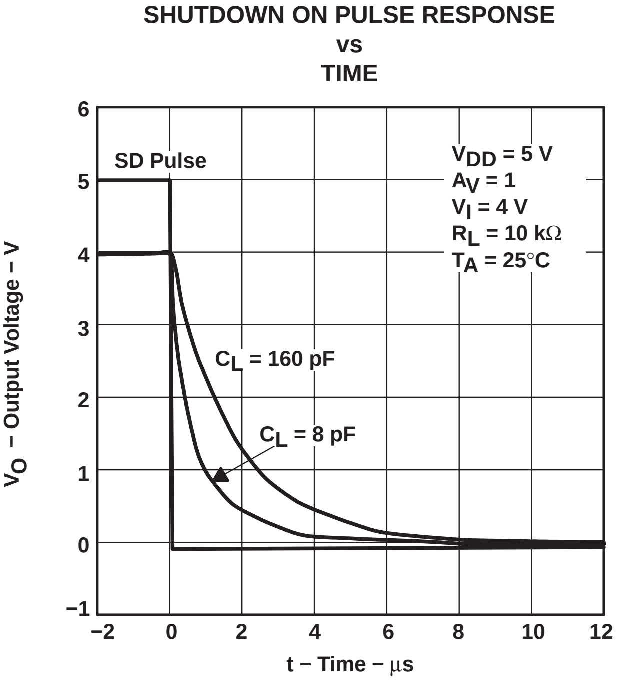


Figure 45

TYPICAL CHARACTERISTICS

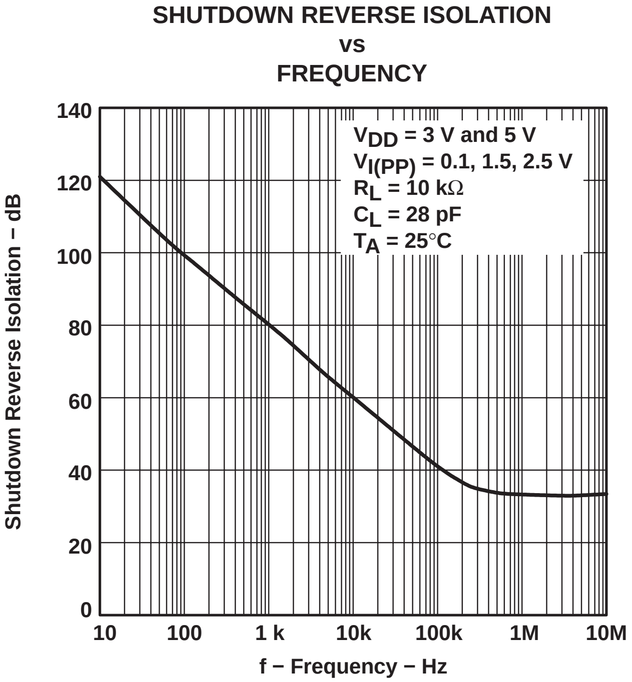


Figure 46

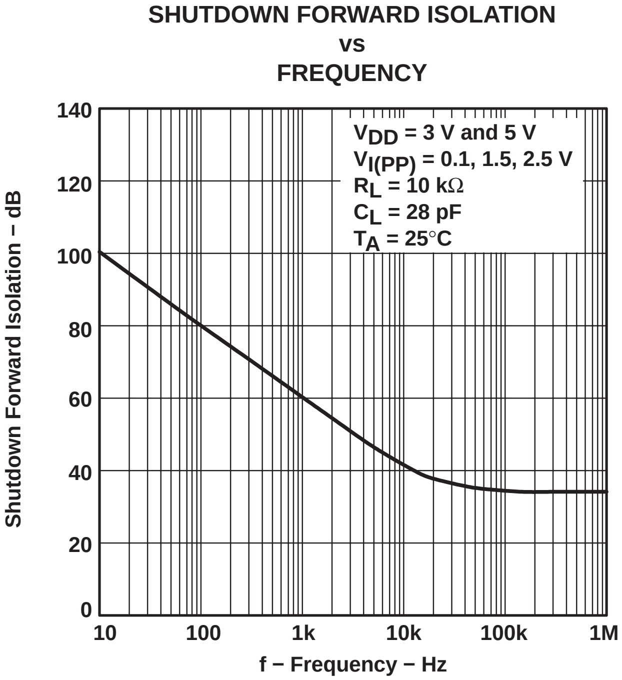


Figure 47

PARAMETER MEASUREMENT INFORMATION

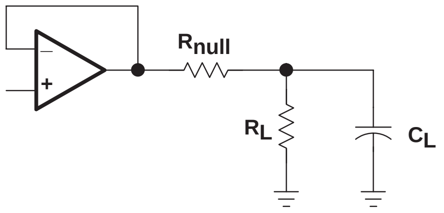


Figure 48

APPLICATION INFORMATION

shutdown function

Three members of the TLV245x family (TLV2450/3/5) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is pulled to the voltage level on the GND terminal of the device, the supply current is reduced to 16 nA/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal must be pulled high. The shutdown terminal should never be left floating. The shutdown terminal threshold is always referenced to the GND terminal of the device. Therefore, when operating the device with split supply voltages (e.g. ±2.5 V), the shutdown terminal needs to be pulled to $V_{DD}-$ (not system ground) to disable the operational amplifier.

The amplifier's output with a shutdown pulse is shown in Figures 42, 43, 44, and 45. The amplifier is powered with a single 5-V supply and configured as a noninverting configuration with a gain of 5. The amplifier turnon and turnoff times are measured from the 50% point of the shutdown pulse to the 50% point of the output waveform. The times for the single, dual, and quad are listed in the data tables.

Figures 46 and 47 show the amplifier's forward and reverse isolation in shutdown. The operational amplifier is powered by ±1.35-V supplies and configured as a voltage follower ($A_V = 1$). The isolation performance is plotted across frequency using 0.1-V_{PP}, 1.5-V_{PP}, and 2.5-V_{PP} input signals. During normal operation, the amplifier would not be able to handle a 2.5-V_{PP} input signal with a supply voltage of ±1.35 V since it exceeds the common-mode input voltage range (V_{ICR}). However, this curve illustrates that the amplifier remains in shutdown even under a worst case scenario.

driving a capacitive load

When the amplifier is configured in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 49. A minimum value of 20 Ω should work well for most applications.

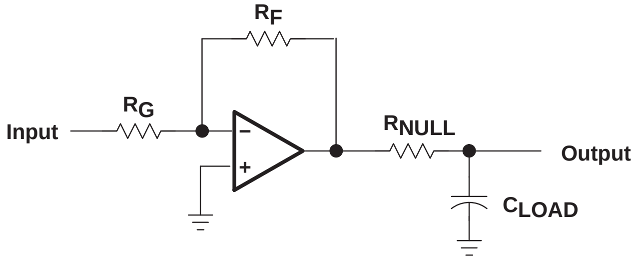
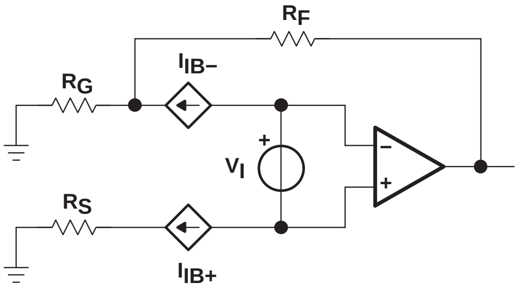


Figure 49. Driving a Capacitive Load

APPLICATION INFORMATION

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

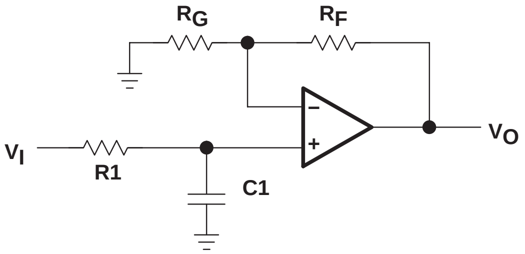


$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm \left(I_{IB+}\right) \times R_S\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm \left(I_{IB-}\right) \times R_F$$

Figure 50. Output Offset Voltage Model

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 51).

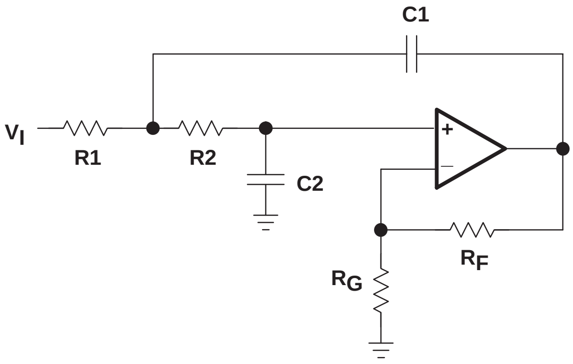


$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

Figure 51. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.



R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 52. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

general power dissipation considerations

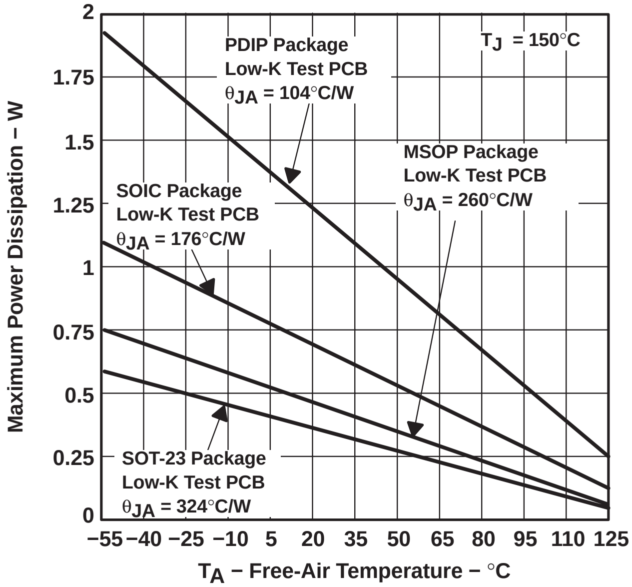
For a given θ_{JA}, the maximum power dissipation is shown in Figure 53 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of TLV245x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

**MAXIMUM POWER DISSIPATION
vs
FREE-AIR TEMPERATURE**



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 53. Maximum Power Dissipation vs Free-Air Temperature

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 1) and subcircuit in Figure 54 are generated using the TLV245x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 1: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers,” *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).

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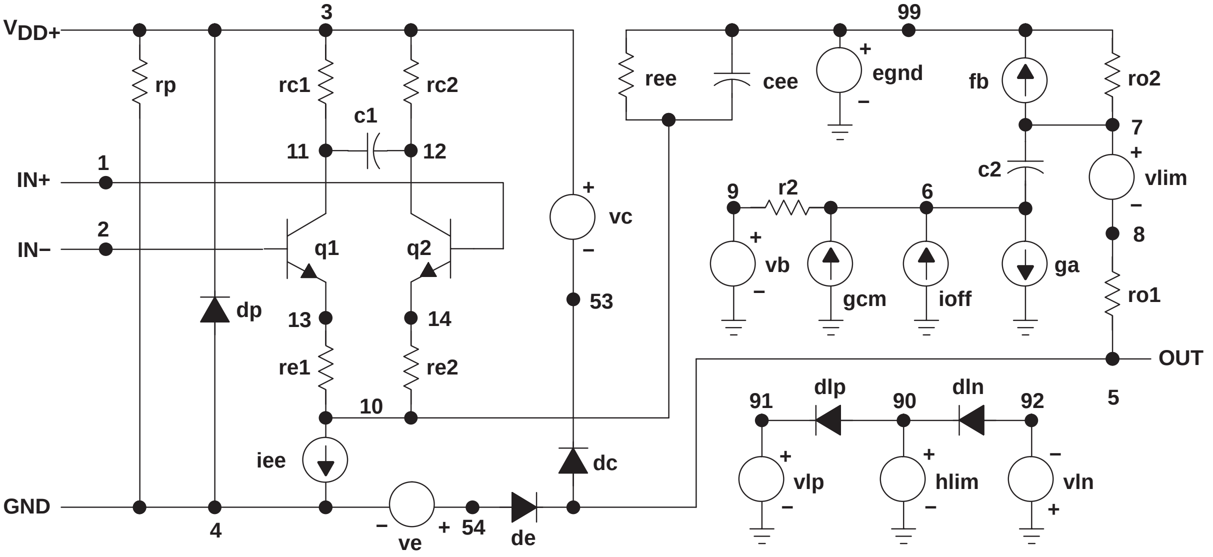
APPLICATION INFORMATION



```
* AMP_TLV2450−X operational amplifier ”macromodel” subcircuit
* created using Parts release 8.0 on 10/12/98 at 11:06
* Parts is a MicroSim product.
*
* connections:              noninverting input
*                           |  inverting input
*                           |  |  positive power supply
*                           |  |  |  negative power supply
*                           |  |  |  |  output
*                           |  |  |  |  |
.subckt AMP_TLV2450−X 1 2 3 4 5
*
        C1      11      12      354.48E−15
        C2      6       7       7.5000E−12
        CEE     10      99      42.237E−15
        DC      5       53      dy
        DE      54      5       dy
        DLP     90      91      dx
        DLN     92      90      dx
        DP      4       3       dx
        EGND    99      0       poly(2) (3,0) (4,0) 0 .5 .5
        FB      7       99      poly(5) vb vc ve vlp vln 0
        + 207.31E6 −1E3 1E3 210E6 −210E6
        GA      6       0       11      12 15.254E−6
        GCM     0       6       10      99 48.237E−12
IEE     10      4       dc      938.61E−9
HLIM    90      0       vlim 1K
Q1      11      2       13 qx1
Q2      12      1       14 qx2
R2      6       9       100.00E3
RC1     3       11      65.557E3
RC2     3       12      65.557E3
RE1     13      10      10.367E3
RE2     14      10      10.367E3
REE     10      99      213.08E6
RO1     8       5       10
RO2     7       99      10
RP      3       4       147.06
VB      9       0       dc 0
VC      3       53      dc .82
VE      54      4       dc .82
VLIM    7       8       dc 0
VLP     91      0       dc 38
VLN     0       92      dc 38
.model  dx      D(Is=800.00E−18)
.model  dy      D(Is=800.00E−18 Rs=1m Cjo=10p)
.model  qx1     NPN(Is=800.00E−18 Bf=843.08)
.model  qx2     NPN(Is=800.0000E−18 Bf=843.08)
.ends
```

Figure 54. Boyle Macromodel and Subcircuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2450AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450AI	Samples
TLV2450AIP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2450AI	Samples
TLV2450CDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	VAQC	Samples
TLV2450CDBVT	OBSOLETE	SOT-23	DBV	6		TBD	Call TI	Call TI	0 to 70	VAQC	
TLV2450CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLV2450C	Samples
TLV2450ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2450I	Samples
TLV2450IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAQI	Samples
TLV2450IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VAQI	Samples
TLV2451AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2451AI	Samples
TLV2451AIP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2451AI	Samples
TLV2451CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2451C	Samples
TLV2451CDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	VARC	Samples
TLV2451CDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	VARC	Samples
TLV2451CDG4	ACTIVE	SOIC	D	8	75	TBD	Call TI	Call TI	0 to 70		Samples
TLV2451CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2451C	Samples
TLV2451CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLV2451C	Samples
TLV2451IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VARI	Samples
TLV2451IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VARI	Samples
TLV2451IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2451I	Samples
TLV2451IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2451I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2452AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2452AI	Samples
TLV2452AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2452AI	Samples
TLV2452AIP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2452AI	Samples
TLV2452CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2452C	Samples
TLV2452CDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	ABI	Samples
TLV2452CDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	ABI	Samples
TLV2452CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	2452C	Samples
TLV2452ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2452I	Samples
TLV2452IDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ABJ	Samples
TLV2452IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ABJ	Samples
TLV2452IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples
TLV2452IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2452I	Samples
TLV2452IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2452IP	Samples
TLV2453CDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ABK	Samples
TLV2453CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV2453C	Samples
TLV2453IDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ABL	Samples
TLV2454AID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2454AI	Samples
TLV2454AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2454AI	Samples
TLV2454AIN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2454AI	Samples
TLV2454AIPW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI		TY2454A	
TLV2454AIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2454A	Samples
TLV2454CD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	0 to 70	2454C	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2454CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLV2454C	Samples
TLV2454CPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TV2454	Samples
TLV2454CPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TV2454	Samples
TLV2454ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2454I	Samples
TLV2454IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2454I	Samples
TLV2454IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2454I	Samples
TLV2454IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2454	Samples
TLV2454IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2454	Samples
TLV2455AID	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2455AI	Samples
TLV2455AIDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2455AI	Samples
TLV2455AIN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2455AI	Samples
TLV2455AIPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2455A	Samples
TLV2455IDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2455I	Samples
TLV2455IPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2455	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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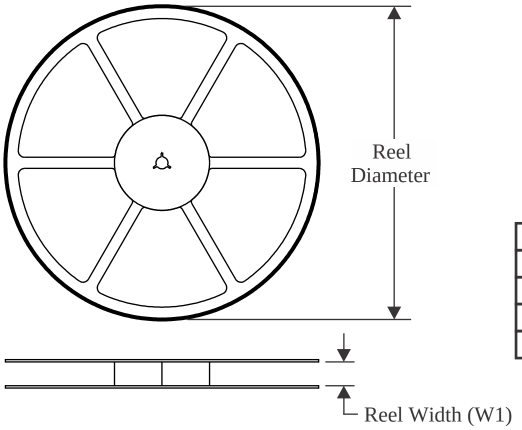
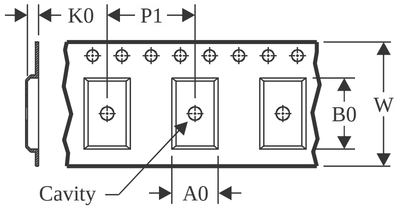
TAPE AND REEL INFORMATION

REEL DIMENSIONS

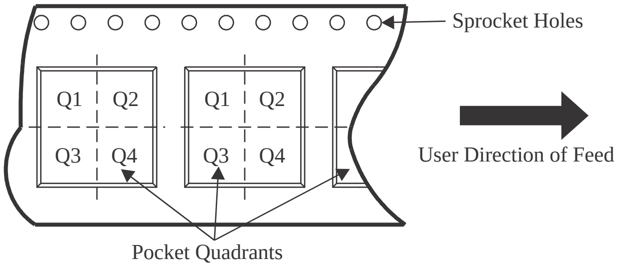


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

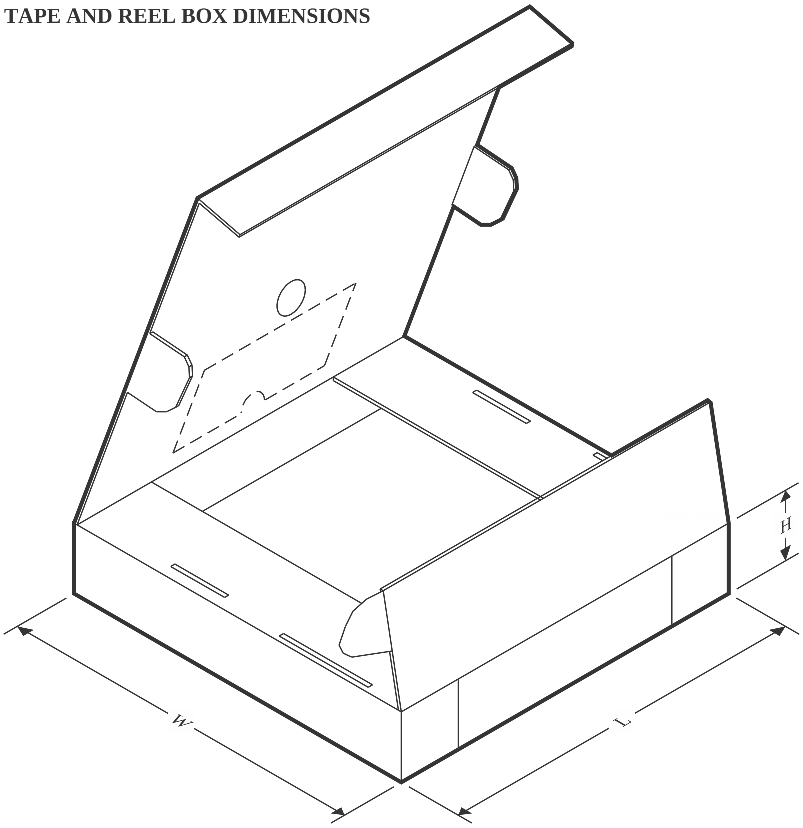


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2450AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2450CDBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2450CDBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2450IDBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2450IDBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2451AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2451CDBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2451CDBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2451CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2451IDBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2451IDBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2451IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2452AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2452CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2452CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2452CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2452IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2452IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2452IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2453CDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2453CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2453IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2454AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2454AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2454CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2454IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2454IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2455AIDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLV2455AIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2455IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

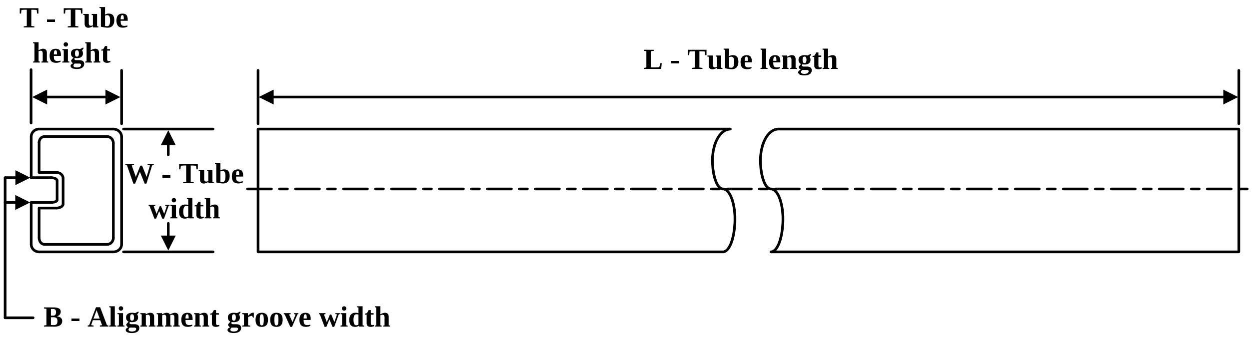


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2450AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2450CDBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TLV2450CDBVT	SOT-23	DBV	6	250	182.0	182.0	20.0
TLV2450IDBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TLV2450IDBVT	SOT-23	DBV	6	250	182.0	182.0	20.0
TLV2451AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2451CDBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TLV2451CDBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
TLV2451CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2451IDBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
TLV2451IDBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
TLV2451IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2452AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2452CDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV2452CDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV2452CDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2452IDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV2452IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0

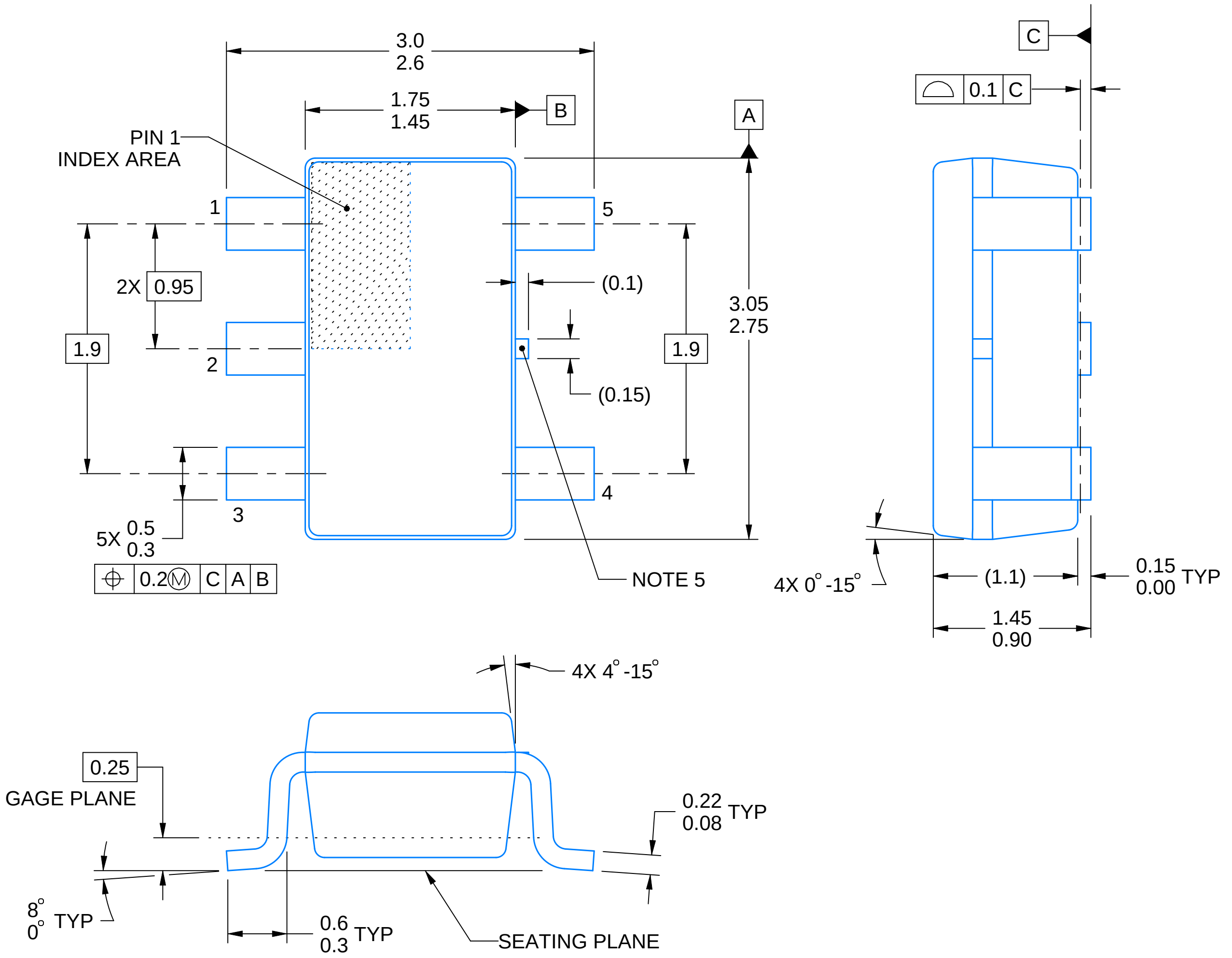
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2452IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2453CDGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TLV2453CDR	SOIC	D	14	2500	350.0	350.0	43.0
TLV2453IDGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TLV2454AIDR	SOIC	D	14	2500	350.0	350.0	43.0
TLV2454AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV2454CPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV2454IDR	SOIC	D	14	2500	350.0	350.0	43.0
TLV2454IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV2455AIDR	SOIC	D	16	2500	350.0	350.0	43.0
TLV2455AIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TLV2455IDR	SOIC	D	16	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

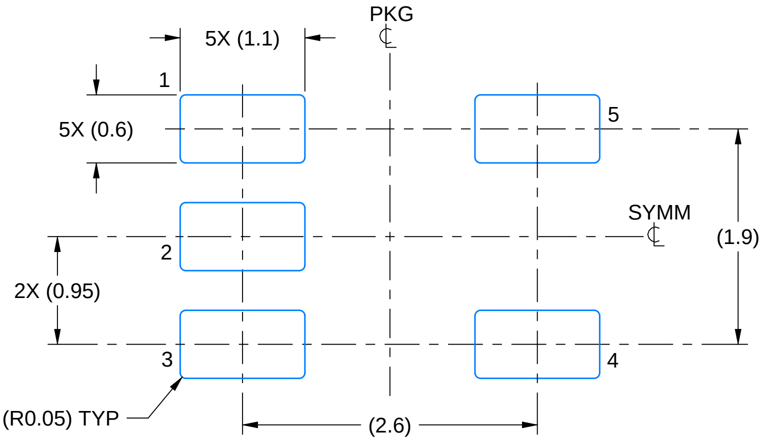
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV2450AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2450CP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2450ID	D	SOIC	8	75	505.46	6.76	3810	4
TLV2450ID	D	SOIC	8	75	507	8	3940	4.32
TLV2451AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2451CD	D	SOIC	8	75	505.46	6.76	3810	4
TLV2451CD	D	SOIC	8	75	507	8	3940	4.32
TLV2451CP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2451IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2452AID	D	SOIC	8	75	505.46	6.76	3810	4
TLV2452AID	D	SOIC	8	75	507	8	3940	4.32
TLV2452AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2452CD	D	SOIC	8	75	507	8	3940	4.32
TLV2452CD	D	SOIC	8	75	505.46	6.76	3810	4
TLV2452CDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
TLV2452ID	D	SOIC	8	75	507	8	3940	4.32
TLV2452ID	D	SOIC	8	75	505.46	6.76	3810	4
TLV2452IDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
TLV2452IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2454AID	D	SOIC	14	50	505.46	6.76	3810	4
TLV2454AIN	N	PDIP	14	25	506	13.97	11230	4.32
TLV2454CN	N	PDIP	14	25	506	13.97	11230	4.32
TLV2454CPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLV2454ID	D	SOIC	14	50	505.46	6.76	3810	4
TLV2454IN	N	PDIP	14	25	506	13.97	11230	4.32
TLV2454IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLV2455AID	D	SOIC	16	40	505.46	6.76	3810	4
TLV2455AIN	N	PDIP	16	25	506	13.97	11230	4.32
TLV2455IPW	PW	TSSOP	16	90	530	10.2	3600	3.5



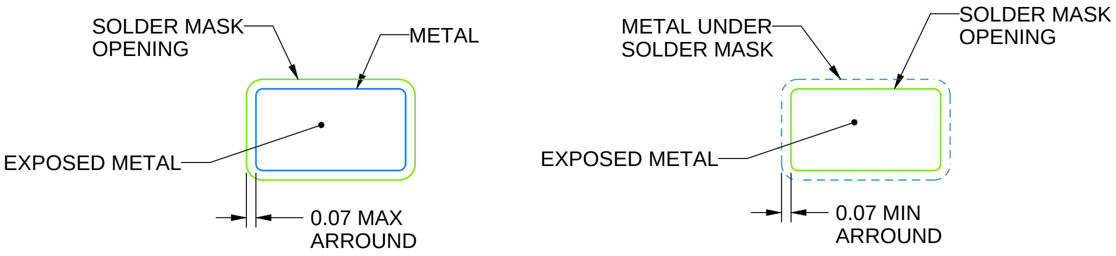
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

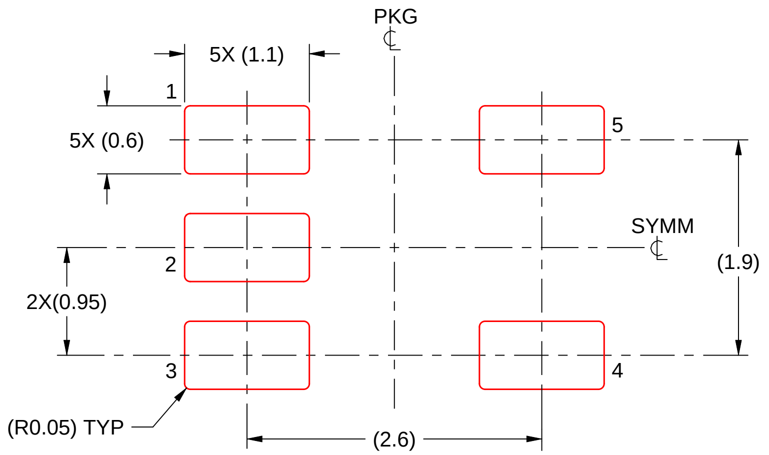
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

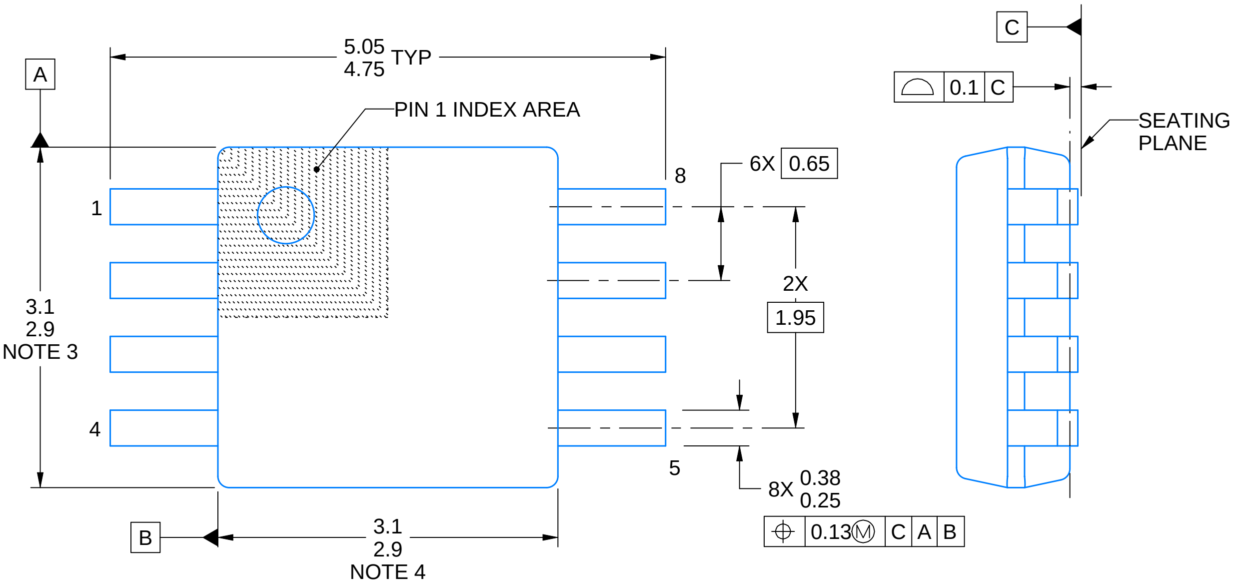


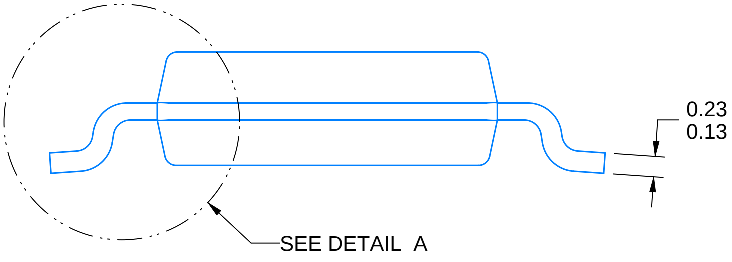
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

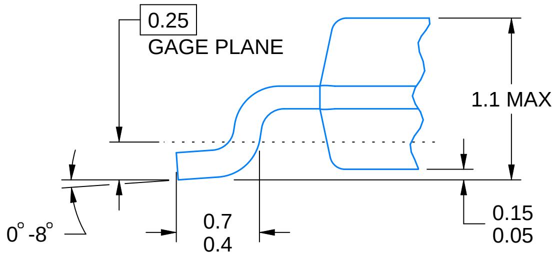
4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.







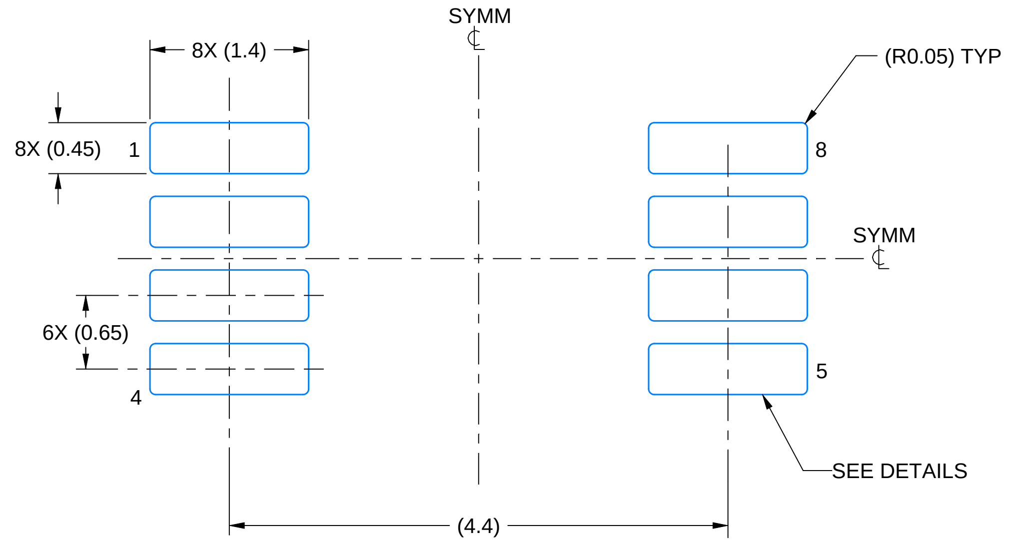
DETAIL A
TYPICAL

4214862/A 04/2023

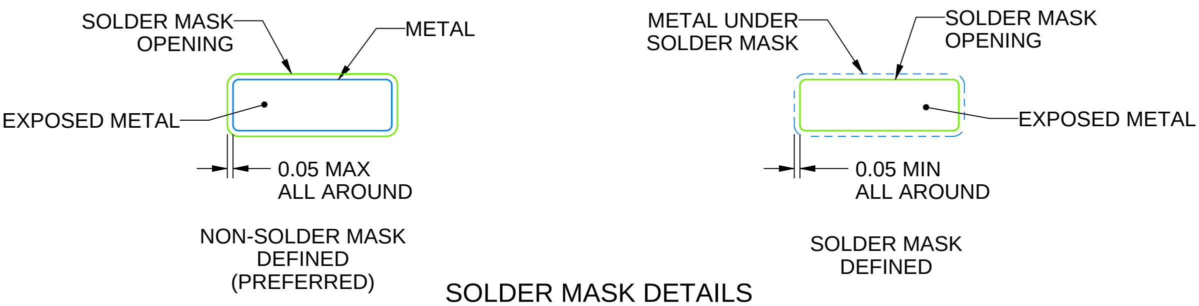
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



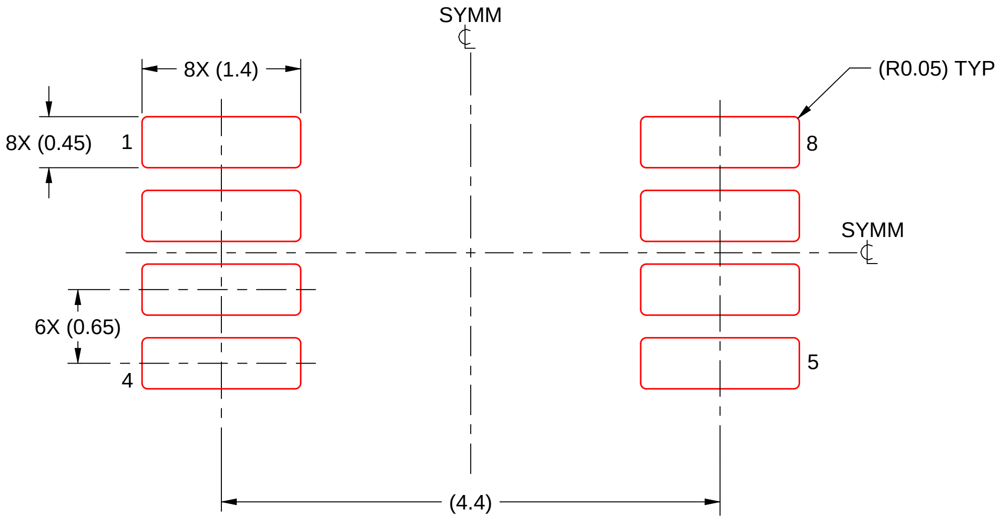
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



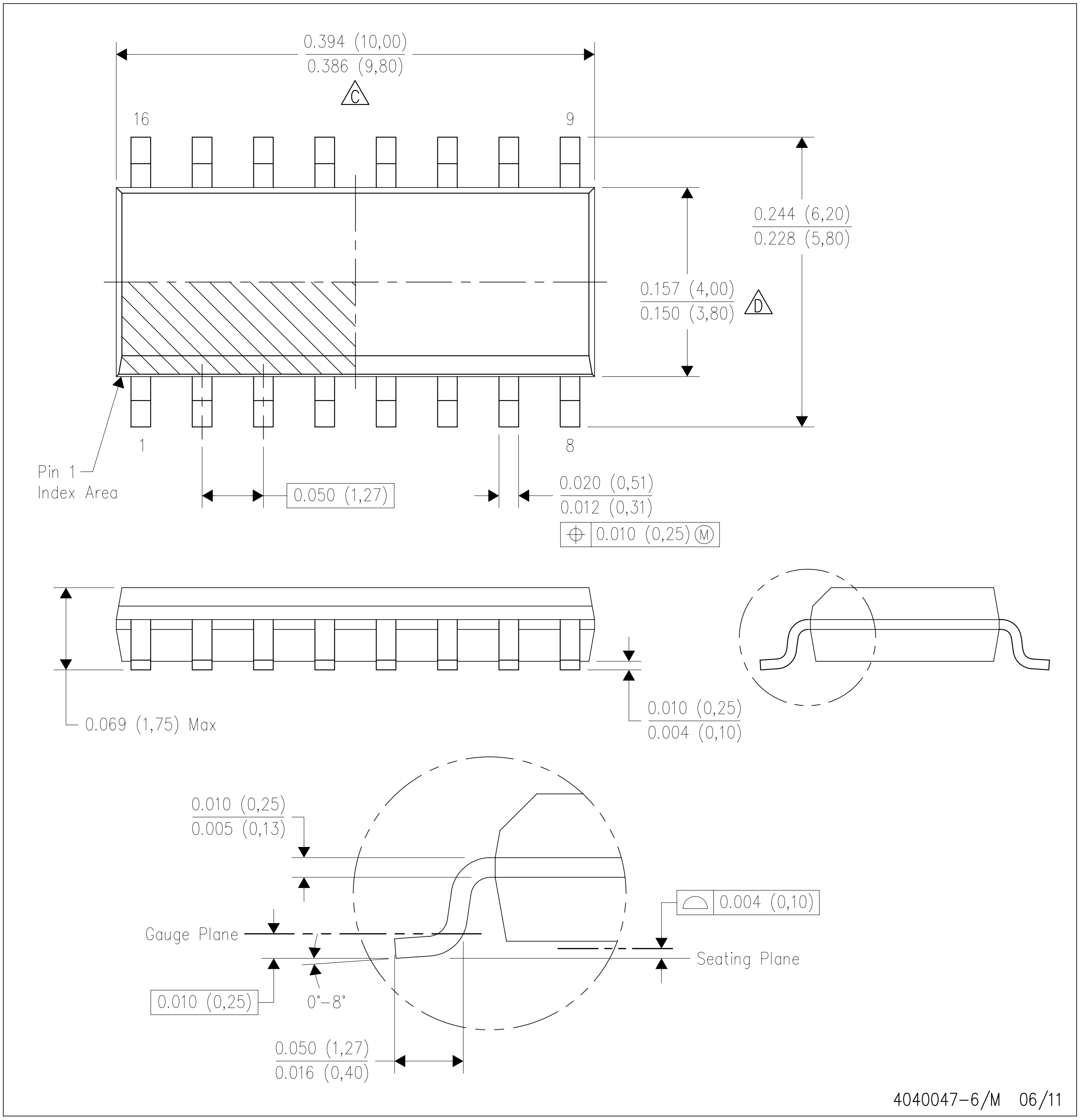
SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

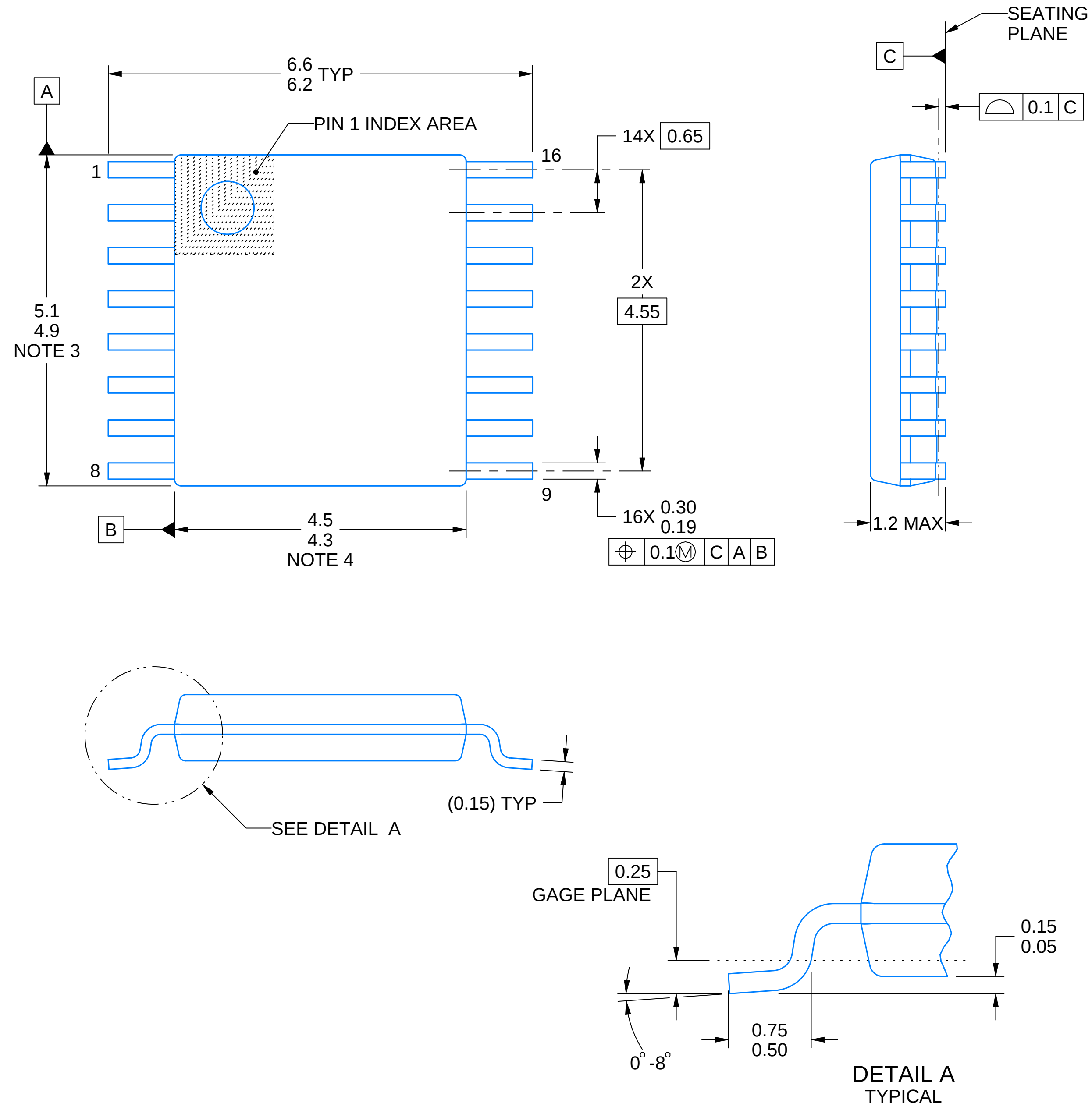
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



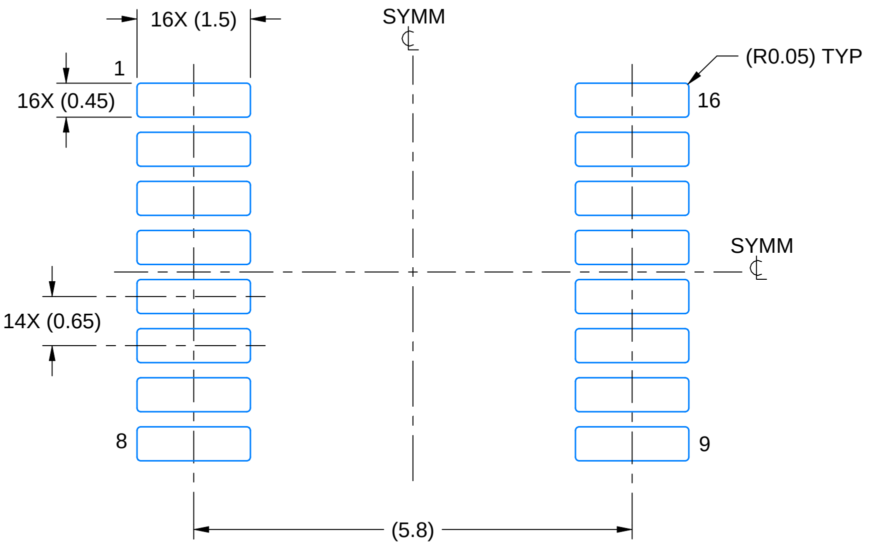
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK
DEFINED
(PREFERRED)

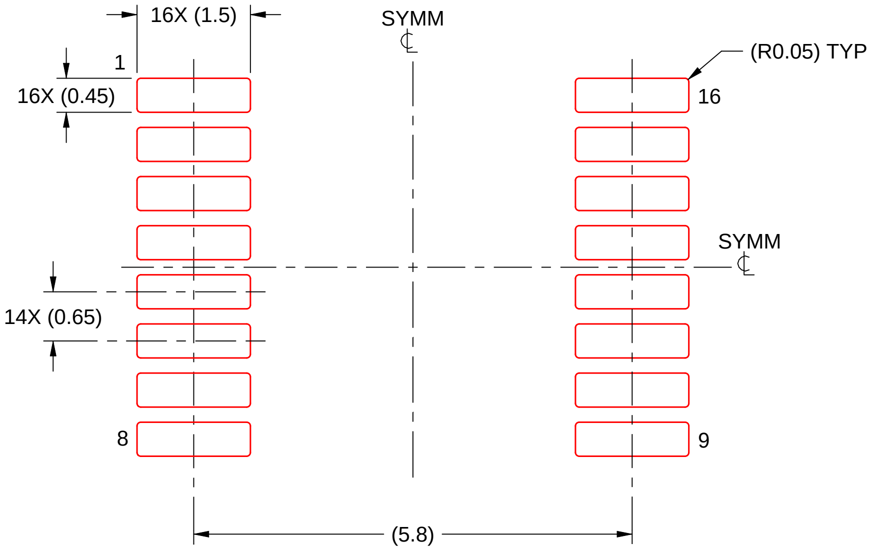
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



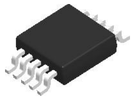
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

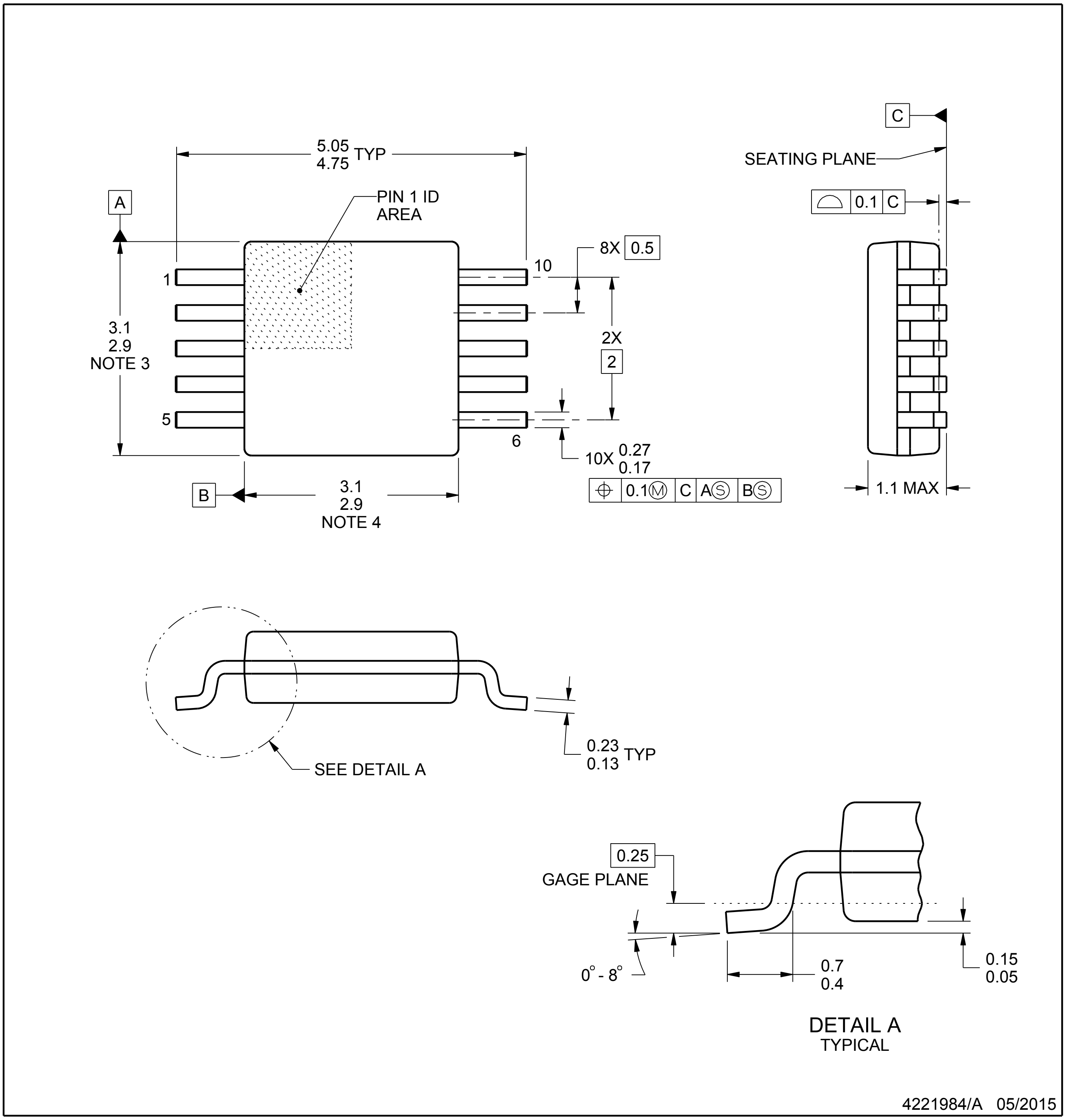
PACKAGE OUTLINE



DGS0010A

VSSOP - 1.1 mm max height

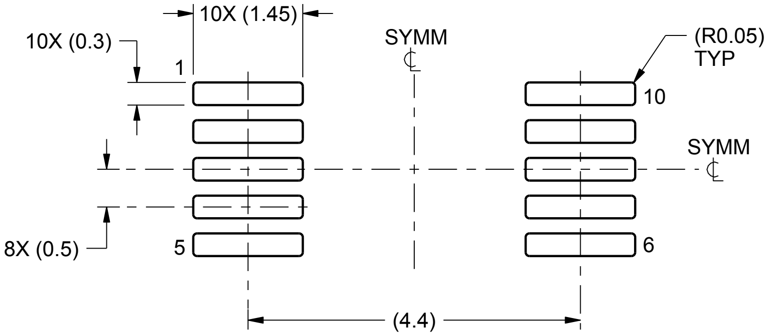
SMALL OUTLINE PACKAGE



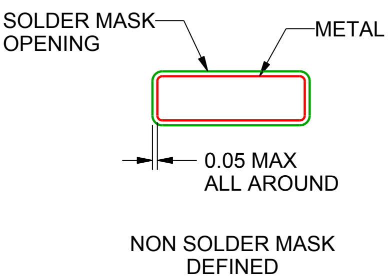
4221984/A 05/2015

NOTES:

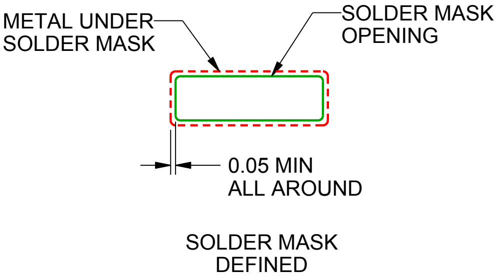
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED



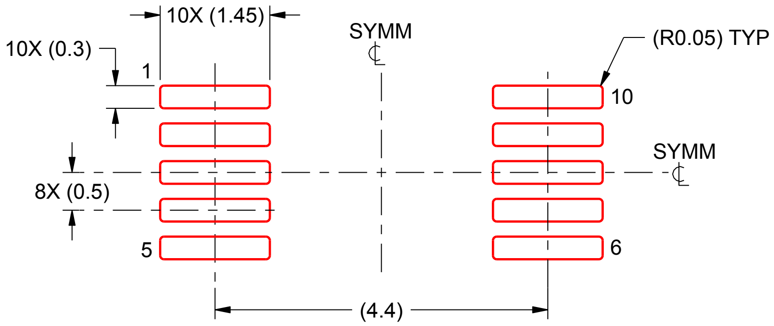
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

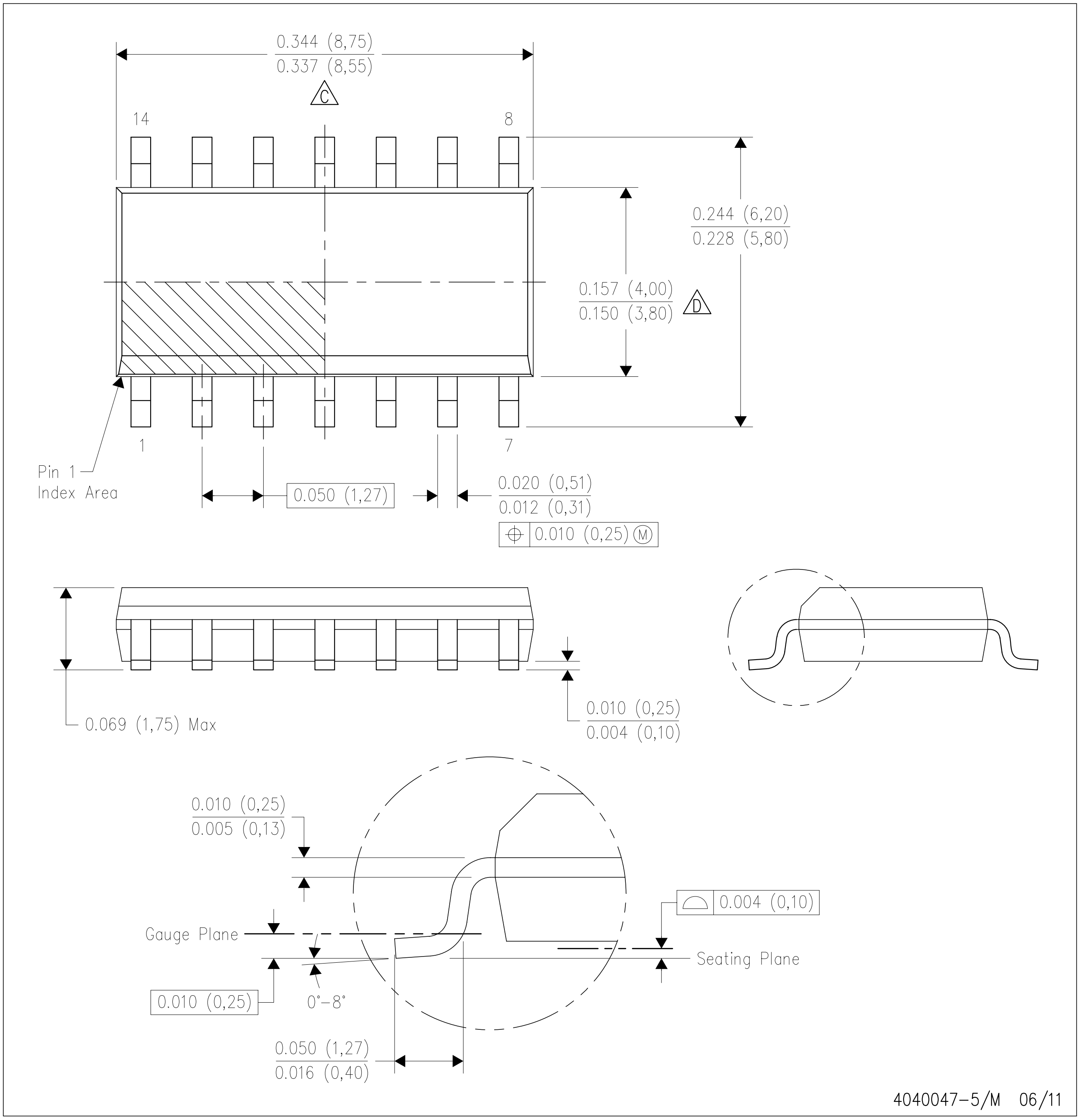


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

NOTES: (continued)

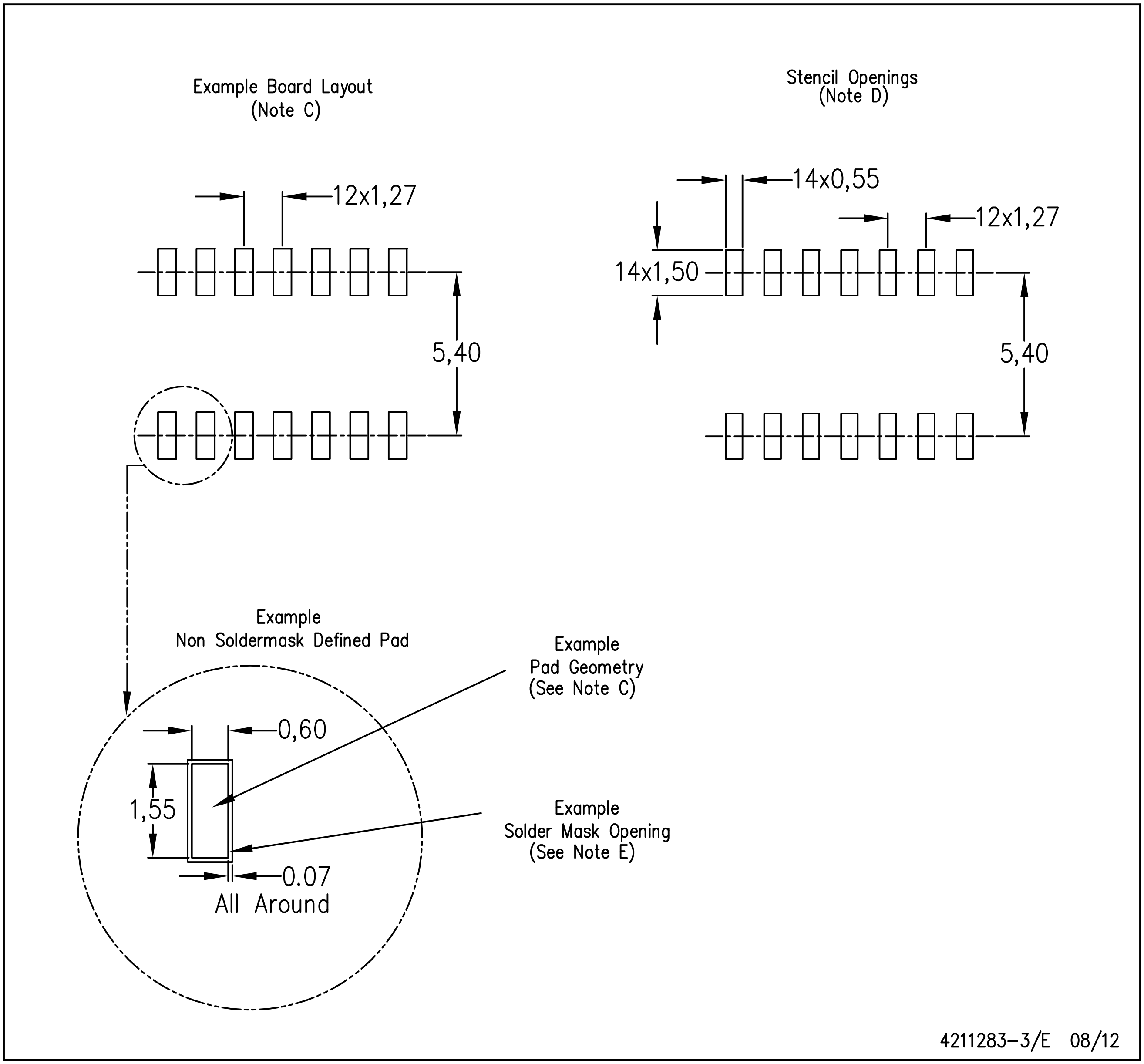
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



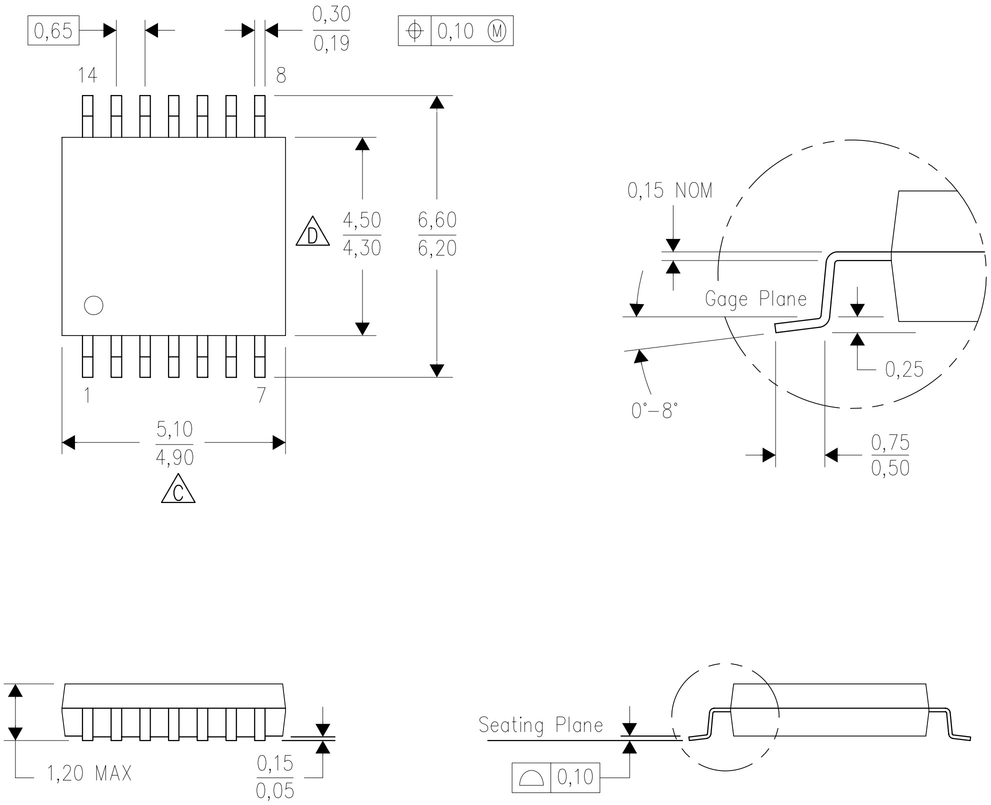
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

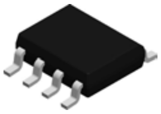
PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



4040064-3/G 02/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153

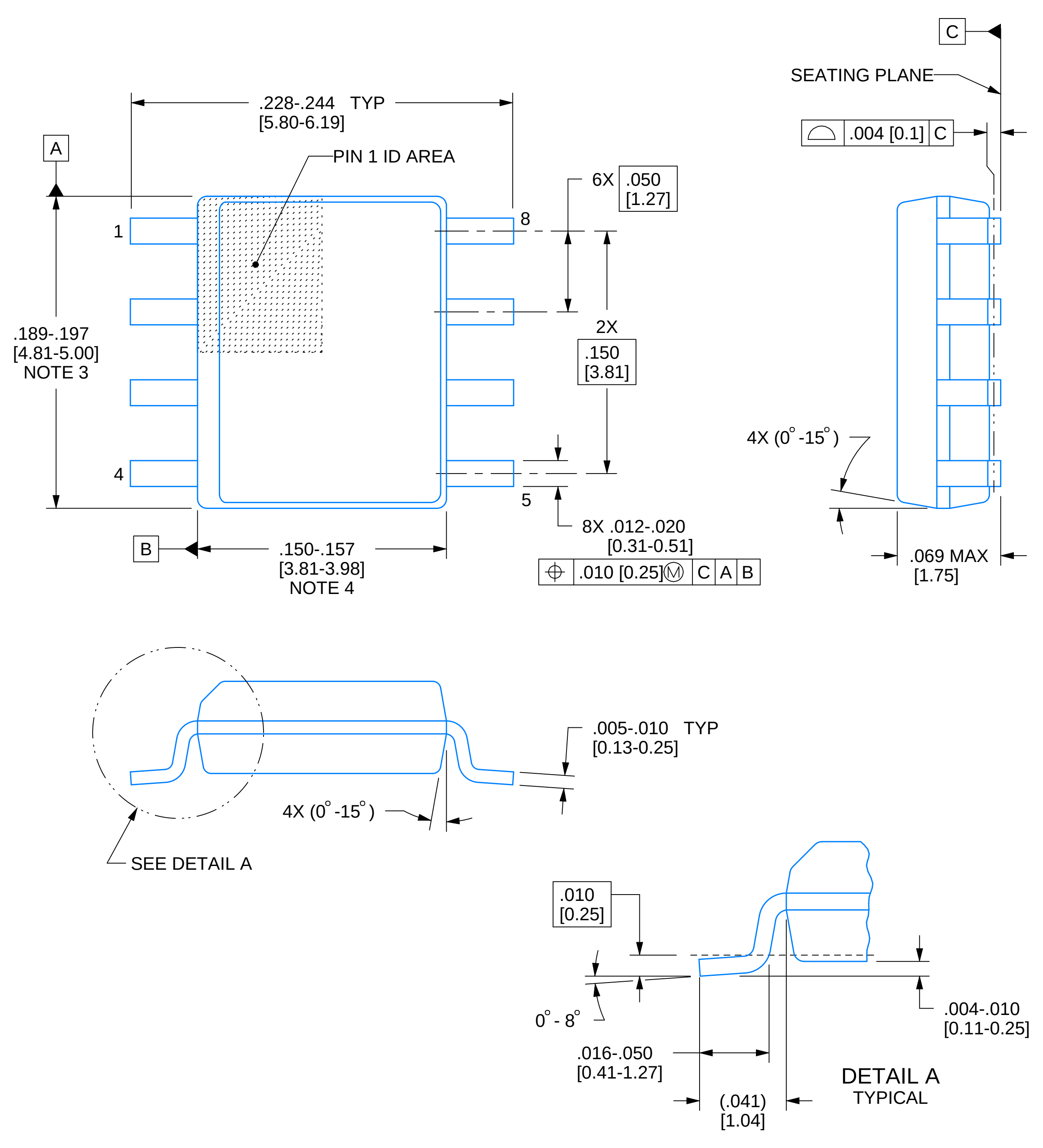
D0008A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

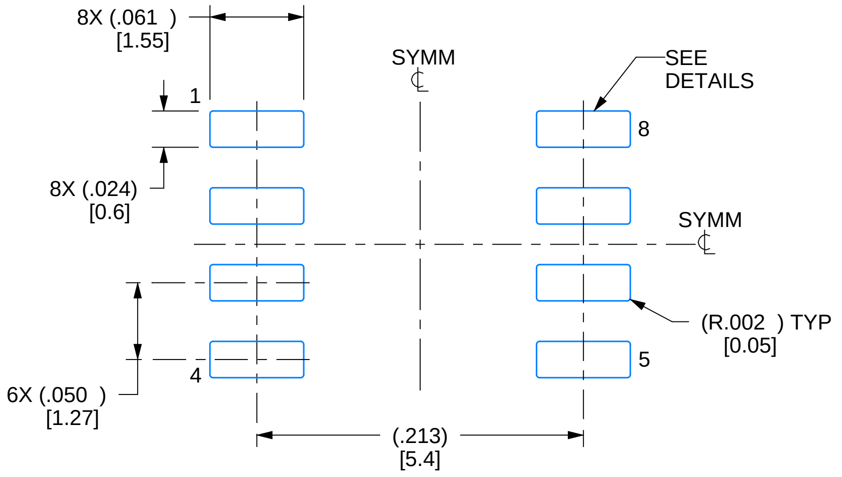
SMALL OUTLINE INTEGRATED CIRCUIT



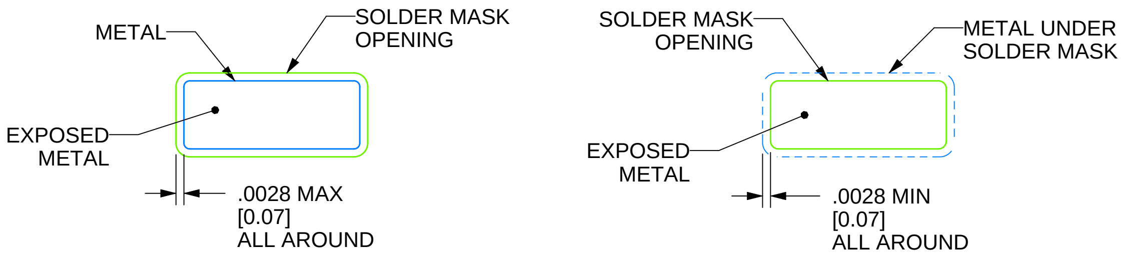
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



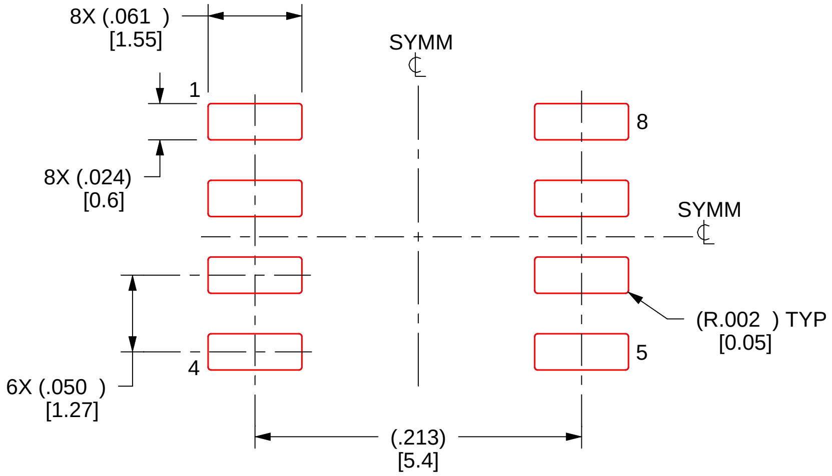
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

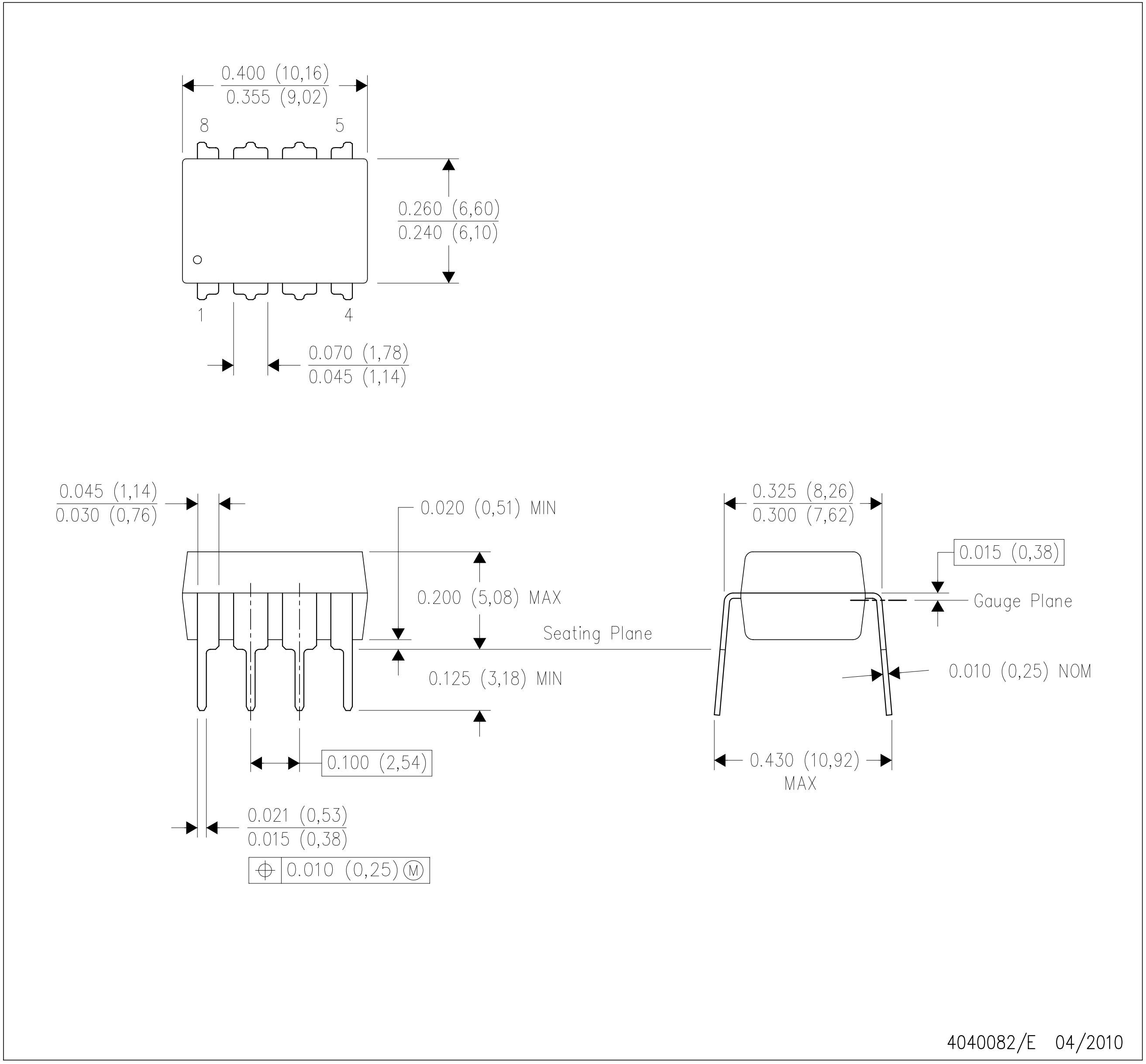


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

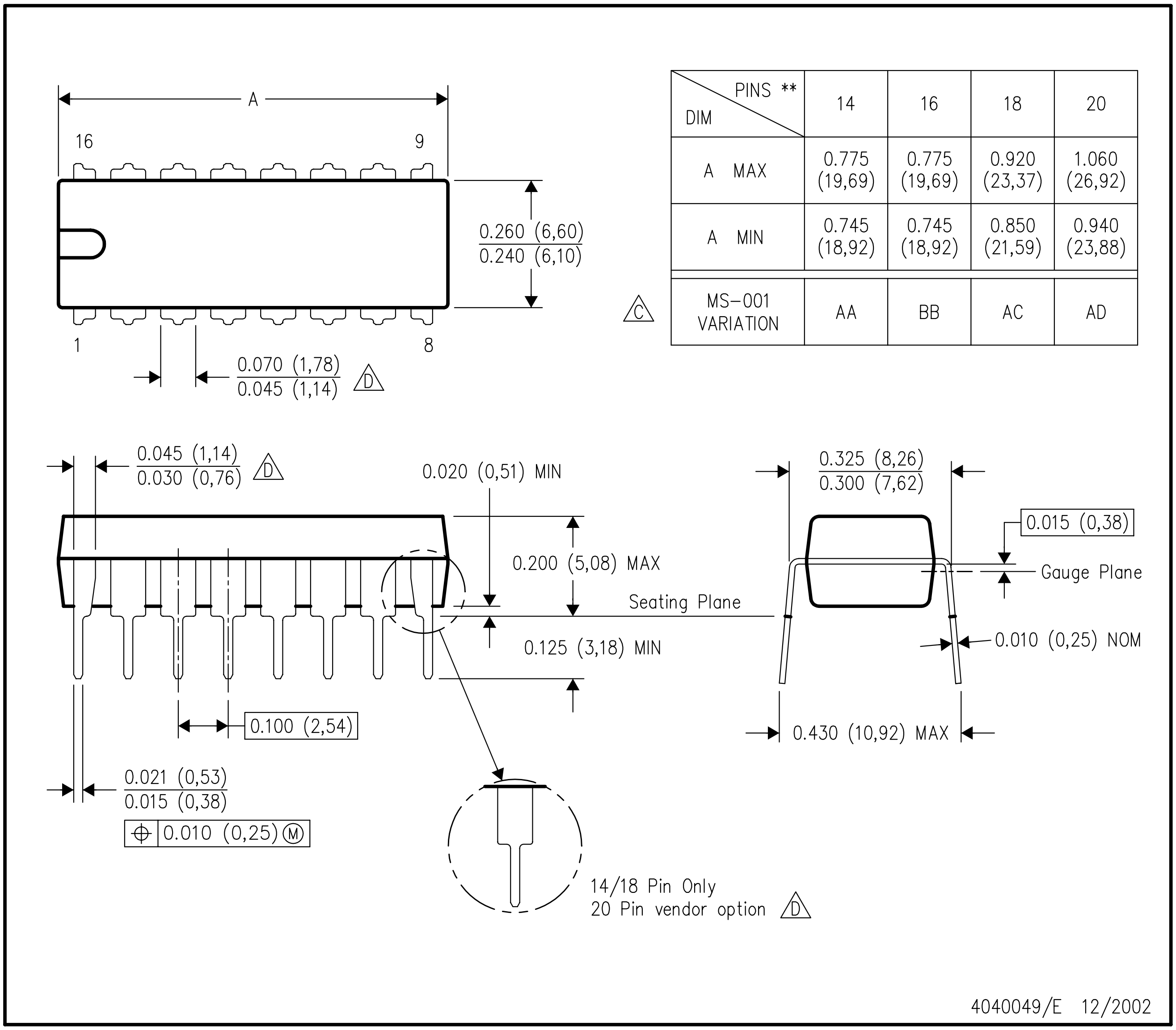
P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

N (R–PDIP–T**)　　PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS–001 VARIATION	AA	BB	AC	AD

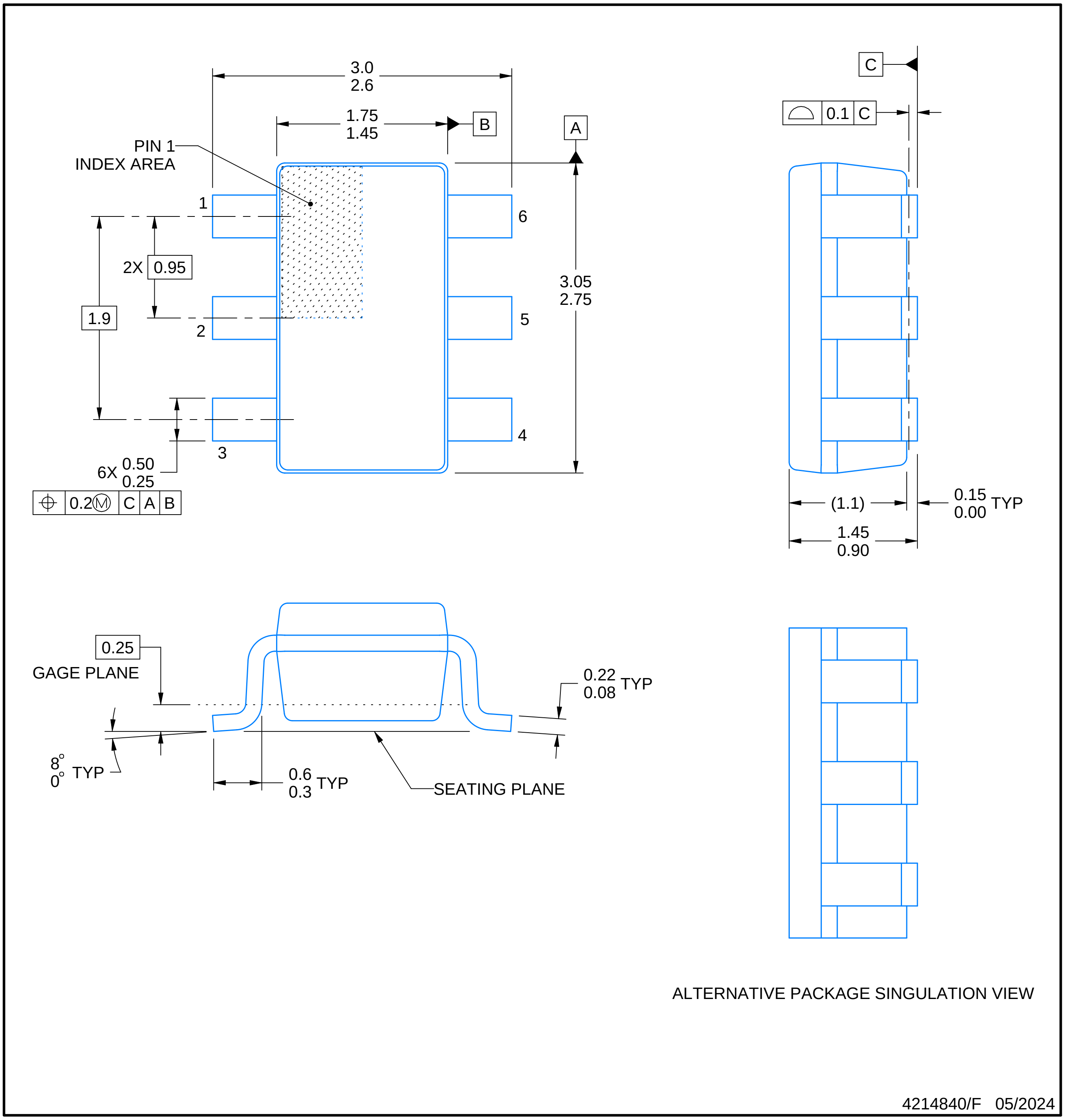
4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

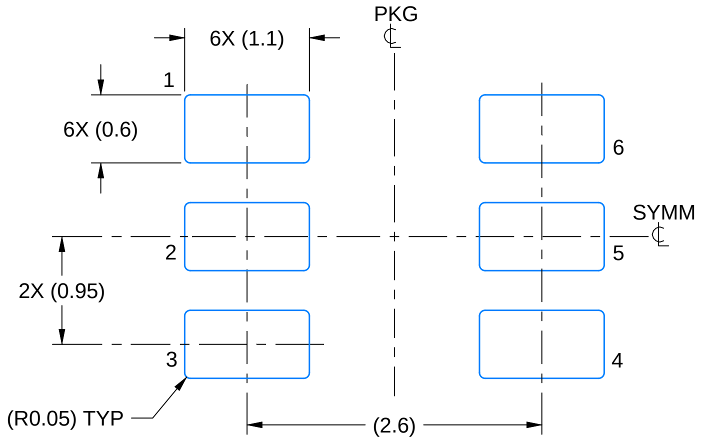
SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

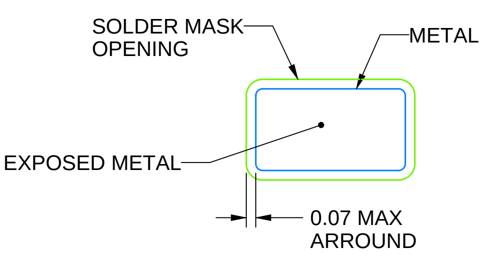


NOTES:

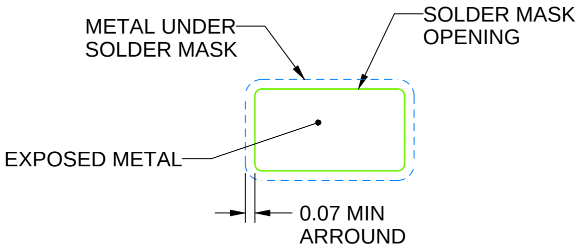
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

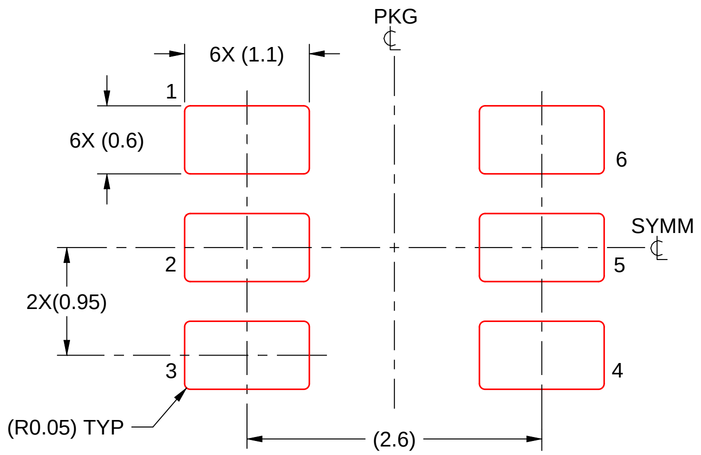


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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