TLV323x 20ns High-Speed Comparator with Rail-to-Rail Input

1 Features

- Propagation delay: 20ns
- Input offset voltage: +/- 4mV maximum
- Low supply current: 200µA per channel
- Input voltage range extends 100mV beyond either rail
- Internal hysteresis: 1.55mV
- Power-on-reset provides a known startup condition (Dual channel only)
- Push-pull output
- Temperature range: -40°C to +125°C

2 Applications

- Mobile phones & tablets
- Headsets/headphones & earbuds
- PC & notebooks
- Gas detector
- Smoke & heat detector
- Motion Detector
- Gas meter
- Servo drive position sensor

3 Description

The TLV323x are a family of 5V single and dual channel comparators with push-pull outputs. The family has an excellent speed-to-power combination with a propagation delay of 20ns and a full supply voltage range of 2.7V to 5V with a quiescent supply current of only 200µA per channel.

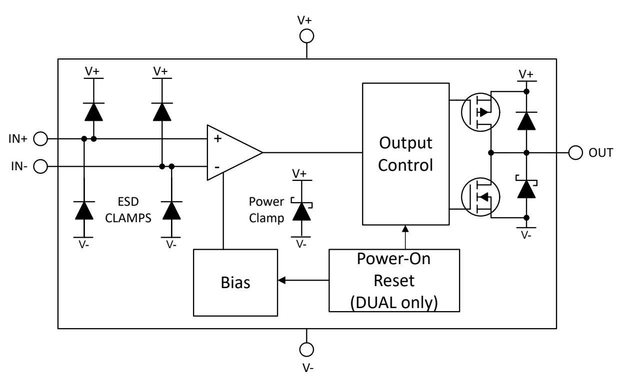
Likewise, the TLV323x are conveniently available in standard leaded and leadless packages with features such as rail-to-rail inputs, low offset voltage, and large output drive current. These features along with fast response time make the comparators well-suited for current sensing, zero-cross detection, and a variety of other applications where precision and speed is critical.

All devices are specified for operation across the expanded temperature range of –40°C to 125°C.

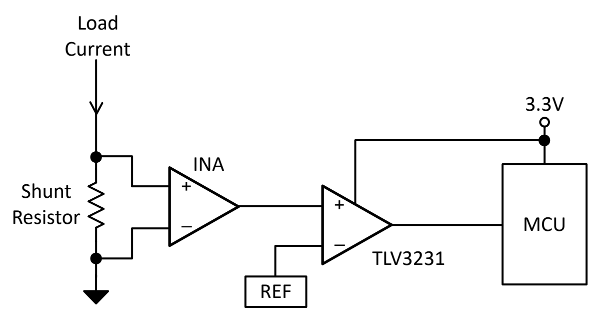
Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM (2)
TLV3231	SC-70 (5)	1.25mm × 2.00mm
	SOT-23 (5)	1.60mm × 2.90mm
TLV3232	VSSOP (8)	3.00mm × 3.00mm
	WSON (8)	2.00mm × 2.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Block Diagram



Low-Side Current Sensing

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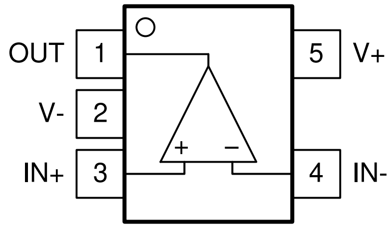
4 Pin Configuration and Functions

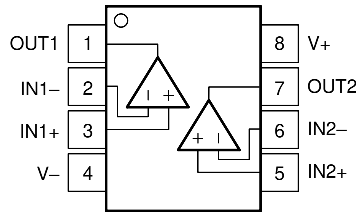
Pin Configurations: TLV3231 and TLV3232



DCK, DBV Packages
SC70, SOT-23-5
Top View
(Standard "North West" Pinout)

Table 4-1. Pin Functions: TLV3231

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1	O	Output
V-	2	-	Negative supply voltage
IN+	3	I	Non-inverting (+) input
IN-	4	I	Inverting (-) input
V+	5	-	Positive supply voltage



DGK, DSG Packages
8-Pin VSSOP, WSON
Top View

Table 4-2. Pin Functions: TLV3232

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	1	I	Noninverting input, channel 1
IN1–	2	I	Inverting input, channel 1
IN2–	3	I	Inverting input, channel 2
IN2+	4	I	Noninverting input, channel 2
OUT1	7	O	Output, channel 1
OUT2	6	O	Output, channel 2
V-	5	-	Negative (lowest) supply or ground
V+	8	-	Positive (highest) supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

	MIN	MAX	UNIT
Supply voltage V_S = (V+) - (V-)		6	V
Differential input voltage, VID	-6	6	V
Input pins (IN+, IN–) from (V-) [(2)]	– 0.5	(V+) + 0.5	V
Current into input pins (IN+, IN-)	-10	10	mA
Output short-circuit current	-100	100	mA
Output short-circuit duration		10	s
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Input terminals are diode-clamped to (V–) and (V+). Input signals that can swing more than 0.5V beyond the supply rails must be current-limited to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage V_S = (V+) - (V-)	2.7	5.5	V
Input voltage range	(V-) - 0.1	(V+) + 0.1	V
Ambient temperature, T_A	–40	125	°C

5.4 Thermal Information, TLV3231

THERMAL METRIC (1)		TLV3231 DBV (SOT-23) 5 PINS	TLV3231 DCK (SC70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	196.4	220	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	94	135	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63	65	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	30.5	34	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.6	65	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Thermal Information, TLV3232

THERMAL METRIC (1)		TLV3232 DGK (VSSOP) 8 PINS	TLV3232 DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	154.5	78.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.8	99.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.1	44.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.8	5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	87.4	44.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	19.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Electrical Characteristics

V_S = 2.7V to 5V, V_{CM} = V_S / 2; at T_A = 25°C (unless otherwise noted). Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Input Characteristics						
V_{IO}	Input Offset Voltage	V_S = 5V, V_{CM} = V_S / 2		±0.5	±4	mV
V_{IO}	Input Offset Voltage	V_S = 5V, V_{CM} = V_S / 2, T_A = -40 to 125℃			±4.5	mV
V_{HYS}	Hysteresis	V_S = 5V, V_{CM} = V_S / 2	0.5	1.55	3	mV
V_{HYS}	Hysteresis	V_S = 5V, V_{CM} = V_S / 2, T_A = -40 to 125℃			3.5	mV
V_{CM}	Common-mode voltage range		(V-) - 0.1		(V+)+0.1	V
I_B	Input bias current	V_S = 5V, V_{CM} = V_S / 2, T_A = -40 to 125℃		0.01	10	nA
I_{OS}	Input offset current	V_S = 5V, V_{CM} = V_S / 2			200	pA
C_{IN}	Input capacitance			2		pF
CMRR	Common-mode rejection ratio	V_{CM} = V_{EE} - 0.1V to V_{CC} + 0.1V		82		dB
DC Output Characteristics						
V_{OH}	Voltage swing from (V+)	V_S = 5V, (V-) = 0V, I_{Source} = 2mA			200	mV
V_{OL}	Voltage swing from (V-)	V_S = 5V, (V-) = 0V, I_{Sink} = 2mA			200	mV
I_{SC}	Short-circuit current	V_S = 5V, sourcing		45		mA
		V_S = 5V, sinking		45		
Power Supply						
I_Q	Supply current / Channel	V_S = 2.7V and 5V, no load, Output Low		200	250	uA
I_Q	Supply current / Channel	V_S = 2.7V and 5V, no load, Output Low, T_A = -40 to 125℃			350	uA
$V_{POR\ (postive)}$	Power-On Reset Voltage (dual only)			2.1		V
PSRR	Power Supply Rejection Ratio	V_S = 2.7V to 5.5V, no load, T_A = -40 to 125℃		92		dB

5.7 Switching Characteristics

For V_S = 5V, V_{CM} = V_S / 2; C_L = 15pF at T_A = 25°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high to-low (single)	Midpoint of input to midpoint of output, V_{OD} = 10mV		22		ns
t_{PHL}	Propagation delay time, high to-low (dual)	Midpoint of input to midpoint of output, V_{OD} = 10mV		25		ns
t_{PHL}	Propagation delay time, high to-low (single and dual)	Midpoint of input to midpoint of output, V_{OD} = 50mV		15	25	ns
t_{PLH}	Propagation delay time, low-to high (single)	Midpoint of input to midpoint of output, V_{OD} = 10mV		20		ns
t_{PLH}	Propagation delay time, low-to high (dual)	Midpoint of input to midpoint of output, V_{OD} = 10mV		25		ns
t_{PLH}	Propagation delay time, low-to high (single and dual)	Midpoint of input to midpoint of output, V_{OD} = 50mV		15	25	ns
f_{TOGGLE}	Input toggle frequency	V_{IN} = 200mV_{PP} Sine Wave, When output high reaches 90% of V_{CC} - V_{EE} or output low reaches 10% of V_{CC} - V_{EE}		55		MHz
t_R	Rise time	Measured from 20% to 80%		1.6		ns
t_F	Fall time	Measured from 20% to 80%		1.6		ns
t_{ON}	Power-up time	During power on, (V+) must exceed 2.1V for 4µs before the output reflects the input.		4.5		µs

5.8 Typical Characteristics

T_A = 25°C, V_S = 5V, C_L = 15pF, V_{CM} = V_S/2V, $V_{UNDERDRIVE}$ = 50mV, $V_{OVERDRIVE}$ = 50mV unless otherwise noted.

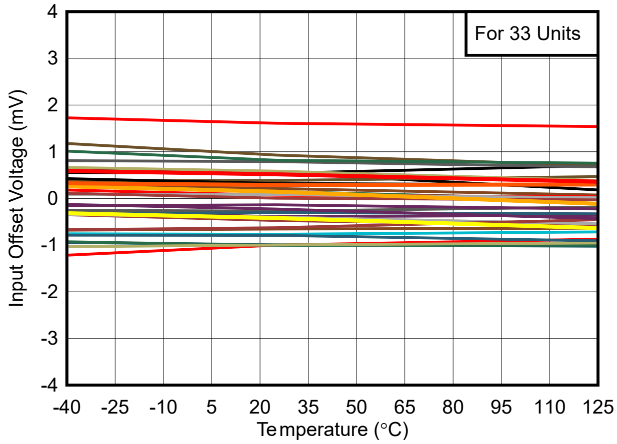


Figure 5-1. Offset vs. Temperature

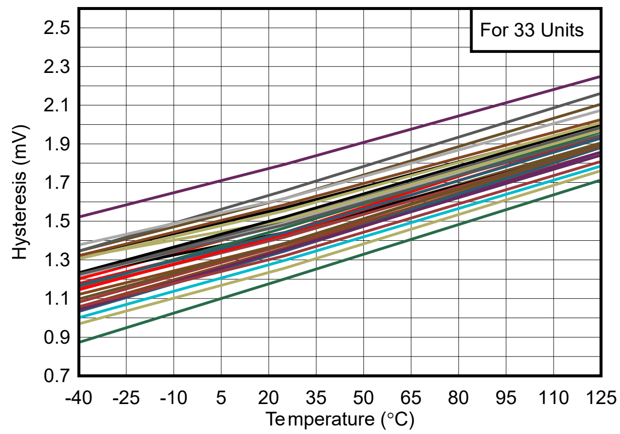


Figure 5-2. Hysteresis vs. Temperature

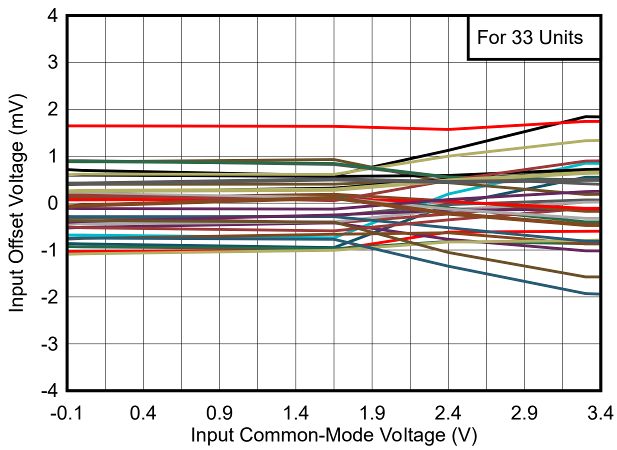


Figure 5-3. Offset vs. Common-Mode, 3.3V

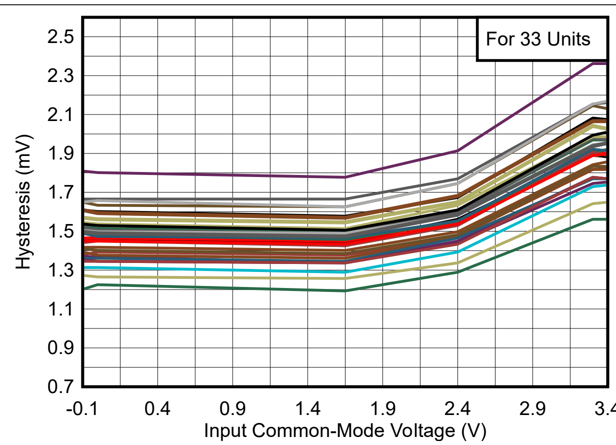


Figure 5-4. Hysteresis vs. Common-Mode, 3.3V

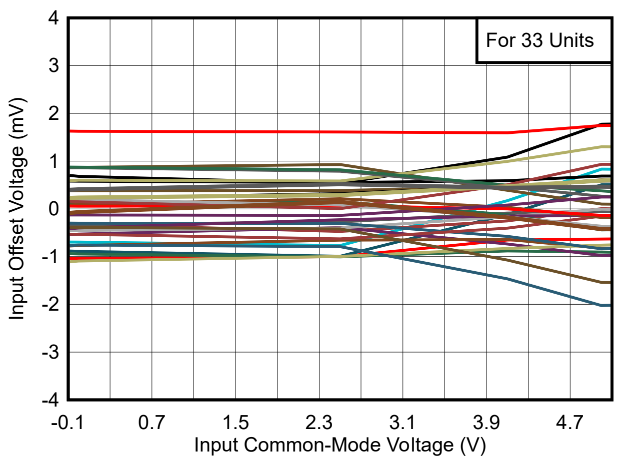


Figure 5-5. Offset vs. Common-Mode, 5V

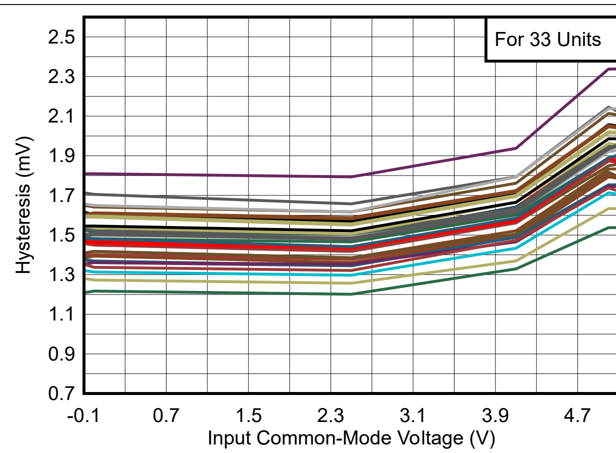


Figure 5-6. Hysteresis vs. Common-Mode, 5V

5.8 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, C_L = 15pF, V_{CM} = V_S/2V, $V_{UNDERDRIVE}$ = 50mV, $V_{OVERDRIVE}$ = 50mV unless otherwise noted.

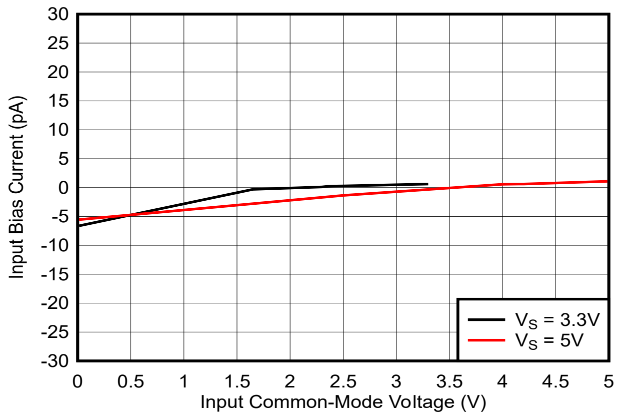


Figure 5-7. Bias Current vs. Common-Mode

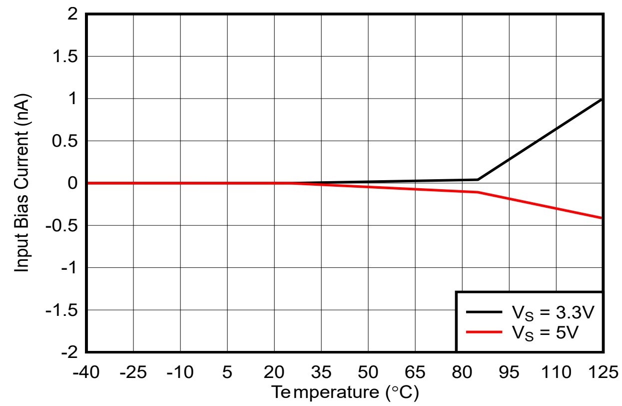


Figure 5-8. Bias Current vs. Temperature

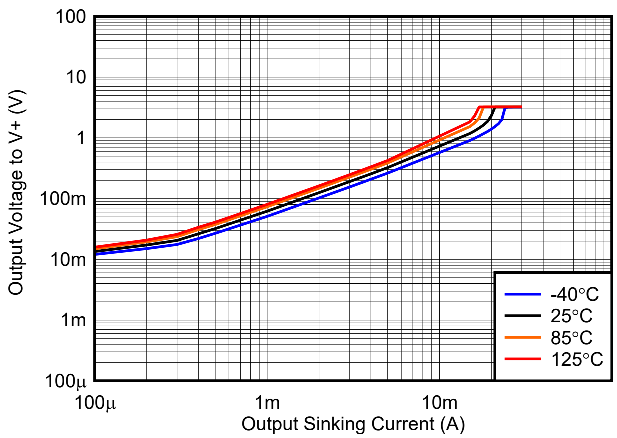


Figure 5-9. Output Voltage vs. Output Sourcing Current, 3.3V

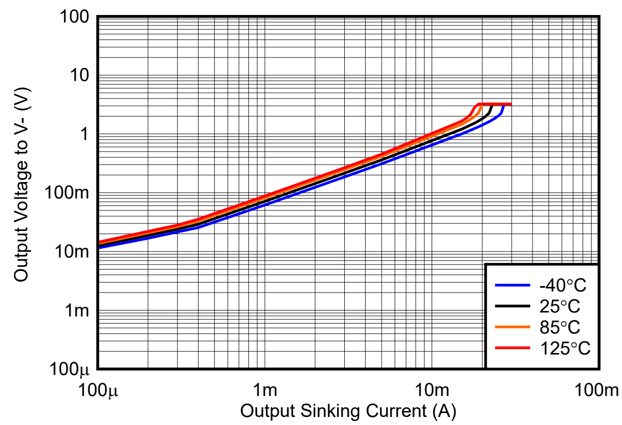


Figure 5-10. Output Voltage vs. Output Sinking Current, 3.3V

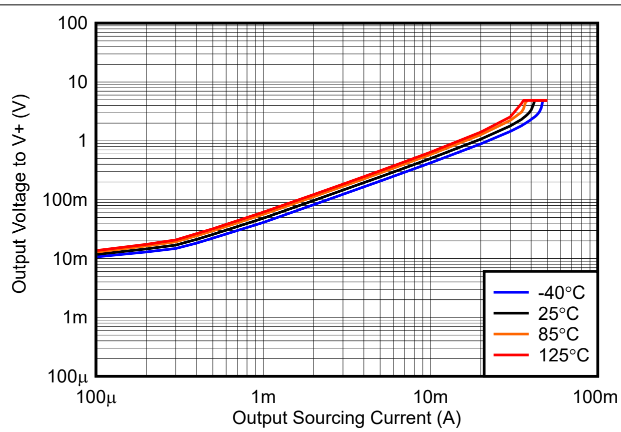


Figure 5-11. Output Voltage vs. Output Sourcing Current, 5V

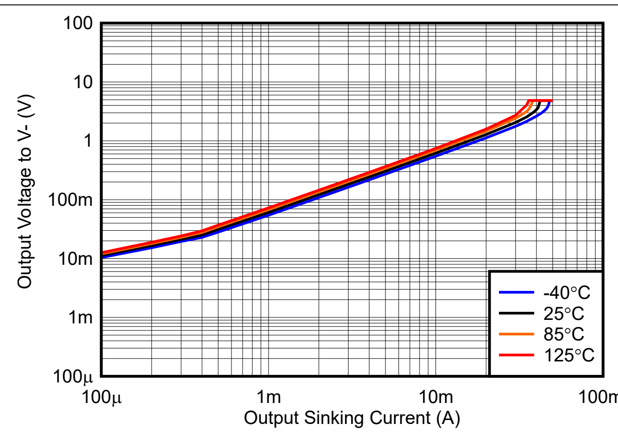


Figure 5-12. Output Voltage vs. Output Sinking Current, 5V

5.8 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, C_L = 15pF, V_{CM} = V_S/2V, $V_{UNDERDRIVE}$ = 50mV, $V_{OVERDRIVE}$ = 50mV unless otherwise noted.

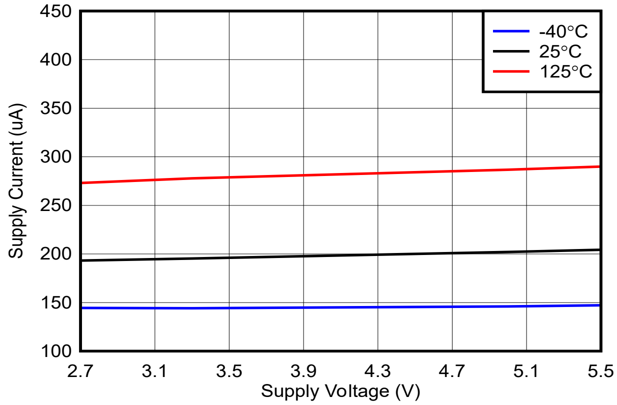


Figure 5-13. Supply Current vs. Supply Voltage (Output Low)

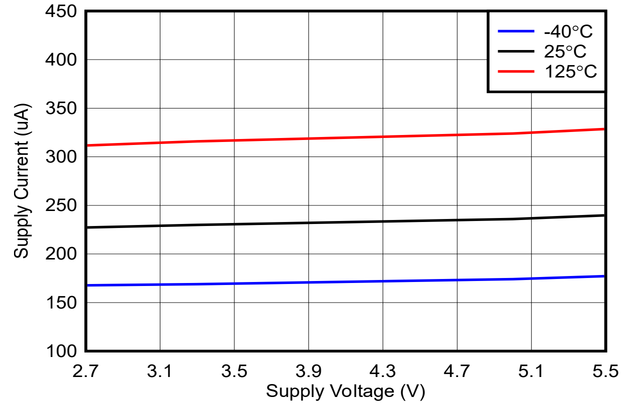


Figure 5-14. Supply Current vs. Supply Voltage (Output High)

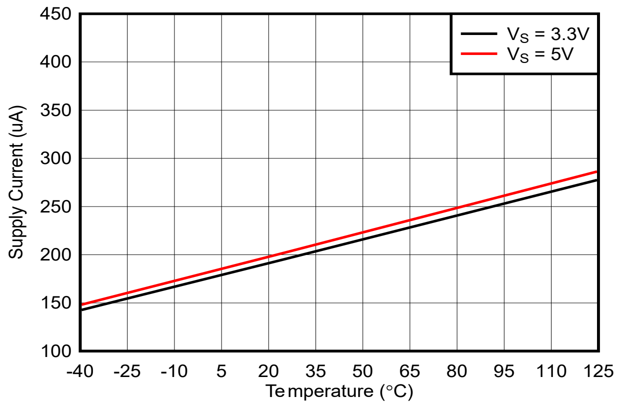


Figure 5-15. Supply Current vs. Temperature (Output Low)

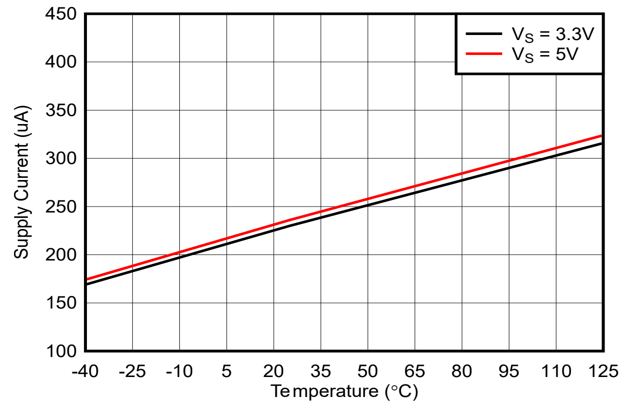


Figure 5-16. Supply Current vs. Temperature (Output High)

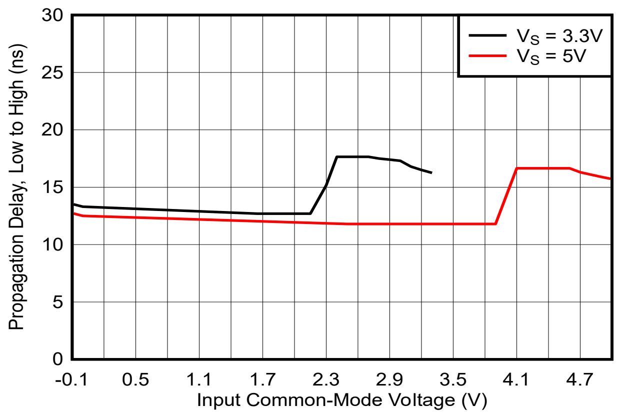


Figure 5-17. Propagation Delay (Low to High) vs. Common-Mode

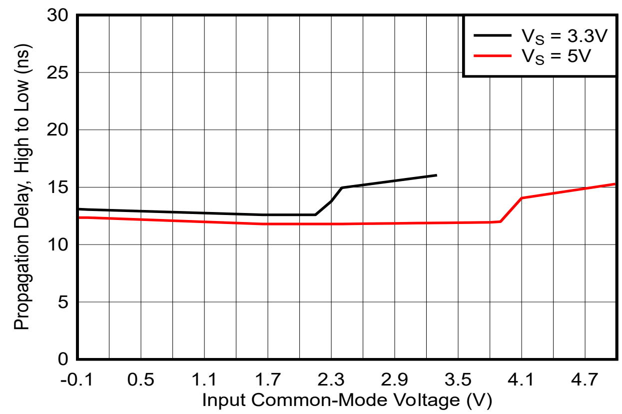


Figure 5-18. Propagation Delay (High to Low) vs. Common-Mode

5.8 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, C_L = 15pF, V_{CM} = V_S/2V, $V_{UNDERDRIVE}$ = 50mV, $V_{OVERDRIVE}$ = 50mV unless otherwise noted.

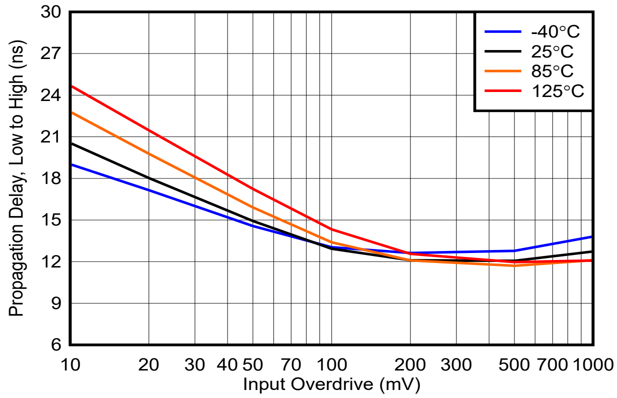


Figure 5-19. SINGLE Propagation Delay (Low to High) vs. Overdrive (3.3V)

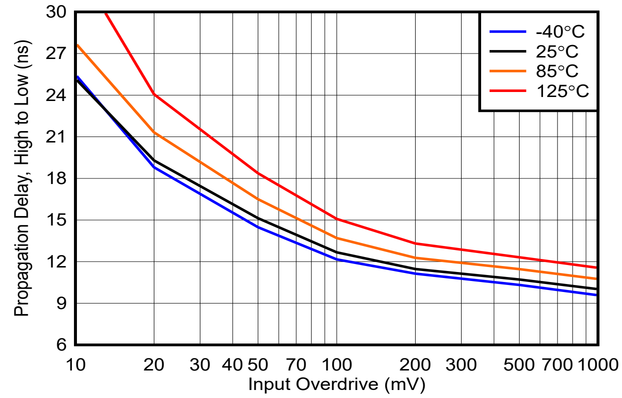


Figure 5-20. SINGLE Propagation Delay (High to Low) vs. Overdrive (3.3V)

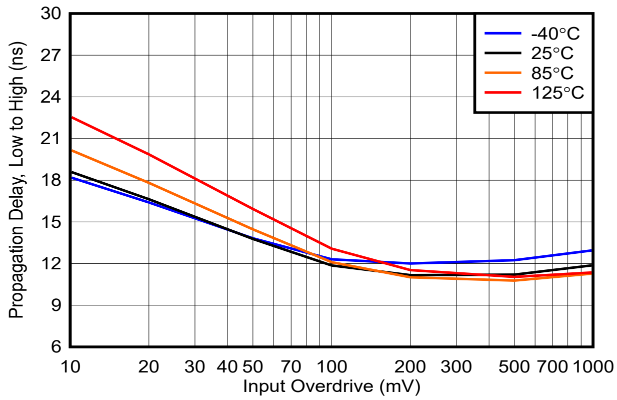


Figure 5-21. SINGLE Propagation Delay (Low to High) vs. Overdrive (5V)

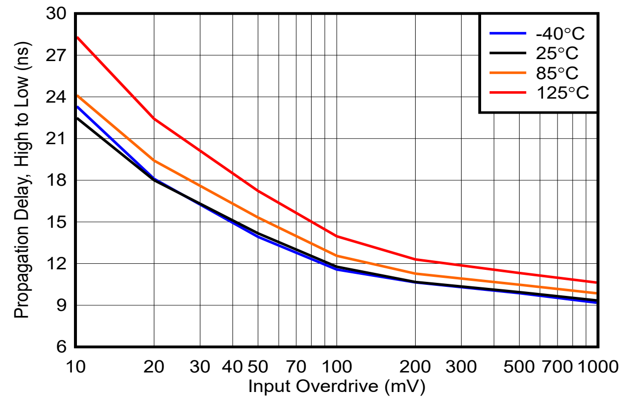


Figure 5-22. SINGLE Propagation Delay (High to Low) vs. Overdrive (5V)

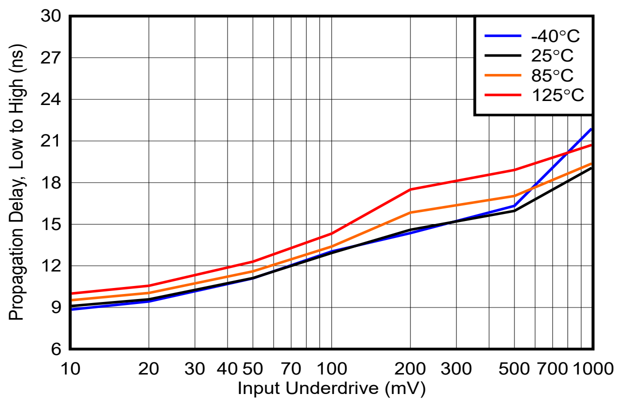


Figure 5-23. SINGLE Propagation Delay (Low to High) vs. Underdrive (3.3V)

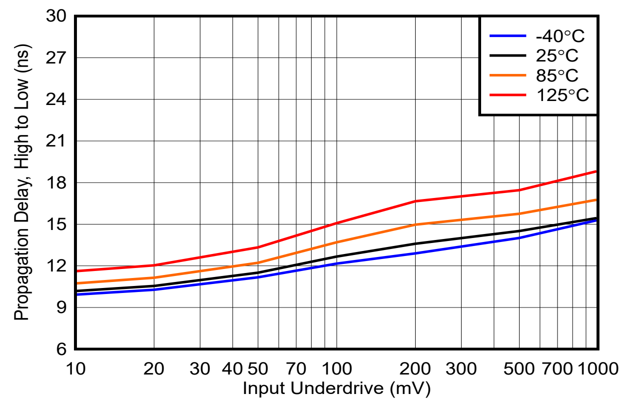


Figure 5-24. SINGLE Propagation Delay (High to Low) vs. Underdrive (3.3V)

5.8 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, C_L = 15pF, V_{CM} = V_S/2V, $V_{UNDERDRIVE}$ = 50mV, $V_{OVERDRIVE}$ = 50mV unless otherwise noted.

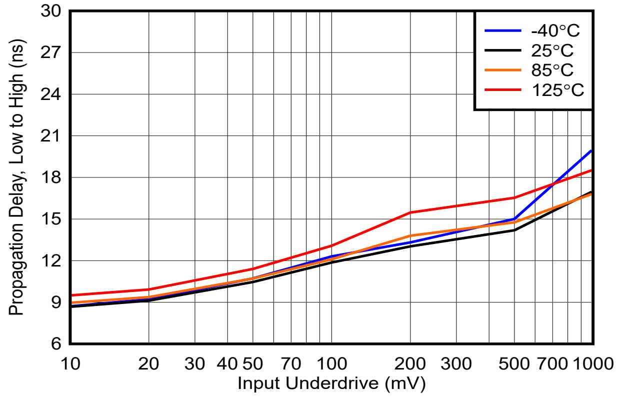


Figure 5-25. SINGLE Propagation Delay (Low to High) vs. Underdrive (5V)

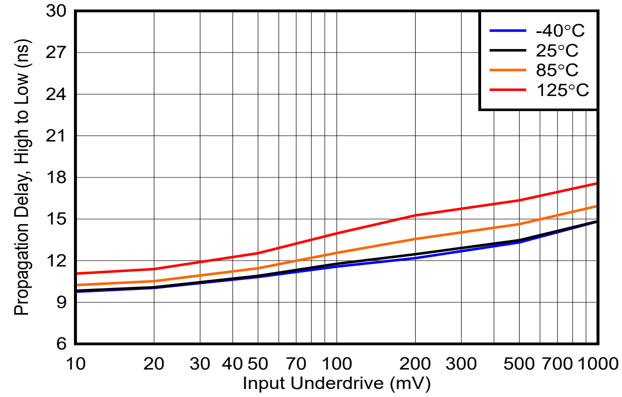


Figure 5-26. SINGLE Propagation Delay (High to Low) vs. Underdrive (5V)

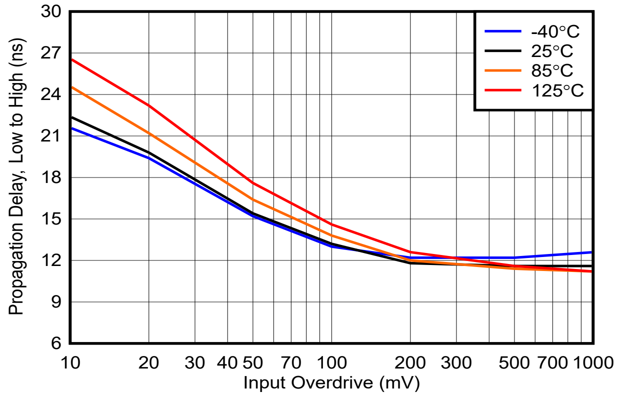


Figure 5-27. DUAL Propagation Delay (Low to High) vs. Overdrive (3.3V)

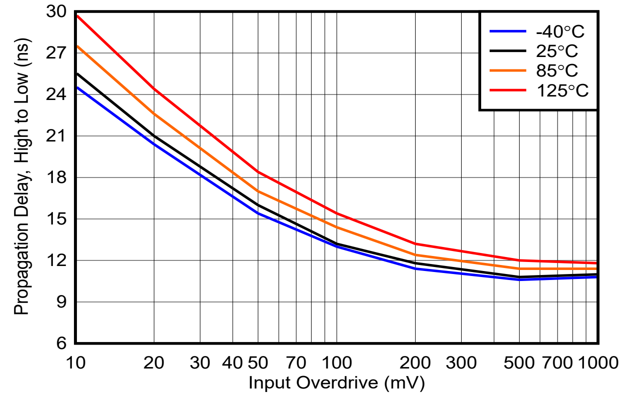


Figure 5-28. DUAL Propagation Delay (High to Low) vs. Overdrive (3.3V)

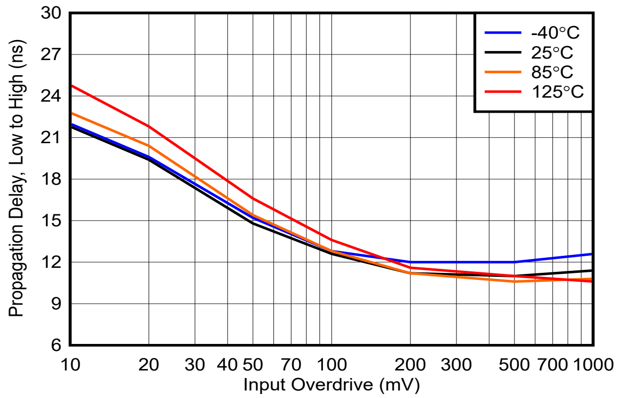


Figure 5-29. DUAL Propagation Delay (Low to High) vs. Overdrive (5V)

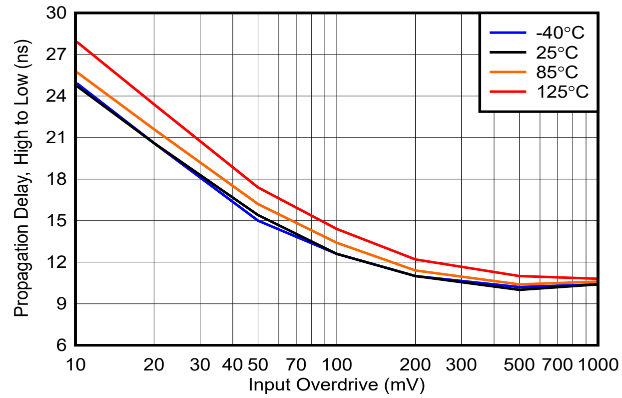


Figure 5-30. DUAL Propagation Delay (High to Low) vs. Overdrive (5V)

5.8 Typical Characteristics (continued)

T_A = 25°C, V_S = 5V, C_L = 15pF, V_{CM} = V_S/2V, $V_{UNDERDRIVE}$ = 50mV, $V_{OVERDRIVE}$ = 50mV unless otherwise noted.

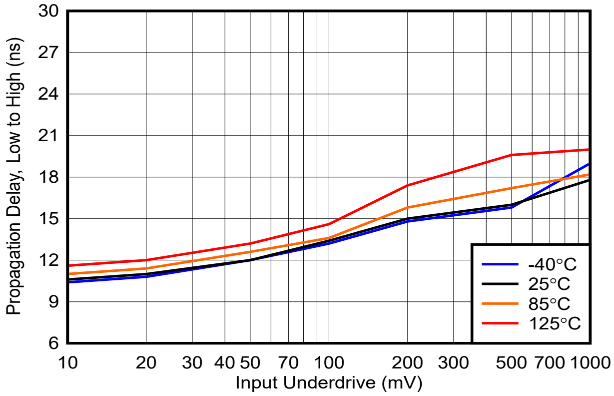


Figure 5-31. DUAL Propagation Delay (Low to High) vs. Underdrive (3.3V)

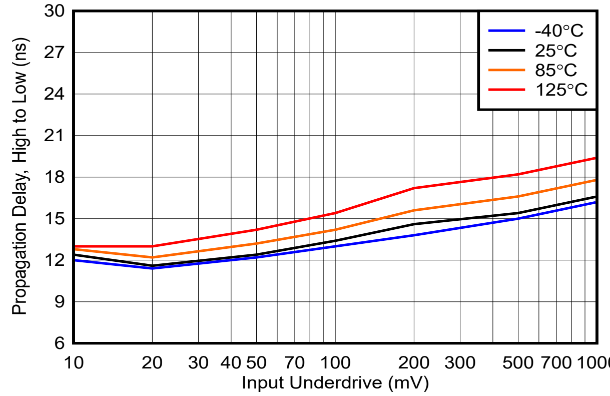


Figure 5-32. DUAL Propagation Delay (High to Low) vs. Underdrive (3.3V)

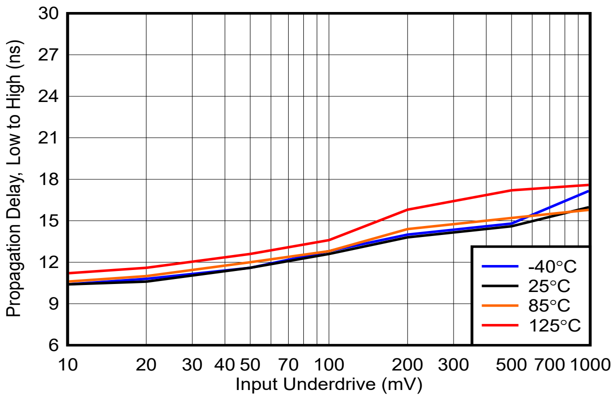


Figure 5-33. DUAL Propagation Delay (Low to High) vs. Underdrive (5V)

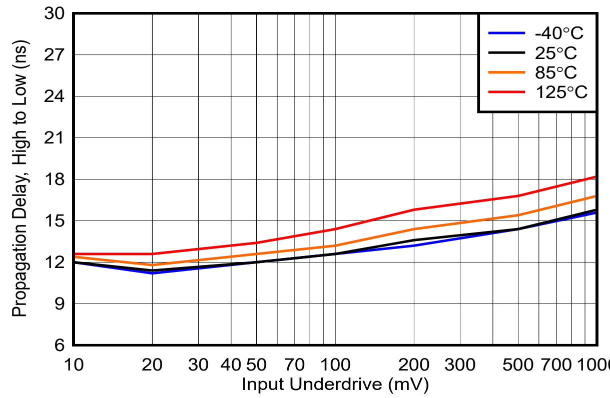


Figure 5-34. DUAL Propagation Delay (High to Low) vs. Underdrive (5V)

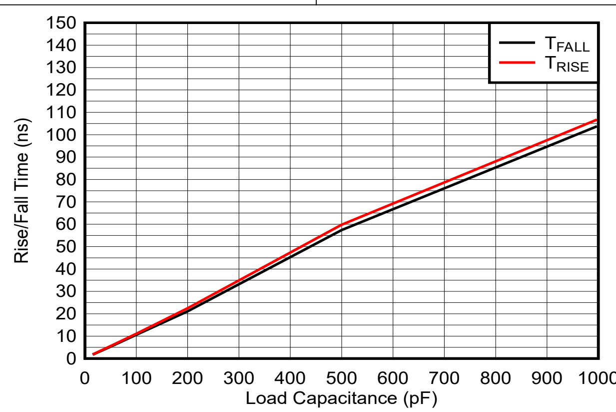


Figure 5-35. Rise and Fall Times vs. Capacitive Loads

6 Detailed Description

6.1 Overview

The TLV323x devices are high-speed comparators with push-pull outputs.

6.2 Functional Block Diagrams

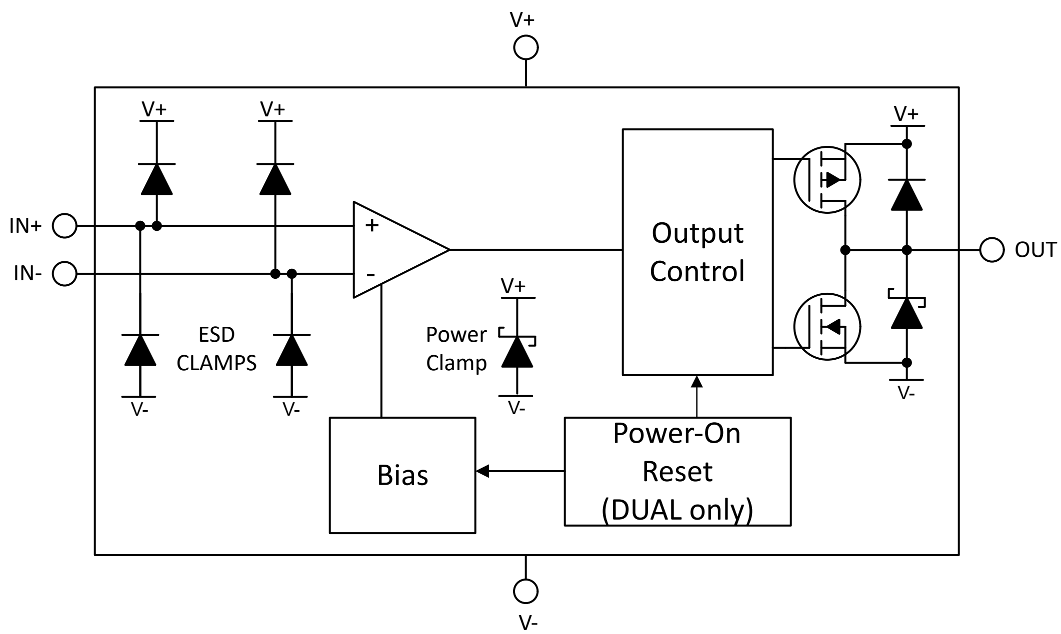


Figure 6-1. Block Diagram

6.3 Feature Description

The TLV323x consumes 200µA per channel with 20ns of propagation delay. The TLV323x detects fast voltage and current transients while maintaining low power consumption with single-ended, push-pull outputs.

6.4 Device Functional Modes

6.4.1 Inputs

The inputs incorporate internal ESD protection circuits to (V+) and (V-). Voltages on the inputs are limited to 0.3V beyond the rails.

When connecting to a low impedance source such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents if the clamps conduct. Limit the current to 10mA or less. One form of series resistance is any resistive input dividers or networks.

6.4.2 Internal Hysteresis

The device hysteresis transfer curve is shown below. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and V_{IN-}. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

  (typically 1.55mV for the TLV323x family)

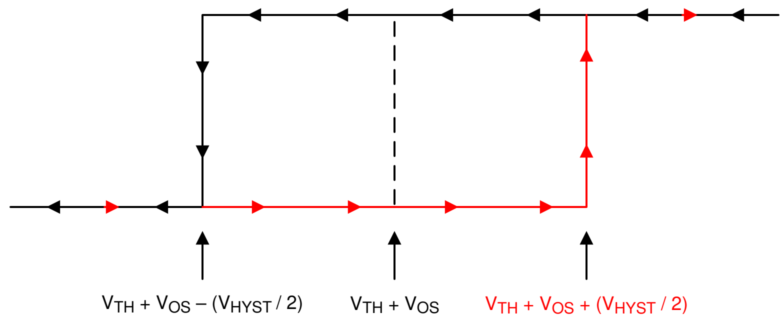


Figure 6-2. Hysteresis Transfer Curve

6.4.3 Outputs

The TLV323x features a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Directly shorting the output to the supply rails ((V+) when output "low" or (V-) when output "High") can result in thermal runaway and eventual device destruction. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused push-pull outputs must be left floating, and never tied to a supply, ground, or another output.

6.4.4 ESD Protection

The inputs and outputs incorporate internal ESD protection circuits to (V+) and (V-).

Voltages on the inputs are limited to 0.3V beyond the rails. If the inputs are to be connected to a low impedance source, such as a power supply or buffered reference line, TI recommends adding a current-limiting resistor in series with the input to limit any transient currents in case the clamps conduct. Limit the current to 10mA or less.

6.4.5 Power-On Reset (POR) - Dual Channel Only

The TLV3232 devices have an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V+) is ramping up or ramping down, the POR circuitry is activated for up to 2.5us after the V_{POR} of 2.2V is crossed. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}).

For the TLV3232 devices, the output is held low during the POR period (t_{on}) as shown below.

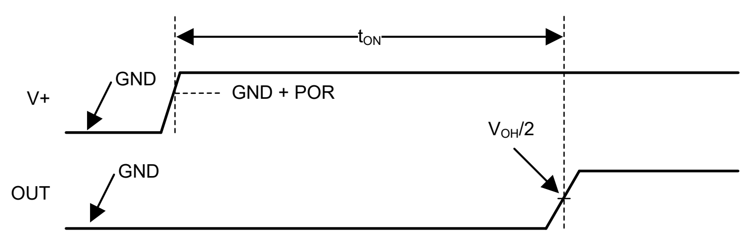


Figure 6-3. Power-On Reset Timing Diagram

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Basic Comparator Definitions

7.1.1.1 Operation

The basic comparator compares the input voltage (V_{IN}) on one input to a reference voltage (V_{REF}) on the other input. In the Figure 7-1 example below, if V_{IN} is less than V_{REF}, the output voltage (V_O) is logic low (V_{OL}). If V_{IN} is greater than V_{REF}, the output voltage (V_O) is at logic high (V_{OH}). Table 7-1 summarizes the output conditions. The output logic can be inverted by simply swapping the input pins.

Table 7-1. Output Conditions

Inputs Condition	Output
IN+ > IN-	HIGH (V_{OH})
IN+ = IN-	Indeterminate (chatters - see Hysteresis)
IN+ < IN-	LOW (V_{OL})

7.1.1.2 Propagation Delay

There is a delay between from when the input crosses the reference voltage and the output responds. This is called the Propagation Delay. Propagation delay can be different between high-to low and low-to-high input transitions. This is shown as t_{pLH} and t_{pHL} in Figure 7-1 and is measured from the mid-point of the input to the midpoint of the output.

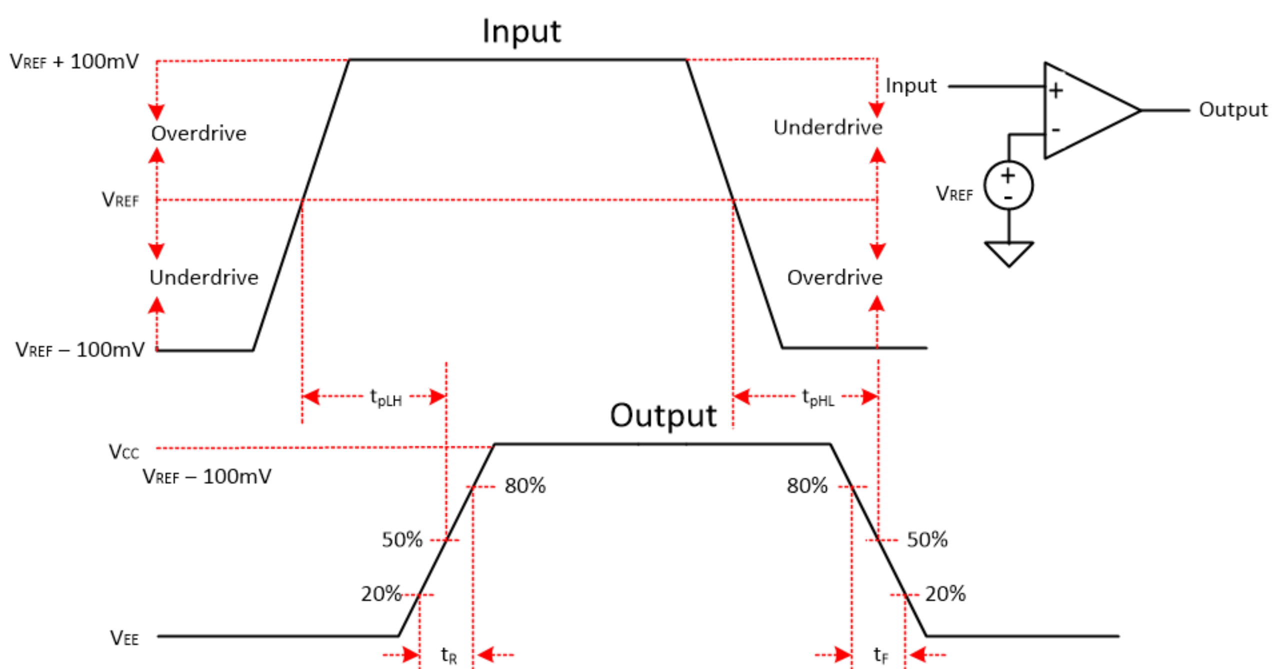


Figure 7-1. Comparator Timing Diagram

7.1.1.3 Overdrive Voltage

The overdrive voltage, V_{OD}, is the amount of input voltage beyond the reference voltage (and not the total input peak-to-peak voltage). The overdrive voltage can influence the propagation delay (t_p). The smaller the overdrive voltage, the longer the propagation delay, particularly when <100mV. If the fastest speeds are desired, TI recommends applying the highest amount of overdrive possible.

The risetime (t_r) and falltime (t_f) is the time from the 20% and 80% points of the output waveform.

7.1.2 Hysteresis

The basic comparator configuration can produce a noisy "chatter" output if the applied differential input voltage is near the comparator's offset voltage. This typically occurs when the input signal is moving very slowly across the switching threshold of the comparator. This problem can be prevented by adding external hysteresis to the comparator.

Since the TLV323x devices only have a minimal amount of internal hysteresis of 1.55mV, external hysteresis can be applied in the form of a positive feedback loop that adjusts the trip point of the comparator depending on the current output state.

The hysteresis transfer curve is shown in Figure 7-2. This curve is a function of three components: V_{TH}, V_{OS}, and V_{HYST}:

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

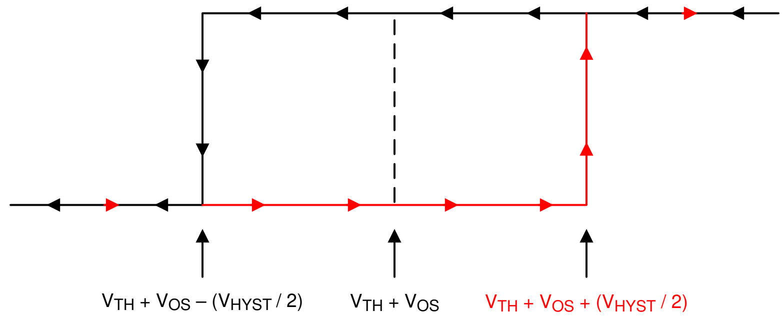


Figure 7-2. Hysteresis Transfer Curve

For more information, please see Application Note SBOA219 "Comparator with and without hysteresis circuit".

7.1.2.1 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in Figure 7-3.

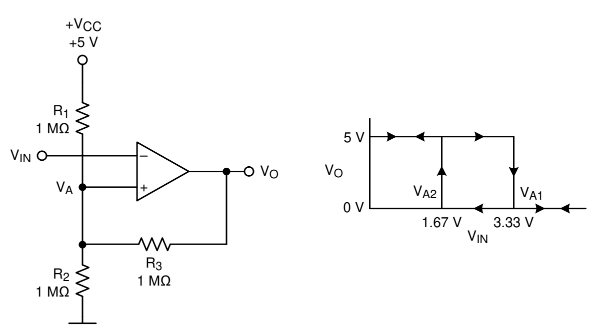


Figure 7-3. TLV3231 in an Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 7-3.

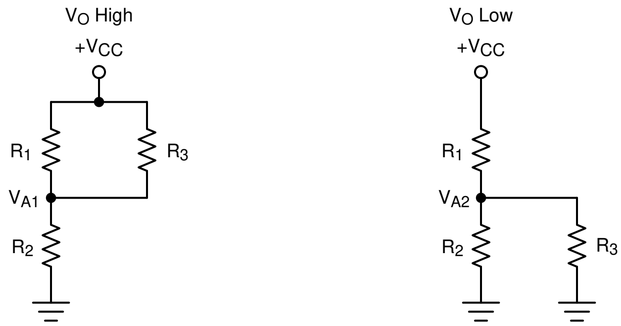


Figure 7-4. Inverting Configuration Resistor Equivalent Networks

When V_{IN} is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2, as shown in Figure 7-4.

Equation 1 below defines the high-to-low trip voltage (V_{A1}).

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than V_A, the output voltage is low. In this case, the three network resistors can be presented as R2 || R3 in series with R1, as shown in Equation 2.

Use Equation 2 to define the low to high trip voltage (V_{A2}).

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

Equation 3 defines the total hysteresis provided by the network.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

7.1.2.2 Non-Inverting Comparator With Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network and a voltage reference (V_{REF}) at the inverting input, as shown in Figure 7-5,

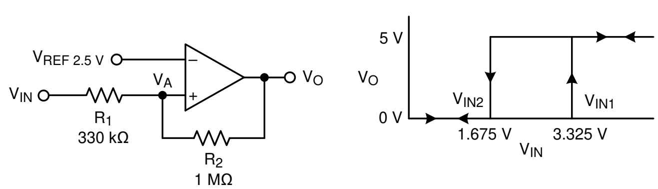


Figure 7-5. TLV3231 in a Non-Inverting Configuration With Hysteresis

The equivalent resistor networks when the output is high and low are shown in Figure 7-6.

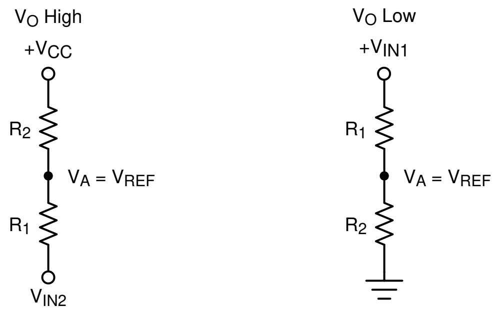


Figure 7-6. Non-Inverting Configuration Resistor Networks

When V_{IN} is less than V_{REF}, the output is low. For the output to switch from low to high, V_{IN} must rise above the V_{IN1} threshold. Use Equation 4 to calculate V_{IN1}.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} + V_{REF} \tag{4}$$

When V_{IN} is greater than V_{REF}, the output is high. For the comparator to switch back to a low state, V_{IN} must drop below V_{IN2}. Use Equation 5 to calculate V_{IN2}.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as shown in Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

For more information, please see Application Notes SNOA997 "Inverting comparator with hysteresis circuit" and SBOA313 "Non-Inverting Comparator With Hysteresis Circuit".

7.2 Typical Applications

7.2.1 Low-Side Current Sensing

The figure below shows a simple low-side current sensing circuit using a high-speed comparator. Since this design does not utilze an amplifier, the response time is only limited by the propagation delay of the comparator. With faster response time, the design is well-suited for short-circuit detection when speed is more important than accuracy. When the voltage across the shunt resistor reaches the critical over-current threshold created by R1 and R2, the comparator output changes state.

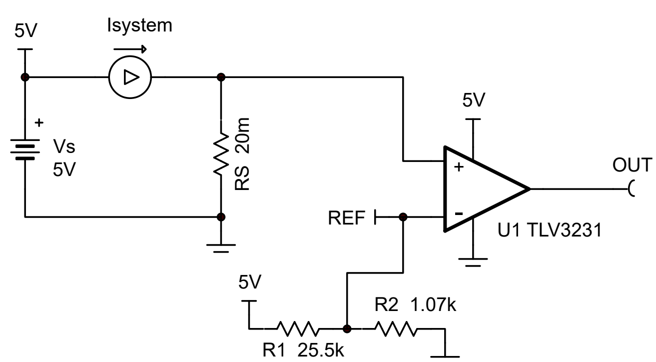


Figure 7-7. Current Sensing

7.2.1.1 Design Requirements

For this design, follow these design requirements:

- Alert (overcurrent) event occurs when system current (Isystem) reaches 10A
- Alert signal (OUT) is active high
- Operate from a 5V power supply

7.2.1.2 Detailed Design Procedure

To minimize power dissipation and voltage drop across the shunt resistor (RS), a value of 20mΩ is selected. Since the overcurrent level of 10A creates a 200mV drop across RS, R1 and R2 are calculated to create the voltage divider value of 200mV from the regulated 5V supply voltage. If the system is expected to operate close to the 10A maximum, hysteresis can be added to the design as shown in Non-Inverting Comparator With Hysteresis.

7.2.1.3 Application Curve

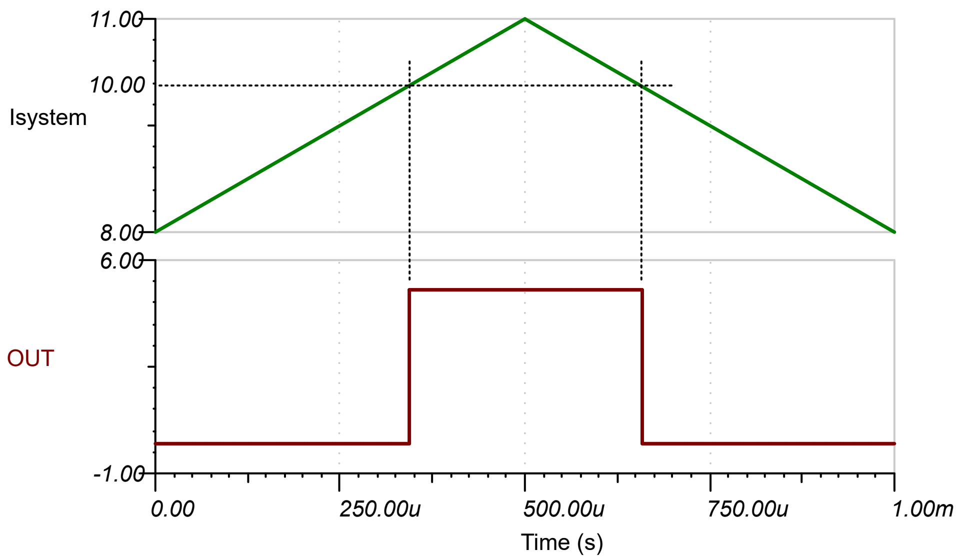


Figure 7-8. Overcurent Results

7.3 Power Supply Recommendations

Due to the fast output edges, bypass capacitors are required on the supply pin to prevent supply ringing and false triggers and oscillations. Bypass the supply directly at *each* device with a low ESR 0.1µF ceramic bypass capacitor directly between the (V+) pin and ground pins. Narrow peak currents can be drawn during the output transition time, particularly for the push-pull output device. These narrow pulses can cause un-bypassed supply lines and poor grounds to ring, possibly causing variation that can eat into the input voltage range and create an inaccurate comparison or even oscillations.

The device can be powered from both "split" supplies ((V+) &(V-)), or "single" supplies ((V+) and GND), with GND applied to the (V-) pin. Input signals must stay within the recommended input range for either type. Note that with a "split" supply the output now swings "low" (V_{OL}) to (V-) potential and not GND.

7.4 Layout

7.4.1 Layout Guidelines

Accurate comparator applications require a stable power supply with minimized noise and glitches. Output rise and fall times are in the tens of nanoseconds, and must be treated as high speed logic devices. The bypass capacitor must be as close to the supply pin as possible and connected to a solid ground plane, and preferably directly between the (V+) and GND pins.

Minimize coupling between outputs and inputs to prevent output oscillations. Do not run output and input traces in parallel unless there is a (V+) or GND trace between output to reduce coupling. When series resistance is added to inputs, place resistor close to the device. A low value (<100Ω) resistor can also be added in series with the output to dampen any ringing or reflections on long, non-impedance controlled traces. For best edge shapes, controlled impedance traces with back-terminations can be used when routing long distances.

7.4.2 Layout Example

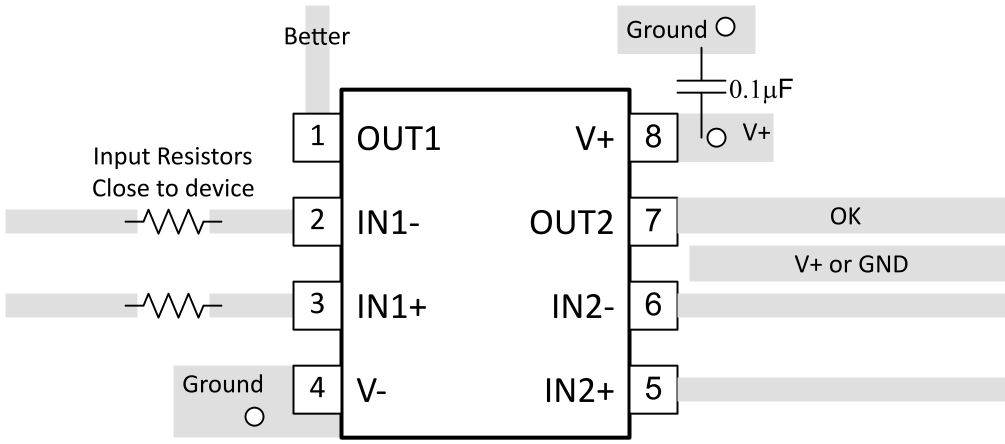


Figure 7-9. Dual Layout Example

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

Analog Engineers Circuit Cookbook: Amplifiers (See Comparators section) - SLYY137

Precision Design, Comparator with Hysteresis Reference Design— TIDU020

Comparator with and without hysteresis circuit - SBOA219

Inverting comparator with hysteresis circuit - SNOA997

Non-Inverting Comparator With Hysteresis Circuit - SBOA313

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2024) to Revision C (June 2025)	Page
• Added separate propagation delay data for DUAL channel option	1

Changes from Revision A (September 2024) to Revision B (December 2024)	Page
• Released the dual TLV3232 throughout document	1

Changes from Revision * (August 2024) to Revision A (September 2024)	Page
• Production Data release for the SOT-23	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV3231DBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3HGH
TLV3231DBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	3HGH
TLV3231DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SQ
TLV3231DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1SQ
TLV3232DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3MSS
TLV3232DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3MSS
TLV3232DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3232

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV3231, TLV3232 :

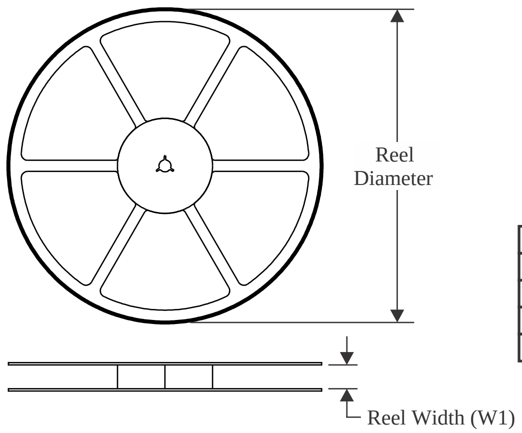
- Automotive : TLV3231-Q1, TLV3232-Q1

NOTE: Qualified Version Definitions:

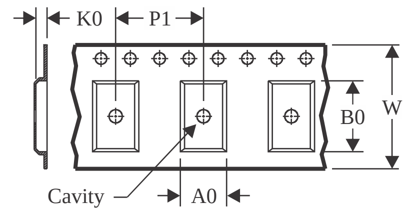
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

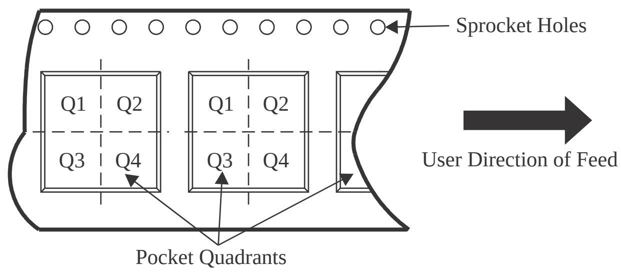


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

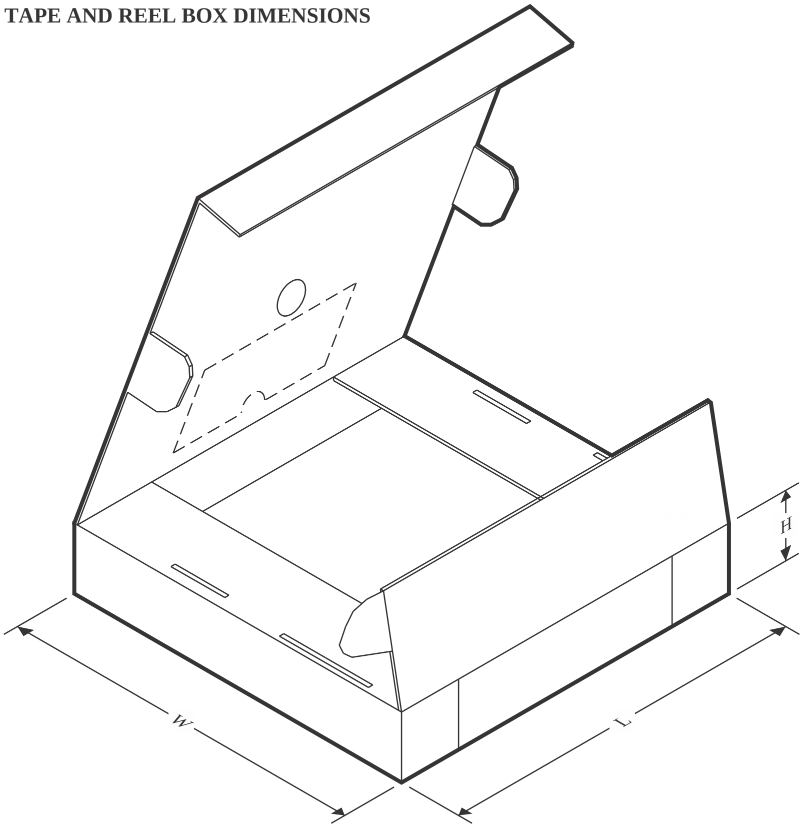
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

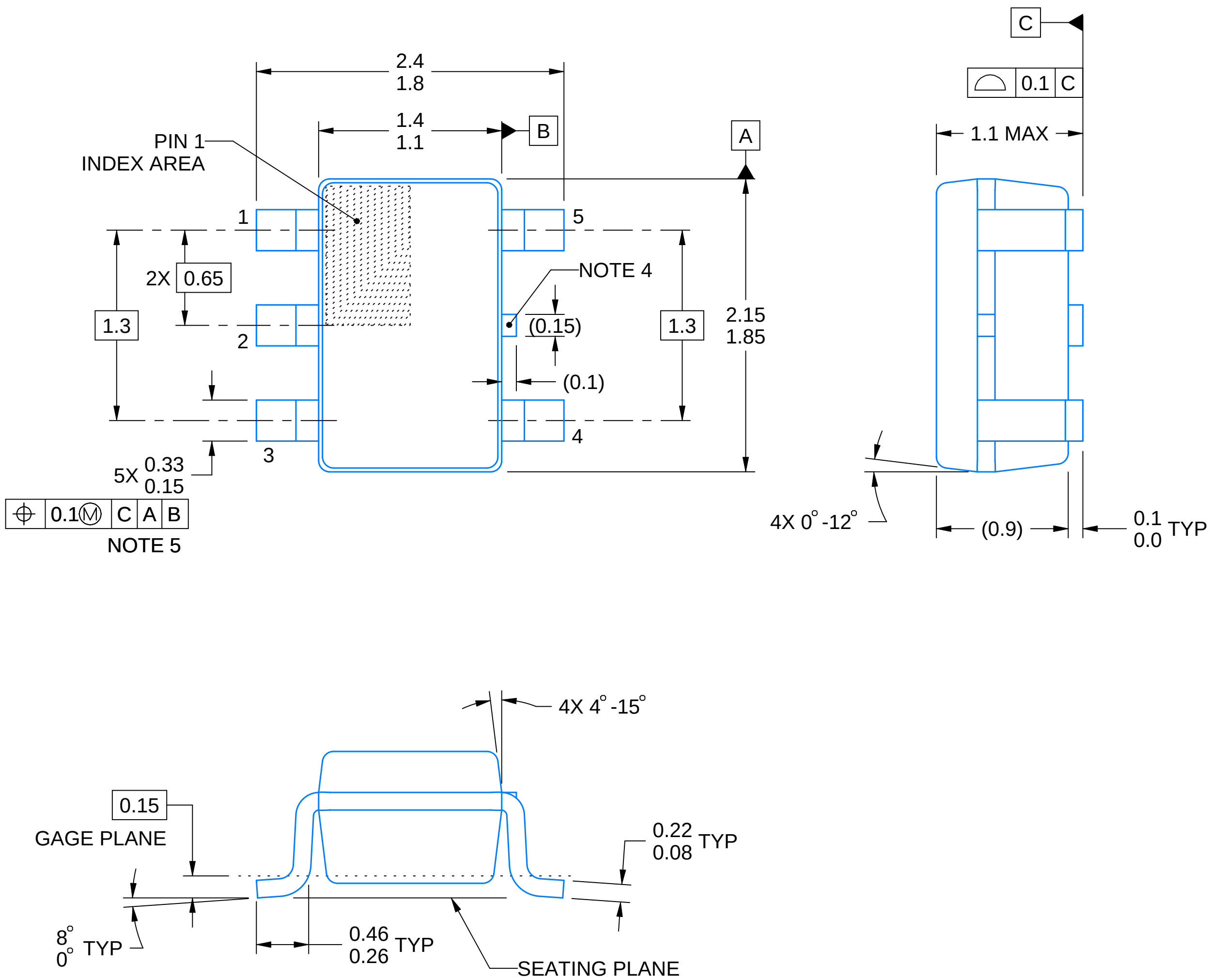
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3231DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV3231DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.55	1.2	4.0	8.0	Q3
TLV3232DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV3232DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3231DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV3231DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TLV3232DGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV3232DSGR	WSON	DSG	8	3000	210.0	185.0	35.0



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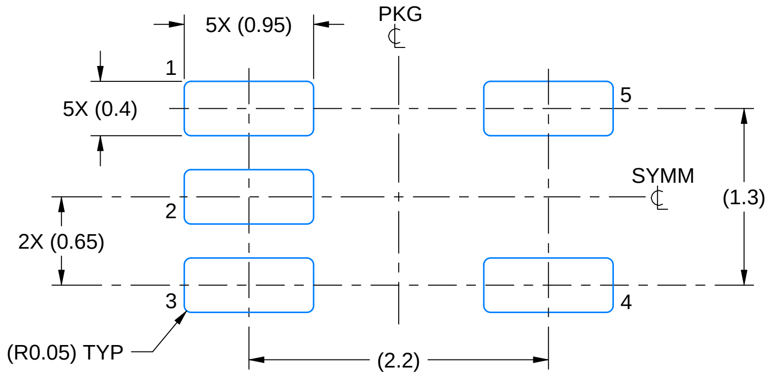
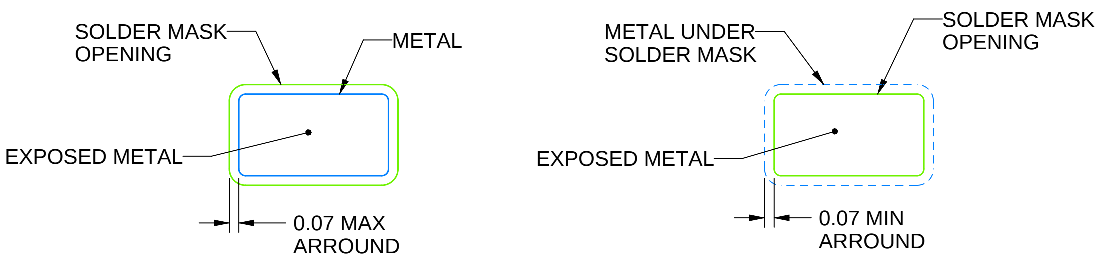
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK
DEFINED
(PREFERRED)

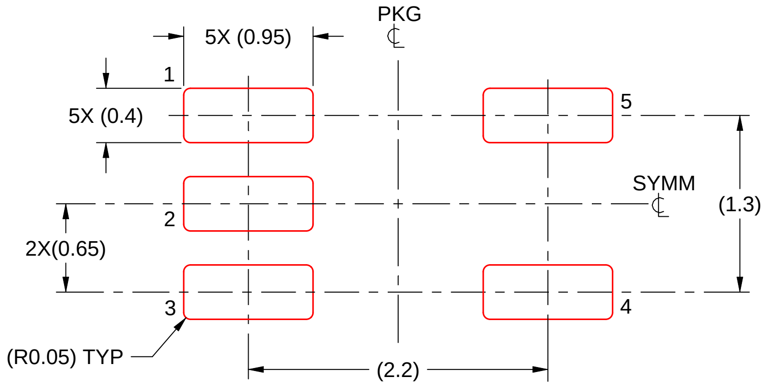
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

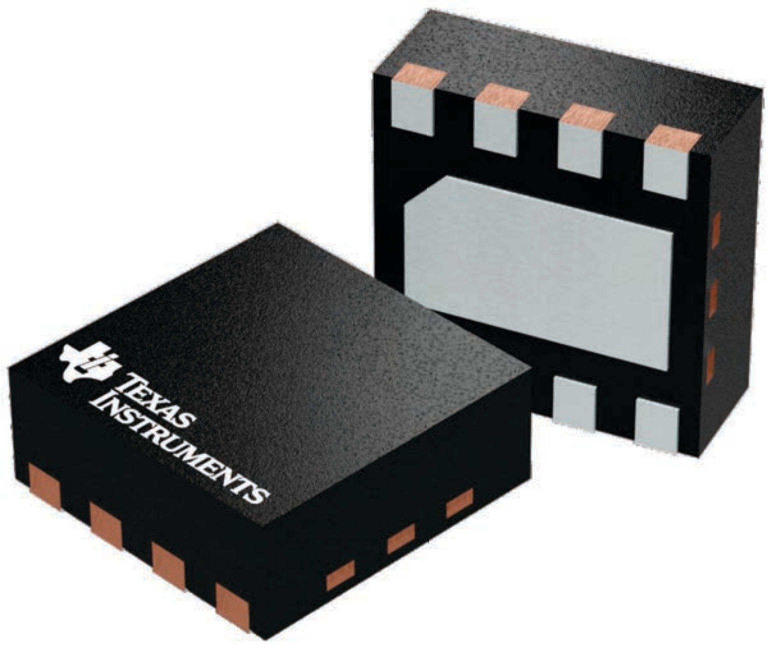
DSG 8

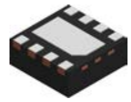
WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



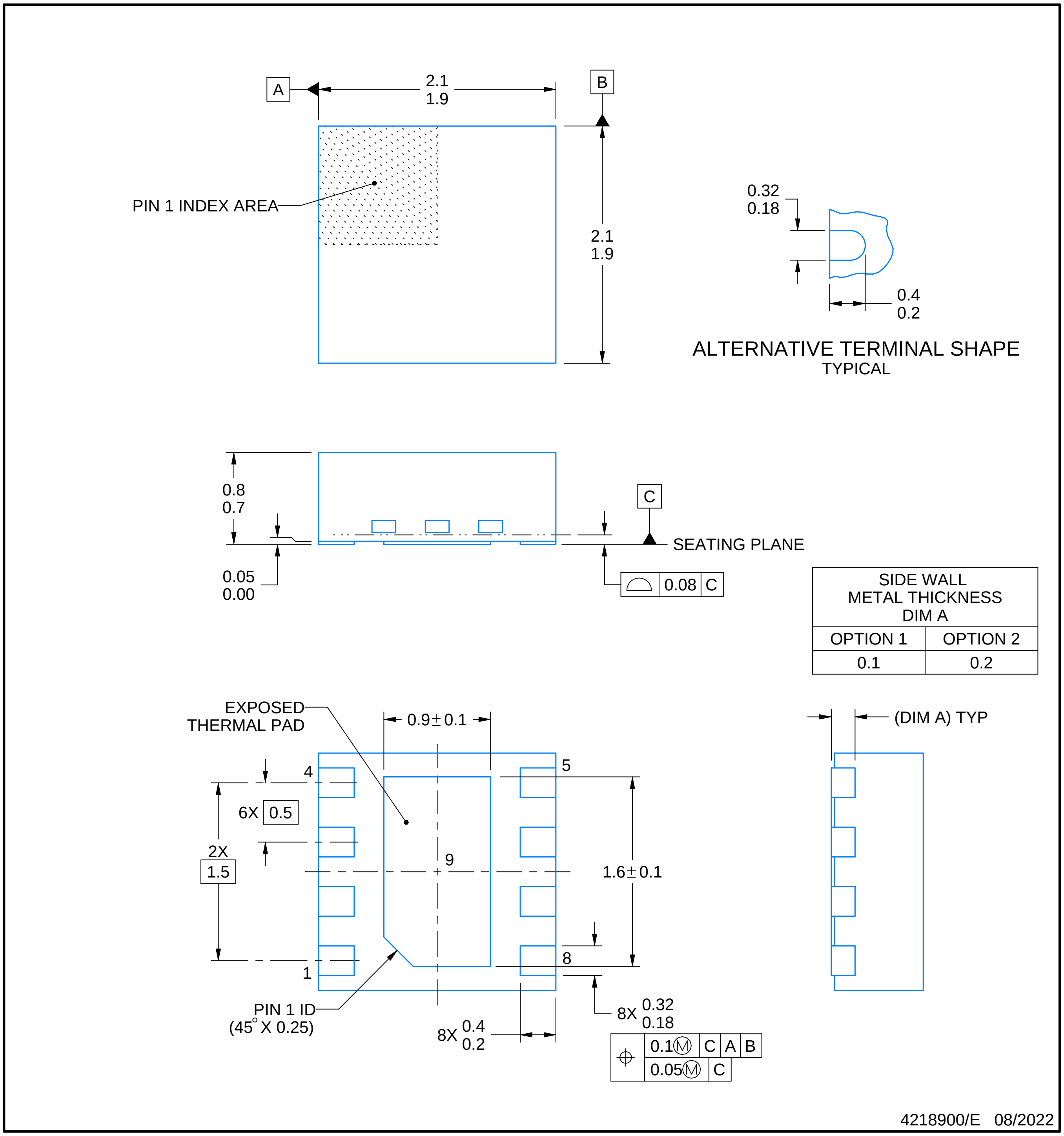


DSG0008A

PACKAGE OUTLINE

WSON - 0.8 mm max height

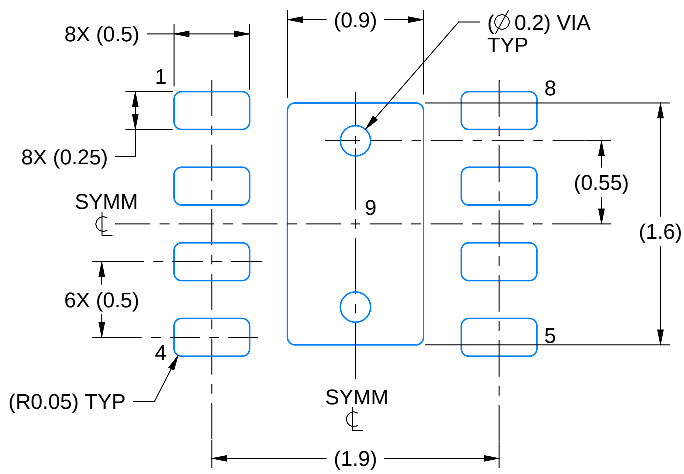
PLASTIC SMALL OUTLINE - NO LEAD



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

NON SOLDER MASK
DEFINED
(PREFERRED)

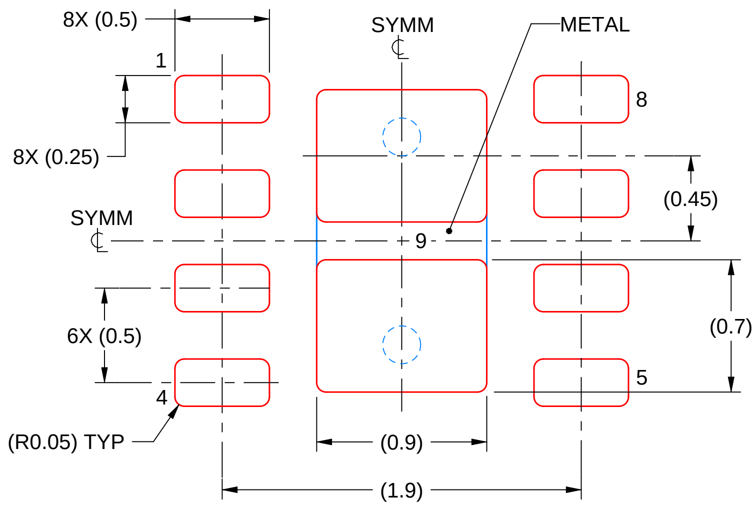
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



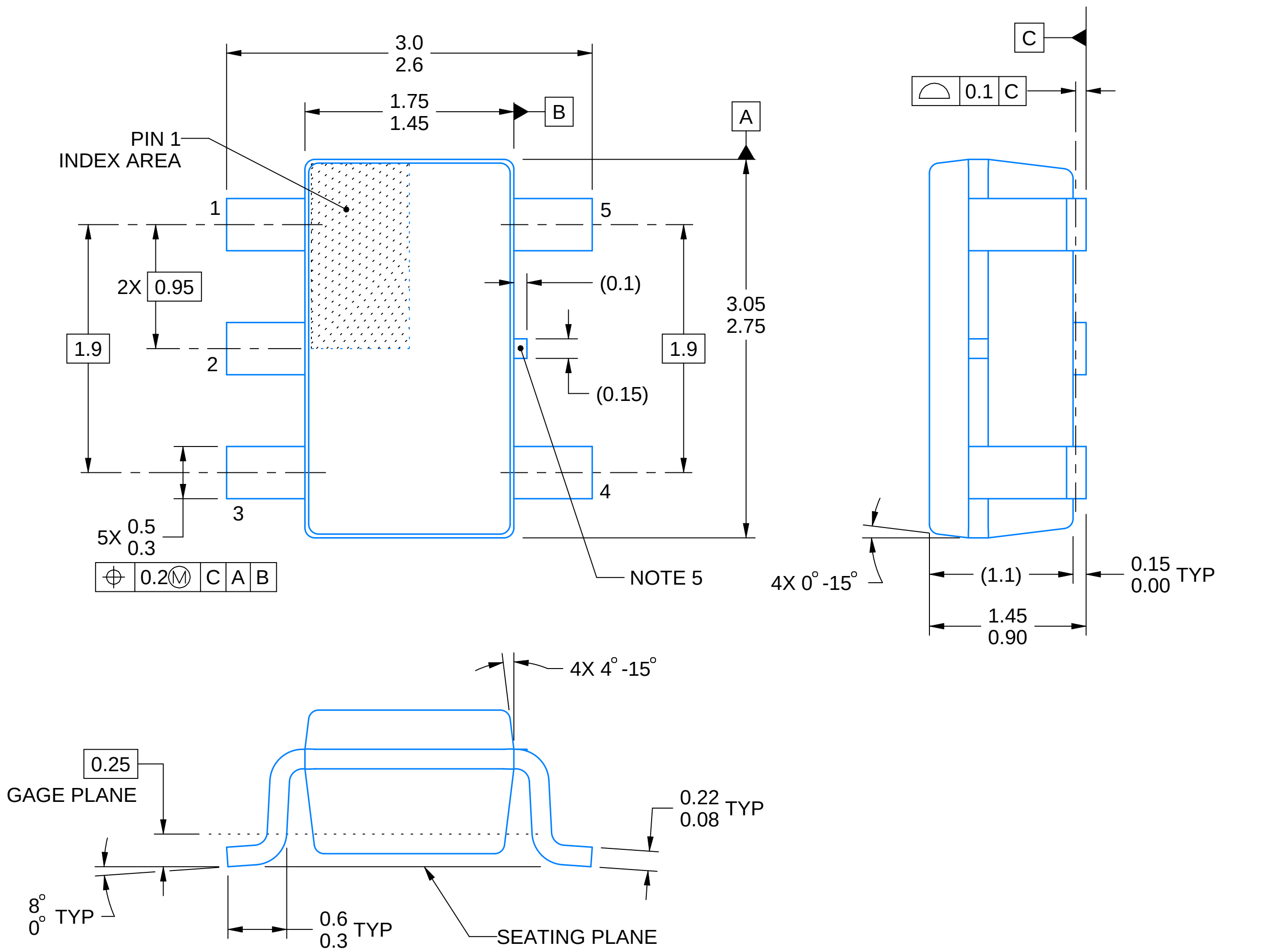
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

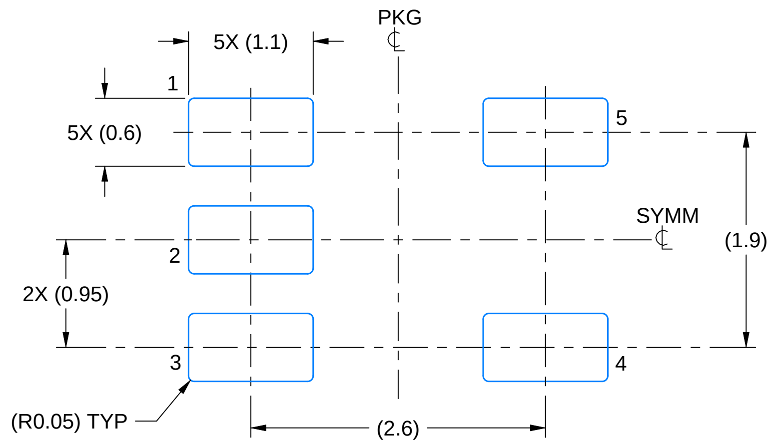
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



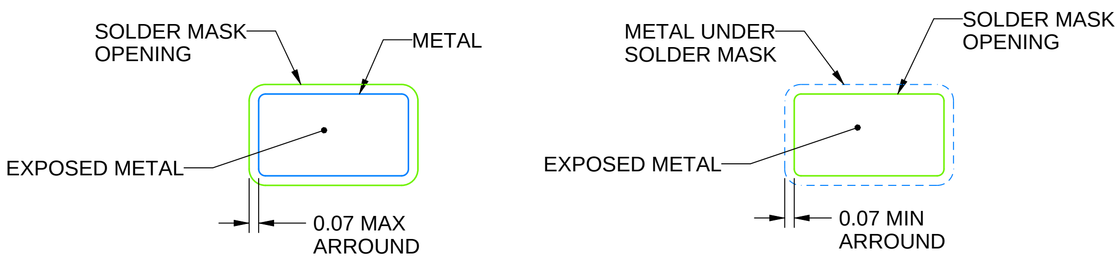
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

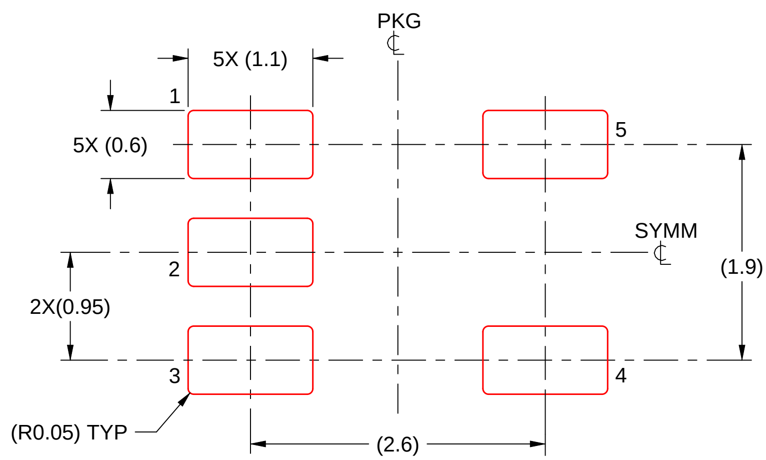
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

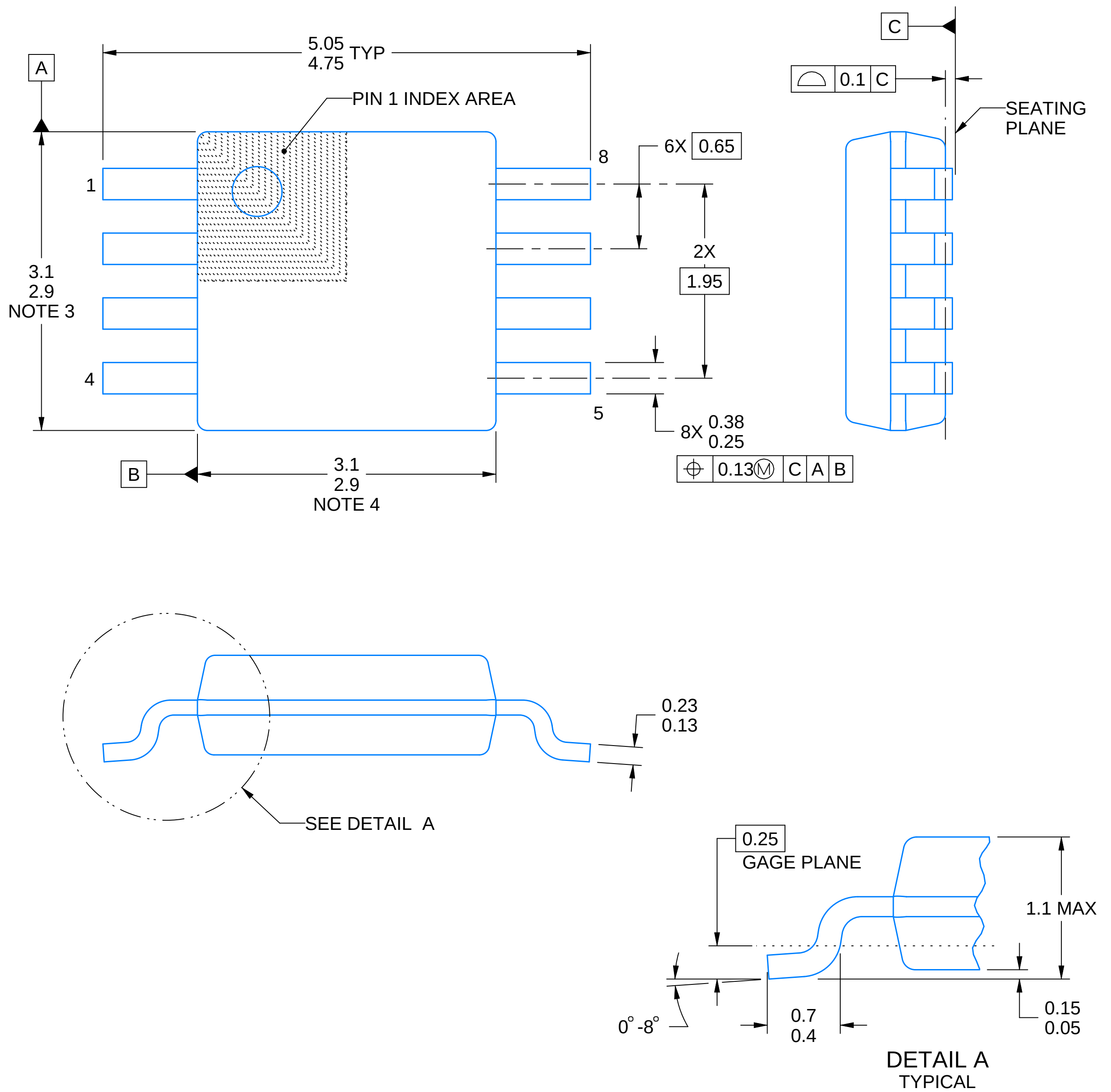


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

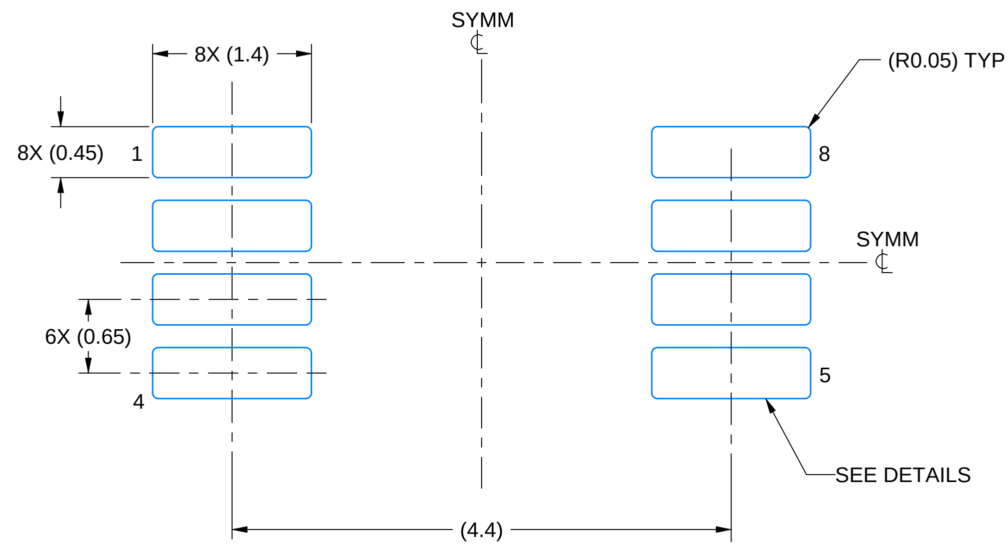


4214862/A 04/2023

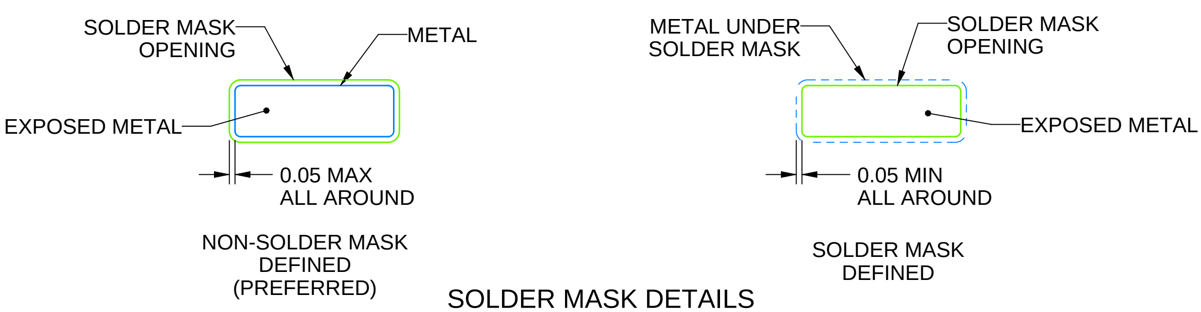
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

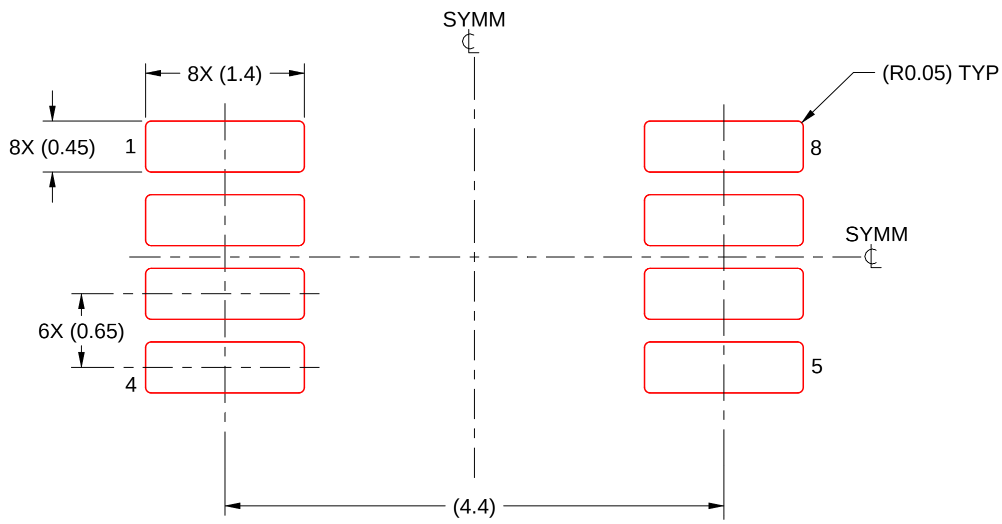


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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