

1.8 V, NANOPower, PUSH/PULL OUTPUT COMPARATORS

FEATURES

- Very Low Supply Current: 0.8 μ A (Typical)
- Input Common Mode Range 200 mV Beyond Supply Rails
- Supply Voltage: 1.8 V to 5.5 V
- High Speed: 6 μ s
- Push/Pull CMOS Output Stage
- Controlled Baseline
 - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product Change Notification
- Qualification Pedigree

Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

APPLICATIONS

- Portable Medical Equipment
- Wireless Security Systems
- Remote Control Systems
- Handheld Instruments
- Ultra-Low Power Systems

DESCRIPTION/ORDERING INFORMATION

The TLV349x family of push/pull output comparators features a fast 6 μ s response time and <1.2 μ A (max) nanopower capability, allowing operation from 1.8 V to 5.5 V. Input common-mode range beyond supply rails make the TLV349x an ideal choice for low-voltage applications.

The TLV349x is excellent for power-sensitive, low-voltage (2-cell) applications.

TLV349x RELATED PRODUCTS

| PRODUCT | FEATURES |
|---------|---|
| TLV370x | 550 nA, 2.5 V to 16 V, Push-Pull CMOS Output Stage Comparator |
| TLV340x | 550 nA, 2.5 V to 16 V, Open-Drain Output Stage Comparator |

ORDERING INFORMATION⁽¹⁾

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR ⁽²⁾ | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERABLE PART NUMBER | TRANSPORT MEDIA, QUANTITY |
|---------|--------------|-----------------------------------|--|-----------------|------------------------------|---------------------------|
| TLV3491 | SO-8 | D | -55°C to 125°C | 3491EP | TLV3491AMDREP ⁽³⁾ | Tape and Reel, 2500 |
| TLV3492 | SO-8 | D | -55°C to 125°C | 3492EP | TLV3492AMDREP | Tape and Reel, 2500 |
| TLV3494 | SO-14 | D | -55°C to 125°C | 3494EP | TLV3494AMDREP ⁽³⁾ | Tape and Reel, 2500 |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(3) Product Preview. Contact your Texas Instruments Sales Representative for availability.

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

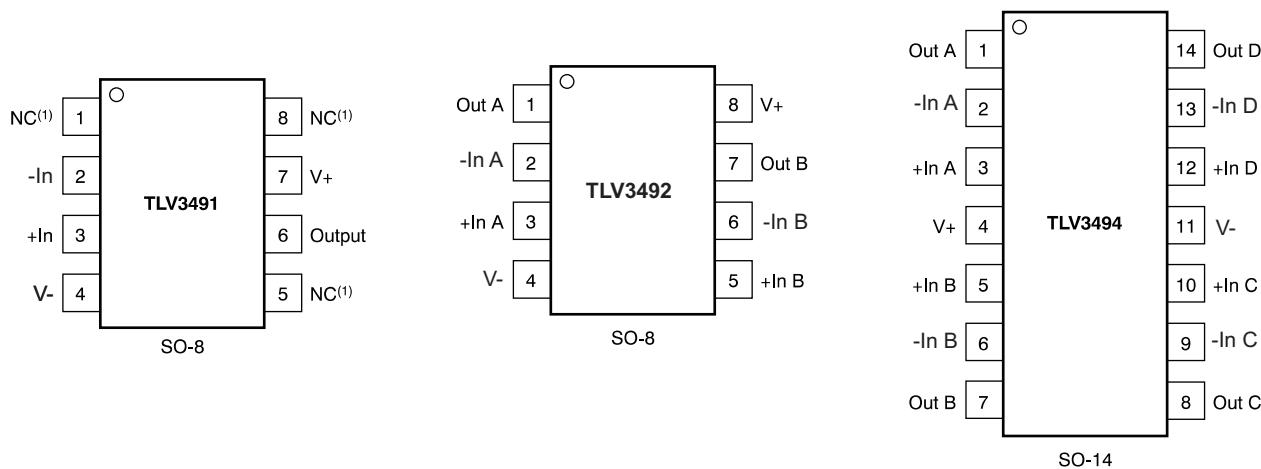
 ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

 Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | | VALUE | UNIT |
|-------------------------------------|------------------------|--|------|
| Supply Voltage | | 5.5 | V |
| Signal Input Terminals | Voltage ⁽²⁾ | (V ₋) – 0.5 to (V ₊) + 0.5 | V |
| | Current ⁽²⁾ | ±10 | mA |
| Output Short-Circuit ⁽³⁾ | | Continuous | |
| Operating Temperature | | –55 to 125 | °C |
| Storage Temperature | | –65 to 150 | °C |
| Junction Temperature | | 150 | °C |
| Lead Temperature (soldering, 10s) | | 300 | °C |
| ESD Rating (Human Body Model) | | 3000 | V |

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

PIN CONFIGURATIONS**Top View**

ELECTRICAL CHARACTERISTICS

 At $T_A = 25^\circ\text{C}$, and $V_S = 1.8 \text{ V to } 5.5 \text{ V}$, unless otherwise noted.

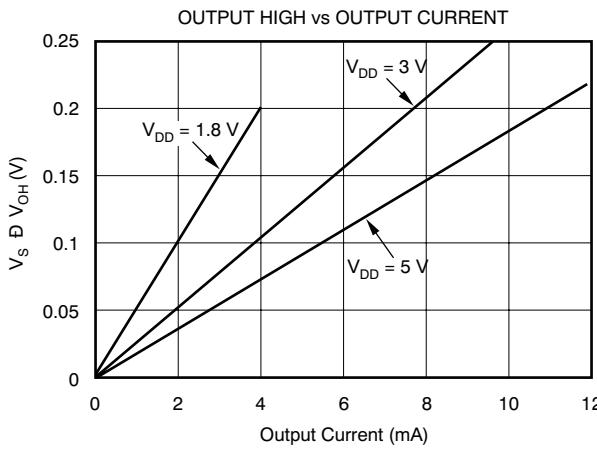
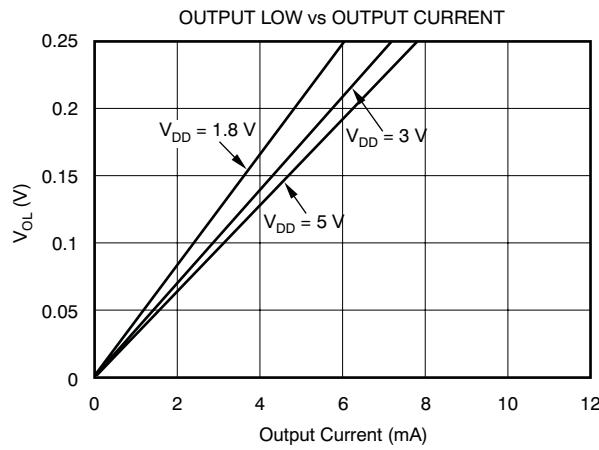
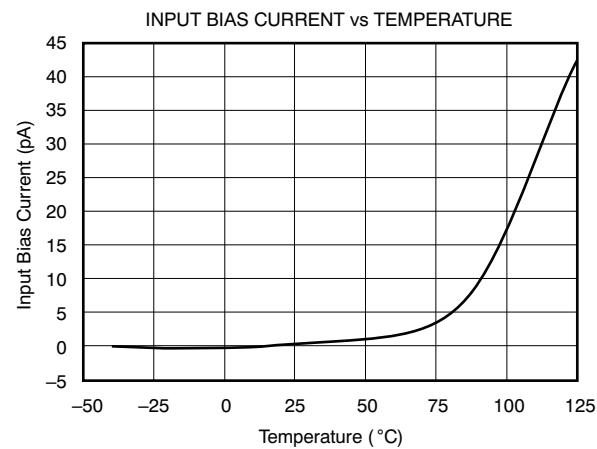
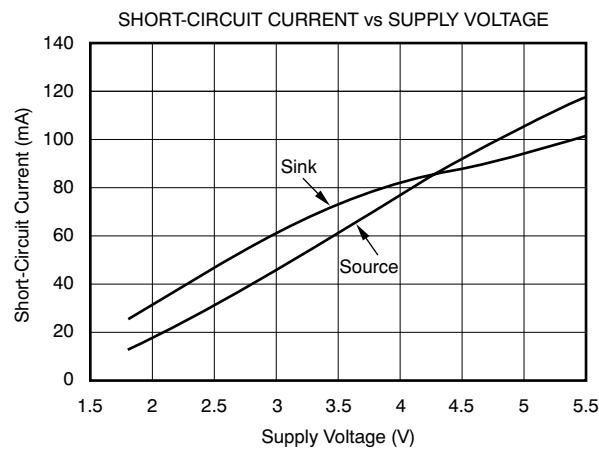
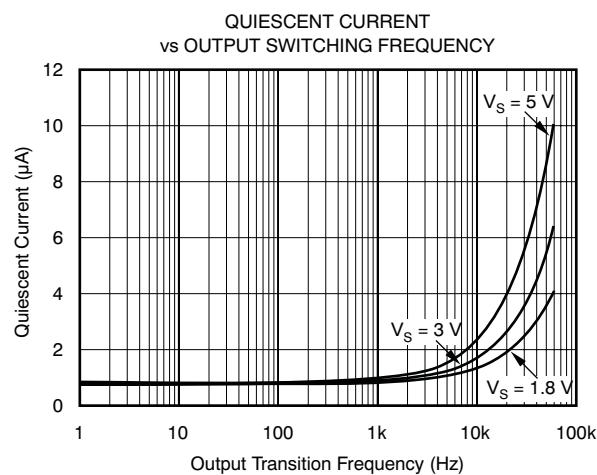
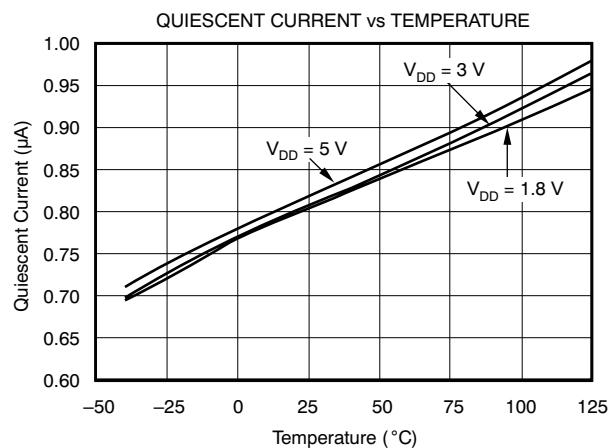
| PARAMETER | TEST CONDITIONS | | $T_A^{(1)}$ | MIN | TYP | MAX | UNIT |
|---|--|--------------------------|-------------|-----------------------------|--------------|------------------------------|------|
| OFFSET VOLTAGE | | | | | | | |
| Input Offset Voltage V_{OS} | $V_{CM} = 0\text{V}$, $I_O = 0\text{mA}$ | 25°C | | ± 3 | ± 15 | μV | |
| | | Full Range | | | ± 25 | | |
| vs Temperature dV_{OS}/dT | $T_A = -55^\circ\text{C to } 125^\circ\text{C}$ | | | ± 12 | | $\mu\text{V}/^\circ\text{C}$ | |
| vs Power Supply $PSRR$ | $V_S = 1.8 \text{ V to } 5.5 \text{ V}$ | 25°C | | 350 | 1000 | $\mu\text{V/V}$ | |
| | | Full Range | | | 1600 | | |
| INPUT BIAS CURRENT | | | | | | | |
| Input Bias Current I_B | $V_{CM} = V_{CC}/2$ | 25°C | | ± 1 | ± 50 | pA | |
| | | Full Range | | | ± 1600 | | |
| Input Offset Current I_{OS} | $V_{CM} = V_{CC}/2$ | 25°C | | ± 1 | ± 50 | pA | |
| | | Full Range | | | ± 200 | | |
| INPUT VOLTAGE RANGE | | | | | | | |
| Common-Mode Voltage Range V_{CM} | | | | $(V-) - 0.2$ | $(V+) + 0.2$ | V | |
| Common-Mode Rejection Ratio $CMRR$ | $V_{CM} = -0.2 \text{ V to } (V+) - 1.5 \text{ V}$ | 25°C | | 60 | 74 | | |
| | | Full Range | | 55 | | | |
| | $V_{CM} = -0.2 \text{ V to } (V+) + 0.2 \text{ V}$ | 25°C | | 54 | 62 | | |
| | | Full Range | | 50 | | | |
| INPUT CAPACITANCE | | | | | | | |
| Common-Mode | | | | 2 | | pF | |
| Differential | | | | 4 | | pF | |
| SWITCHING CHARACTERISTICS | | | | | | | |
| Propagation Delay Time, Low-to-High t_{PLH} | $f = 10 \text{ kHz}$, $V_{STEP} = 1 \text{ V}$ | Input Overdrive = 10 mV | | 12 | | μs | |
| | | Input Overdrive = 100 mV | | 6 | | μs | |
| Propagation Delay Time, High-to-Low t_{PHL} | $f = 10 \text{ kHz}$, $V_{STEP} = 1 \text{ V}$ | Input Overdrive = 10 mV | | 13.5 | | μs | |
| | | Input Overdrive = 100 mV | | 6.5 | | μs | |
| Rise Time t_R | $C_L = 10 \text{ pF}$ | | | 100 | | ns | |
| Fall Time t_F | $C_L = 10 \text{ pF}$ | | | 100 | | ns | |
| OUTPUT | | | | | | | |
| Voltage Output High from Rail V_{OH} | $V_S = 5 \text{ V}$, $I_{OUT} = -5 \text{ mA}$ | Full Range | | 90 | 300 | mV | |
| Voltage Output Low from Rail V_{OL} | $V_S = 5 \text{ V}$, $I_{OUT} = 5 \text{ mA}$ | Full Range | | 160 | 300 | mV | |
| Short-Circuit Current I_{SC} | | | | See Typical Characteristics | | | |
| POWER SUPPLY | | | | | | | |
| Specified Voltage Range V_S | | | | 1.8 | 5.5 | V | |
| Quiescent Current ⁽²⁾ I_Q | $V_S = 5.5 \text{ V}$, $V_O = \text{High}$ | 25°C | | 0.85 | 1.2 | μA | |
| | | Full Range | | | 2.1 | | |
| TEMPERATURE RANGE | | | | | | | |
| Specified Range T_A | | | | -55 | 125 | $^\circ\text{C}$ | |
| Storage Range | | | | -65 | 150 | $^\circ\text{C}$ | |
| Thermal Resistance, θ_{JA} | | | | | | | |
| SO-8 | | | | 165 | | $^\circ\text{C/W}$ | |
| SO-14 | | | | 133 | | $^\circ\text{C/W}$ | |

 (1) Full Range is $-55^\circ\text{C to } 125^\circ\text{C}$.

 (2) I_Q per channel.

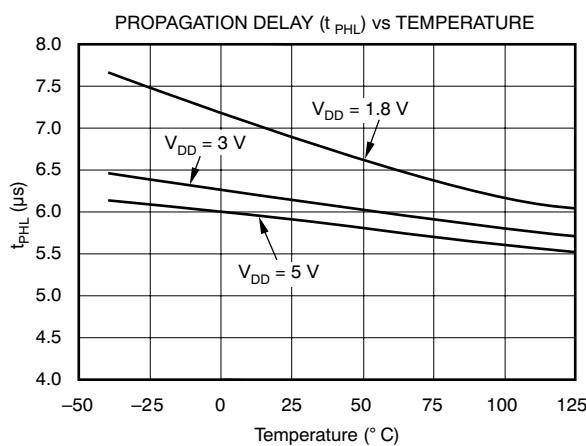
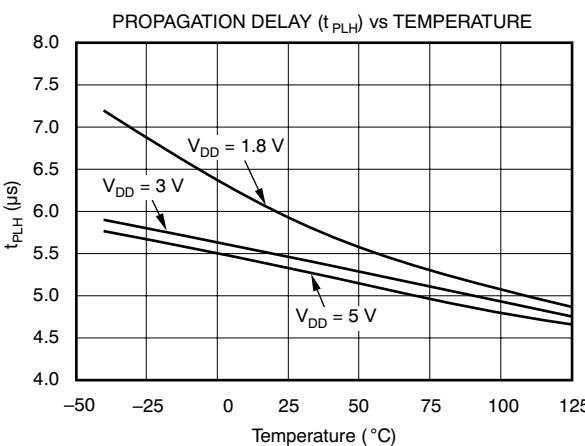
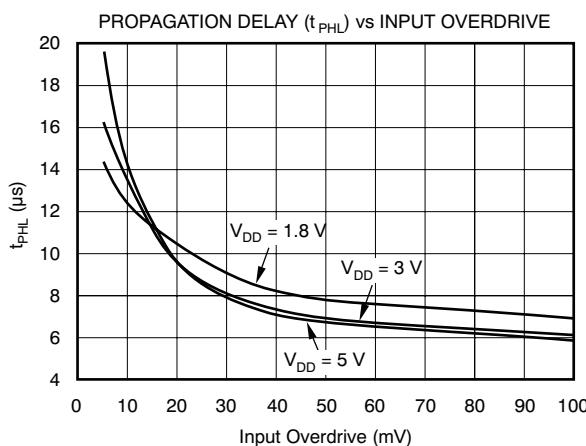
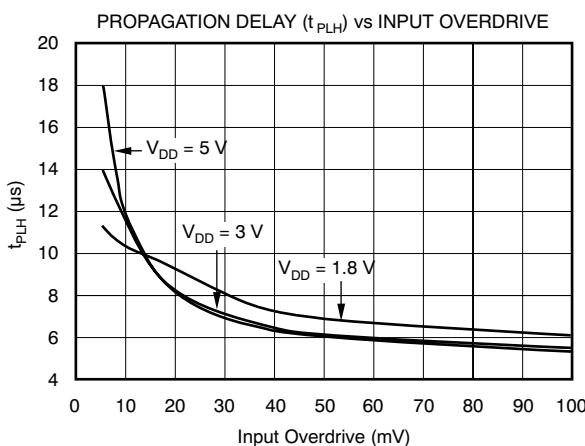
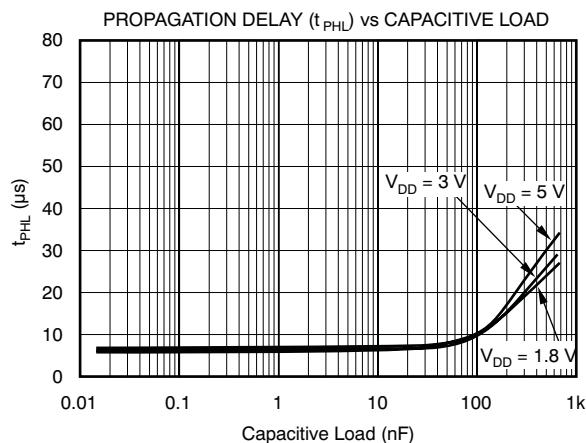
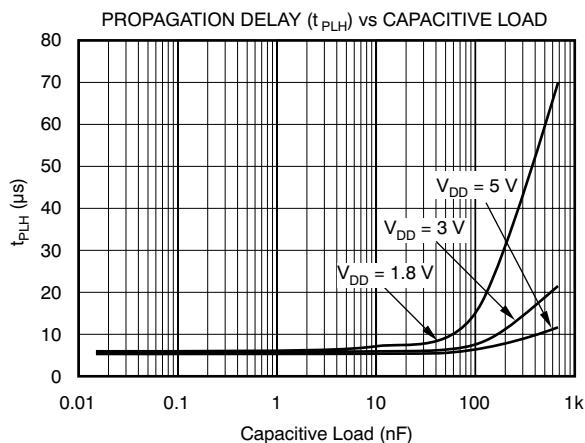
TYPICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$, $V_S = 1.8\text{ V}$ to 5.5 V , and Input Overdrive = 100 mV , unless otherwise noted.



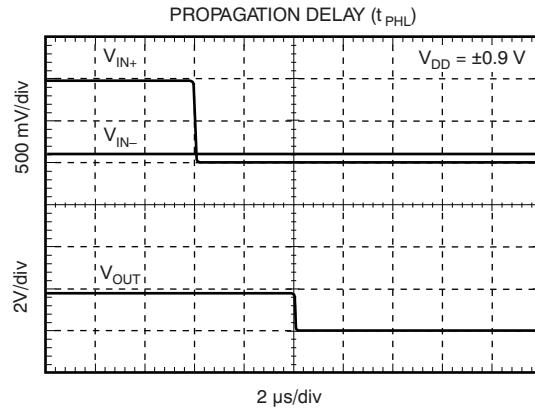
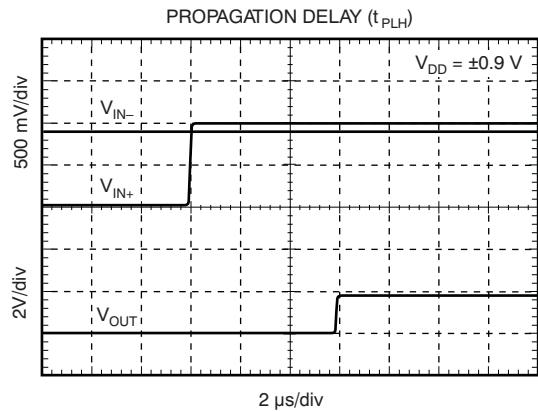
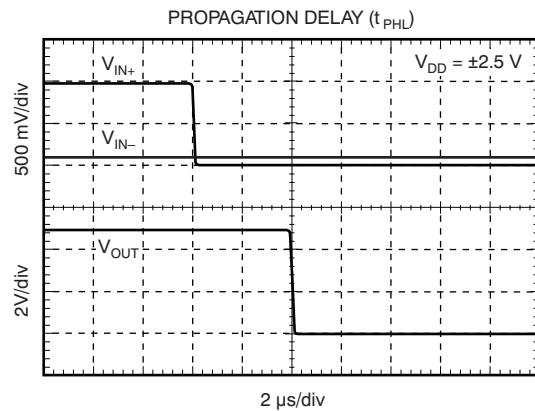
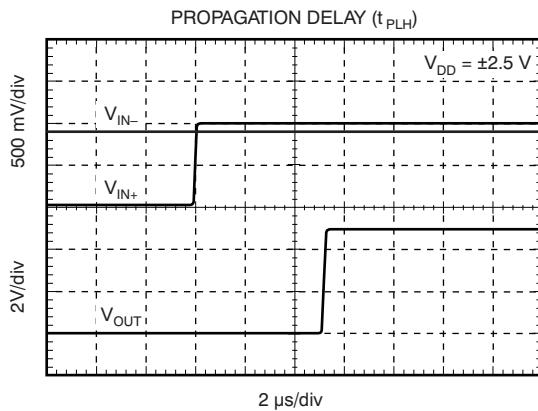
TYPICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ\text{C}$, $V_S = 1.8 \text{ V}$ to 5.5 V , and Input Overdrive = 100 mV , unless otherwise noted.



TYPICAL CHARACTERISTICS (continued)

At $T_A = 25^\circ\text{C}$, $V_S = 1.8 \text{ V}$ to 5.5 V , and Input Overdrive = 100 mV , unless otherwise noted.



APPLICATION INFORMATION

The TLV349x family of comparators features rail-to-rail input and output on supply voltages as low as 1.8 V. The push/pull output stage is optimal for reduced power budget applications and features no shoot-through current. Low supply voltages, common-mode input range beyond supply rails, and a typical supply current of 0.8 μ A make the TLV349x family an excellent candidate for battery-powered applications with single-cell operation.

BOARD LAYOUT

Figure 1 shows the typical connections for the TLV349x. To minimize supply noise, power supplies should be capacitively decoupled by a 0.01 μ F ceramic capacitor in parallel with a 10 μ F electrolytic capacitor. Comparators are very sensitive to input noise. Proper grounding (use of ground plane) will help maintain specified performance of the TLV349x family.

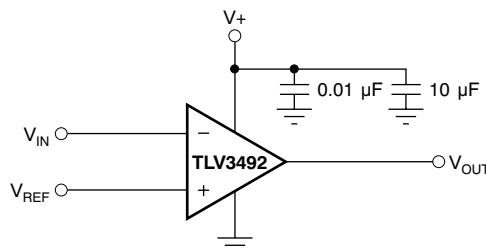


Figure 1. Basic Connections of the TLV3492

SETTING REFERENCE VOLTAGE

It is important to use a stable reference when setting the transition point for the TLV349x. The REF1004 provides a 1.25-V reference voltage with low drift and only 8 μ A of quiescent current.

EXTERNAL HYSTERESIS

Comparator inputs have no noise immunity within the range of specified offset voltage (± 15 mV). For noisy input signals, the comparator output may display multiple switching as input signals move through the switching threshold. The typical comparator threshold of the TLV349x is ± 15 mV. To prevent multiple switching within the comparator threshold of the TLV349x, external hysteresis may be added by connecting a small amount of feedback to the positive input. Figure 2 shows a typical topology used to introduce hysteresis, described by the equation:

$$V_{HYST} = \frac{V^+ \times R1}{R1 + R2}$$

V_{HYST} will set the value of the transition voltage required to switch the comparator output by increasing the threshold region, thereby reducing sensitivity to noise.

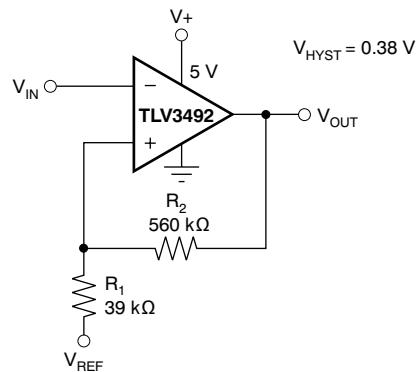


Figure 2. Adding Hysteresis to the TLV3492

RELAXATION OSCILLATOR

The TLV3492 can be configured as a relaxation oscillator to provide a simple and inexpensive clock output (see Figure 3). The capacitor is charged at a rate of 0.69 RC . It also discharges at a rate of 0.69 RC . Therefore, the period is 1.38 RC . R_1 may be a different value than R_2 .

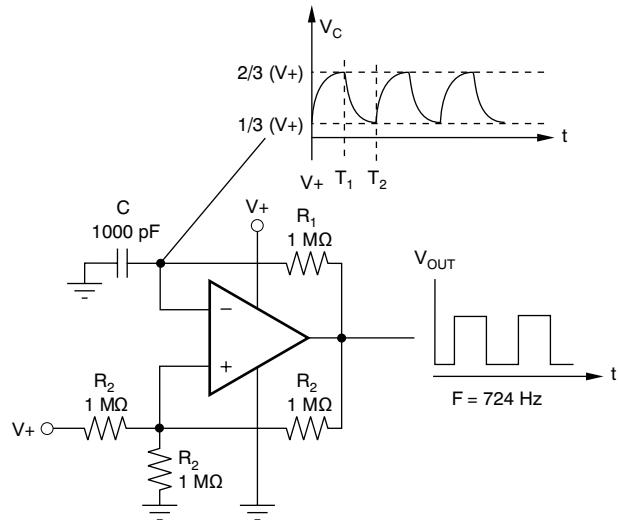


Figure 3. TLV3492 Configured as a Relaxation Oscillator

POWER-ON RESET

The reset circuit shown in Figure 4 provides a time delayed release of reset to the MSP430 microcontroller. Operation of the circuit is based on a stabilization time constant of the supply voltage, rather than on a predetermined voltage value. The negative input is a reference voltage created by a simple resistor divider. These resistor values should be relatively high to reduce the current consumption of the circuit. The positive input is an RC circuit that provides a power-up delay. When power is applied, the output of the comparator is low, holding the processor in the reset condition. Only after allowing time for the supply voltage to stabilize does the positive input of the comparator become higher than the negative input, resulting in a high output state and releasing the processor for operation. The stabilization time required for the supply voltage is adjustable by the selection of the RC component values. Use of a lower-valued resistor in this portion of the circuit will not increase current consumption because no current flows through the RC circuit after the supply has stabilized. The reset delay time needed depends on the power-up characteristics of the system power supply. R_1 and C_1 are selected to allow enough time for the power supply to stabilize. D_1 provides rapid reset if power is lost. In this example, the $R_1 \cdot C_1$ time constant is 10 ms.

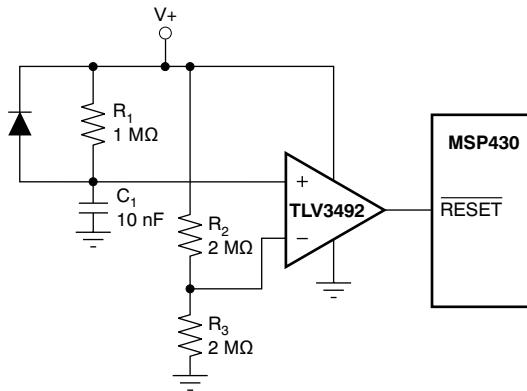


Figure 4. The TLV349x Configured as a Reset Circuit for the MSP430.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TLV3492AMDREP | Last Time Buy | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | 3492EP |
| V62/07635-02XE | Last Time Buy | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | 3492EP |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

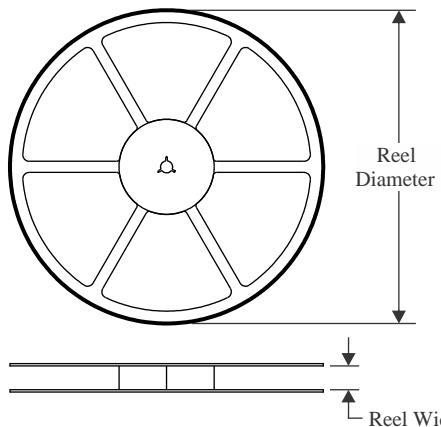
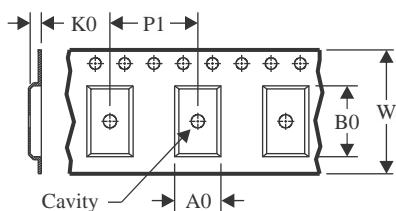
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

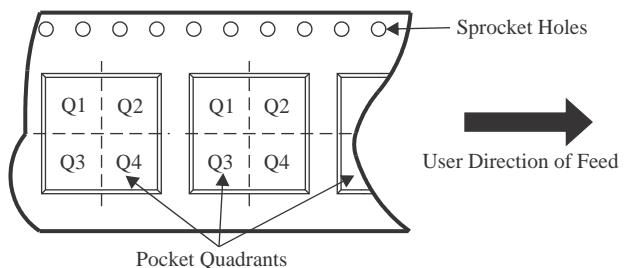
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


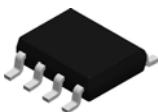
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV3492AMDREP | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV3492AMDREP | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |

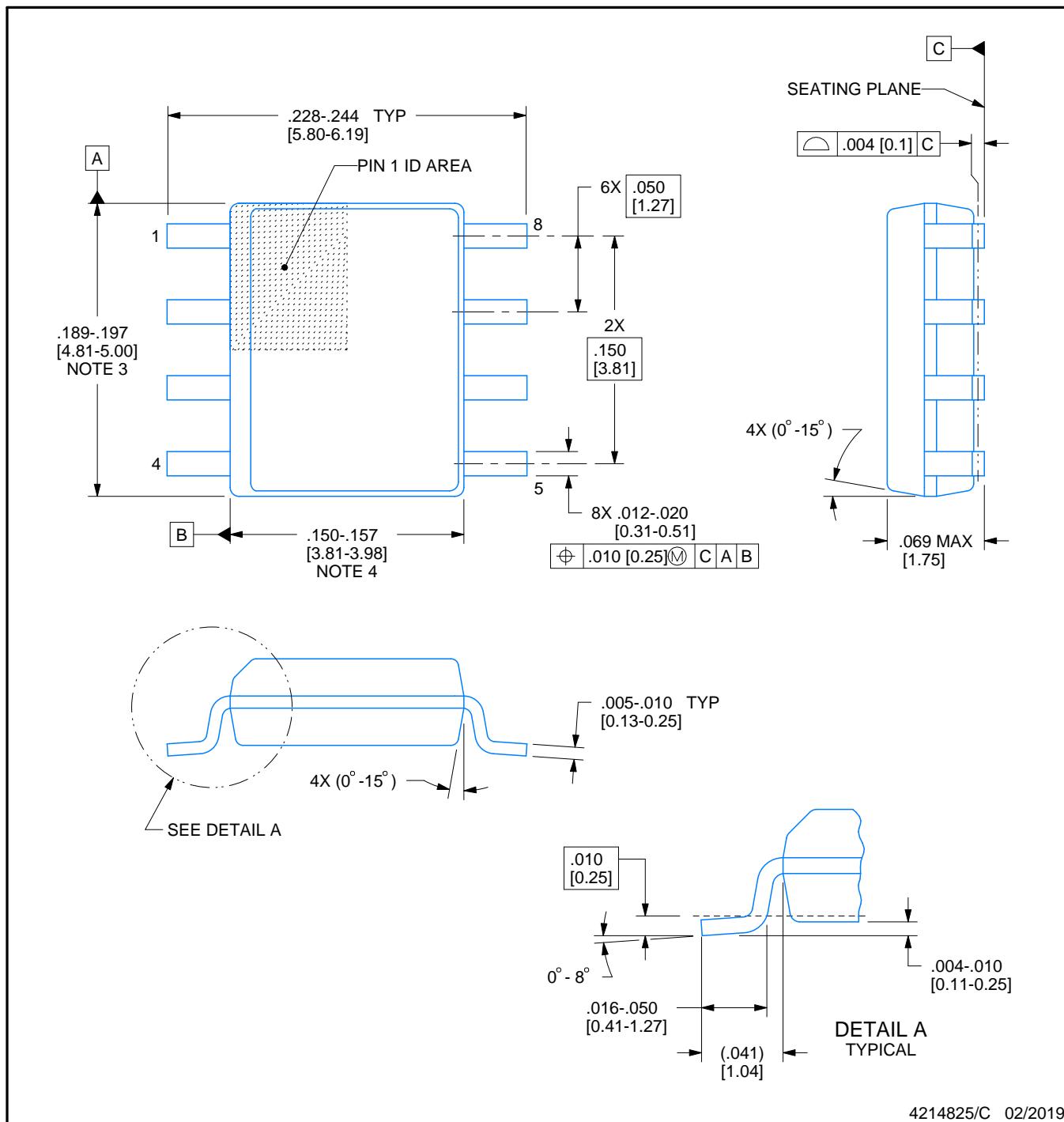


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

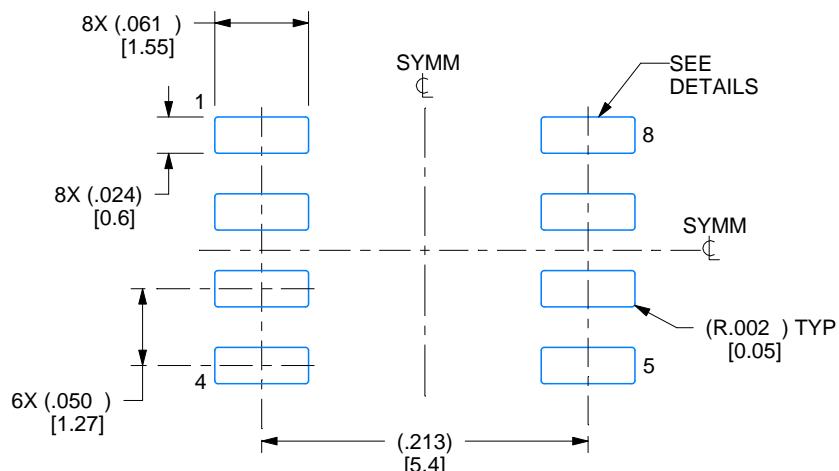
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

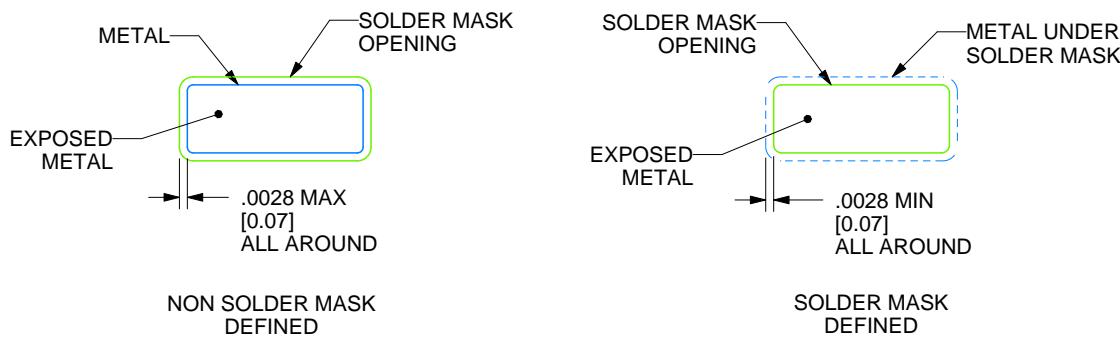
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

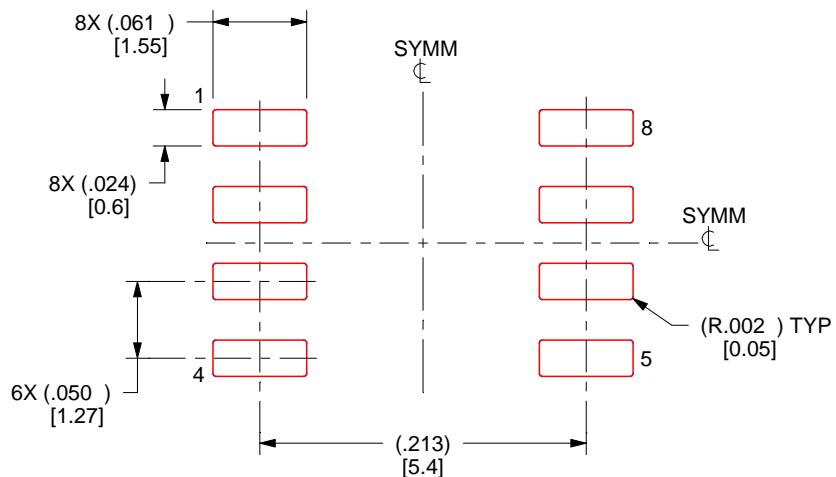
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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