TLV354x 200MHz, Rail-to-Rail I/O, CMOS Operational Amplifiers for Cost-Sensitive Systems

1 Features

- Wide-bandwidth amplifier for cost-sensitive systems
- Unity-gain bandwidth: 200MHz
- High slew rate: 150V/µs
- Low noise: 7.5nV/√Hz
- Rail-to-rail I/O
- High output current: > 100mA
- Excellent video performance:
  - Diff gain: 0.02%, diff phase: 0.09°
  - 0.1dB gain flatness: 40MHz
- Low input bias current: 3pA
- Quiescent current: 5.2mA
- Thermal shutdown
- Supply range: 2.5V to 5.5V

2 Applications

- High-resolution ADC driver amplifiers
- IR touch
- Low-voltage, high-frequency signal processing
- Video processing
- Base transceiver stations
- Optical networking, tunable lasers
- Photodiode transimpedance amplifiers
- Barcode scanners
- Fast current-sensing amplifiers
- Ultrasound imaging

3 Description

The TLV3541, TLV3542 and TLV3544 are single-channel, dual-channel, and quad-channel, low-power (5.2mA per channel), high-speed, unity-gain stable, rail-to-rail input/output operational amplifiers (op amps) designed for video and other applications that require wide bandwidth.

Consuming only 6.5mA (maximum) of supply current, these devices feature 200MHz gain-bandwidth product, 150V/µs slew rate, and a low 7.5nV/√Hz of input noise at f = 1MHz. The combination of high bandwidth, high slew rate, and low noise make the TLV354x family an excellent choice for low voltage, high-speed signal conditioning systems.

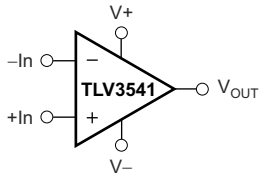
The TLV354x series of op amps are optimized for operation on single or dual supplies as low as 2.5V (±1.25V) and up to 5.5V (±2.75V). Common-mode input range extends beyond the supplies. The output swing is within 100mV of the rails, and supports a wide dynamic range.

The TLV354x devices are specified from –40°C to +125°C. Use the TLV354x family as a plug-in replacement for many commercially available wide bandwidth op amps.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TLV3541	SOIC (8)	3.91mm × 4.90mm
	SOT-23 (5)	2.90mm × 1.60mm
TLV3542	SOIC (8)	3.91mm × 4.90mm
	VSSOP (8)	3.00mm × 3.00mm
TLV3544	SOIC (14)	8.65mm × 3.91mm
	TSSOP (14)	5.00mm × 4.40mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

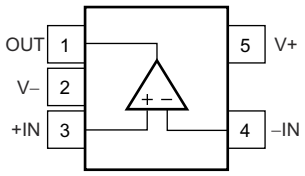
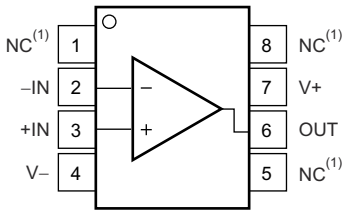


Figure 4-1. TLV3541: DBV Package 5-Pin SOT-23(Top View)



A. NC means no internal connection.

Figure 4-2. TLV3541: D Package 8-Pin SOIC(Top View)

Table 4-1. Pin Functions: TLV3541

PIN			TYPE(1)	DESCRIPTION
NAME	DBV (SOT-23)	D (SOIC)		
+IN	3	3	I	Non inverting input
–IN	4	2	I	Inverting input
NC	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	1	6	O	Output
V–	2	4	—	Negative (lowest) supply
V+	5	7	—	Positive (highest) supply

(1) I = input, O = output

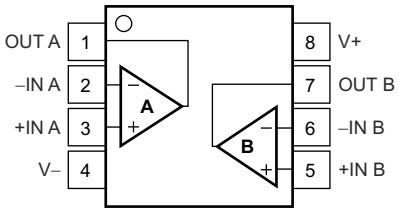


Figure 4-3. TLV3542: DGK and D Packages 8-Pin VSSOP, SOIC(Top View)

Table 4-2. Pin Functions: TLV3542

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
+IN A	3	I	Non inverting input, channel A
+IN B	5	I	Non inverting input, channel B
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) supply
V+	8	—	Positive (highest) supply

(1) I = input, O = output

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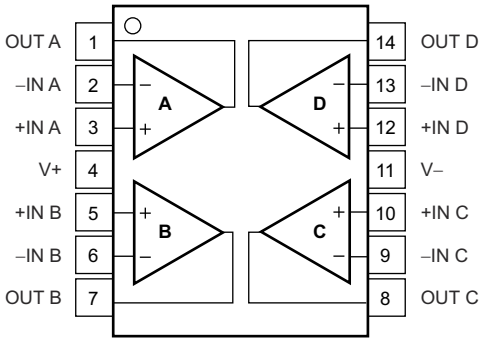

Figure 4-4. TLV3544: D and PW Packages 14-Pin SOIC, TSSOP(Top View)

Table 4-3. Pin Functions: TLV3544

PIN			TYPE[1]	DESCRIPTION
NAME	TLV3544			
	D (SOIC)	PW (TSSOP)		
–IN A	2	2	I	Inverting input, channel A
–IN B	6	6	I	Inverting input, channel B
–IN C	9	9	I	Inverting input, channel C
–IN D	13	13	I	Inverting input, channel D
+IN A	3	3	I	Non inverting input, channel A
+IN B	5	5	I	Non inverting input, channel B
+IN C	10	10	I	Non inverting input, channel C
+IN D	12	12	I	Non inverting input, channel D
OUT A	1	1	O	Output, channel A
OUT B	7	7	O	Output, channel B
OUT C	8	8	O	Output, channel C
OUT D	14	14	O	Output, channel D
V–	11	11	—	Negative (lowest) supply
V+	4	4	—	Positive (highest) supply

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)		7.5	V
V_I	Signal input terminals	(V–) – 0.5	(V+) + 0.5	V
I_I	Signal input terminals	–10	+10	mA
I_{SC}	Output short-circuit(2)	Continuous		
T_A	Operating temperature	–55	125	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage, V– to V+	2.5		5.5	V
T_A	Specified temperature	–40		125	°C

5.4 Thermal Information TLV3541

THERMAL METRIC(1)		TLV3541		UNIT
		D (SOIC)	DBV (SOT-23)	
		8 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158.76	216.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	94.00	115.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	102.70	83.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	38.24	50.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	102.06	82.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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5.5 Thermal Information TLV3542

THERMAL METRIC[1]		TLV3542		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113.9	175.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	60.4	67.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.1	97.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.1	9.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.6	95.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.6 Thermal Information TLV3544

THERMAL METRIC[1]		TLV3544		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.8	92.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.7	27.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.5	33.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.6	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.7	33.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.7 Electrical Characteristics

at T_A = 25°C, R_F = 0Ω, R_L = 1kΩ, and connected to V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5V, T_A = 25°C		±2	±10	mV
dV_{OS}/dT	Input offset voltage drift	V_S = 5V, T_A = –40°C to +125°C		±4.5		µV/°C
PSRR	Input offset voltage vs power supply	V_S = 2.7V to 5.5V, V_{CM} = (V_S / 2) − 0.55V	60	70		dB
INPUT BIAS CURRENT						
I_B	Input bias current			3		pA
I_{OS}	Input offset current			±1		pA
NOISE						
en	Input voltage noise density	f = 1MHz		7.5		nV/√Hz
i_n	Input current noise density	f = 1MHz, for TLV3542 and TLV3544		50		fA/√Hz
i_n	Input current noise density	f = 1MHz, for TLV3541		300		fA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5V, –0.1V < V_{CM} < 3.5V, T_A = 25°C	66	80		dB
CMRR	Common-mode rejection ratio	V_S = 5.5V, –0.1V < V_{CM} < 5.6V, T_A = 25°C	56	68		dB
INPUT IMPEDANCE						

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5.7 Electrical Characteristics (continued)

at T_A = 25°C, R_F = 0Ω, R_L = 1kΩ, and connected to V_S/2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Differential			10^{13} || 2		Ω || pF
	Common-mode			10^{13} || 2		
OPEN-LOOP GAIN						
A_{OL}	Open-loop gain	V_S = 5V, 0.3V < V_O < 5.2V, T_A = 25°C	92	108		dB
FREQUENCY RESPONSE						
f_{-3dB}	Small-signal bandwidth	G = +1, V_O = 100mV_{PP} R_F = 25Ω		200		MHz
		G = +2, V_O = 100mV_{PP}		90		
GBW	Gain-bandwidth product	G = +10		100		MHz
$f_{0.1dB}$	Bandwidth for 0.1dB gain flatness	G = +2, V_O = 100mV_{PP}		40		MHz
SR	Slew rate	V_S = 5V, G = +1, 4V step		150		V/µs
		V_S = 5V, G = +1, 2V step		130		
	Rise-and-fall time	G = +1, V_O = 200mV_{PP}, 10% to 90%, for TLV3542 and TLV3544		2		ns
	Rise-and-fall time	G = +1, V_O = 200mV_{PP}, 10% to 90%, for TLV3541		3		ns
		G = +1, V_O = 2V_{PP}, 10% to 90%		11		
	Settling time	0.1%, V_S = 5V, G = +1, 2V output step		30		ns
	Settling time	0.01%, V_S = 5V, G = +1, 2V output step		60		
	Overload recovery time	V_{IN} × G = V_S		5		ns
HD2	Second-order harmonic distortion	G = +1, f = 1MHz, V_O = 2V_{PP}, R_L = 200Ω, V_{CM} = 1.5V		–75		dBc
HD3	Third-order harmonic distortion	G = +1, f = 1MHz, V_O = 2V_{PP}, R_L = 200Ω, V_{CM} = 1.5V		-83		dBc
	Differential gain error	NTSC, R_L = 150Ω		0.02%		
	Differential phase error	NTSC, R_L = 150Ω		0.09		°
	Channel-to-channel crosstalk	TLV3542, f = 5MHz		–100		dB
		TLV3544, f = 5MHz		–84		
OUTPUT						
	Voltage output swing from rail	V_S = 5V, R_L = 1kΩ, A_{OL} > 90dB, T_A = –40°C to +125°C		0.1	0.3	V
I_O	Output current	V_S = 5V	100			mA
		V_S = 3V		50		
	Closed-loop output impedance	f < 100kHz		0.05		Ω
R_O	Open-loop output resistance	For TLV3542 and TLV3544		35		Ω
R_O	Open-loop output resistance	For TLV3541		39		Ω
POWER SUPPLY						
V_S	Specified voltage		2.7		5	V
V_S	Operating voltage		2.5		5.5	V
I_Q	Quiescent current (per amplifier)	T_A = 25°C, V_S = 5V, I_O = 0A		5.2	6.5	mA
THERMAL SHUTDOWN: JUNCTION TEMPERATURE						
	Shutdown			160		°C
	Reset from Shutdown			140		°C

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5.8 Typical Characteristics

at T_A = 25°C, V_S = 5V, G = 1V/V, R_F = 0Ω, R_L = 1kΩ, and connected to V_S / 2, unless otherwise noted.

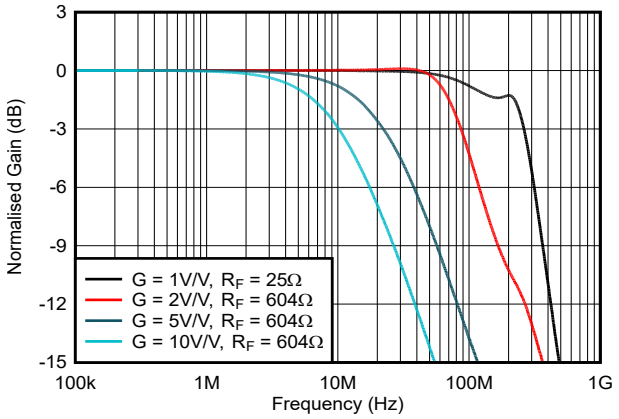
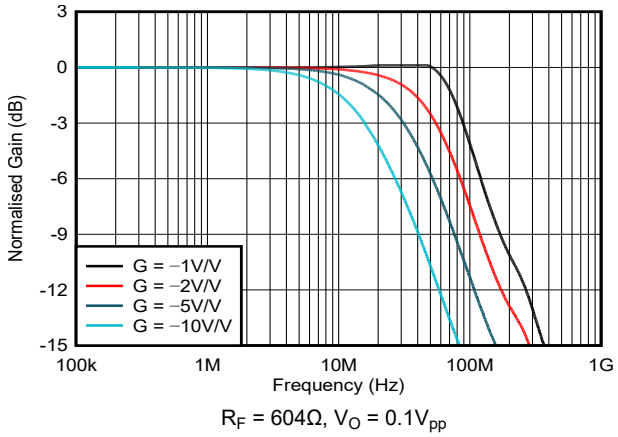


Figure 5-1. Non-Inverting Small-Signal Frequency Response



R_F = 604Ω, V_O = 0.1V_{pp}

Figure 5-2. Inverting Small-Signal Frequency Response

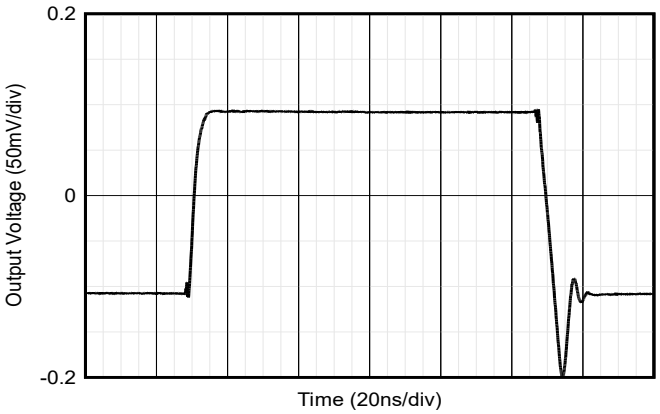


Figure 5-3. Non-Inverting Small- Signal Step Response

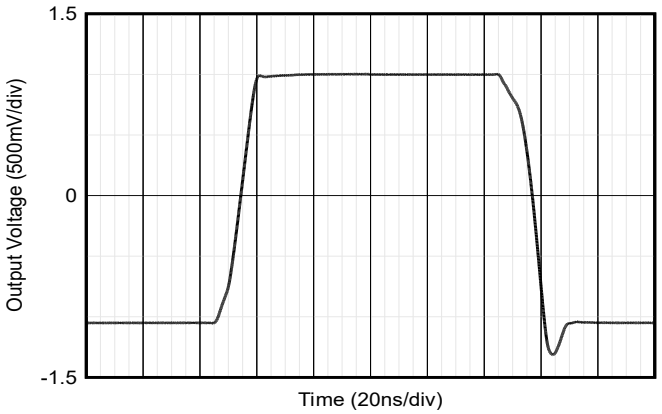
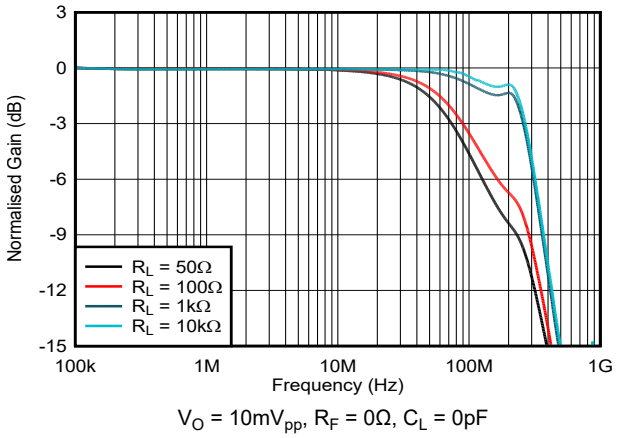
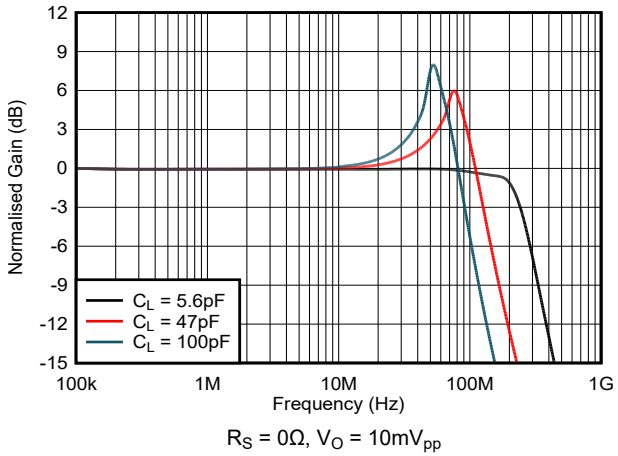


Figure 5-4. Non-Inverting Large- Signal Step Response



V_O = 10mV_{pp}, R_F = 0Ω, C_L = 0pF

Figure 5-5. Frequency Response vs Various R_L Values



R_S = 0Ω, V_O = 10mV_{pp}

Figure 5-6. Frequency Response for Various C_L

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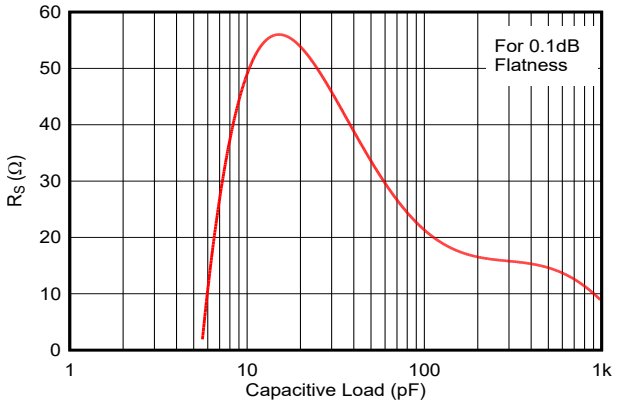

Figure 5-7. Recommended R_S vs Capacitive Load

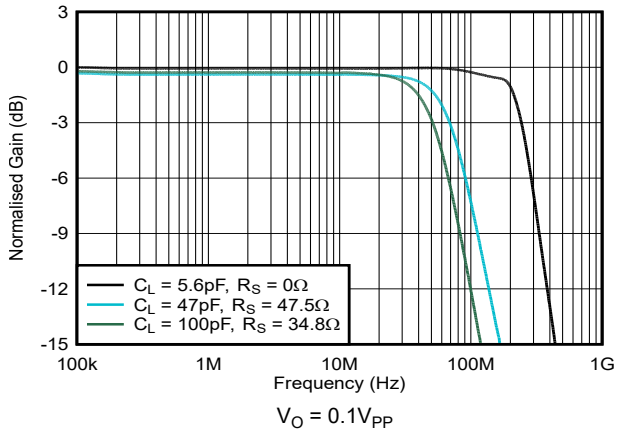

Figure 5-8. Frequency Response vs Capacitive Load

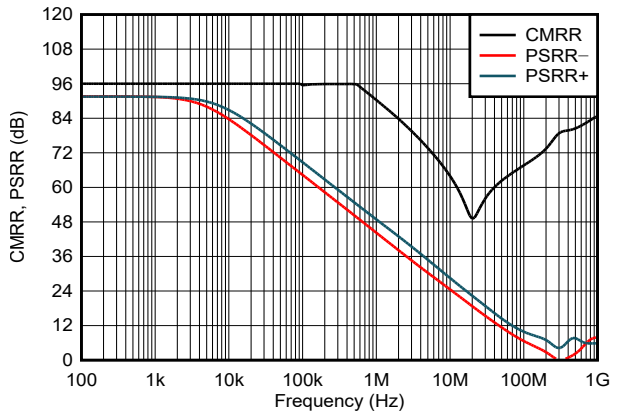

Figure 5-9. Common- Mode Rejection Ratio and Power- Supply Rejection Ratio vs Frequency

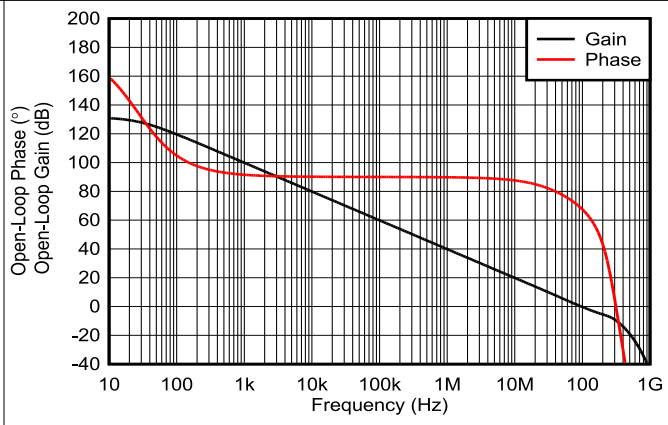

Figure 5-10. Open-Loop Gain and Phase

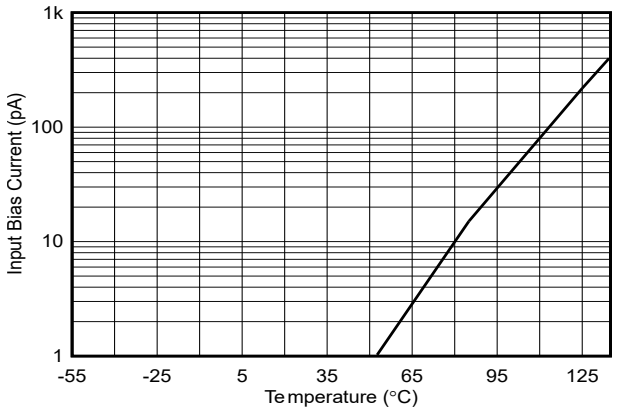

Figure 5-11. Input Bias Current vs Temperature

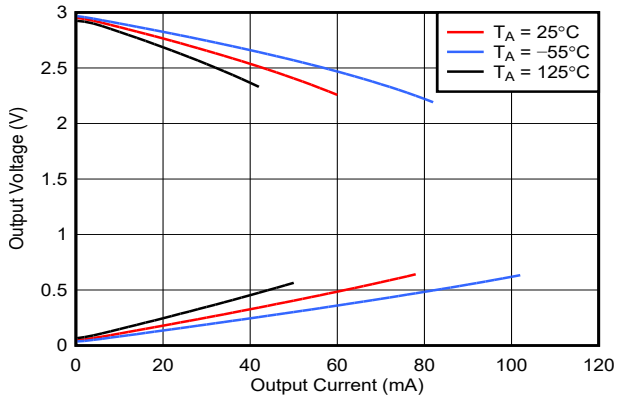

Figure 5-12. Output Voltage Swing vs Output Current for V_S = 3V

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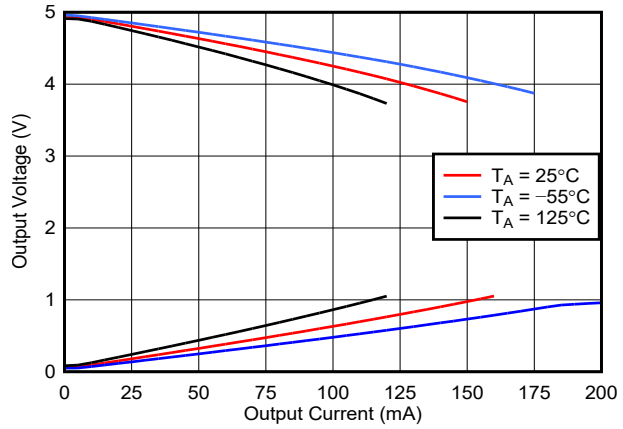

Figure 5-13. Output Voltage Swing vs Output Current for V_S = 5V

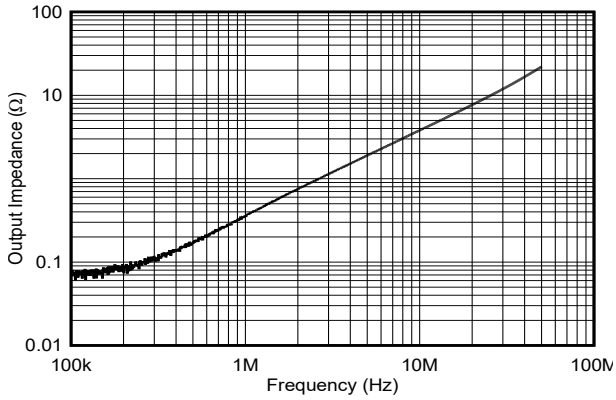

Figure 5-14. Closed-loop Output Impedance vs Frequency

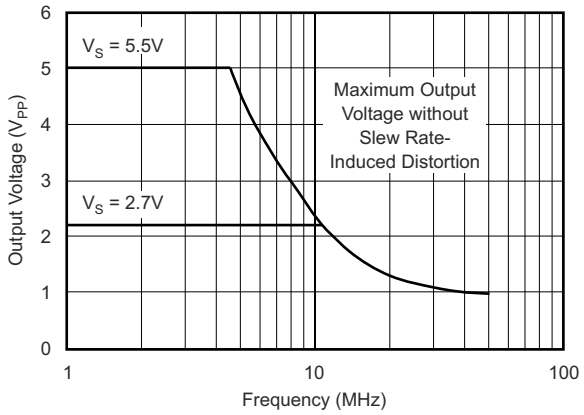

Figure 5-15. Maximum Output Voltage vs Frequency

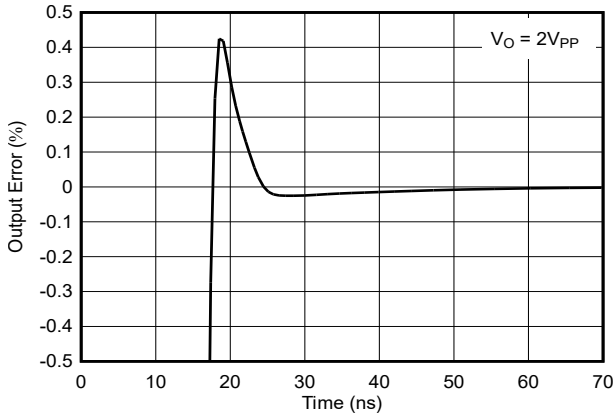

Figure 5-16. Output Settling Time to 0.1%

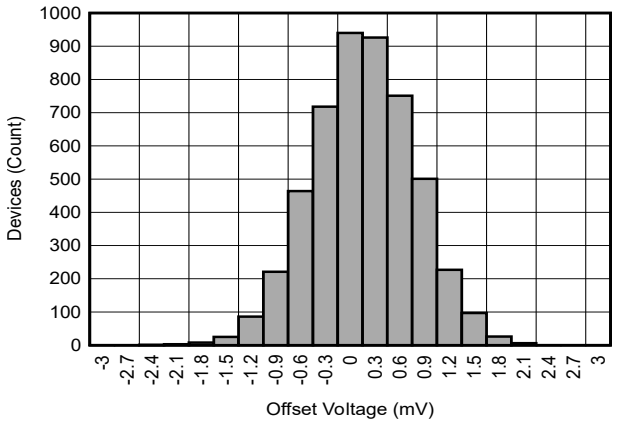

Figure 5-17. Offset Voltage Production Distribution

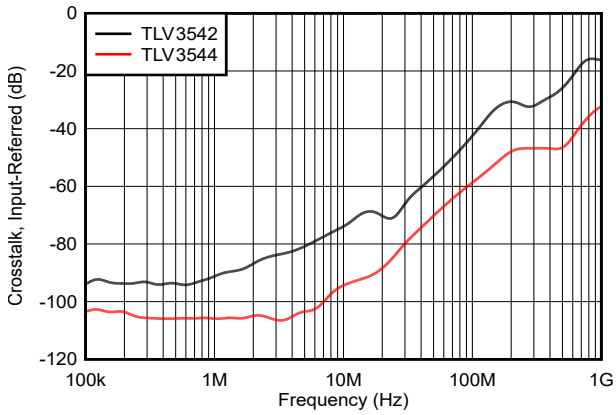

Figure 5-18. Channel-to-Channel Crosstalk

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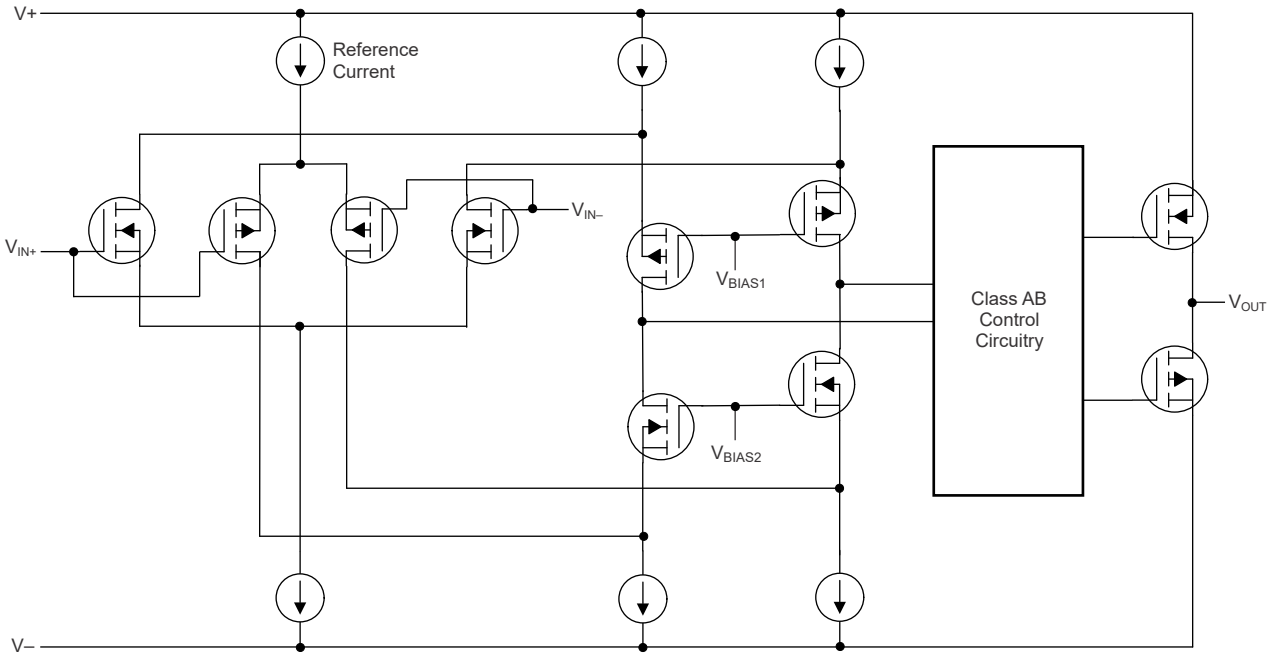
6 Detailed Description

6.1 Overview

The TLV354x is a CMOS, rail-to-rail I/O, high-speed, voltage-feedback operational amplifier designed for video, high-speed, and other applications. The device is available as a single, dual, or quad op amp.

The amplifier features a 100MHz gain bandwidth and a 150V/µs slew rate, but the amplifier is unity-gain stable and operates as a +1V/V voltage follower.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Operating Voltage

The TLV354x is specified over a power-supply range of 2.7V to 5.5V (±1.35V to ±2.75V). However, the supply voltage may range from 2.5V to 5.5V (±1.25V to ±2.75V). Supply voltages higher than 7.5V (absolute maximum) can permanently damage the amplifier.

Parameters that vary over supply voltage or temperature are shown in the *Section 5.8* section.

6.3.2 Rail-to-Rail Input

The specified input common-mode voltage range of the TLV354x extends 100mV beyond the supply rails. This extended range is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Section 6.2*. The N-channel pair is active for input voltages close to the positive rail, typically (V+) − 1.2V to 100mV above the positive supply, while the P-channel pair is on for inputs from 100mV below the negative supply to approximately (V+) − 1.2V. There is a small transition region, typically (V+) − 1.5V to (V+) − 0.9V, in which both pairs are on. This 600mV transition region can vary ±500mV with process variation. Thus, the transition region (with both input stages on) can range from (V+) − 2.0V to (V+) − 1.5V on the low end, up to (V+) − 0.9V to (V+) − 0.4V on the high end.

A double-folded cascode adds the signal from the two input pairs and presents a differential signal to the class AB output stage.

6.3.3 Rail-to-Rail Output

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. For high-impedance loads (> 200Ω), the output voltage swing is typically 100mV from the supply rails. With 10Ω loads,

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a useful output swing can be achieved while maintaining high open-loop gain. See the typical characteristic curves, *Output Voltage Swing vs Output Current* (Figure 5-12 and Figure 5-13).

6.3.4 Output Drive

The TLV354x output stage can supply a continuous output current of ±100mA and yet provide approximately 2.7V of output swing on a 5V supply, as shown in Figure 6-1. For maximum reliability, it is not recommended to run a continuous DC current in excess of ±100mA. Refer to the typical characteristic curves, *Output Voltage Swing vs Output Current* (Figure 5-12 and Figure 5-13). For supplying continuous output currents greater than ±100mA, the TLV354x may be operated in parallel, as shown in Figure 6-2.

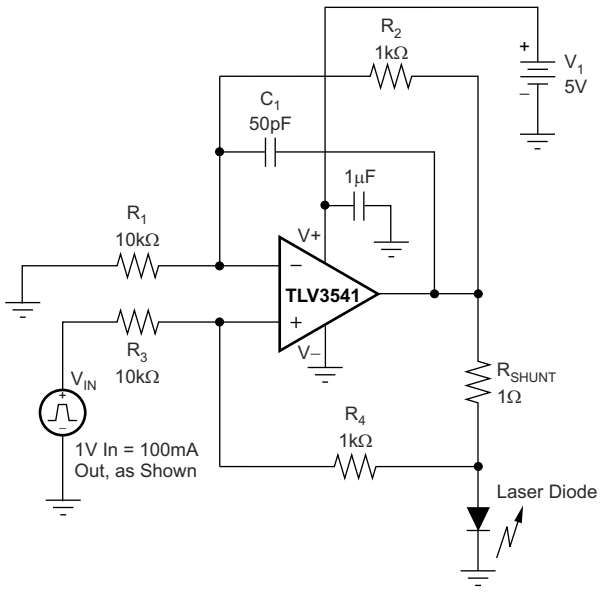

Figure 6-1. Laser Diode Driver

The TLV354x provides peak currents up to 200mA, which corresponds to the typical short-circuit current. Therefore, an on-chip thermal shutdown circuit is provided to protect the TLV354x from dangerously high junction temperatures. At 160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools to below +140°C.

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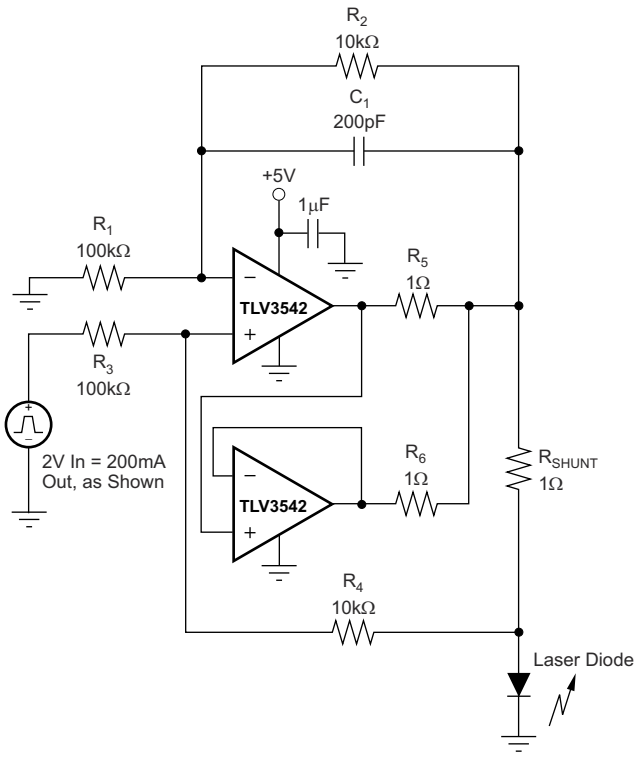

Figure 6-2. Parallel Operation

6.3.5 Video

The TLV354x output stage is capable of driving standard back-terminated 75Ω video cables, as shown in Figure 6-3. By back-terminating a transmission line, the device does not exhibit a capacitive load to its driver. A properly back-terminated 75Ω cable does not appear as capacitance; the device presents a 150Ω resistive load to the TLV354x output.

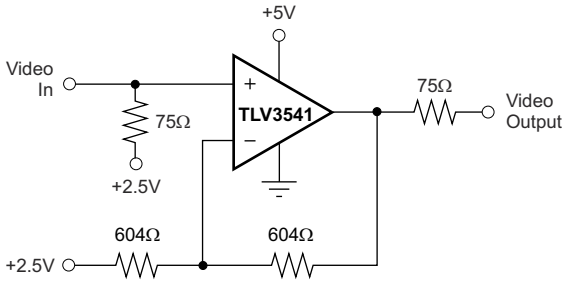

Figure 6-3. Single-Supply Video Line Driver

The TLV3542 can be used as an amplifier for RGB graphic signals, which have a voltage of zero at the video black level, by offsetting and AC-coupling the signal. See Figure 6-4.

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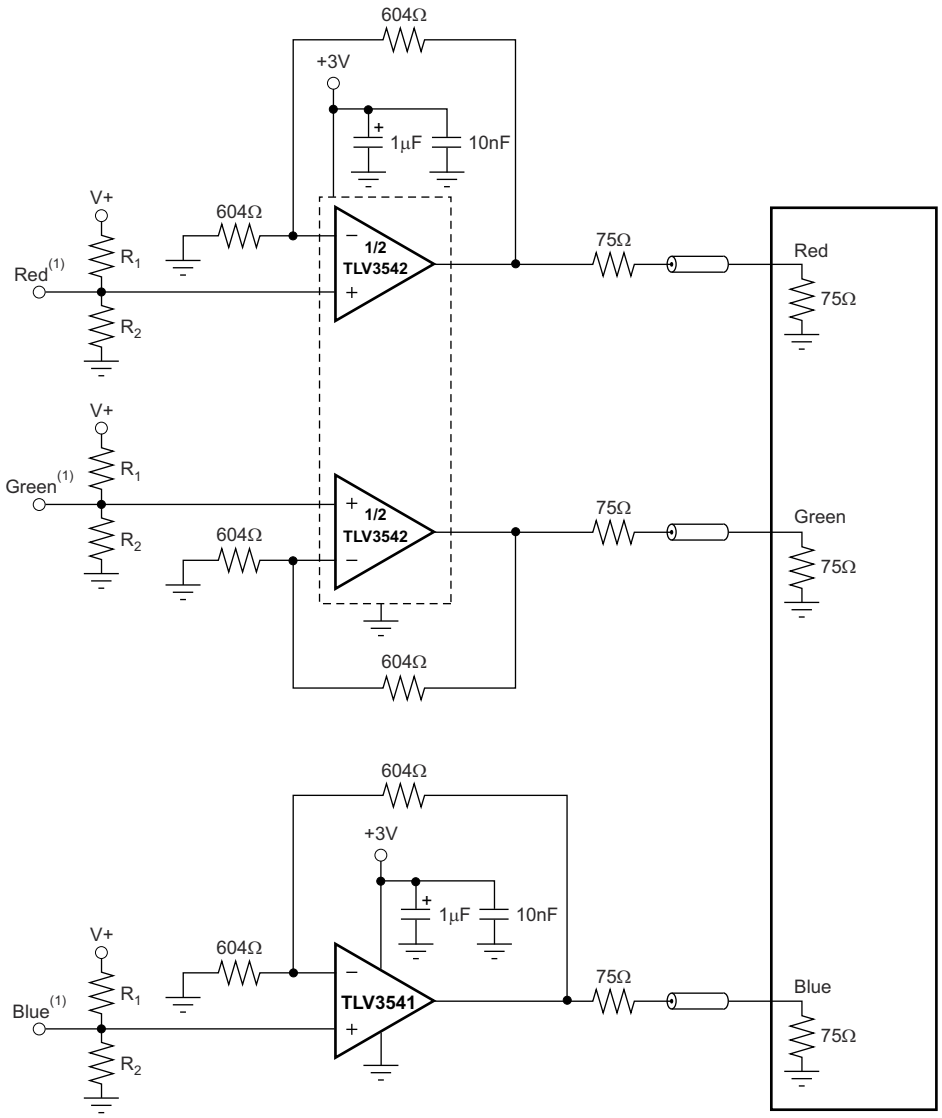

A. Source video signal offsets 300mV above ground to accommodate op amp swing−to−ground capability.

Figure 6-4. RGB Cable Driver

6.3.6 Driving Analog-to-Digital Converters

The TLV354x series op amps offer 60ns of settling time to 0.01%, making the op amps a good choice for driving high- and medium-speed sampling A/D converters and buffering reference circuits. The TLV354x series provide an effective means of buffering the A/D converter input capacitance and resulting charge injection while providing signal gain. For applications requiring high DC accuracy, TI recommends using the OPA350 series.

Figure 6-5 shows the TLV3541 driving an A/D converter. With the TLV3541 in an inverting configuration, a capacitor across the feedback resistor can filter high-frequency noise in the signal.

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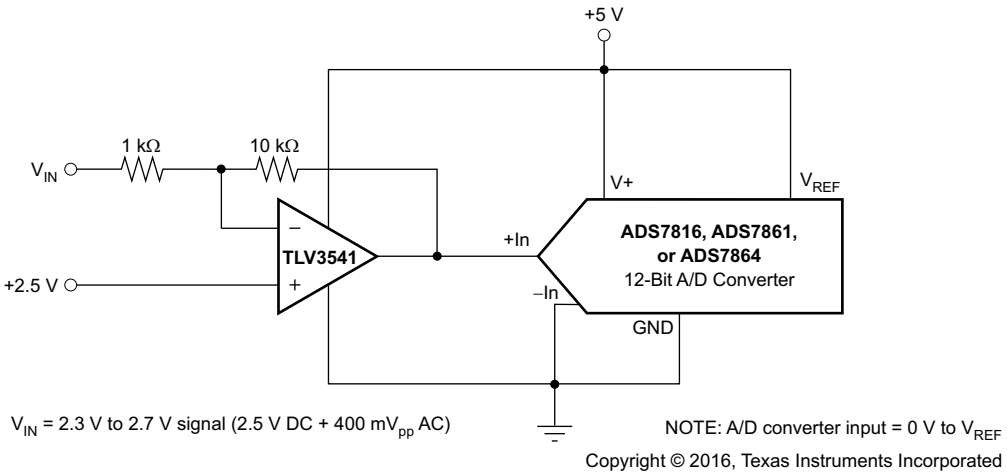

Figure 6-5. The TLV3541 in Inverting Configuration Driving the ADS7816

6.3.7 Capacitive Load and Stability

The TLV354x series op amps can drive a wide range of capacitive loads. However, all op amps under certain conditions may become unstable. Op amp configuration, gain, and load value are just a few of the factors to consider when determining stability. An op amp in unity-gain configuration is most susceptible to the effects of capacitive loading. The capacitive load reacts with the device output resistance, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin. Refer to the typical characteristic curve, *Frequency Response for Various C_L* (Figure 5-6) for details.

The TLV354x topology enhances the ability to drive capacitive loads. In unity gain, these op amps perform well with large capacitive loads. Refer to the typical characteristic curves, *Recommended R_S vs Capacitive Load* (Figure 5-7) and *Frequency Response vs Capacitive Load* (Figure 5-8) for details.

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10Ω to 20Ω resistor in series with the output, as shown in Figure 6-6. This configuration significantly reduces ringing with large capacitive loads. See the typical characteristic curve, *Frequency Response vs Capacitive Load* (Figure 5-8). However, if there is a resistive load in parallel with the capacitive load, R_S creates a voltage divider. This voltage division introduces a DC error at the output and slightly reduces output swing. This error may be insignificant. For instance, with R_L = 10kΩ and R_S = 20Ω, there is an error of approximately 0.2% at the output.

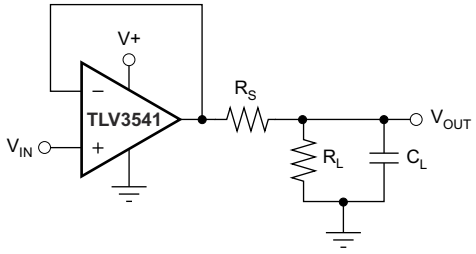

Figure 6-6. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive

6.3.8 Wideband Transimpedance Amplifier

Wide bandwidth, low input bias current, and low input voltage and current noise make the TLV354x a appropriate wideband photodiode transimpedance amplifier for low-voltage, single-supply applications. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design, as shown in Figure 6-7, are the expected diode capacitance (including the parasitic input common-mode and differential-mode input capacitance (2 + 2) pF for the TLV354x), the desired transimpedance gain (R_F), and the Gain-Bandwidth Product (GBW) for the TLV354x (100MHz,

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typical). With these three variables set, the feedback capacitor value (C_F) can be set to control the frequency response.

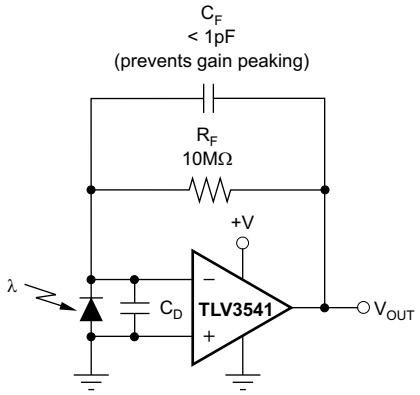

Figure 6-7. Transimpedance Amplifier

To achieve a flat, second-order, Butterworth frequency response, the feedback pole must be set as shown in Equation 1:

$$\frac{1}{2\,\pi\,R_F\,C_F} = \sqrt{\frac{GBP}{4\,\pi\,R_F\,C_D}} \quad (1)$$

Typical surface-mount resistors have a parasitic capacitance of approximately 0.2pF that must be deducted from the calculated feedback capacitance value. Bandwidth is calculated by Equation 2:

$$f_{-3dB} = \sqrt{\frac{GBP}{2\,\pi\,R_F\,C_D}}\ Hz \quad (2)$$

For even higher transimpedance bandwidth, the high-speed CMOS OPA355 (200MHz GBW) or the OPA655 (400MHz GBW) can be used.

6.4 Device Functional Modes

The TLV354x has dual functional modes and is operational when the power-supply voltage is greater than 2.5V (±1.25V). The maximum power-supply voltage for the TLV354x is 5.5V (±2.75V). At +160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools to below +140°C.

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLV354x are wide bandwidth, low-noise, rail-to-rail input and output amplifiers. These devices operate from 2.5V to 5.5V, are unity-gain stable, and suitable for a wide range of general-purpose applications The input common-mode voltage range includes both rails, and allows the TLV354x device to be used in any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes the device ideal for driving analog-to-digital converters (ADCs).

The TLV354x family of devices features a 200MHz bandwidth and 150V/µs slew rate with only 7.5nV/√Hz of broadband noise.

7.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier, as shown in Figure 7-1. An inverting amplifier takes a positive voltage on the input and outputs a signal inverted to the input, making a negative voltage of the same magnitude. In the same manner, the amplifier makes negative input voltages positive on the output. In addition, amplification can be added by selecting the input resistor R_I and the feedback resistor R_F.

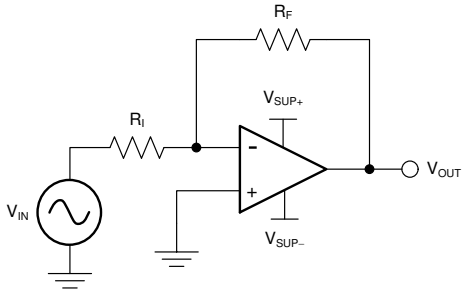

Figure 7-1. Application Schematic

7.2.1 Design Requirements

The supply voltage must be chosen to be larger than the input voltage range and the desired output range. The limits of the input common-mode range (V_{CM}) and the output voltage swing to the rails (V_O) must be considered. For instance, this application scales a signal of ±0.5V (1V) to ±1.8V (3.6V). Setting the supply at ±2.5V is sufficient to accommodate this application.

7.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using Equation 3 and Equation 4:

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (3)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (4)$$

When the desired gain is determined, select a value for R_I or R_F. Selecting a value in the kilo ohm range is desirable for general-purpose applications because the amplifier circuit uses currents in the milliamp range. This milliamp current range confirms the device does not draw too much current. The trade-off is that large resistors (100s of kilo ohms) draw the smallest current but generate the highest noise. Small resistors (100s of ohms)

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generate low noise but draw high current. This example uses 10kΩ for R_I, meaning 36kΩ is used for R_F. These values are determined by Equation 5:

$$A_V = -\frac{R_F}{R_I} \quad (5)$$

7.2.3 Application Curve

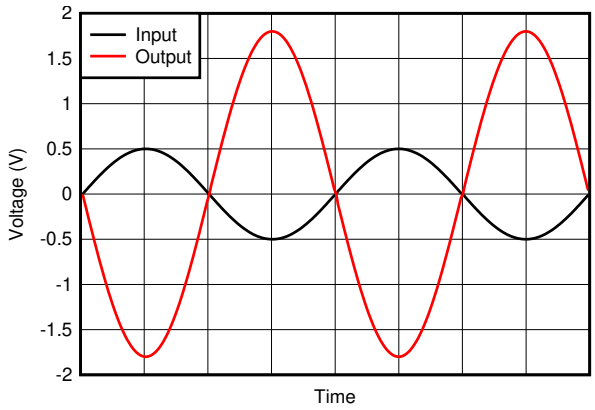

Figure 7-2. Inverting Amplifier Input and Output

7.3 System Examples

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting terminal of the amplifier, as shown in Figure 7-3.

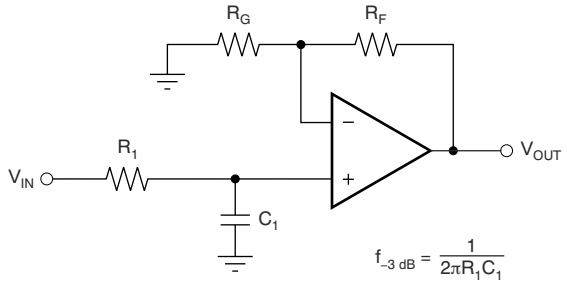

Figure 7-3. Single-Pole, Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task, as shown in Figure 7-4. For best results, the amplifier must have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to follow this guideline can result in phase shift of the amplifier.

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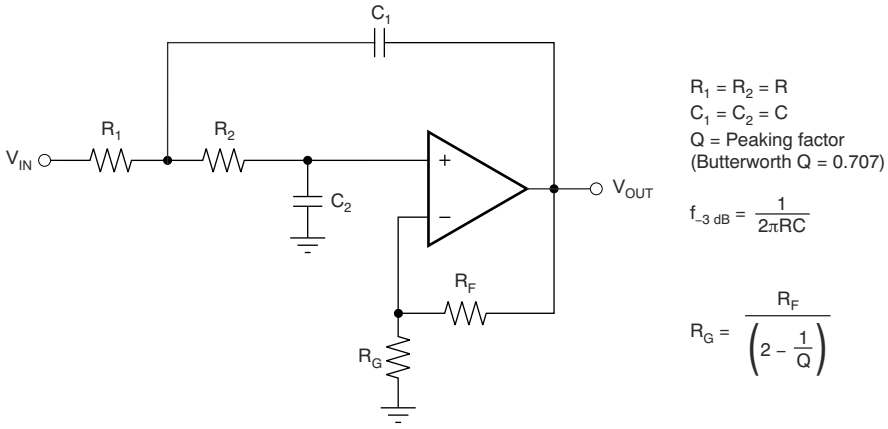

Figure 7-4. Two-Pole, Low-Pass, Sallen-Key Filter

7.4 Power Supply Recommendations

The TLV354x family is specified from 2.7V to 5.5V (±1.35V to ±2.75V), although the devices can operate from 2.5V to 5.5V (±1.25V to ±2.75V); many specifications apply from –40°C to +125°C. *Section 5.8* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7.5V can permanently damage the device. (See Section 5.1).

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Section 7.5.1*.

7.4.1 Input and ESD Protection

The TLV354x family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10mA, as stated in the *Absolute Maximum Ratings* table. Figure 7-5 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input, which must be kept to a minimum in noise-sensitive applications.

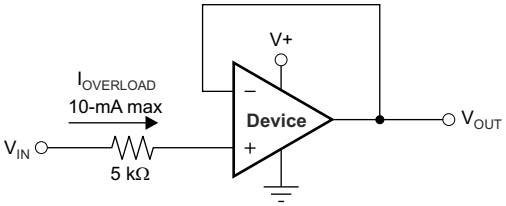

Figure 7-5. Input Current Protection

7.5 Layout

7.5.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise propagates into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.

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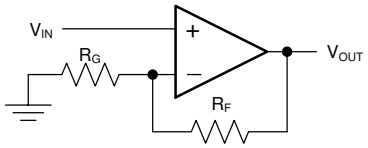
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keep R_F and R_G close to the inverting input to minimize parasitic capacitance, as shown in Figure 7-6.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

7.5.2 Layout Example



(Schematic Representation)

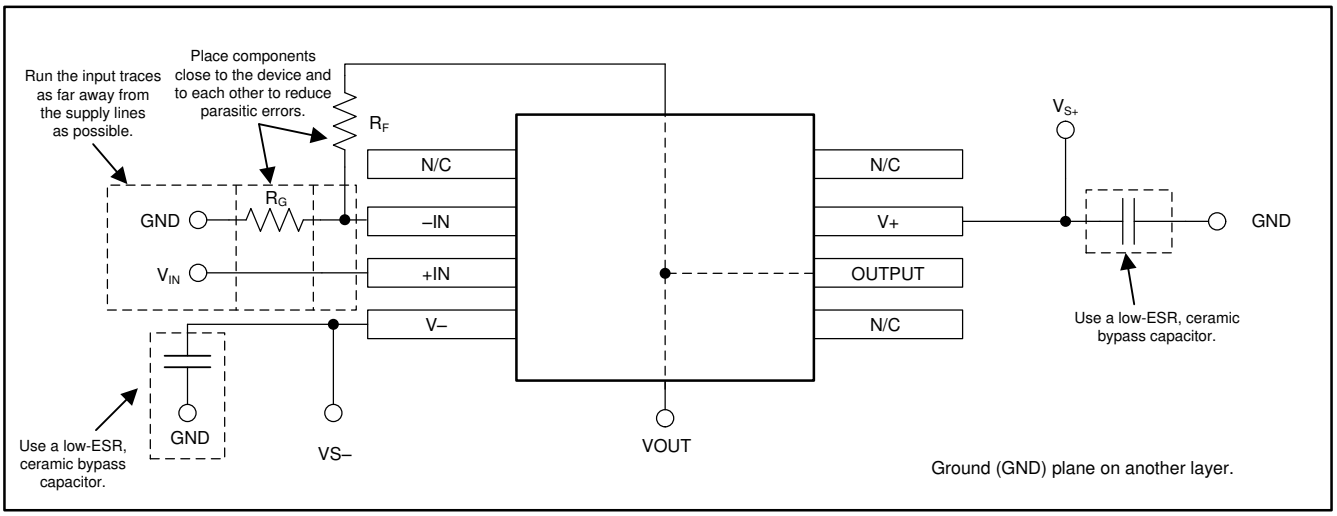


Figure 7-6. Operational Amplifier Board Layout for Noninverting Configuration

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8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

TI recommends using the following reference documents for the TLV354x device. All are available for download at www.ti.com unless otherwise noted.

- *Handbook of Operational Amplifier Applications*
- *Analog Engineer's Pocket Reference*

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2016) to Revision A (August 2026)	Page
• Updated Thermal information, current noise, rise-and-fall time, Open-loop output resistance in Specifications table for TLV3541	6
• Updated new format plots in Typical Characteristics	8

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10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV3541IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17MD
TLV3541IDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17MD
TLV3541IDBVR.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17MD
TLV3541IDBVRG4	Last Time Buy	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17MD
TLV3541IDBVRG4.A	Last Time Buy	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17MD
TLV3541IDBVRG4.B	Last Time Buy	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17MD
TLV3541IDBVT	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17MD
TLV3541IDBVT.B	Active	Production	SOT-23 (DBV) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17MD
TLV3541IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL3541
TLV3541IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL3541
TLV3541IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL3541
TLV3542IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	18TE
TLV3542IDGKR.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	18TE
TLV3542IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	18TE
TLV3542IDGKT.B	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	18TE
TLV3542IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL3542
TLV3542IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL3542
TLV3542IDR.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL3542
TLV3544IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV3544A
TLV3544IDR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV3544A
TLV3544IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 3544
TLV3544IPWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV 3544

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV3544 :

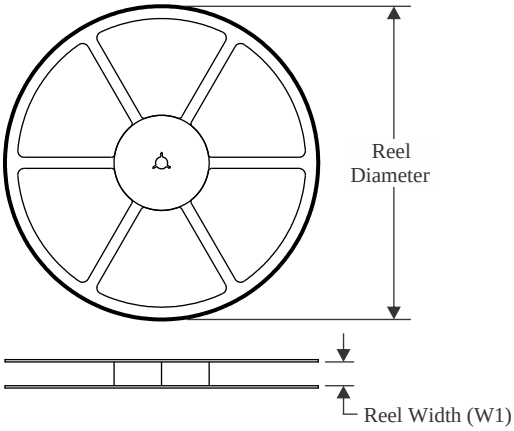
- Automotive : TLV3544-Q1

NOTE: Qualified Version Definitions:

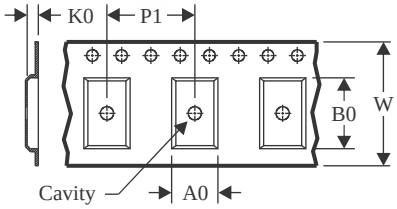
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

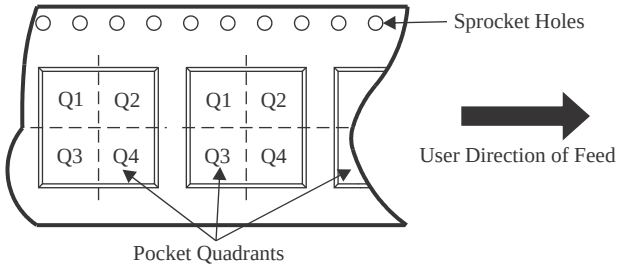


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

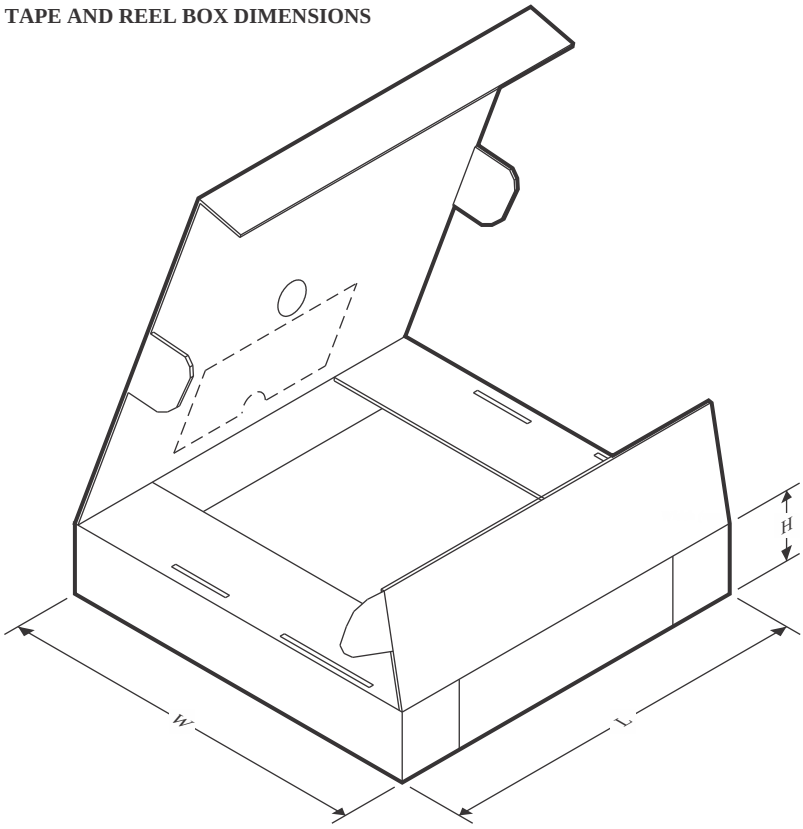
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3541IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV3541IDBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV3541IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV3541IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV3542IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV3542IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV3542IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TLV3542IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV3542IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
TLV3542IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV3544IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV3544IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

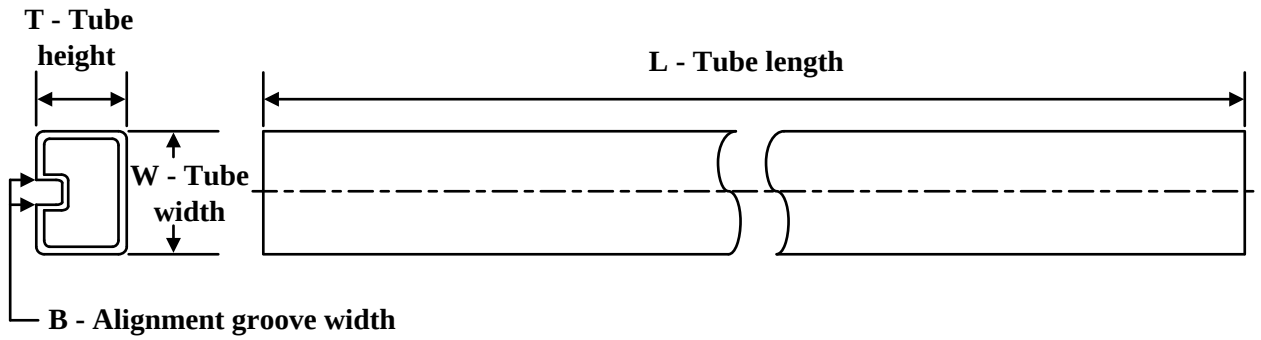
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

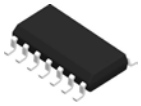
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3541IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV3541IDBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV3541IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV3541IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV3542IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV3542IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV3542IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV3542IDGKT	VSSOP	DGK	8	250	353.0	353.0	32.0
TLV3542IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TLV3542IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV3544IDR	SOIC	D	14	2500	353.0	353.0	32.0
TLV3544IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV3541IDR	D	SOIC	8	2500	507	7.85	3750	2.24
TLV3541IDR.A	D	SOIC	8	2500	507	7.85	3750	2.24
TLV3541IDR.B	D	SOIC	8	2500	507	7.85	3750	2.24
TLV3542IDR	D	SOIC	8	2500	507	7.85	3750	2.24
TLV3542IDR.A	D	SOIC	8	2500	507	7.85	3750	2.24
TLV3542IDR.B	D	SOIC	8	2500	507	7.85	3750	2.24

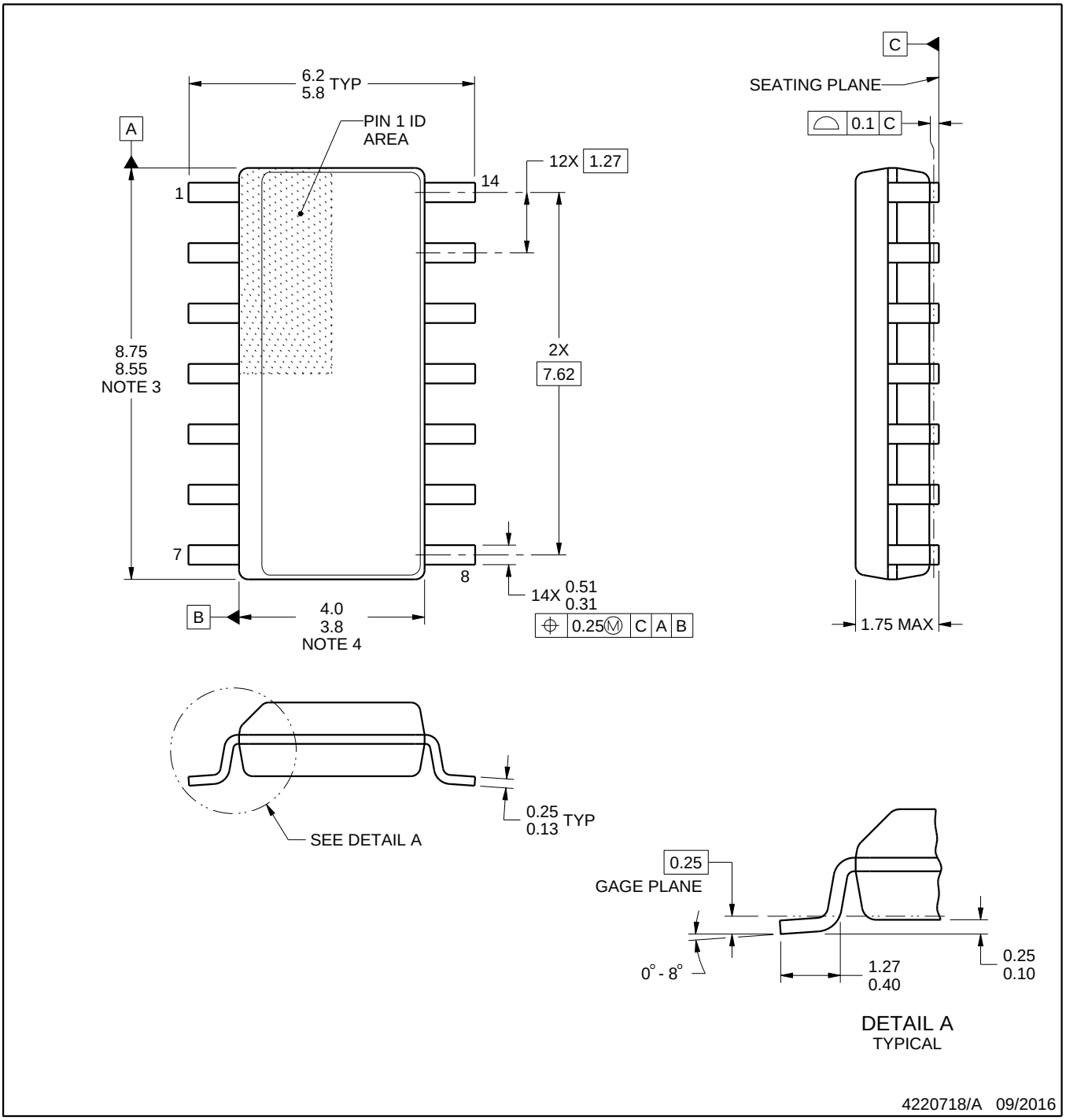


PACKAGE OUTLINE

D0014A

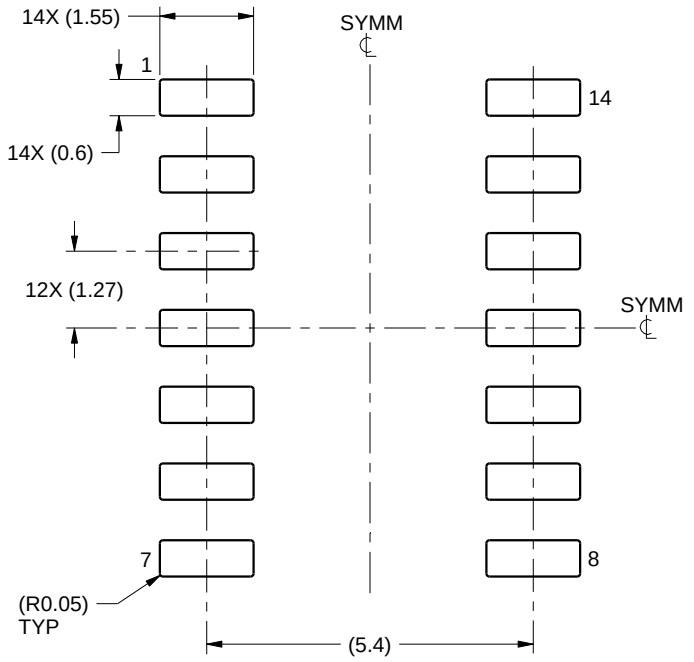
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

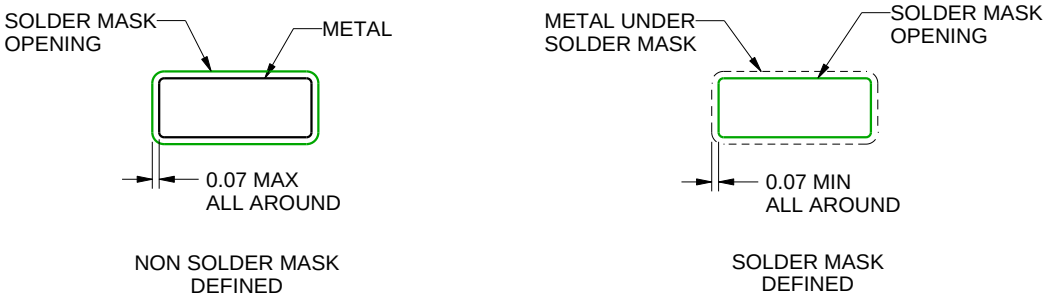


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

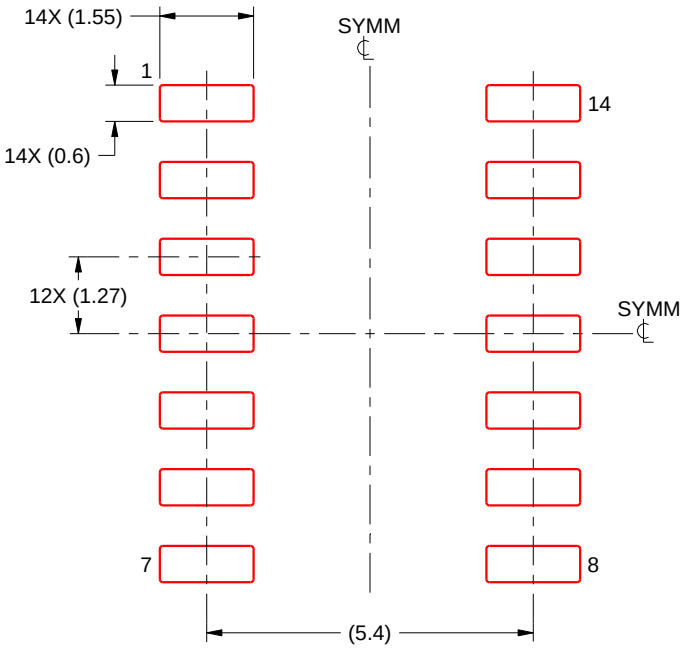
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

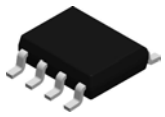


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

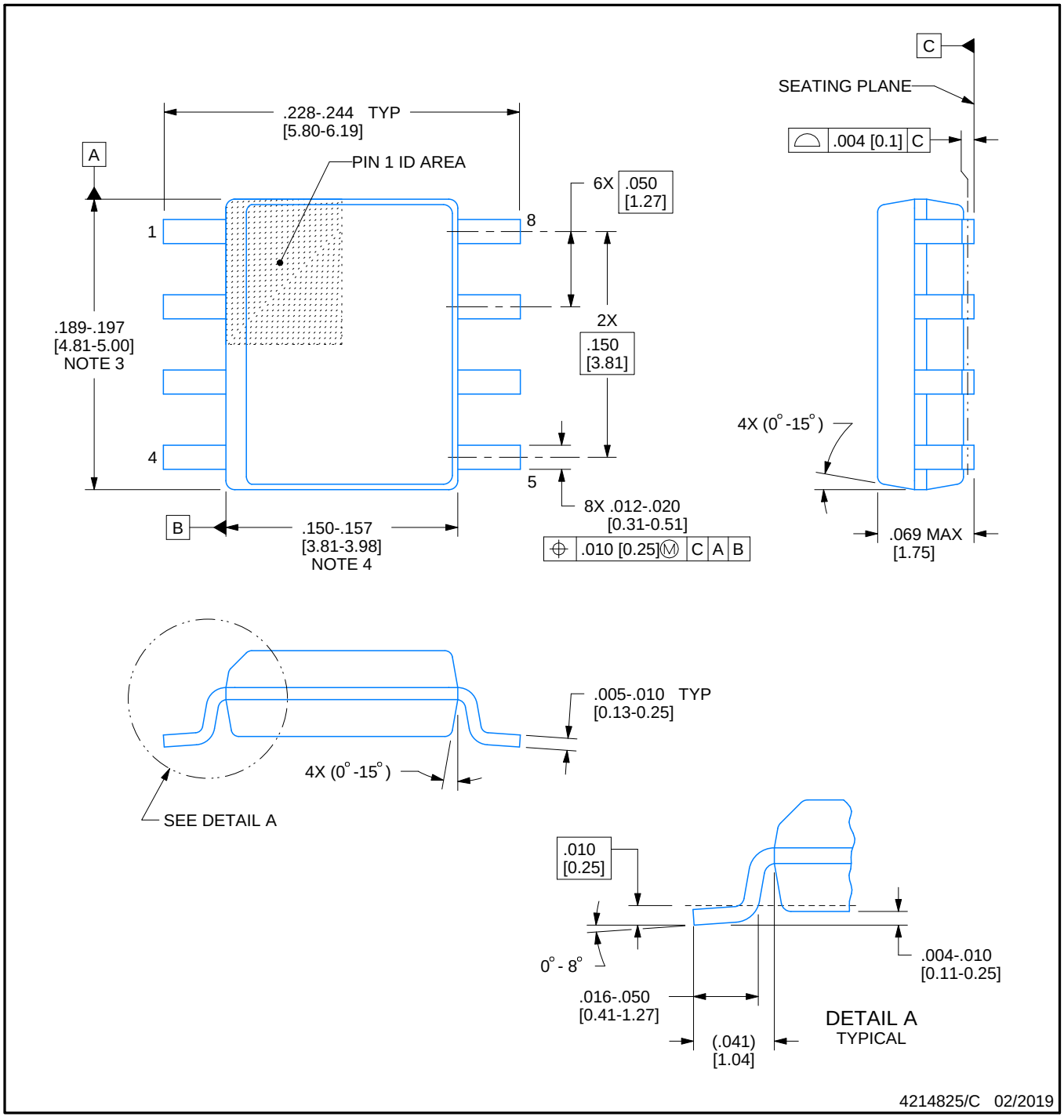


PACKAGE OUTLINE

D0008A

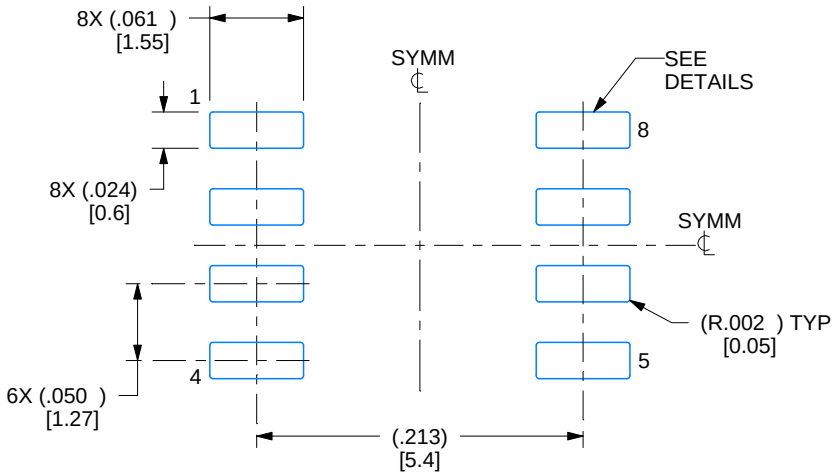
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

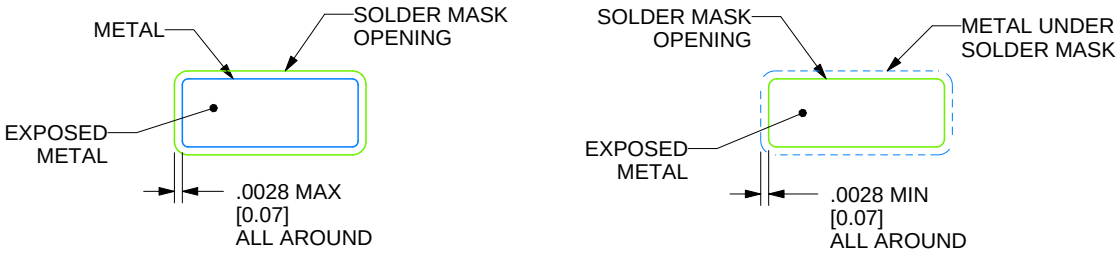


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

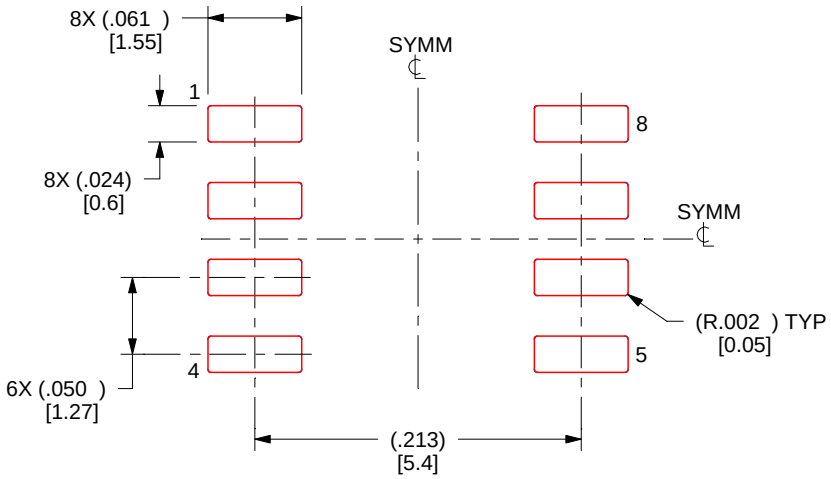
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

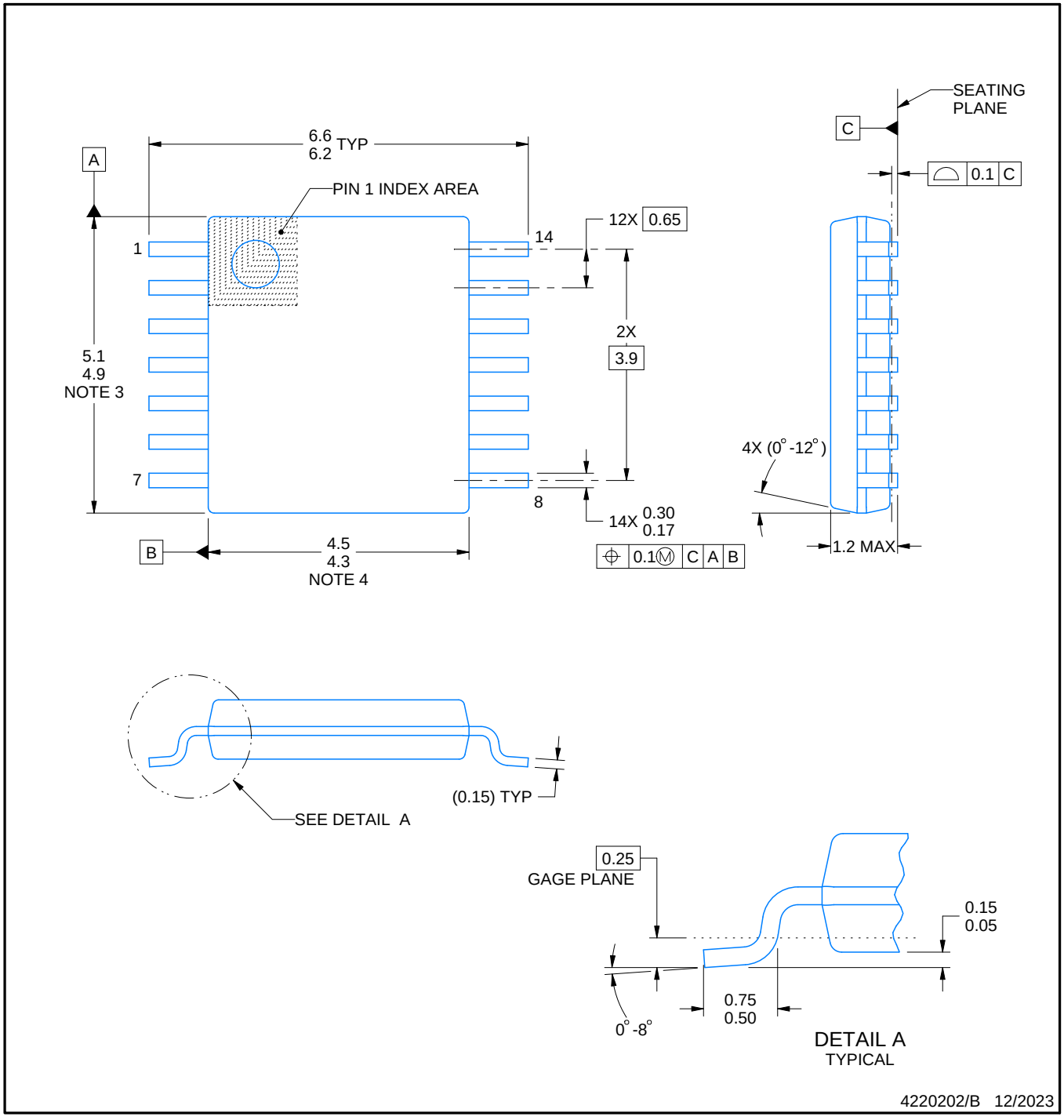
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

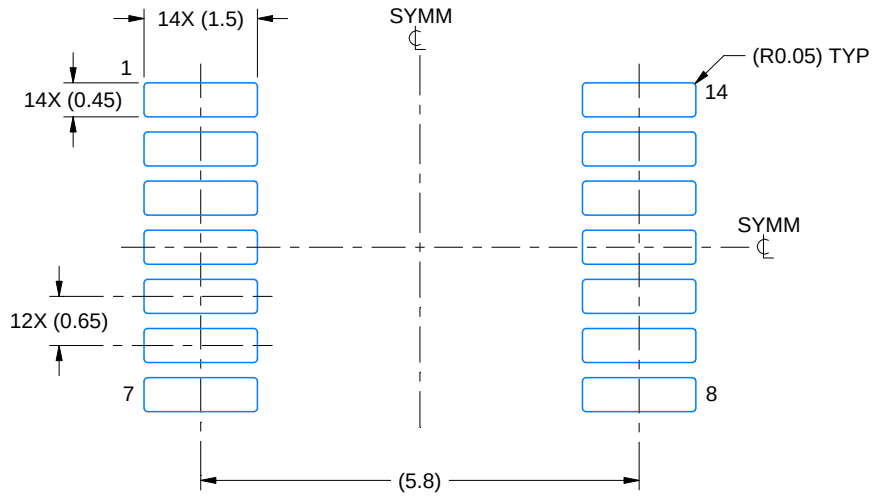
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

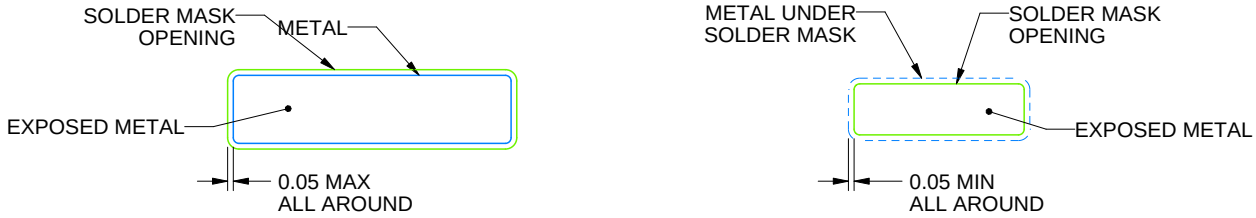


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

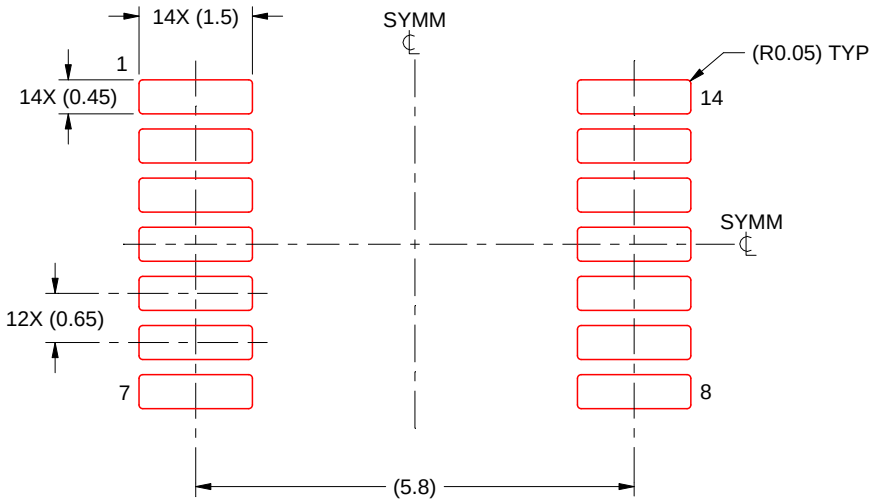


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

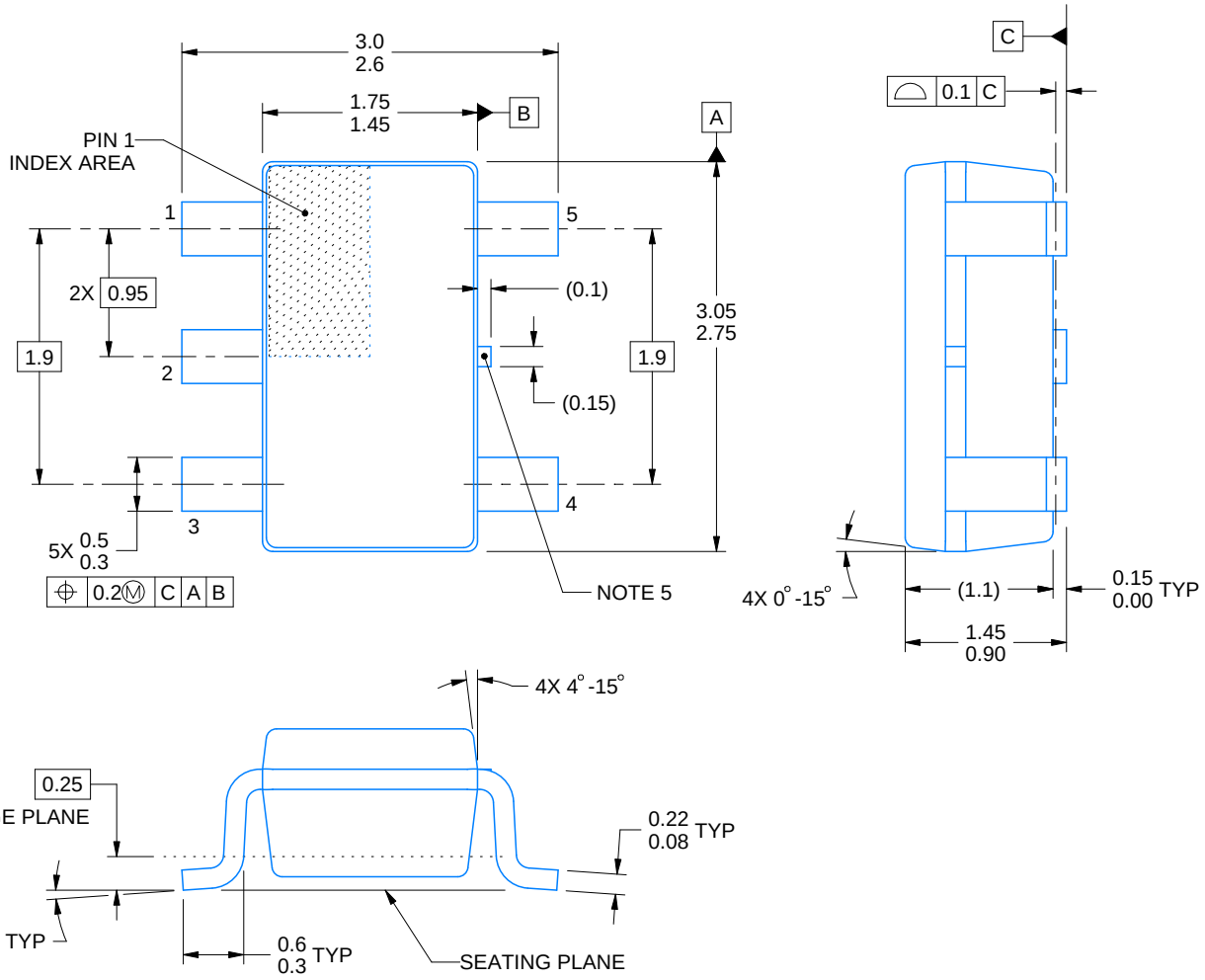
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

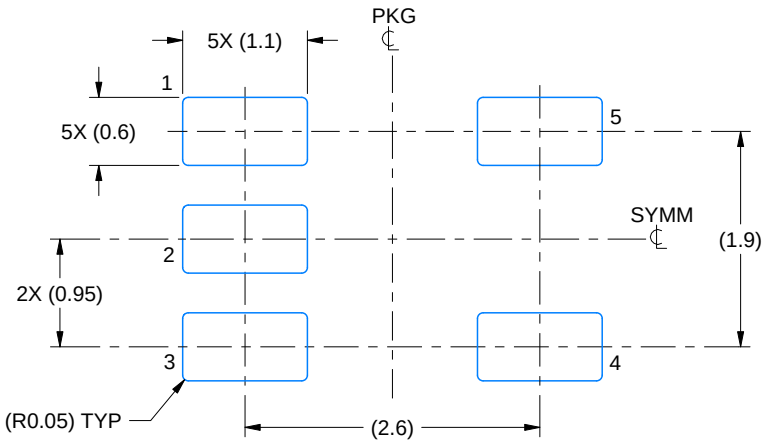
SMALL OUTLINE TRANSISTOR



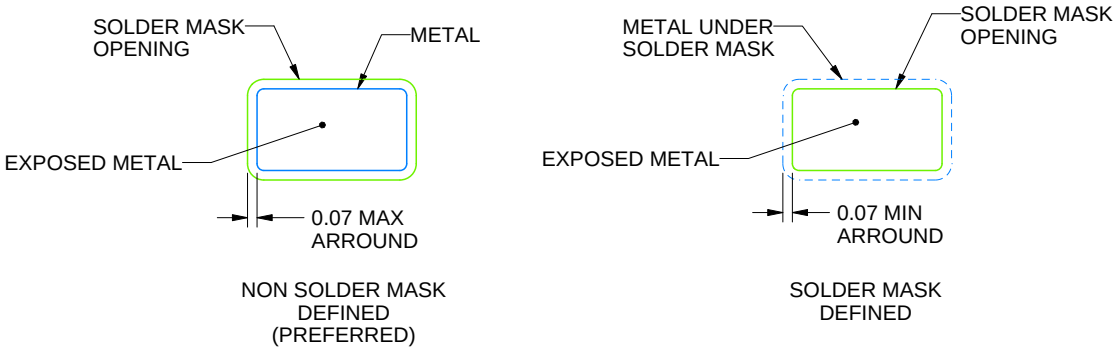
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

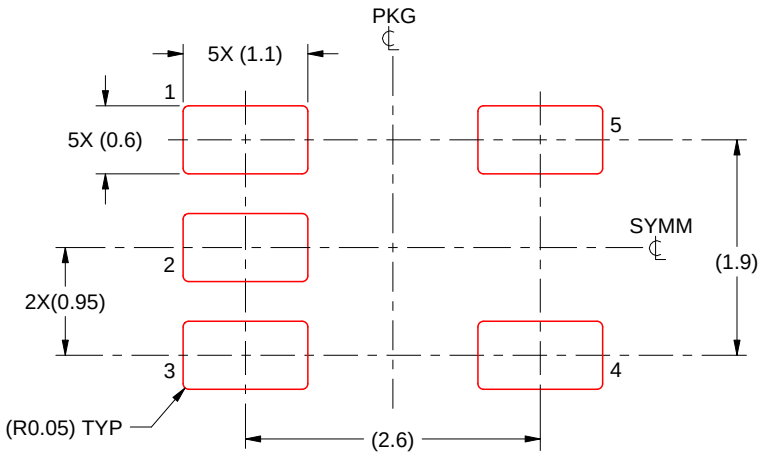


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

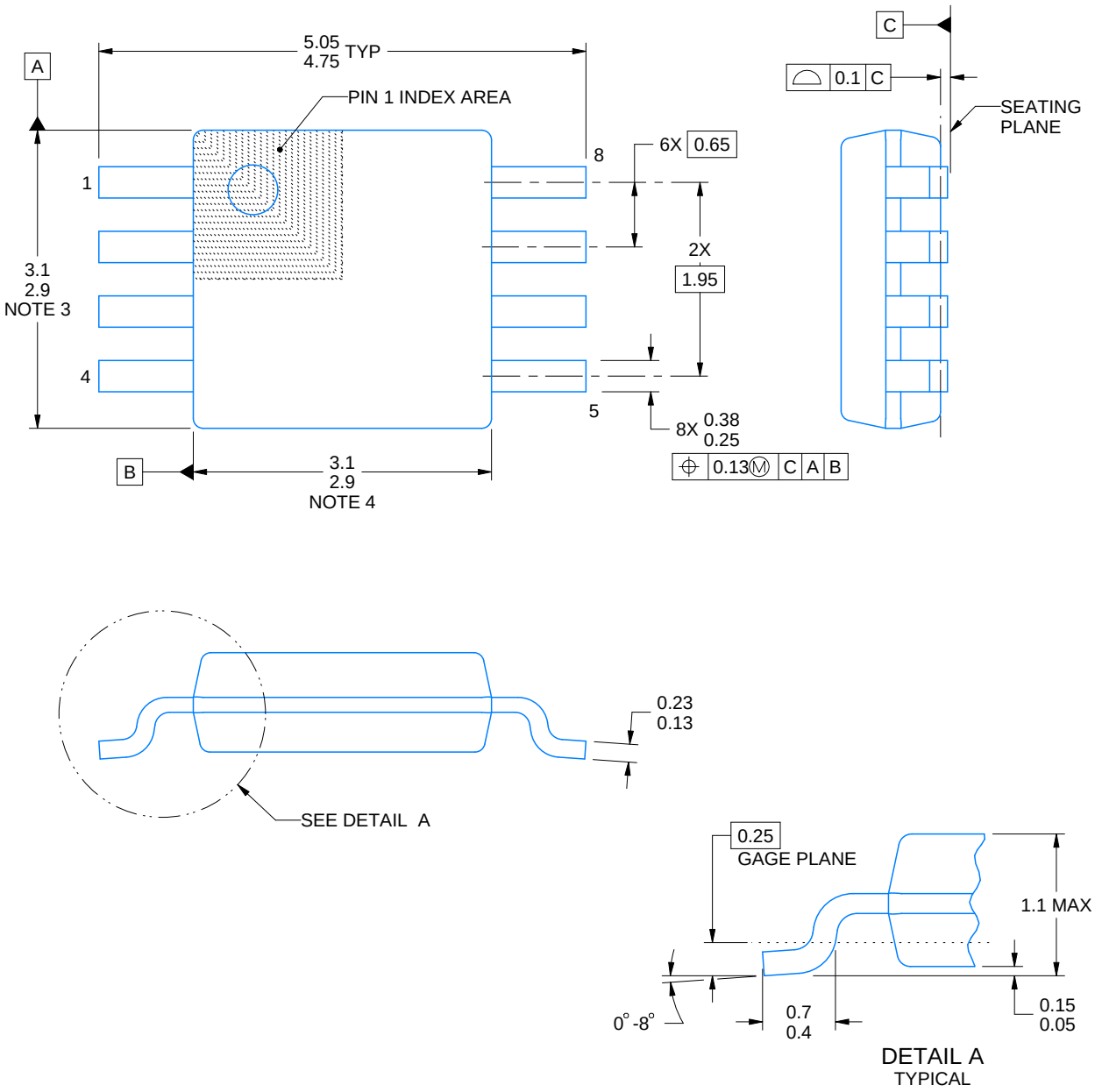
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

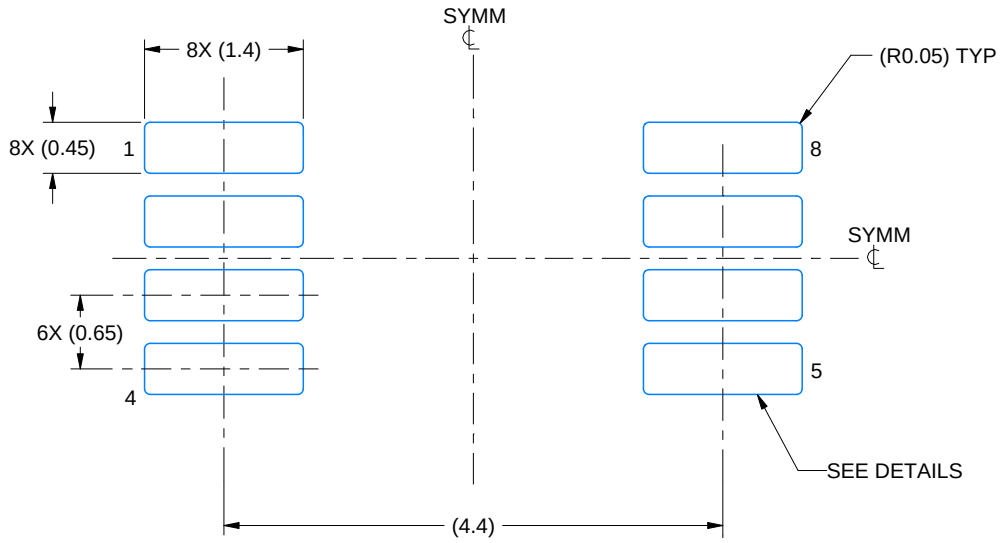
SMALL OUTLINE PACKAGE



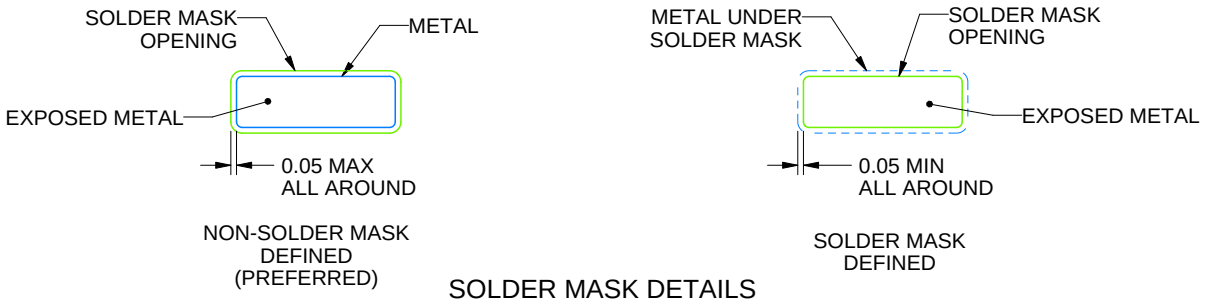
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

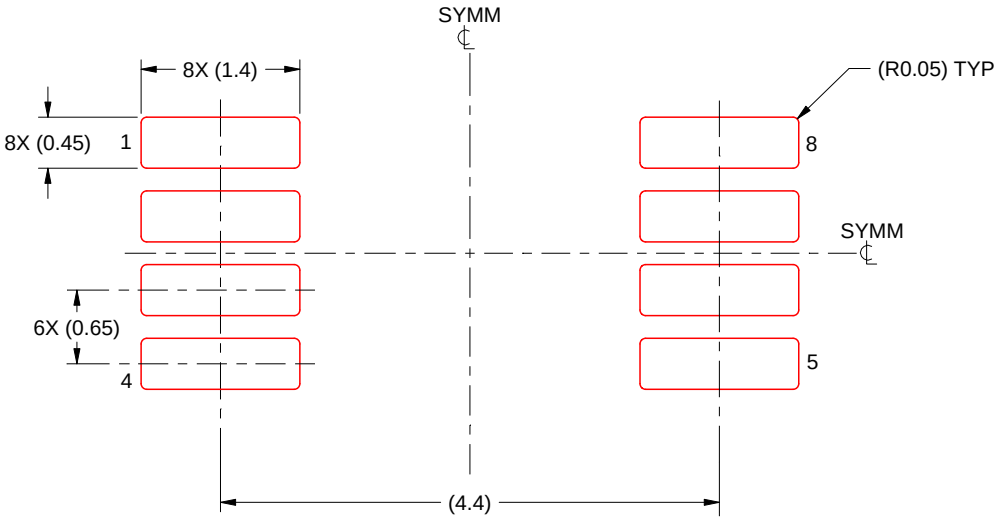


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025