

TLV370x-Q1 Family of 16V, Nanopower Comparators with Push-Pull Outputs

1 Features

- Qualified for Automotive Applications
- ESD Protection Exceeds 2000V Per MIL-STD-883, Method 3015; Exceeds 200V Using Machine Model (C = 200pF, R = 0)
- Low Supply Current . . . 560nA/Per Channel
- Input Common-Mode Range Exceeds the Rails . . . -0.1V to 16V
- Supply Voltage Range . . . 2.7V to 16V
- Reverse Battery Protection Up to 18V
- Push-Pull CMOS Output Stage
- Specified Temperature Range -40°C to 125°C – Automotive Grade
- Ultrasmall Packaging 5-Pin SOT-23 (TLV3701)
- Universal Op-Amp EVM (Reference SLOU060 for more information)

2 Applications

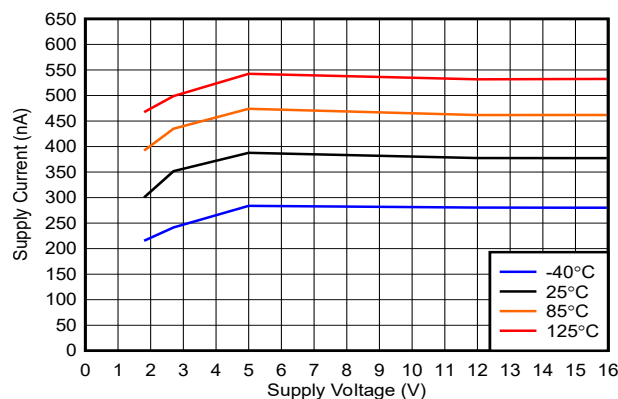
- Low Power Automotive Electronics
- Security Detection Systems

3 Description

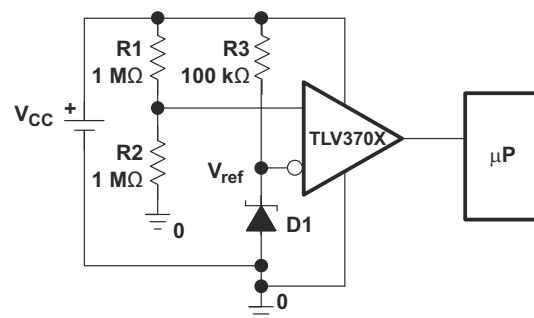
The TLV370x is Texas Instruments' first family of nanopower comparators with less than 560nA per channel supply current, which make this device well suited for low power applications.

The TLV370x has a minimum operating supply voltage of 2.7V over the extended automotive temperature range ($T_A = -40^{\circ}\text{C}$ to 125°C), while having an input common-mode range of -0.1 to 16V. The low supply current makes it well suited for low power applications where quiescent current is the primary concern. Reverse battery protection guards the amplifier from an over-current condition due to improper battery installation. For harsh environments, the inputs can be taken 5V above the positive supply rail without damage to the device.

Devices are available in SOIC with the singles in the small SOT-23 package. Other package options may be made available upon request.



Supply Current vs. Supply Voltage



High Side Voltage Sense Circuit



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4 Device Comparison Table

Table 4-1. A Selection Of Output Comparators

All specifications are typical values measured at 5V.

| DEVICE | V _{CC} (V) | V _{IO} (μ V) | I _{CC} /Ch (μ A) | I _{IB} (pA) | t _{PLH} (μ s) | t _{PHL} (μ s) | t _f (μ s) | t _r (μ s) | RAIL-TO RAIL | OUTPUT STAGE |
|------------|------------------------|-------------------------------|-----------------------------------|-------------------------|--------------------------------|--------------------------------|------------------------------|------------------------------|-----------------|-----------------|
| TLV370x | 2.5 – 16 | 250 | 0.56 | 80 | 56 | 83 | 22 | 8 | I | PP |
| TLV340x | 2.5 – 16 | 250 | 0.47 | 80 | 55 | 30 | 5 | – | I | OD |
| TLC3702/4 | 3 – 16 | 1200 | 9 | 5 | 1.1 | 0.65 | 0.5 | 0.125 | – | PP |
| TLC393/339 | 3 – 16 | 1400 | 11 | 5 | 1.1 | 0.55 | 0.22 | – | – | OD |
| TLC372/4 | 3 – 16 | 1000 | 75 | 5 | 0.65 | 0.65 | – | – | – | OD |

Table 4-2. TLV3701 Available Options

| T _A | V _{IO} max AT 25°C | PACKAGED DEVICES ^{(1) (2)} | | |
|----------------|--------------------------------|-------------------------------------|--------------------------------|--------|
| | | SMALL OUTLINE (D) | SOT-23 (DBV) ⁽³⁾ | SYMBOL |
| –40°C to 125°C | 5000 μ V | TLV3701QDRQ1 | TLV3701QDBVRQ1 | VBCQ |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

(2) Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

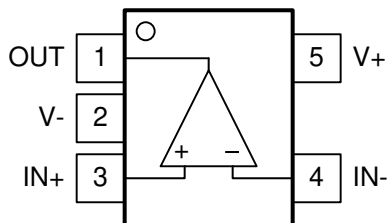
(3) This package is only available taped and reeled with standard quantities of 3000 pieces per reel.

Table 4-3. TLV3702 Available Options

| T _A | V _{IO} max AT 25°C | PACKAGED DEVICES | |
|----------------|--------------------------------|-------------------|--------|
| | | SMALL OUTLINE (D) | SYMBOL |
| –40°C to 125°C | 5000 μ V | TLV3702QDRQ1 | 3702Q1 |

5 Pin Configuration and Functions

Pin Configuration: TLV3701



**DBV, DCK Packages
SOT-23-5, SC-70-5
Top View
(Standard "North West" Pinout)**

Table 5-1. Pin Functions: TLV3701

| PIN | | I/O | DESCRIPTION |
|------|-----|-----|-------------------------|
| NAME | NO. | | |
| OUT | 1 | O | Output |
| V- | 2 | - | Negative supply voltage |
| IN+ | 3 | I | Non-inverting (+) input |
| IN- | 4 | I | Inverting (-) input |
| V+ | 5 | - | Positive supply voltage |

Pin Configurations: TLV3702

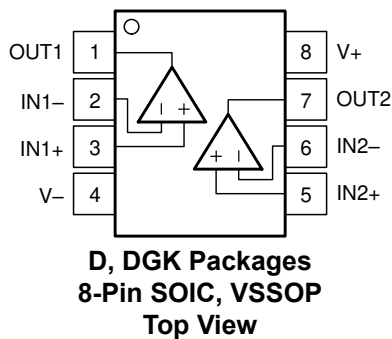


Table 5-2. Pin Functions: TLV3702

| PIN | | I/O | DESCRIPTION |
|------|-----|-----|--|
| NAME | NO. | | |
| OUT1 | 1 | O | Output pin of the comparator 1 |
| IN1– | 2 | I | Inverting input pin of comparator 1 |
| IN1+ | 3 | I | Noninverting input pin of comparator 1 |
| V– | 4 | — | Negative supply voltage |
| IN2+ | 5 | I | Noninverting input pin of comparator 2 |
| IN2– | 6 | I | Inverting input pin of comparator 2 |
| OUT2 | 7 | O | Output pin of the comparator 2 |
| V+ | 8 | — | Positive supply voltage |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | VALUE | UNIT |
|---|------------------------------|------|
| Supply voltage, (V+) ⁽²⁾ | 17 | V |
| Differential input voltage, V_{ID} | ±20 | V |
| Input voltage range, V_I ⁽²⁾ | –0.3 to 20 | V |
| Input current range, I_I | ±10 | mA |
| Output current range, I_O | ±10 | mA |
| Continuous total power dissipation | See Dissipation Rating Table | |
| Operating free-air temperature range, T_A : Q suffix | –40 to 125 | °C |
| Maximum junction temperature, T_J | 150 | °C |
| Storage temperature range, T_{stg} | –65 to 150 | °C |
| Lead temperature 1.6mm (1/16 inch) from case for 10 seconds | 260 | °C |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to GND.

6.2 Dissipation Rating Table

| PACKAGE | θ_{JC} (°C/W) | θ_{JA} (°C/W) |
|---------|-------------------------|-------------------------|
| D (8) | 64.6 | 121.6 |
| DBV (5) | 68.1 | 168.1 |

6.3 Recommended Operating Conditions

| | | MIN | MAX | UNIT |
|--|---------------|-------|-----|------|
| Supply voltage, (V+) | Single supply | 2.7 | 16 | V |
| | Split supply | ±1.35 | ±8 | |
| Common-mode input voltage range, V_{ICR} | | –0.1 | 16 | V |
| Operating free-air temperature, T_A | Q-suffix | –40 | 125 | °C |

6.4 Electrical Characteristics

at specified operating free-air temperature, $V_+ = 2.7V, 5V, 15V$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | T _A ⁽¹⁾ | MIN | TYP | MAX | UNIT |
|------------------------------|---|---|----------------------|-------------------------------|-----|-------------|------|-------|
| DC Performance | | | | | | | | |
| V _{IO} | Input offset voltage | V _{IC} = (V+)/2,R _S = 50Ω | | 25°C | | 250 | 5000 | μV |
| | | | | Full range | | | 7000 | |
| α _{VIO} | Offset voltage drift | V _{IC} = (V+)/2,R _S = 50Ω | | 25°C | | 3 | | μV/°C |
| V _{HYS} | Input hysteresis voltage | V _{IC} = (V+)/2,R _S = 50Ω | | 25°C | 1 | 2.8 | 5 | mV |
| CMRR | Common mode rejection ratio | V _{IC} = 0 to 2.7V | R _S = 50Ω | 25°C | | 72 | | dB |
| | | V _{IC} = 0 to 5V | R _S = 50Ω | 25°C | | 76 | | |
| | | V _{IC} = 0 to 15V | R _S = 50Ω | 25°C | | 88 | | |
| A _{VD} | Large-signal differential voltage amplification | | | 25°C | | 1000 | | V/mV |
| Input/Output Characteristics | | | | | | | | |
| I _{IO} | Input offset current | V _{IC} = (V+)/2, R _S = 50Ω | | 25°C | | 20 | 100 | pA |
| | | | | Full range | | | 1000 | |
| I _{IB} | Input bias current | | | 25°C | | 80 | 250 | pA |
| | | | | Full range | | | 2000 | |
| r _{i(d)} | Differential input resistance | | | 25°C | | 300 | | MΩ |
| V _{OH} | High-level output voltage | V _{IC} =(V+)/2, I _{OH} = 2μA, V _{ID} = 1V | | 25°C | | (V+) – 0.08 | | mV |
| | | V _{IC} = (V+)/2, I _{OH} = –50μA, V _{ID} = 1V | | 25°C | | (V+) – 320 | | |
| | | | | Full range | | (V+) – 450 | | |
| V _{OL} | Low-level output voltage | V _{IC} = (V+)/2, I _{OH} = 2μA, V _{ID} –1V | | 25°C | | 8 | | mV |
| | | V _{IC} = (V+)/2, I _{OH} = 50μA, V _{ID} –1V | | 25°C | | 80 | 200 | |
| | | | | Full range | | | 300 | |
| Power Supply | | | | | | | | |
| I ₊ | Supply current (per channel) | Output state high | | 25°C | | 560 | 800 | nA |
| | | | | Full range | | | 1200 | |
| PSRR | Power supply rejection ratio | V _{IC} = (V+)/2, No load | (V+) = 2.7V to 5V | 25°C | 75 | 100 | | dB |
| | | | | Full range | 70 | | | |
| | | | (V+) = 5V to 15V | 25°C | 85 | 105 | | |
| | | | | Full range | 80 | | | |

(1) Full range is $-40^\circ C$ to $125^\circ C$ for Q suffix.

6.5 Switching Characteristics

For $V_S = (V+) - (V-) = 12V$, $V_{CM} = V_S / 2$ at $T_A = 25^\circ C$ (Unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|---|---|-----|-----|-----|---------|
| OUTPUT | | | | | | |
| T_{PD-HL} | Propagation delay time, high-to-low | $V_{OD} = 10mV$, $C_L = 25pF$, $V_{STEP} = 100mV$ | | 45 | | μs |
| | | $V_{OD} = 50mV$, $C_L = 25pF$, $V_{STEP} = 100mV$ | | 16 | | μs |
| | | $V_{OD} = 100mV$, $C_L = 25pF$, $V_{STEP} = 200mV$ | | 13 | | μs |
| T_{PD-LH} | Propagation delay time, low-to-high (Push-Pull output) | $V_{OD} = 10mV$, $C_L = 10pF$, $V_{STEP} = 100mV$ | | 34 | | μs |
| T_{PD-LH} | Propagation delay time, low-to-high (Push-Pull output) | $V_{OD} = 50mV$, $C_L = 10pF$, $V_{STEP} = 100mV$ | | 16 | | μs |
| T_{PD-LH} | Propagation delay time, low-to-high (Push-Pull output) | $V_{OD} = 100mV$, $C_L = 10pF$, $V_{STEP} = 200mV$ | | 14 | | μs |
| T_{PD-LH} | Propagation delay time, low-to-high (Open-Drain output) | $V_{OD} = 10mV$, $C_L = 25pF$, $R_P = 1M\Omega$, $V_{STEP} = 100mV$ | | 57 | | μs |
| | | $V_{OD} = 50mV$, $C_L = 25pF$, $R_P = 1M\Omega$, $V_{STEP} = 100mV$ | | 36 | | μs |
| | | $V_{OD} = 100mV$, $C_L = 25pF$, $R_P = 1M\Omega$, $V_{STEP} = 200mV$ | | 35 | | μs |
| T_{RISE} | Output Rise Time, 20% to 80%, push-pull output | $C_L = 25pF$ | | 0.2 | | μs |
| T_{FALL} | Output Fall Time, 80% to 20% | $C_L = 25pF$ | | 0.2 | | μs |
| POWER ON TIME | | | | | | |
| T_{ON} | Power on-time | | | 3 | | ms |

6.6 Typical Characteristics

At $T_A = 25^\circ\text{C}$, $V_S = 12\text{V}$, $V_{CM} = V_S/2\text{ V}$, $R_P = 1\text{M}\Omega$ (Open Drain only), $C_L = 25\text{pF}$, $V_{\text{OVERDRIVE}} = 100\text{mV}$ unless otherwise noted.

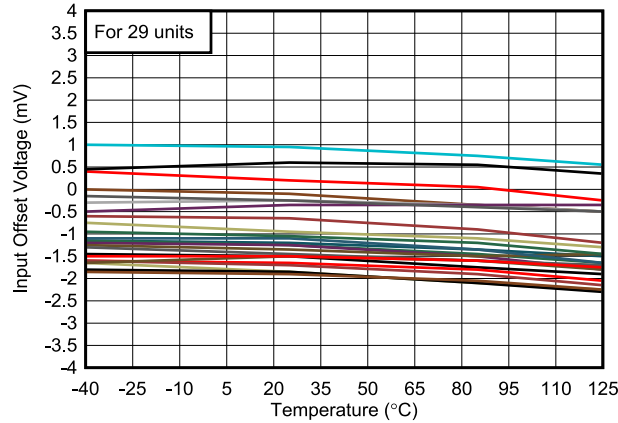


Figure 6-1. Offset vs. Temperature

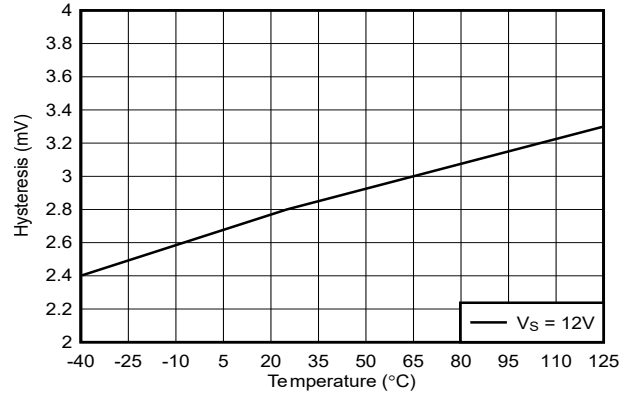


Figure 6-2. Hysteresis vs. Temperature

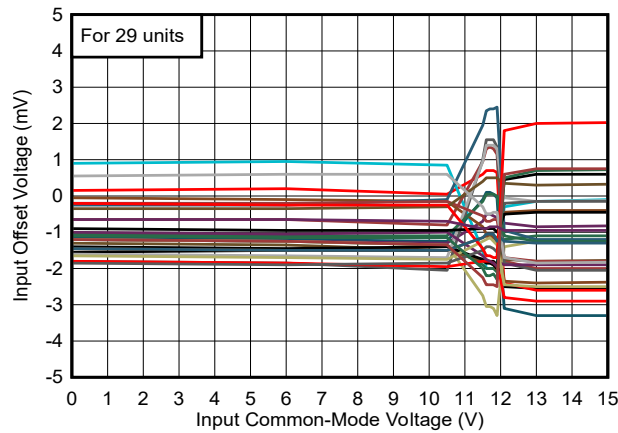


Figure 6-3. Offset vs. Common-Mode, 12V

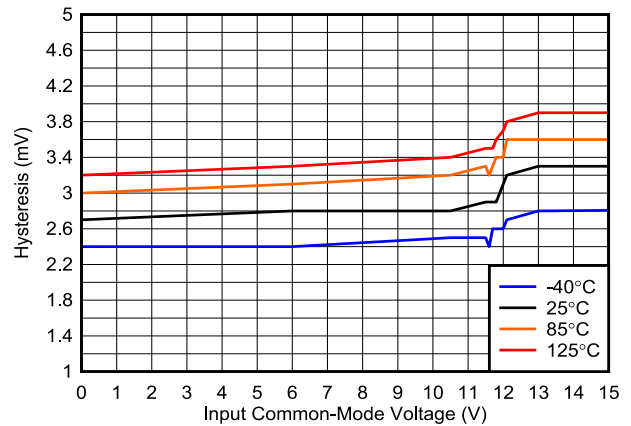


Figure 6-4. Hysteresis vs. Common-Mode, 12V

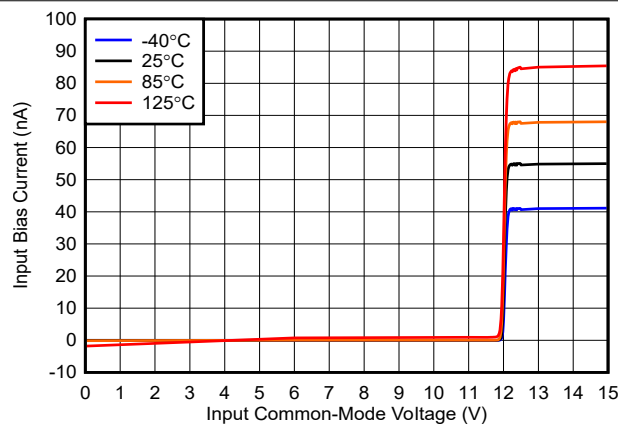


Figure 6-5. Bias Current vs. Common-Mode, 12V

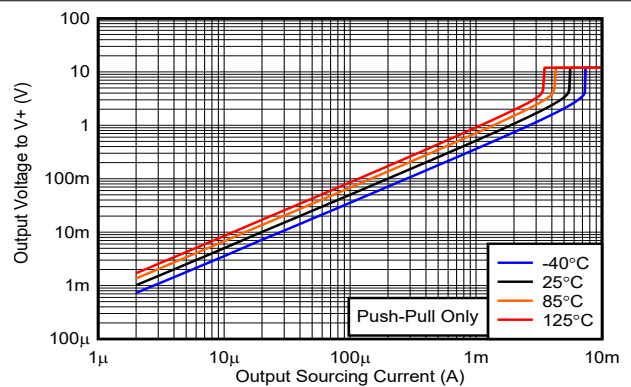


Figure 6-6. Output Voltage vs. Output Sourcing Current, 12V

6.6 Typical Characteristics (continued)

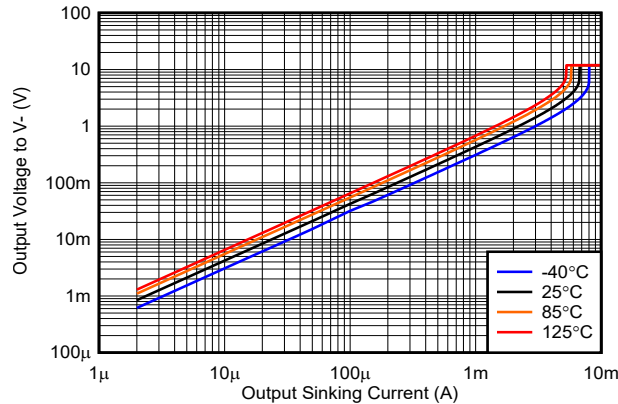


Figure 6-7. Output Voltage vs. Output Sinking Current, 12V

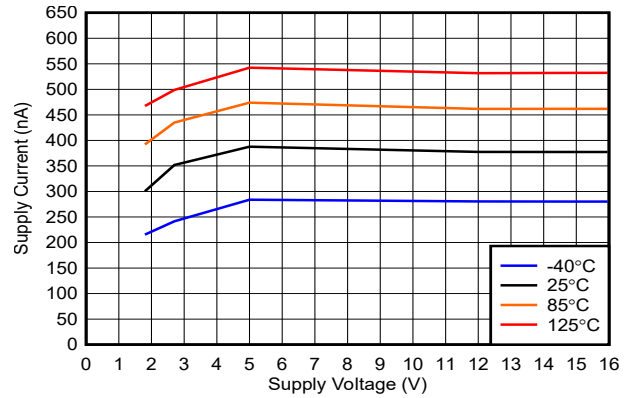


Figure 6-8. Supply Current vs. Supply Voltage (Output Low), Push-Pull

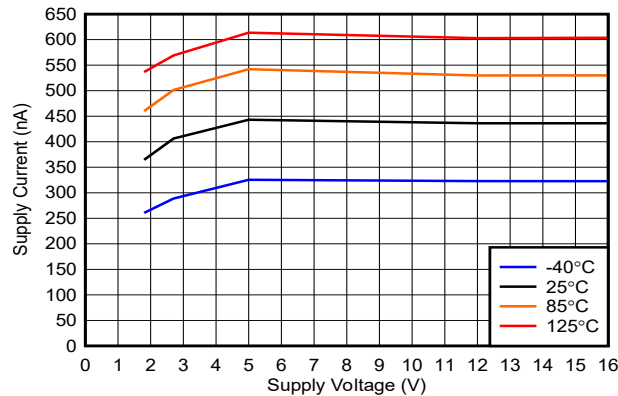


Figure 6-9. Supply Current vs. Supply Voltage (Output High), Push-Pull

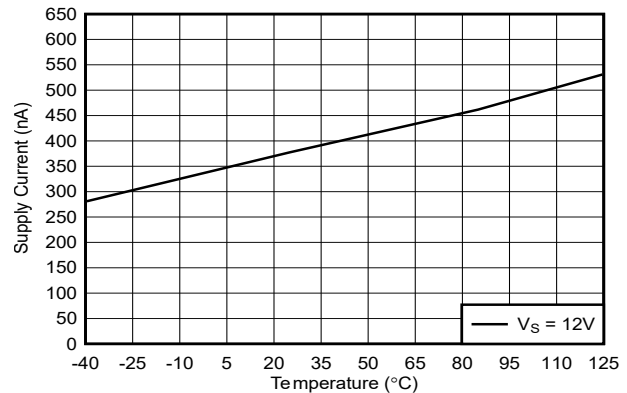


Figure 6-10. Supply Current vs. Temperature (Output Low), Push-Pull

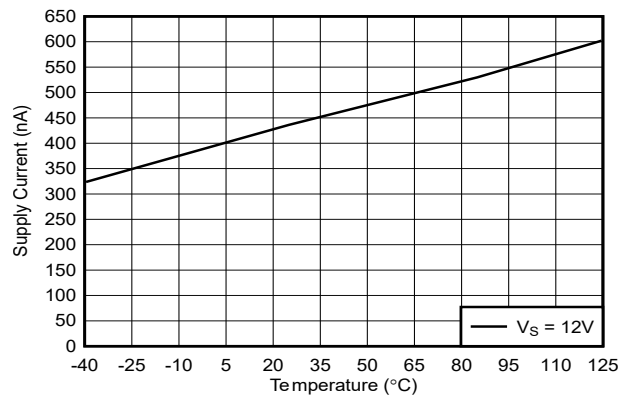


Figure 6-11. Supply Current vs. Temperature (Output High), Push-Pull

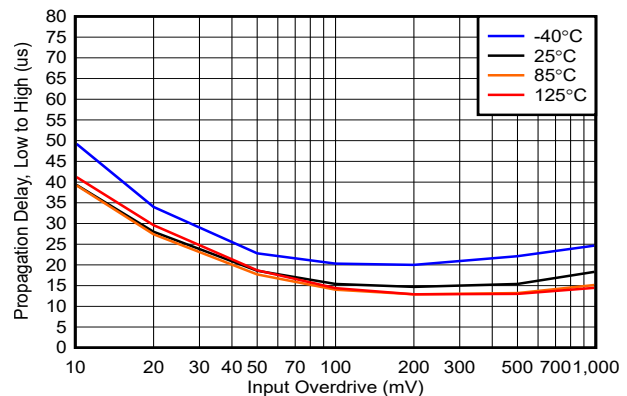


Figure 6-12. Propagation Delay, Low to High, 12V, Push-Pull

6.6 Typical Characteristics (continued)

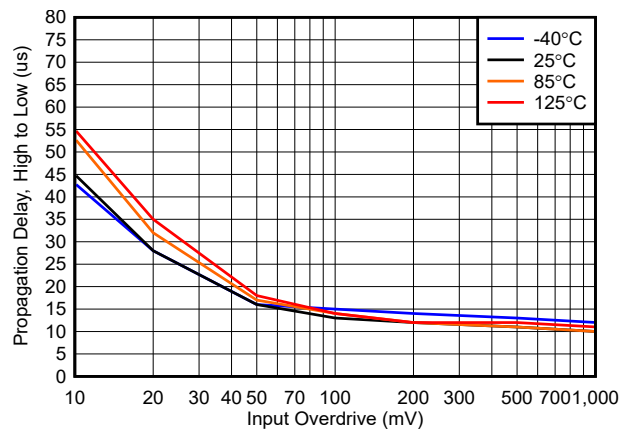


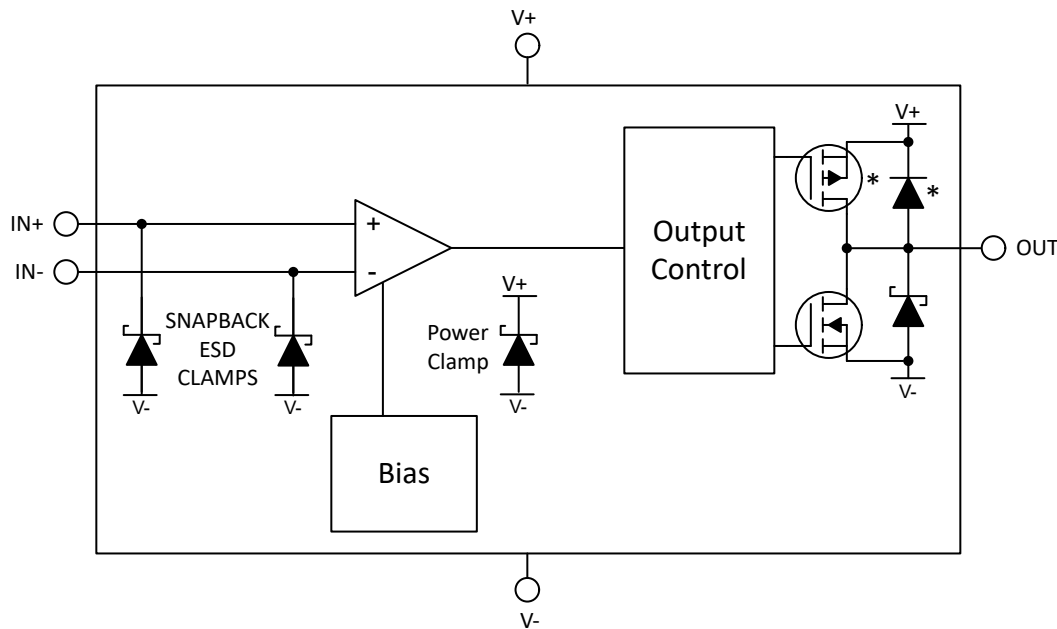
Figure 6-13. Propagation Delay, High to Low, 12V

7 Detailed Description

7.1 Overview

The TLV370x devices are nanopower comparators with push-pull output options. Operating down to 2.7V while only consuming only 560nA per channel, the TLV370x devices are well suited for voltage, current, and temperature sensing in low and high voltage low-power, always-on systems. An internal power-on reset circuit makes sure that the output remains in a known state during power-up and power-down. Inputs have fail-safe inputs that can tolerate input transients without damage or false outputs.

7.2 Functional Block Diagrams



Block Diagram

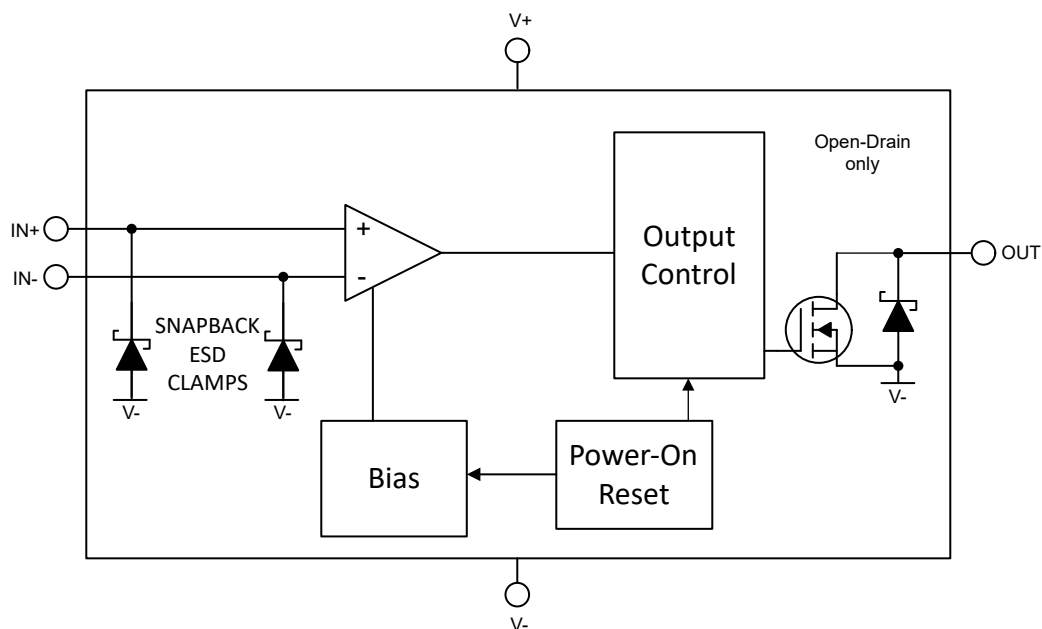


Figure 7-1. Block Diagram

7.3 Feature Description

The TLV370x devices are nano-power comparators that are capable of operating at high voltages. This family of comparators feature a fail safe input stage and over the rail operating condition mode capable of operating up to 16V, independent of V_+ . The comparators also have an internal reverse battery protection feature and Power-On-Reset for known start-up conditions.

7.4 Device Functional Modes

7.4.1 Inputs

7.4.1.1 Operating Common-Mode Ranges

The TLV370x devices have two operating common-mode ranges: within-the-rail and over-the-rail.

Within-the-Rail Operation: IN_+ and IN_- are less than (V_+)

When an input pin is operating less than (V_+) , there are two operating regions defined where input voltages can be compared: low common-mode and high-common mode. In low-common mode which extends typically from 0V to $(V_+) - 1V$, the typical input bias current is less than 1pA. In high common-mode which extends typically from $(V_+) - 1V$ to (V_+) , the typical input bias current is less than 14nA.

Over-the-Rail Operation: IN_+ and/or IN_- are greater than (V_+)

The TLV370x devices have a distinctive input stage that allows the input common mode range to extend from 0V to 16V independent of the supply voltage. This feature means that operation at low supply voltages does not limit the range of input voltages that can be compared. When an input pin is operating over-the-rail (above (V_+)), the bias current increases to a typical value of 55nA.

7.4.1.2 Fail-Safe Inputs

A feature of the TLV370x family is that the inputs are fail safe up to 16V, independent of (V_+) . The inputs are maintained as high input impedance and can be of any value between -0.1V and 16V, even while (V_+) is unpowered or below the minimum supply voltage. This feature avoids power sequencing or transient issues since the inputs are not diode clamped to (V_+) .

7.4.1.3 Unused Inputs

If a channel is not to be used, DO NOT tie the inputs together. Due to the high equivalent bandwidth and low offset voltage, tying the inputs directly together can cause high frequency oscillations as the device triggers on it's own internal wideband noise. Instead, the inputs should be tied to any available voltage that resides within the specified input voltage range and provides a minimum of 50mV differential voltage. For example, one input can be grounded and the other input connected to a reference voltage, or even (V_+) .

7.4.2 Internal Hysteresis

The device hysteresis transfer curve is shown in [Figure 7-2](#). This curve is a function of three components: V_{TH} , V_{OS} , and V_{HYST} :

- V_{TH} is the actual set voltage or threshold trip voltage.
- V_{OS} is the internal offset voltage between V_{IN+} and V_{IN-} . This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST} is the internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

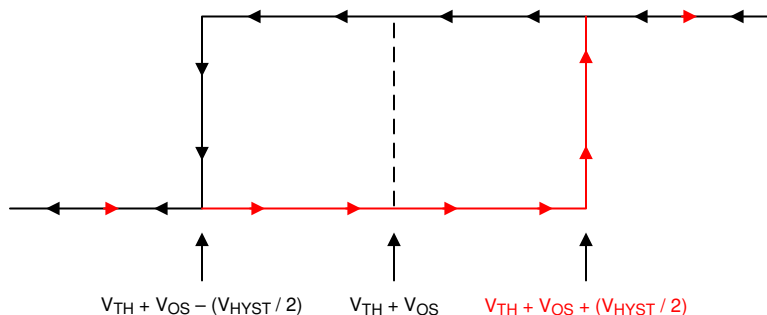


Figure 7-2. Hysteresis Transfer Curve

7.4.3 Outputs

7.4.3.1 Push-Pull Output

The TLV370x devices feature a push-pull output stage capable of both sinking and sourcing current. This allows driving loads such as LED's and MOSFET gates, as well as eliminating the need for a power-wasting external pull-up resistor. The push-pull output must never be connected to another output.

Directly shorting the output to the supply rails ((V+) when output "low" or (V-) when output "High") can result in thermal runaway and eventual device destruction at high (>12V) supply voltages. If output shorts are possible, a series current limiting resistor is recommended to limit the power dissipation.

Unused push-pull outputs must be left floating, and never tied to a supply, ground, or another output.

7.4.4 ESD Protection

7.4.4.1 Inputs

The fail-safe inputs incorporates internal ESD protection circuits on all pins. The fail-safe inputs have ESD protection from each pin to (V-) which allows these pins to exceed the supply voltage (V+) up to 16V. If input voltages are to exceed 16V, an external clamp is required. Likewise, negative voltages on the inputs are ESD clamped to (V-) and must be limited to less than -0.1V.

If the inputs are to be connected to a low impedance source such as a power supply or buffered reference line, add a current-limiting resistor in series with the input to limit any transient currents if the clamps conduct. The current is be limited to 10mA or less. This series resistance can be part of any resistive input dividers or networks.

7.4.4.2 Outputs

The TLV370x push-pull output protection also contains a conventional diode-type ESD clamps between the output and (V-), as the output should not exceed the supply rails.

7.4.5 Power-On Reset (POR)

The TLV370x devices have an internal Power-on-Reset (POR) circuit for known start-up or power-down conditions. While the power supply (V+) is ramping up or ramping down, the POR circuitry is activated for up to 2ms after the V_{POR} of 1.5V is crossed. When the supply voltage is equal to or greater than the minimum supply voltage, and after the delay period, the comparator output reflects the state of the differential input (V_{ID}).

For the TLV370x push-pull output devices, the output is held low during the POR period (t_{on}).

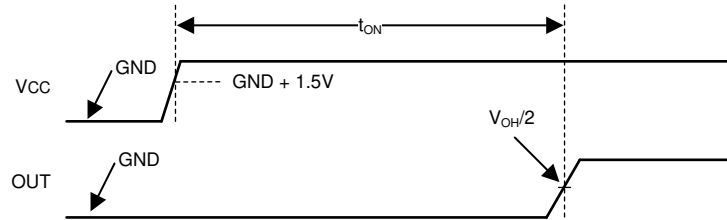


Figure 7-3. Power-On Reset Timing Diagram

7.4.6 Reverse Battery Protection

The TLV370x devices have an internal reverse battery protection feature that prevents damage to the comparator in the event of improper battery installation to the supply pins. This protection feature works up to 18V.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.4 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (October 2000) to Revision F (September 2025) | Page |
|---|--------------------|
| • Updated the numbering format for tables, figures, and cross-references throughout the document..... | 1 |
| • Added hysteresis specification to EC table..... | 7 |
| • Removed min requirements for CMRR in EC table..... | 7 |
| • Updated propagation delay specs in EC table..... | 7 |
| • Updated Typical Performance Curves..... | 9 |
| • Added Detailed Description information..... | 12 |

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|----------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TLV3701QDBVRG4Q1 | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBCQ |
| TLV3701QDBVRG4Q1.A | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | VBCQ |
| TLV3701QDBVRQ1 | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | Call TI Nipdau | Level-1-260C-UNLIM | -40 to 125 | VBCQ |
| TLV3701QDBVRQ1.A | Active | Production | SOT-23 (DBV) 5 | 3000 LARGE T&R | Yes | Call TI | Level-1-260C-UNLIM | -40 to 125 | VBCQ |
| TLV3702QDRG4Q1 | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3702Q1 |
| TLV3702QDRG4Q1.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3702Q1 |
| TLV3702QDRQ1 | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3702Q1 |
| TLV3702QDRQ1.A | Active | Production | SOIC (D) 8 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3702Q1 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV3701-Q1, TLV3702-Q1 :

- Catalog : [TLV3701](#), [TLV3702](#)
- Enhanced Product : [TLV3701-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV3701QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV3701QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV3702QDRG4Q1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV3702QDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV3701QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV3701QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV3702QDRG4Q1 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |
| TLV3702QDRQ1 | SOIC | D | 8 | 2500 | 353.0 | 353.0 | 32.0 |

DBV0005A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

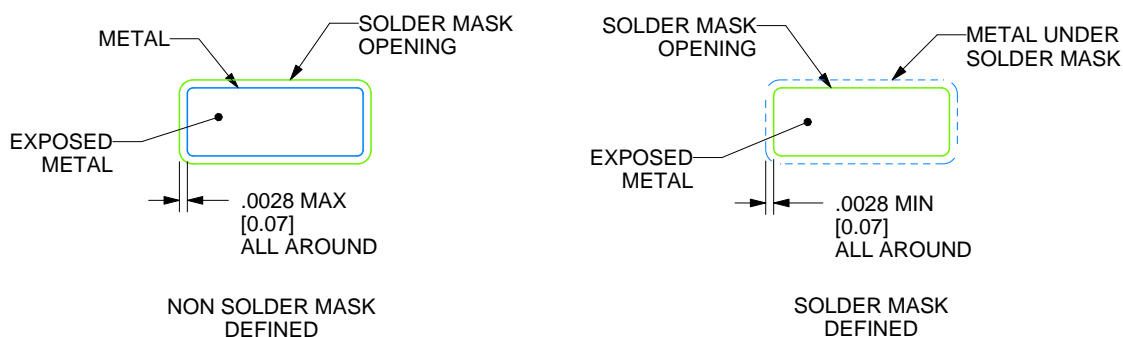
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025