TLVx825 3.5MHz, 1.8V to 5.5V, High Precision, Zero-Drift Operational Amplifiers

1 Features

- Ultra-low offset drift: ±0.02μV/°C
- Flat low frequency noise: 0.3μV_{PP} (0.1 to 10Hz)
- Ultra-low offset: ±4μV
- Rail-to-rail input and output
- Very high A_{OL}, CMRR, PSRR: > 120dB
- Wide input common-mode: 100mV beyond rails
- Low input bias current: ±100pA
- Low thermal noise floor: 15nV/√Hz
- Wide gain bandwidth: 3.5MHz
- High C_L drive: 1nF (no sustained oscillations)
- Low quiescent current: 500μA/channel
- Wide supply range: 1.8V to 5.5V
- Wide temperature range: –40°C to +125°C

2 Applications

- Sensor signal conditioning
  - Weigh scales
  - Pressure transmitters
  - Temperature transmitters
  - Flow transmitters
  - Merchant DC/DC
  - Electricity meters
  - Micro and solar inverters

3 Description

The TLVx825 family of single, dual, and quad channel operational amplifiers enable precision performance such as lower offset, lower offset drift over temperature, greater offset stability over time and a flat noise floor. This level of performance is crucial to a variety of systems focusing on precision voltage sensing from sensors and precision current sensing using smaller shunt resistors.

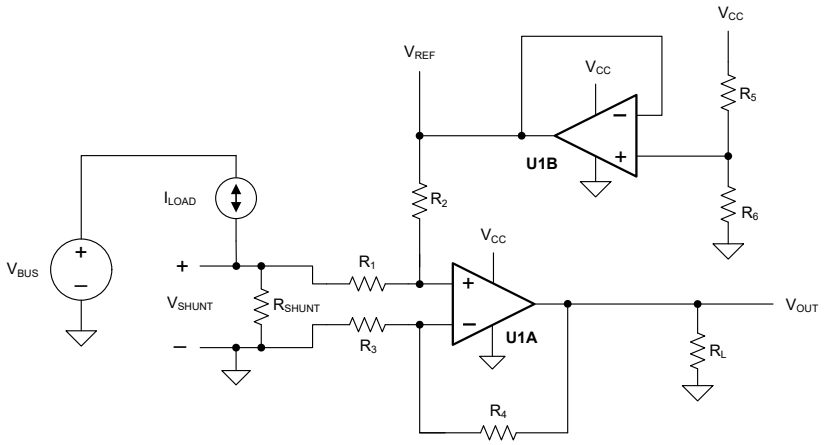
TLVx825 uses zero-drift architecture to achieve an input referred offset voltage of 4μV, an offset drift of 0.02μV/°C and a low frequency noise of 320nV_{PP} in the standard 0.1 – 10Hz range. This combination of specs provides excellent accuracy in high gain applications, thereby greatly reducing the need for system level calibration.

Additionally, with a quiescent current of 500μA, the TLVx825 is able to achieve a bandwidth of 3.5MHz and a broadband noise of 15nV/√Hz. This ability is crucial to achieve higher linearity, and signal-to-noise ratio in applications involving higher resolution, mid-speed analog to digital converters (ADCs) while minimizing system power.

Package Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)	PACKAGE SIZE(2)
TLV825	Single	DBV (SOT-23, 5)(3)	2.9mm × 2.8mm
		DCK (SOT-SC70, 5)(3)	2mm × 2.1mm
		DRL (SOT-5X3, 5)(3)	1.6mm × 1.6mm
TLV2825	Dual	D (SOIC, 8)	4.9mm × 6mm
		DGK (VSSOP, 8)	3mm × 4.9mm
		DDF (SOT-23-THN, 8)(3)	2.9mm × 2.8mm
		DSG (WSON, 8)(3)	2mm × 2mm
TLV4825	Quad	PW (TSSOP, 14)	5mm × 6.4mm
		D (SOIC, 14)	8.65mm × 6mm
		DYY (SOT-23-THN, 14)(3)	3mm × 3mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Preview information (not Advance Information).



Bidirectional Current-Sensing Application

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4 Pin Configuration and Functions

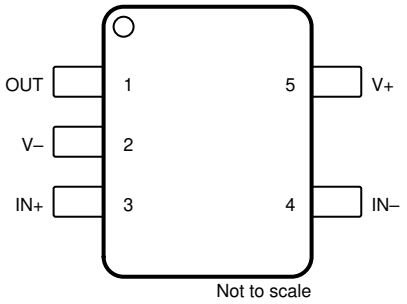

Figure 4-1. TLV825 DBV Package, 5-Pin SOT-23 (Top View)

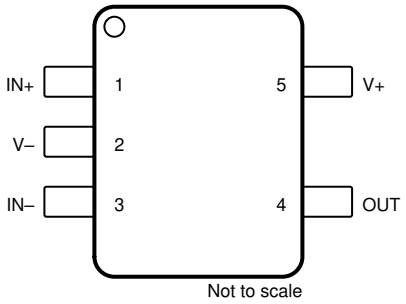

Figure 4-2. TLV825 DCK and DRL Package, 5-Pin SOT-SC70 and SOT-5X3 (Top View)

Table 4-1. Pin Functions: TLV825

PIN			TYPE(1)	DESCRIPTION
NAME	SOT-23	SOT-SC70, SOT-5X3		
IN–	4	3	I	Inverting input
IN+	3	1	I	Noninverting input
OUT	1	4	O	Output
V–	2	2	I	Negative (low) supply or ground (for single-supply operation)
V+	5	5	I	Positive (high) supply

(1) I = input, O = output

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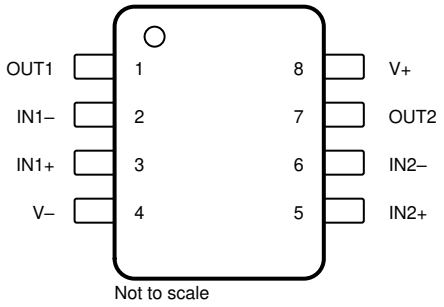
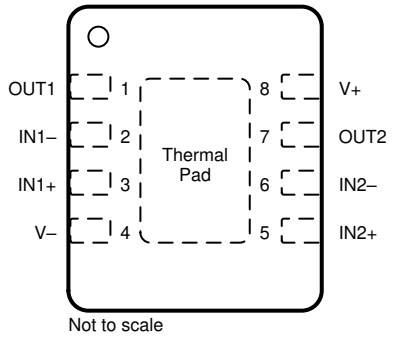


Figure 4-3. TLV2825 D, DGK, and DDF Package, 8-Pin SOIC, VSSOP, and SOT-23-THIN (Top View)



Connect exposed thermal pad to V–.

Figure 4-4. TLV2825 DSG Package, 8-Pin WSON with Exposed Thermal Pad (Top View)

Table 4-2. Pin Functions: TLV2825

PIN		TYPE[(1)]	DESCRIPTION
NAME	SOIC, VSSOP, SOT-23-THIN, WSON		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	I	Negative (low) supply or ground (for single-supply operation)
V+	8	I	Positive (high) supply

(1) I = input, O = output

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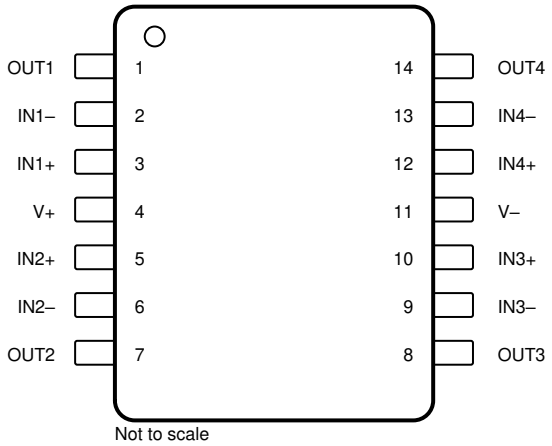

Figure 4-5. TLV4825 D, PW and DYY Package, 14-Pin SOIC, TSSOP, and SOT-23-THIN (Top View)

Table 4-3. Pin Functions: TLV4825

PIN		TYPE[(1)]	DESCRIPTION
NAME	SOIC, TSSOP, SOT-23-THIN		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
IN3–	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4–	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V–	11	I	Negative (low) supply or ground (for single-supply operation)
V+	4	I	Positive (high) supply

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	Single-supply	0	6	V
	Dual-supply	±0	±3	
Signal input pins	Common-mode[3]	(V–) – 0.5	(V+) + 0.5	V
	Differential[3]		(V+) – (V–) + 0.2	
	Current[3]		±10	mA
Output short circuit[2]		Continuous		
Operating temperature, T_A		–55	150	°C
Junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single-supply	1.8		5.5	V
		Dual-supply	±0.9		±2.75	
T_A	Specified temperature		–40		125	°C

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5.4 Thermal Information for Single Channel

THERMAL METRIC[1]		TLV825		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBD	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	TBD	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	TBD	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	TBD	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Thermal Information for Dual Channel

THERMAL METRIC[1]		TLV2825		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	146.6	167.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	85.0	75.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	90.7	98.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	33.7	14.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	90.1	97.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.6 Thermal Information for Quad Channel

THERMAL METRIC[1]		TLV4285		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.0	120.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.6	55.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.2	75.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	20.6	13.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	51.9	74.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

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5.7 Electrical Characteristics

at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_S = 1.8V to 5.5V, V_{CM} = V_S / 2, V_{OUT} = V_S / 2, and min and max specification established from manufacturing final test (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	T_A = 25°C(1)			±4	±15	µV
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C(1)			±0.02		µV/°C
PSRR	Power supply rejection ratio			110	130		dB
		T_A = –40°C to +125°C(1)		105			dB
	Channel separation	f = 0Hz			5		µV/V
					106		dB
INPUT BIAS CURRENT							
I_B	Input bias current				±50	±200	pA
		T_A = –40°C to +125°C(1)				±400	
I_{OS}	Input offset current				±100	±400	pA
		T_A = –40°C to +125°C(1)				±800	
NOISE							
E_N	Input voltage noise	f = 0.1Hz to 10Hz			320		nV_{PP}
					48		nV_{RMS}
e_N	Input voltage noise density	f = 1Hz			15		nV/√Hz
		f = 10Hz			15		
		f = 100Hz			15		
		f = 1kHz			15		
i_N	Input current noise	f = 1kHz			60		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range	T_A = –40°C to +125°C(1)		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5V, (V–) - 0.1V < V_{CM} < (V+) + 0.1V		112	130		dB
			T_A = –40°C to +125°C(1)	110			
		V_S = 1.8V, (V–) - 0.1V < V_{CM} < (V+) + 0.1V		105	120		
			T_A = –40°C to +125°C(1)	104			
INPUT CAPACITANCE							
Z_{ID}	Differential				100 || 6		MΩ || pF
Z_{ICM}	Common-mode				60 || 3.5		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 5.5V, (V–) + 0.1V < V_{OUT} < (V+) – 0.1V		114	124		dB
			T_A = –40°C to +125°C(1)	113			
		V_S = 5.5V, (V–) + 0.15V < V_{OUT} < (V+) – 0.15V, R_L = 2kΩ		114	120		
			T_A = –40°C to +125°C(1)	113			
A_{OL}	Open-loop voltage gain	V_S = 1.8V, (V–) + 0.1V < V_{OUT} < (V+) – 0.1V		104	114		dB
			T_A = –40°C to +125°C(1)	100			

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5.7 Electrical Characteristics (continued)

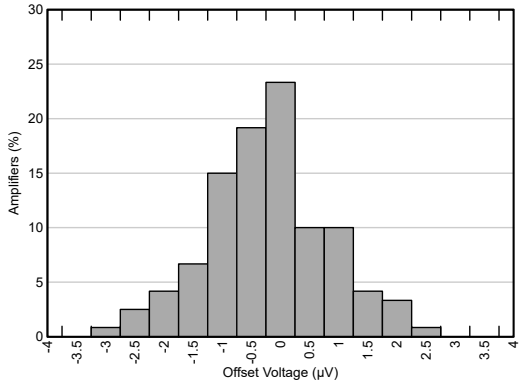
at T_A = 25°C, R_L = 10kΩ connected to V_S / 2, V_S = 1.8V to 5.5V, V_{CM} = V_S / 2, V_{OUT} = V_S / 2, and min and max specification established from manufacturing final test (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				3.5		MHz
SR	Slew rate	V_S = 5.5V, G = +1			1.8		V/µs
t_S	Settling time	To 0.1%, 1V step, G = +1			5		µs
t_{OR}	Overload recovery time	V_{IN} × G > V_S			1.2		µs
f_{CHOP}	Chopping clock frequency(1)				200		kHz
THD+N	Total harmonic distortion + noise	V_{OUT} = 1V_{RMS}, G = +1, f = 1kHz	RL = 10kΩ		0.0007		%
			R_L = 2kΩ		0.0015		
OUTPUT							
	Voltage output swing from rail	R_L = No load			2.5	5	mV
			T_A = –40°C to +125°C(1)			8	
		R_L = 10kΩ			7	10	
			T_A = –40°C to +125°C(1)			15	
		R_L = 2kΩ(1)			25	30	
			T_A = –40°C to +125°C(1)			45	
I_{SC}	Short-circuit current	V_S = 5.5V			±60		mA
		V_S = 1.8V			±10		
	Phase margin	G = +1, R_L = 10kΩ			75		°
C_{LOAD}	Capacitive load drive			See the typical characteristic curve			
R_O	Open-loop output impedance	f = 1MHz			180		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0mA			500	615	µA
			T_A = –40°C to 125°C(1)			625	
	Turn-on time	At V_S = 5.5V, V_S ramp rate > 0.05V/µs, settle to 1%			25		µs

(1) Specification established from device population bench system measurements across multiple lots.

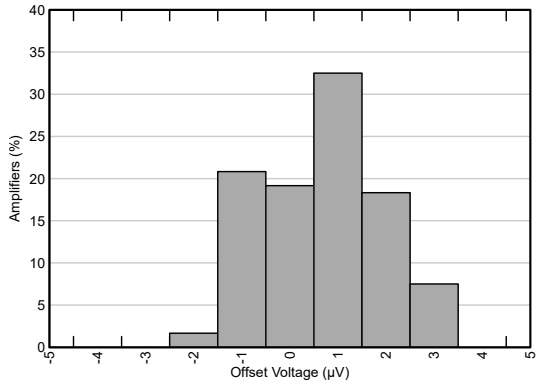
5.8 Typical Characteristics

at T_A = 25°C, V_S = ±2.75V, V_{CM} = V_S / 2, and R_L = 10kΩ (unless otherwise noted)



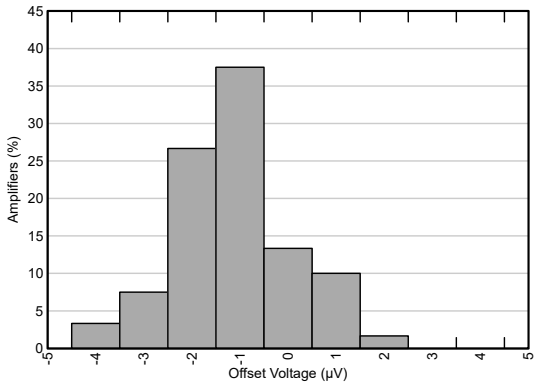
V_S = 5.5V V_{CM} = V_S / 2 T_A = 25°C
N = 120 Mean = 0.03µV Sigma = 1.02µV

Figure 5-1. Offset Voltage Distribution



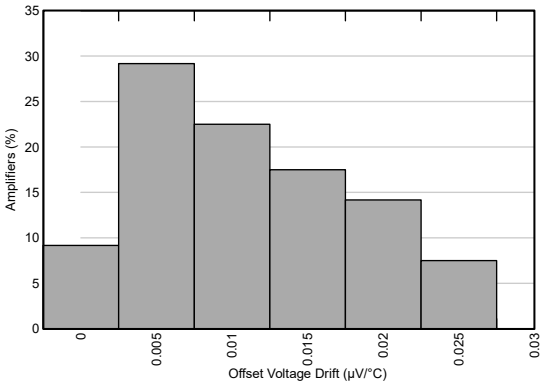
V_S = 5.5V V_{CM} = V_S / 2 T_A = 125°C
N = 120 Mean = 1.17µV Sigma = 1.22µV

Figure 5-2. Offset Voltage Distribution



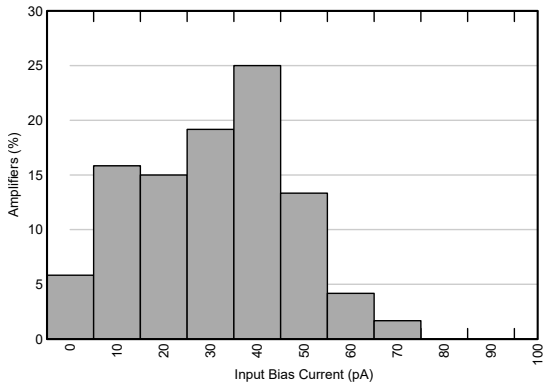
V_S = 5.5V V_{CM} = V_S / 2 T_A = –40°C
N = 120 Mean = –0.64µV Sigma = 1.2µV

Figure 5-3. Offset Voltage Distribution



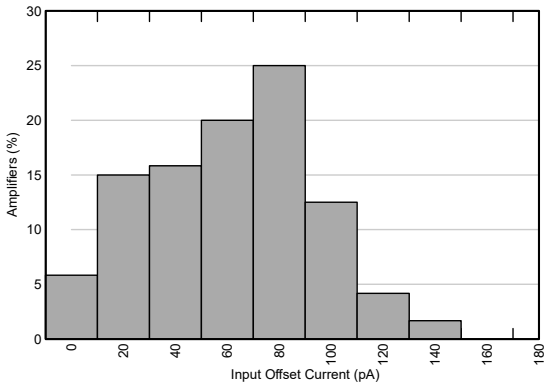
V_S = 5.5V V_{CM} = V_S / 2 N = 120
Mean = 0.013µV/°C Sigma = 0.007µV/°C

Figure 5-4. Offset Voltage Drift



V_S = 5.5V V_{CM} = V_S / 2 T_A = 25°C
N = 120 Mean = 35.9pA Sigma = 16.1pA

Figure 5-5. Input Bias Current Distribution



V_S = 5.5V V_{CM} = V_S / 2 T_A = 25°C
N = 120 Mean = 71.7pA Sigma = 32.1pA

Figure 5-6. Input Offset Current Distribution

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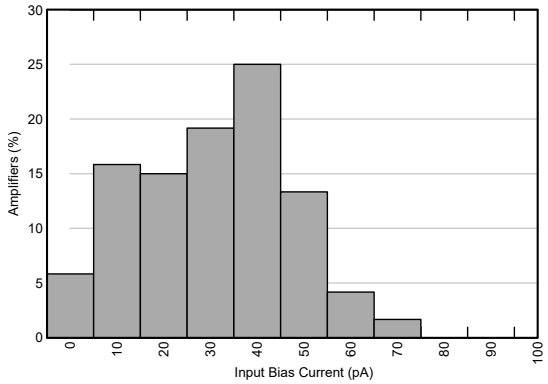
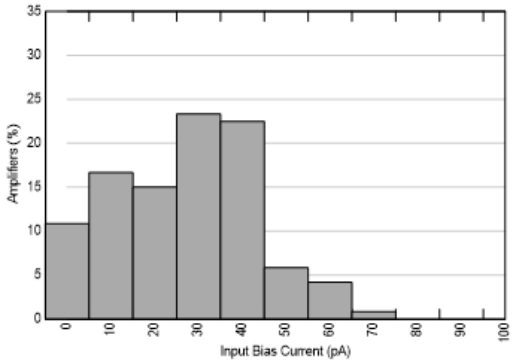
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.75V, V_{CM} = V_S / 2, and R_L = 10kΩ (unless otherwise noted)



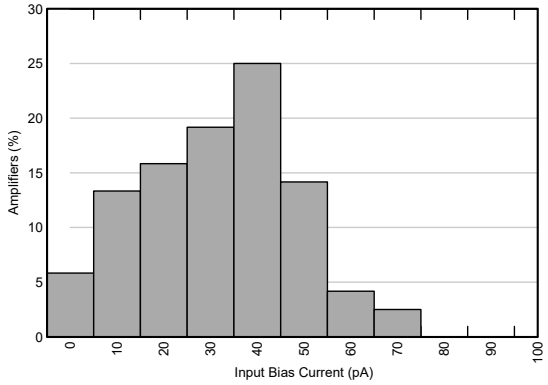
V_S = 5.5V | V_{CM} = V_S / 2 | T_A = 125°C
N = 120 | Mean = 35.9pA | Sigma = 16.1pA

Figure 5-7. Input Bias Current Distribution



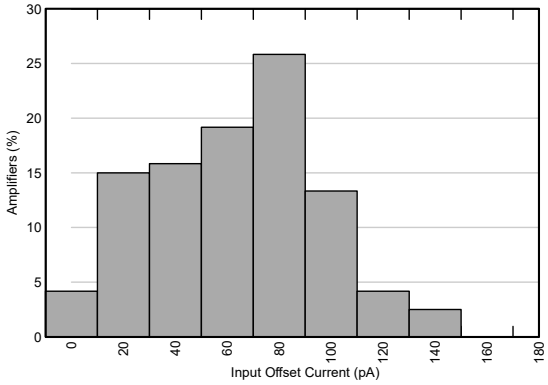
V_S = 5.5V | V_{CM} = V_S / 2 | T_A = 125°C
N = 120 | Mean = 31.5pA | Sigma = 15.7pA

Figure 5-8. Input Offset Current Distribution



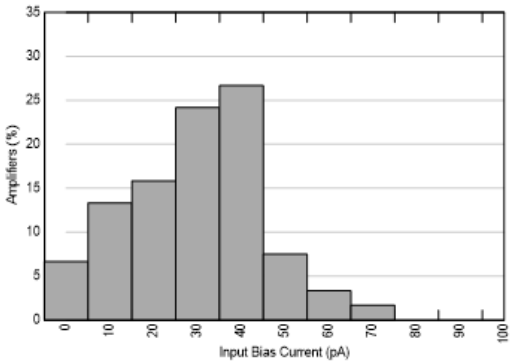
V_S = 1.8V | V_{CM} = V_S / 2 | T_A = 25°C
N = 120 | Mean = 36.7pA | Sigma = 16.3pA

Figure 5-9. Input Bias Current Distribution



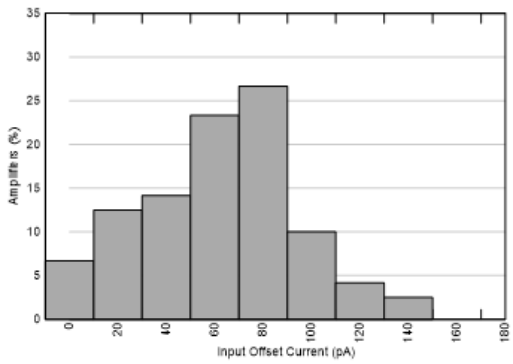
V_S = 1.8V | V_{CM} = V_S / 2 | T_A = 25°C
N = 120 | Mean = 73.1pA | Sigma = 32.4pA

Figure 5-10. Input Offset Current Distribution



V_S = 1.8V | V_{CM} = V_S / 2 | T_A = 125°C
N = 120 | Mean = 34.1pA | Sigma = 16.2pA

Figure 5-11. Input Bias Current Distribution



V_S = 1.8V | V_{CM} = V_S / 2 | T_A = 125°C
N = 120 | Mean = 72pA | Sigma = 32.4pA

Figure 5-12. Input Offset Current Distribution

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5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.75V, V_{CM} = V_S / 2, and R_L = 10kΩ (unless otherwise noted)

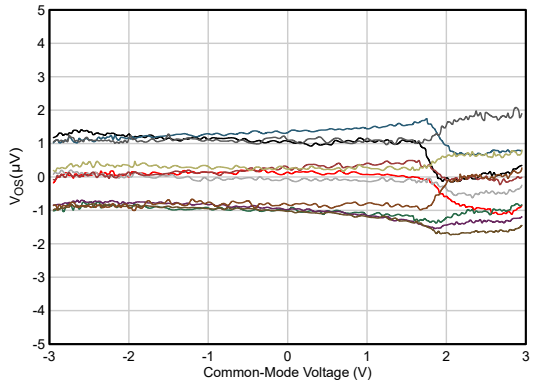

Figure 5-13. Offset Voltage vs Common-Mode Voltage

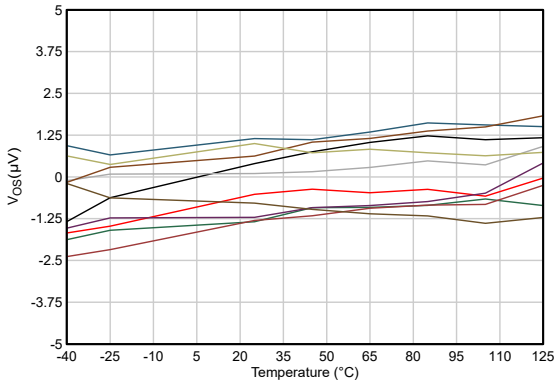

Figure 5-14. Offset Voltage vs Temperature

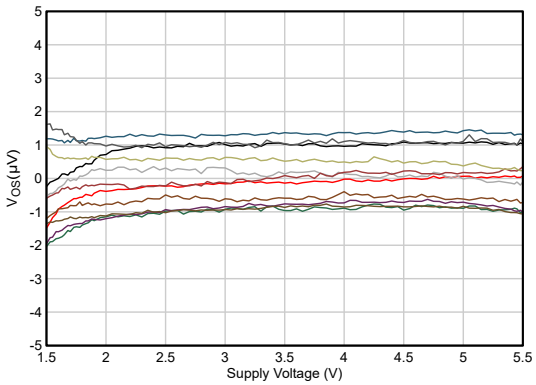

Figure 5-15. Offset Voltage vs Supply Voltage

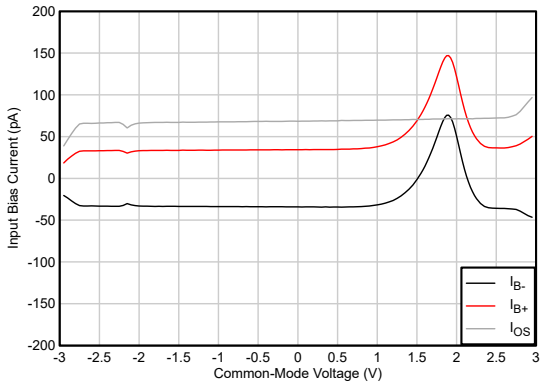

Figure 5-16. Input Bias Current vs Common-Mode Voltage

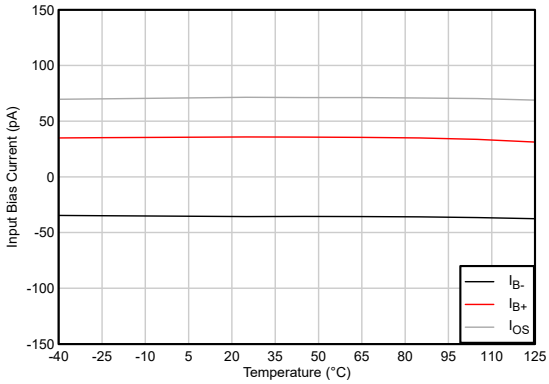

Figure 5-17. Input Bias Current and Offset Current vs Temperature

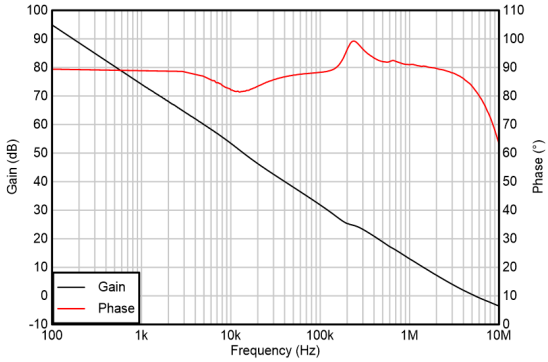

Figure 5-18. Open-Loop Gain and Phase vs Frequency

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5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.75V, V_{CM} = V_S / 2, and R_L = 10kΩ (unless otherwise noted)

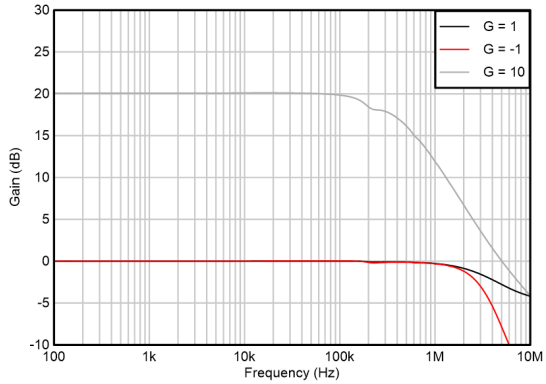


Figure 5-19. Closed-Loop Gain vs Frequency

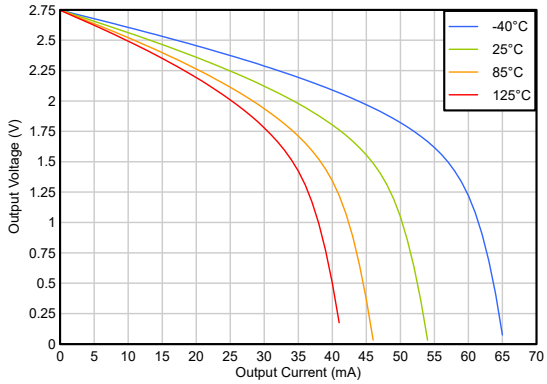


Figure 5-20. Output Voltage Swing vs Output Current (Sourcing)

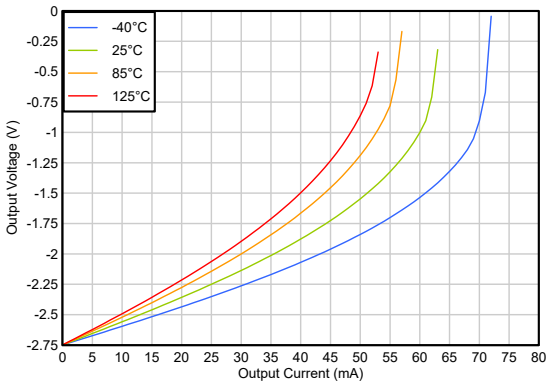
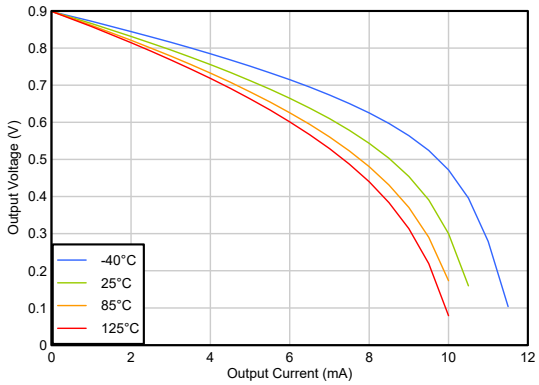
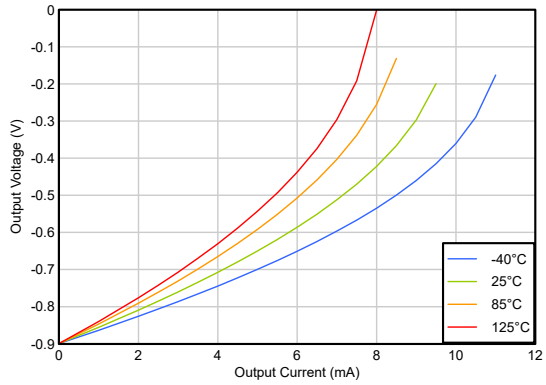


Figure 5-21. Output Voltage Swing vs Output Current (Sinking)



V_S = 1.8V

Figure 5-22. Output Voltage Swing vs Output Current (Sourcing)



V_S = 1.8V

Figure 5-23. Output Voltage Swing vs Output Current (Sinking)

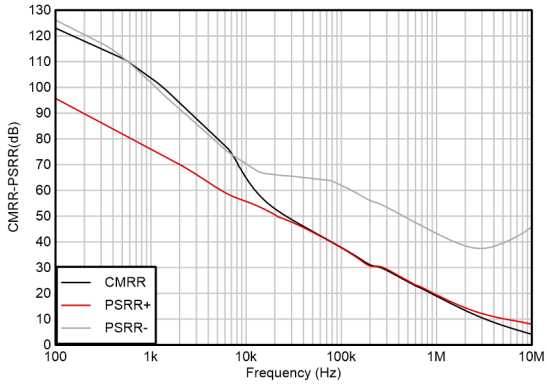


Figure 5-24. CMRR and PSRR vs Frequency

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.75V, V_{CM} = V_S / 2, and R_L = 10kΩ (unless otherwise noted)

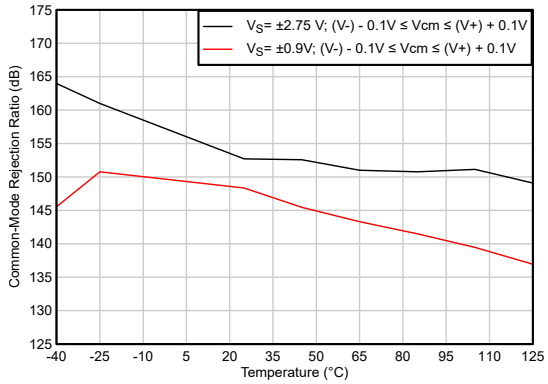


Figure 5-25. CMRR vs Temperature

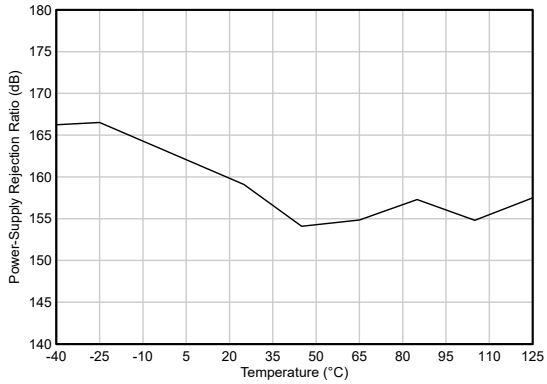


Figure 5-26. PSRR vs Temperature

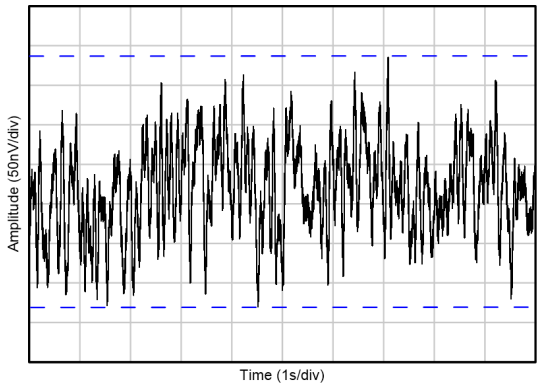


Figure 5-27. 0.1Hz to 10Hz Voltage Noise

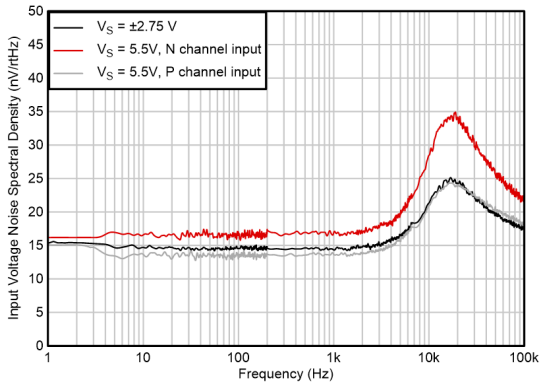


Figure 5-28. Input Voltage Noise Spectral Density vs Frequency

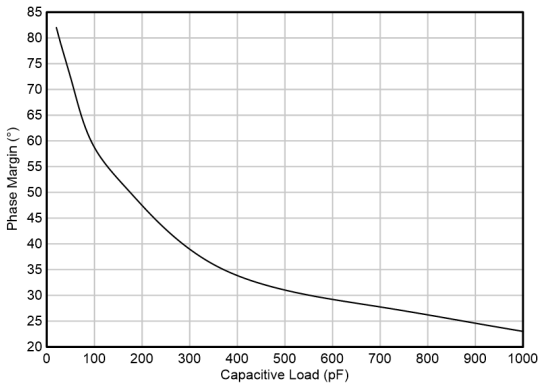
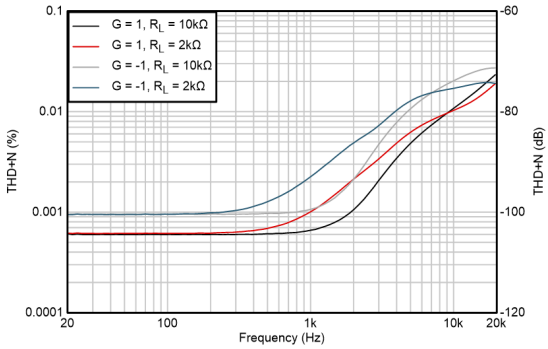


Figure 5-29. Phase Margin vs Cap Load



V_{OUT} = 1V_{RMS}

Figure 5-30. THD+N vs Frequency

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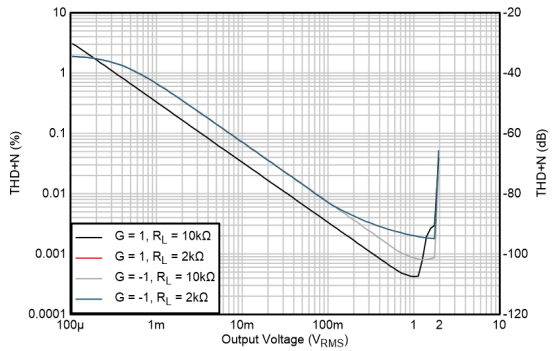
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.75V, V_{CM} = V_S / 2, and R_L = 10kΩ (unless otherwise noted)



f = 1kHz

Figure 5-31. THD+N vs Output Amplitude

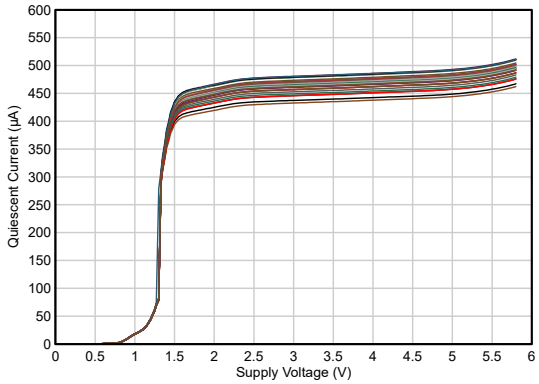


Figure 5-32. Quiescent Current vs Supply Voltage

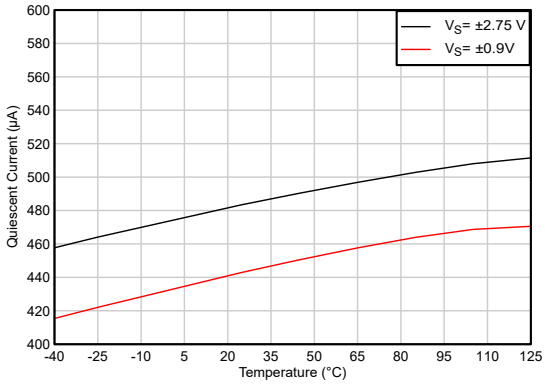


Figure 5-33. Quiescent Current vs Temperature

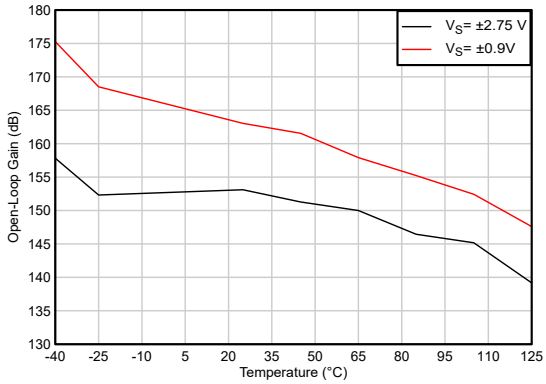


Figure 5-34. Open-Loop Gain vs Temperature

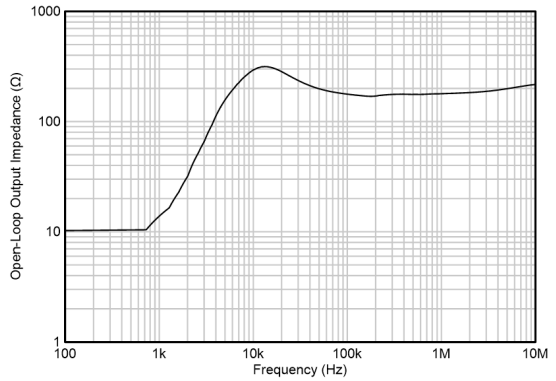
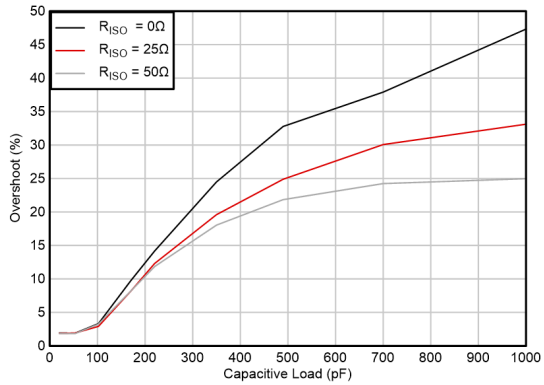


Figure 5-35. Open-Loop Output Impedance vs Frequency

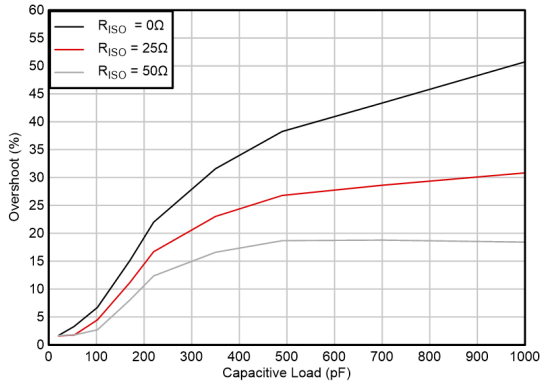


Gain = –1, 10mV step

Figure 5-36. Small-Signal Overshoot vs Capacitive Load

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.75V, V_{CM} = V_S / 2, and R_L = 10kΩ (unless otherwise noted)



Gain = 1, 10mV step

Figure 5-37. Small-Signal Overshoot vs Capacitive Load

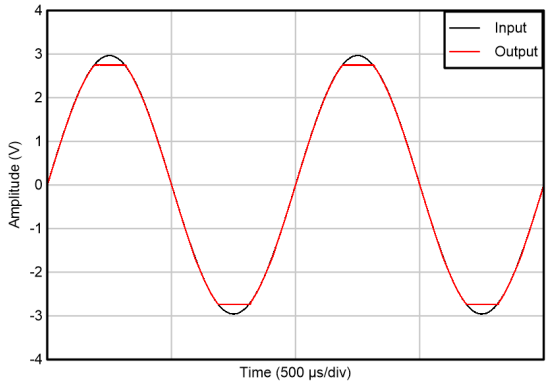


Figure 5-38. No Phase Reversal

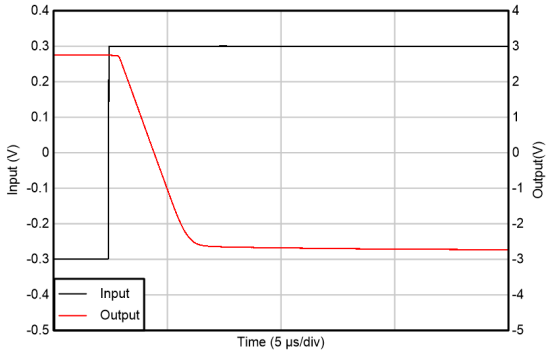


Figure 5-39. Positive Overload Recovery

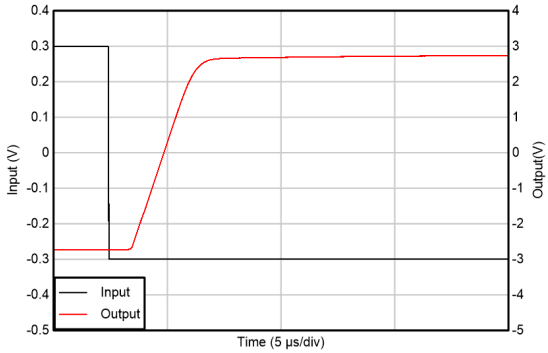
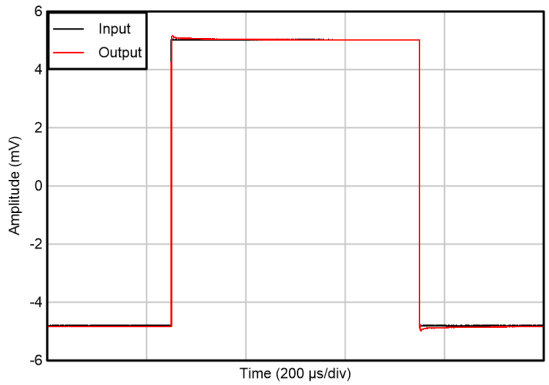
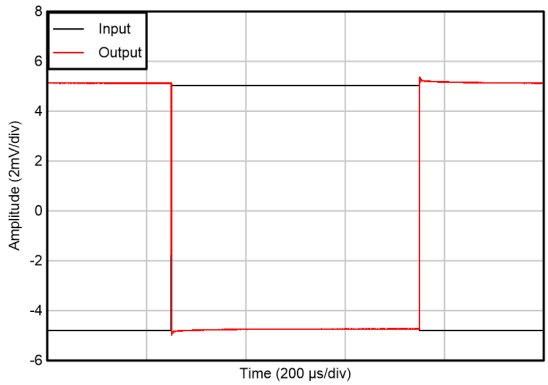


Figure 5-40. Negative Overload Recovery



Gain = 1, 10mV step

Figure 5-41. Small-Signal Step Response



Gain = –1, 10mV step

Figure 5-42. Small-Signal Step Response

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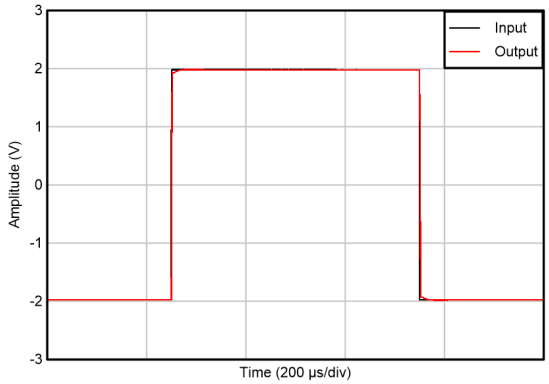
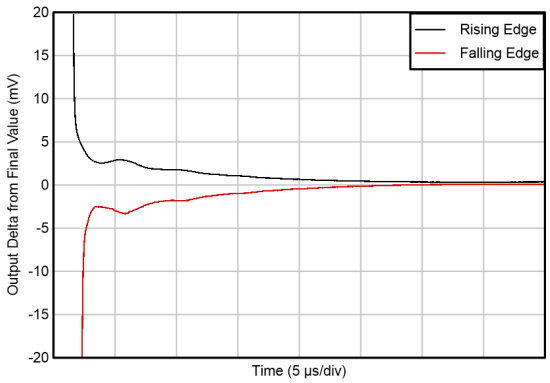
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.75V, V_{CM} = V_S / 2, and R_L = 10kΩ (unless otherwise noted)



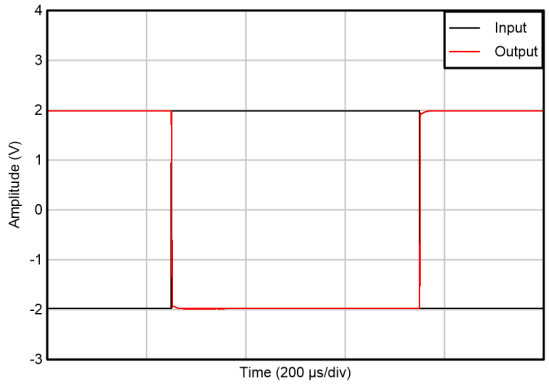
Gain = 1, 4V step

Figure 5-43. Large-Signal Step Response



Gain = 1, 4V step

Figure 5-44. Output Settling to Final Value



Gain = –1, 4V step

Figure 5-45. Large-Signal Step Response

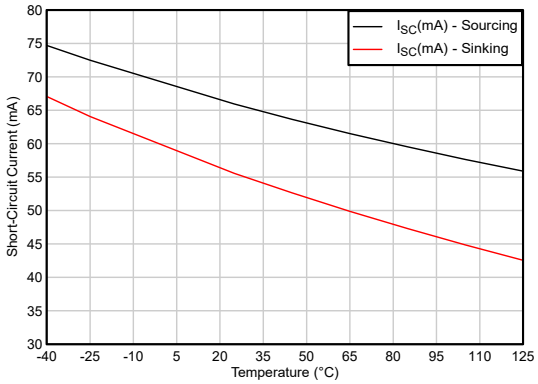


Figure 5-46. Short-Circuit Current vs Temperature

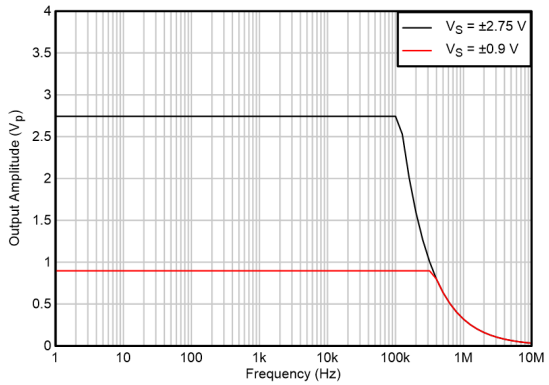


Figure 5-47. Maximum Output Voltage vs Frequency

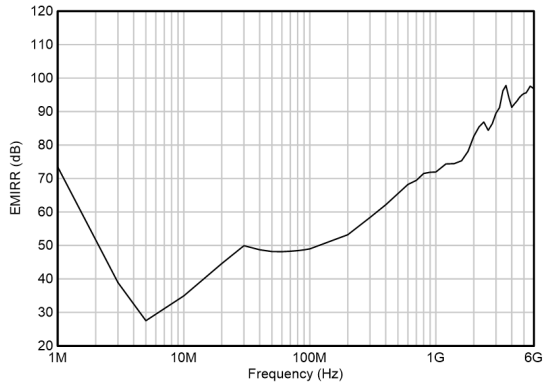


Figure 5-48. EMIRR vs Frequency

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.75V, V_{CM} = V_S / 2, and R_L = 10kΩ (unless otherwise noted)

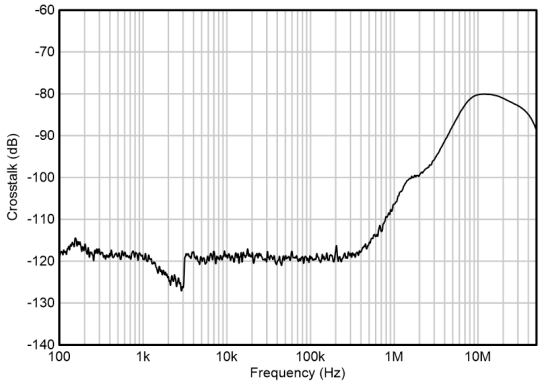


Figure 5-49. Channel Separation

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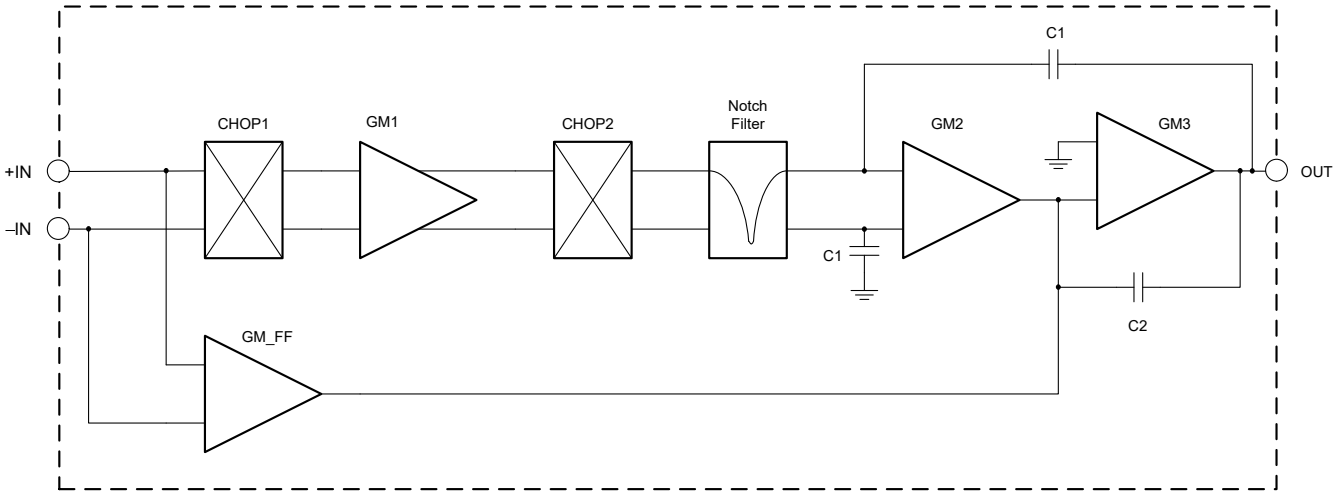
6 Detailed Description

6.1 Overview

The TLVx825 is part of a family of zero-drift operational amplifiers from TI. The zero-drift architecture provides precision performance such as lower offset, lower offset drift over temperature, greater offset stability over time and a flat noise floor. TLVx825 achieves an input referred offset voltage of 4µV, an offset drift of 0.02µV/°C over the entire operating temperature range of –40°C to +125°C, along with a low frequency noise of just 320nV$_{PP}$ in the standard 0.1 – 10Hz range. In addition, this device offers excellent linear performance with high CMRR, PSRR, and A_{OL}. This combination of specs provide excellent accuracy in high gain applications, thereby greatly reducing the need for system level calibration.

The TLVx825 operational amplifiers combine precision offset and drift with excellent overall ac performance, making the device a great choice for a wide variety of precision voltage sensing and current sensing applications. This device operates from 1.8V to 5.5V with a quiescent current of 500µA while achieving a robust cap load drive of 300pF with a 30% overshoot in unity gain. The device also offers good ac performance of 3.5MHz bandwidth, 15nV/√Hz broad-band noise, and a good distortion performance when operating at less than the chopper frequency of 200kHz.

6.2 Functional Block Diagram



6.3 Feature Description

The TLVx825 operational amplifiers use a proprietary, periodic auto-calibration technique to provide extremely low input offset voltage and input offset voltage drift over time and temperature. The devices have several integrated features to help maintain a high level of precision through a variety of applications. These features include a robust cap load stability, phase-reversal protection, and a strong EMI rejection capability.

Several design techniques and considerations to maintain the specified performance of the TLVx825 are detailed in the *Optimizing Chopper Amplifier Accuracy* technical white paper and *Op Amp Offset Voltage and Bias Current Limitations* technical white paper.

6.3.1 Operating Voltage

The TLVx825 series of operational amplifiers is fully specified from 1.8V to 5.5V. In addition, many specifications apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are provided in the *Typical Characteristics* section. TI highly recommends to add low-ESR ceramic bypass capacitors (C_{BYP}) between each supply pin and ground. Only one C_{BYP} is sufficient for single supply operation. Make sure that C_{BYP} is placed as close to the device as possible and the power supply trace routes through C_{BYP} before reaching the amplifier power supply terminals.

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6.3.2 Input Common-Mode Range

The TLVx825 are specified for operation from 1.8V to 5.5V (±0.9V to ±2.75V). The TLVx825 is classified as a rail-to-rail input operational amplifier because of the wide input common-mode voltage (V_{CM}) range that extends 100mV beyond either supply rails. This range makes them an excellent choice for single supply operation and precision low-side, high-side current sensing applications. The device achieves a typical CMRR of 120dB or higher across the entire common-mode range for both 1.8V and 5.5V supply rails.

6.3.3 Output Range

The TLVx825 delivers a robust output drive capability. An output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. The device is designed to have a typical output short circuit current of ±60mA at room temperature and at 5.5V, making the device an excellent choice for driving resistive and current loads. For resistive loads up to 2kΩ and a power supply of 5.5V, the output swings within a maximum of 30mV to either supply rail, thereby using almost the entire input range of an ADC in ADC driver applications.

6.3.4 Capacitive Load and Stability

The TLVx825 is designed for use in applications where driving a capacitive load is required. As with all operational amplifiers, there can be specific instances where the device can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation.

An operational amplifier in the unity-gain (1V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operating at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases when capacitive loading increases. When operating in the unity-gain configuration, the TLVx825 has a phase margin of 60° with 100pF of capacitive load. The device remains stable with pure capacitive loads up to approximately 350pF with acceptable phase margin of 35° and has no sustained oscillations up to 1nF. The equivalent series resistance (ESR) of some very large capacitors (greater than 1µF) is sometimes sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when measuring the overshoot response of the amplifier at higher voltage gains.

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor (typically 10Ω to 50Ω) in series with the output, as shown in Figure 6-1. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. This action is typically the circuit configuration used in ADC driver application with C_{load} serving as a charge bucket for the ADC sampling capacitor.

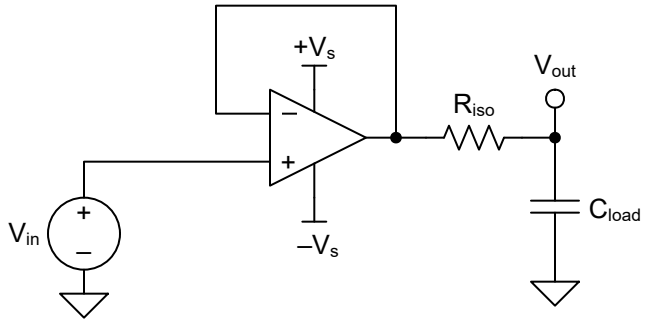

Figure 6-1. Improving Capacitive Load Drive

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6.3.5 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output stage of the operational amplifier enters a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or high gain. After one of the outputs enters the saturation region, the output stage requires additional time to return to the linear operating state which is referred to as overload recovery time. After the output stage returns to linear operating state, the amplifier begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLVx825 family is designed to be approximately 1.5µs typical.

6.3.6 Phase-Reversal Protection

The TLVx825 includes internal phase-reversal protection. Some op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting and unity gain circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The TLVx825 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. Figure 6-2 shows this performance.

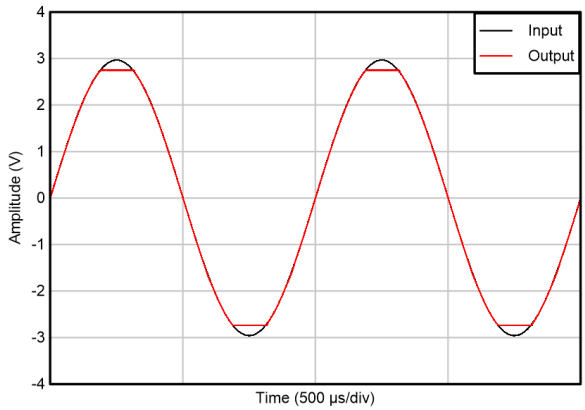

Figure 6-2. No Phase Reversal

6.3.7 Chopping Transients

Zero-drift amplifiers such as the TLVx825 use a switching architecture on the inputs to correct for the intrinsic offset and drift of the amplifier. Charge injection from the integrated switches on the inputs can introduce short transients in the input bias current of the amplifier. The extremely short duration of these pulses prevents the pulses from amplifying; however, the pulses can be coupled to the output of the amplifier through the feedback network. Use low value feedback and input resistors to minimize the input transient effects at the output of the amplifier. Use a low-pass filter, such as an RC network, to minimize any additional noise attributed to the transients. The chopping frequency of the TLVx825 is typically 200kHz.

6.3.8 EMI Rejection

The TLVx825 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLVx825 benefits from these design improvements.

High-frequency signals conducted or radiated to any pin of the operational amplifier can result in adverse effects, as there is insufficient amplifier loop gain to correct for signals with spectral content outside the bandwidth. Conducted or radiated EMI on inputs, power supply, or output can result in unexpected dc offsets, transient voltages, or other unknown behavior. Take care to properly shield and isolate sensitive analog nodes from noisy radio signals and digital clocks and interfaces.

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Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. Figure 6-3 shows the results of this testing on the TLVx825. Table 6-1 lists the EMIRR +IN values for the TLVx825 at particular frequencies commonly encountered in real-world applications. Table 6-1 lists applications that can be centered on or operated near the particular frequency shown. See also the *EMI Rejection Ratio of Operational Amplifiers (With OPA333 and OPA333-Q1 as an Example)* application note.

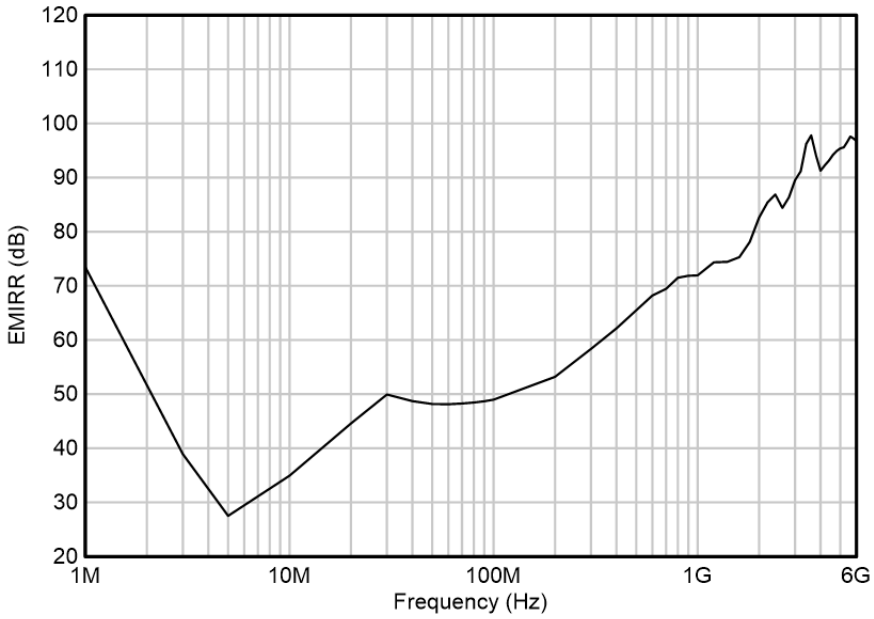

Figure 6-3. EMIRR Testing

Table 6-1. TLVx825 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION AND ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	63dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	72dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	75.5dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	86dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	97dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	95.5dB

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. An op amp that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this section provides the EMIRR +IN, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the op amp. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Op amp input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting op amp inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.

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- EMIRR is more simple to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a PCB. This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.

High-frequency signals conducted or radiated to any pin of the operational amplifier can result in adverse effects, as there is insufficient amplifier loop gain to correct for signals with spectral content outside the bandwidth. Conducted or radiated EMI on inputs, power supply, or output can result in unexpected dc offsets, transient voltages, or other unknown behavior. Take care to properly shield and isolate sensitive analog nodes from noisy radio signals and digital clocks and interfaces.

6.3.9 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 6-4 shows an illustration of the ESD circuits contained in the TLVx825 (shows as the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the op amp. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger or threshold voltage that is greater than the normal operating voltage of the TLVx825, but less than the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

Figure 6-4 shows that when the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive, and do not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits are biased on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

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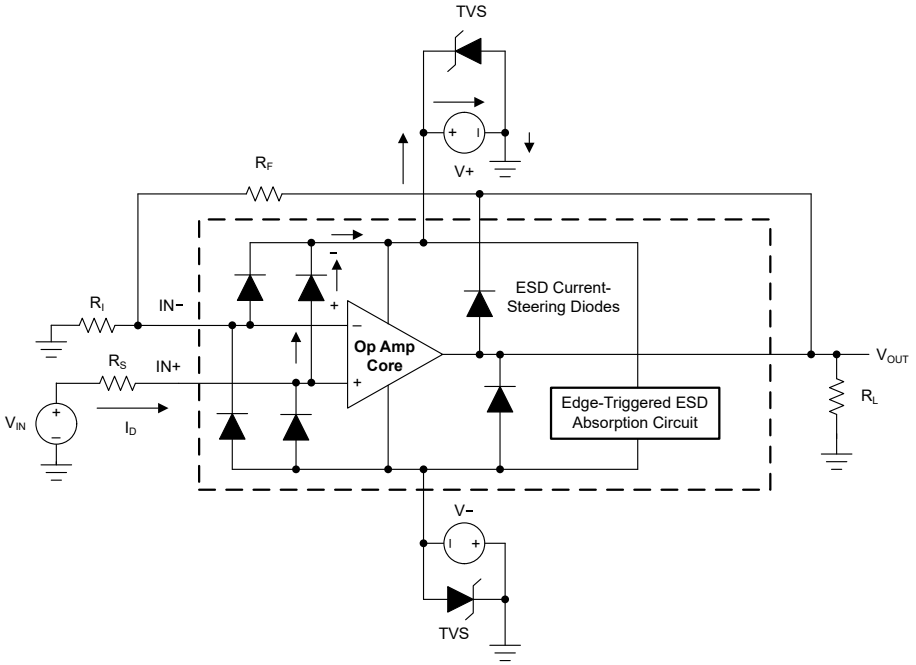

V_{IN} = (V+) + 500mV
TVS: V+ < $V_{TVSBR\ (min)}$ < 6V, where $V_{TVSBR\ (min)}$ is the minimum specified value for the TVS breakdown voltage.
Suggested value for R_S is approximately 5kΩ in an overvoltage condition.

Figure 6-4. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

Figure 6-4 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies V+ or V– are at 0V. Again, this question depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current can be supplied by the input source through the current-steering diodes. This state is not a normal biasing condition for the amplifier and can result in specification degradation or abnormal operation. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external transient voltage suppressor (TVS) diodes to the supply pins; see also Figure 6-4. The breakdown voltage must be selected such that the diode does not turn on during normal operation. However, the breakdown voltage must be low enough so that the TVS diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

6.4 Device Functional Modes

The TLVx825 has a single functional mode, and is operational when the power-supply voltage is at least or greater than 1.8V (±0.9V). The recommended power supply voltage for the TLVx825 is 1.8V to 5.5V (±0.9V to ±2.75V).

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLVx825 operational amplifier combines precision offset and drift with excellent overall performance, making the device an excellent choice for many precision applications. The precision offset drift of only 0.02µV/°C provides stability over the entire temperature range. In addition, the device pairs excellent CMRR, PSRR, and A_{OL} dc performance with outstanding low-noise operation. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1µF capacitors are adequate.

7.1.1 Basic Noise Calculations

Low-noise circuit design requires careful analysis of all noise sources. In many cases, external noise sources can dominate; consider the effect of source resistance on overall op-amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. The source impedance is typically fixed; consequently, select op amp and the feedback resistors that minimize the respective contributions to the total noise.

Figure 7-1 shows the noninverting op-amp circuit configurations with gain. Figure 7-2 shows the inverting op-amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the low current noise of the TLVx825 means that the current noise contribution can be ignored.

The feedback resistor values can generally be chosen to make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

For additional resources on noise calculations, visit *TI Precision Labs*.

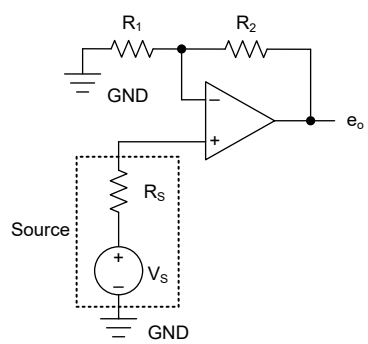

Figure 7-1. Noise Calculation in Noninverting Gain Configurations

$$E_o = e_o\sqrt{BW_N}\ [V_{RMS}] \tag{1}$$

$$e_o = \left(1 + \frac{R_2}{R_1}\right)\sqrt{{e_S}^2 + {e_N}^2 + \left(e_{R_1||R_2}\right)^2 + \left(i_N R_S\right)^2 + \left(i_N \frac{R_1 R_2}{R_1 + R_2}\right)^2}\left[\frac{V}{\sqrt{Hz}}\right] \tag{2}$$

$$e_S = \sqrt{4k_B T(K) R_S} \left[\frac{V}{\sqrt{Hz}}\right] \tag{3}$$

$$e_{R_1||R_2} = \sqrt{4k_B T(K)\left(\frac{R_1 R_2}{R_1 + R_2}\right)} \left[\frac{V}{\sqrt{Hz}}\right] \tag{4}$$

$$k_B = 1.38065 \times 10^{-23} \left[\frac{J}{K}\right] \tag{5}$$

$$T(K) = 2.37.15 + T(°C)\ [K] \tag{6}$$

where

- e_n is the voltage noise spectral density of the amplifier. For the TLVx825, e_n = 15nV/√Hz at 1kHz).
- e_o is the total noise density.
- e_S is the thermal noise of R_S.
- $e_{R_1 || R_2}$ is the thermal noise of R_1 || R_2.
- k_B is the Boltzmann constant.
- T(K) is the temperature in kelvins.

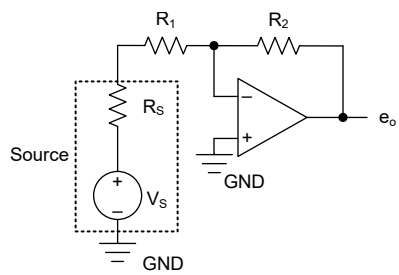

Figure 7-2. Noise Calculation in Inverting Gain Configurations

$$E_o = e_o \sqrt{BW_N}\ [V_{RMS}] \tag{7}$$

$$e_o = \left(1 + \frac{R_2}{R_S + R_1}\right)\sqrt{{e_N}^2 + \left(e_{R_1 + R_S||R_2}\right)^2 + \left(i_N \frac{(R_S + R_1)R_2}{R_S + R_1 + R_2}\right)^2} \left[\frac{V}{\sqrt{Hz}}\right] \tag{8}$$

$$e_{R_1 + R_S||R_2} = \sqrt{4k_B T(K)\left(\frac{(R_S + R_1)R_2}{R_S + R_1 + R_2}\right)} \left[\frac{V}{\sqrt{Hz}}\right] \tag{9}$$

$$k_B = 1.38065 \times 10^{-23} \left[\frac{J}{K}\right] \tag{10}$$

$$T(K) = 2.37.15 + T(°C)\ [K] \tag{11}$$

where

- e_n is the voltage noise spectral density of the amplifier. For the TLVx825, e_n = 15nV/√.Hz at 1kHz)
- e_o is the total noise density.
- e_S is the thermal noise of R_S.
- $e_{(R_1 + R_S) || R_2}$ is the thermal noise of (R_1 + R_S) || R_2.
- k_B is the Boltzmann constant.
- T(K) is the temperature in kelvins.

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7.2 Typical Application

7.2.1 TLVx825 in Low-Side, Current Sensing Application

Figure 7-3 shows the TLVx825 configured in a low-side current sensing application.

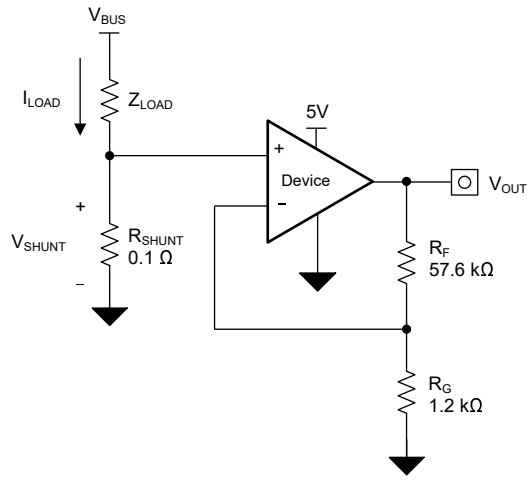

Figure 7-3. TLVx825 in a Low-Side, Current-Sensing Application

7.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0A to 1A
- Maximum output voltage: 4.9V
- Maximum shunt voltage: 100mV

7.2.1.2 Detailed Design Procedure

The transfer function of the circuit in Figure 7-3 is given in Equation 12.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{12}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, the largest shunt resistor is defined using Equation 13.

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100\ mV}{1\ A} = 100\ m\Omega \tag{13}$$

Using Equation 13, R_{SHUNT} is calculated to be 100mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLVx825 to produce an output voltage of approximately 0V to 4.9V. The gain needed by the TLVx825 to produce the necessary output voltage is calculated using Equation 14.

$$Gain = \frac{V_{OUT_MAX} - V_{OUT_MIN}}{V_{IN_MAX} - V_{IN_MIN}} \tag{14}$$

Using Equation 14, the required gain is calculated to be 49V/V, which is set with resistors R_F and R_G. Equation 15 sizes the resistors R_F and R_G, to set the gain of the TLV825 to 49V/V.

$$Gain = 1 + \frac{R_F}{R_G} \tag{15}$$

Selecting R_F as 57.6kΩ and R_G as 1.2kΩ provides a combination that equals 49V/V. Figure 7-4 shows the measured transfer function of the circuit shown in Figure 7-3. Notice that the gain is only a function of the

feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistors values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no impedance selection that works for every system; select an impedance that is best for the system parameters.

7.2.1.3 Application Curve

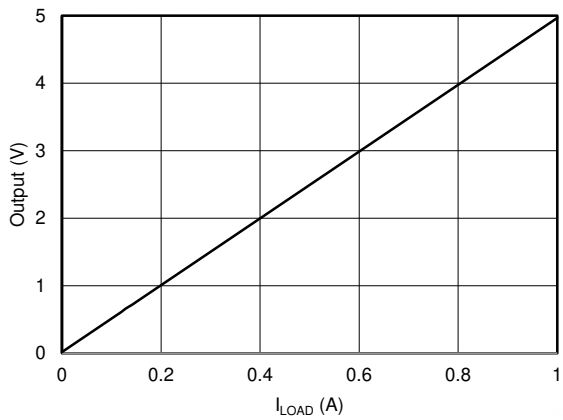

Figure 7-4. Low-Side, Current-Sense Transfer Function

7.3 Power Supply Recommendations

The TLVx825 are specified for operation from 1.8V to 5.5V (±0.9V to ±2.75V). The TLVx825 operates on both single and dual supplies. The TLVx825 do not require symmetrical supplies; the op amps only require a minimum voltage of 1.8V to operate.

> **CAUTION**
> Supply voltages larger than 6V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout*.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power connections of the board and propagate to the power pins of the op amp. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground.
  - Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. One bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, then cross the sensitive trace at a 90 degree angle, which is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in *Layout Example*. Keeping R_1 and R_2 close to the inverting input minimizes parasitic capacitance.

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- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- TI recommends cleaning the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example

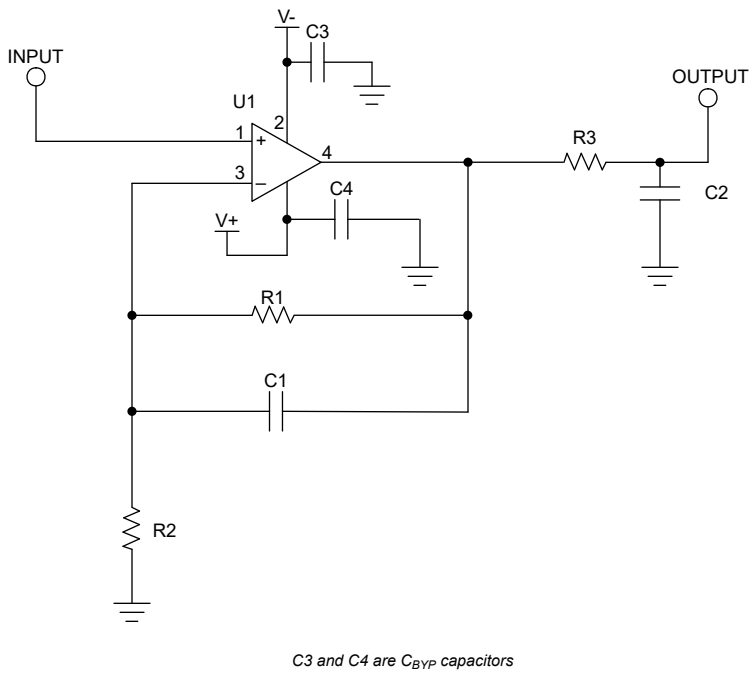

Figure 7-5. Schematic for Noninverting Configuration Layout Example

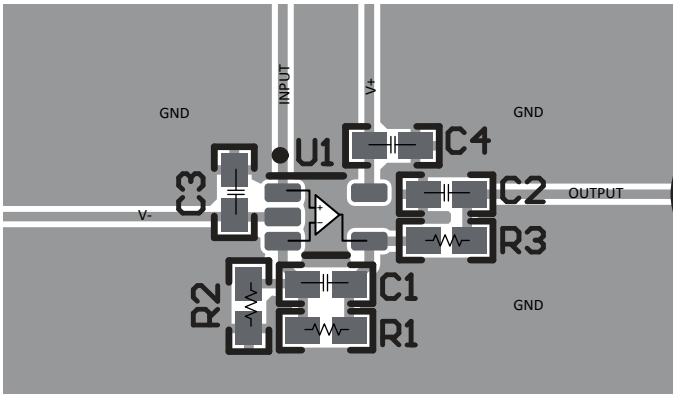

Figure 7-6. Operational Amplifier Board Layout for Noninverting Configuration - SOT-SC70 (DCK) Package

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype designs before committing to layout and fabrication, reducing development cost and time to market.

8.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Design and simulation tools web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI software folder.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Zero-drift Amplifiers: Features and Benefits* application brief
- Texas Instruments, *The PCB is a component of op amp design* analog design journal
- Texas Instruments, *Operational amplifier gain stability, Part 3: AC gain-error analysis* analog design journal
- Texas Instruments, *Operational amplifier gain stability, Part 2: DC gain-error analysis* analog design journal
- Texas Instruments, *Using infinite-gain, MFB filter topology in fully differential active filters* analog design journal
- Texas Instruments, *Op Amp Performance Analysis* application note
- Texas Instruments, *Single-Supply Operation of Operational Amplifiers* application note
- Texas Instruments, *Shelf-Life Evaluation of Lead-Free Component Finishes* application note
- Texas Instruments, *Feedback Plots Define Op Amp AC Performance* application note
- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers (With OPA333 and OPA333-Q1 as an Example)* application note
- Texas Instruments, *Analog Linearization of Resistance Temperature Detectors* analog design journal
- Texas Instruments, *TI Precision Design TIPD102 High-Side Voltage-to-Current (V-I) Converter* reference guide
- Texas Instruments, *Optimizing Chopper Amplifier Accuracy* technical white paper
- Texas Instruments, *Op Amp Offset Voltage and Bias Current Limitations* technical white paper

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2026) to Revision B (September 2026)	Page
• Changed TLV2825 D and DGK packages from Preview to Production Data	1

Changes from Revision * (May 2026) to Revision A (June 2026)	Page
• Changed TLV4825 D and PW packages from Advance Information to Production Data	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2825DR	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	45QT
TLV4825DR	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	45WTLV4825
TLV4825PWR	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	45US825

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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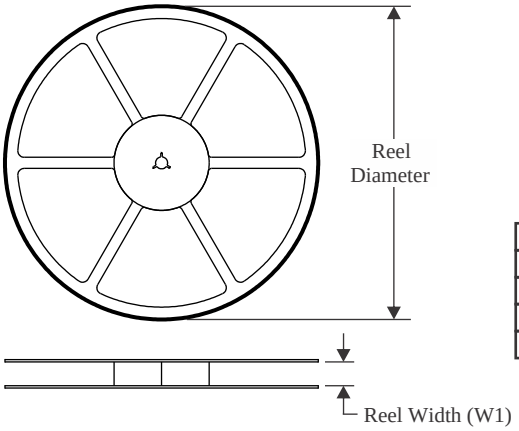
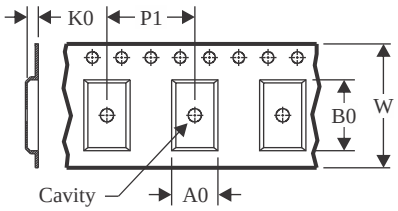
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

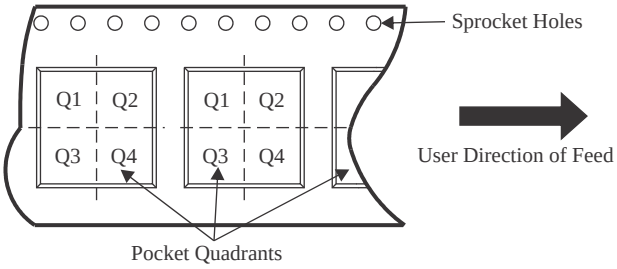


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

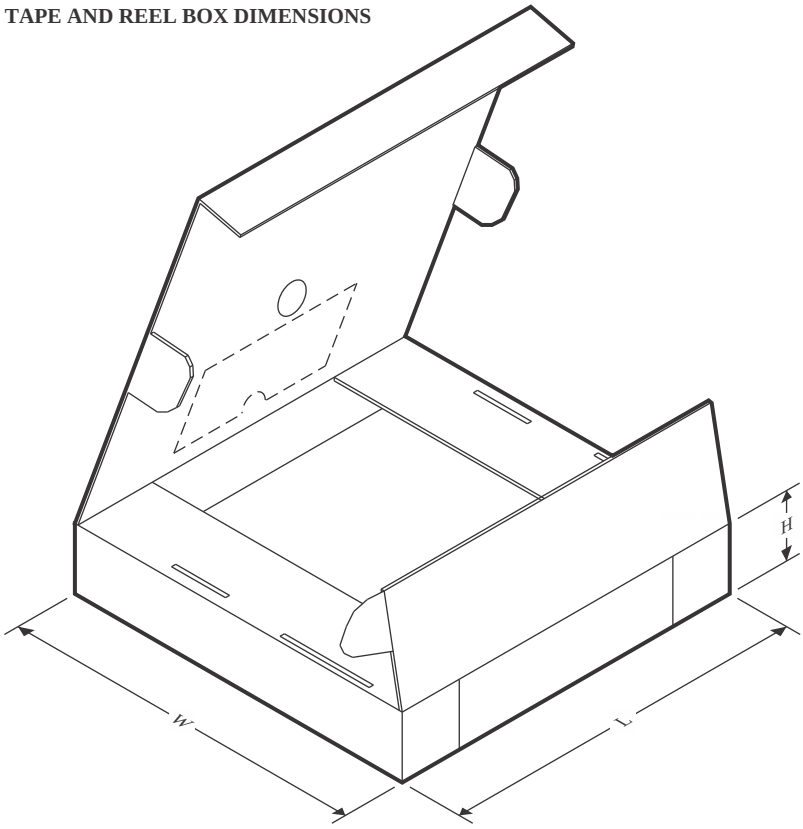
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

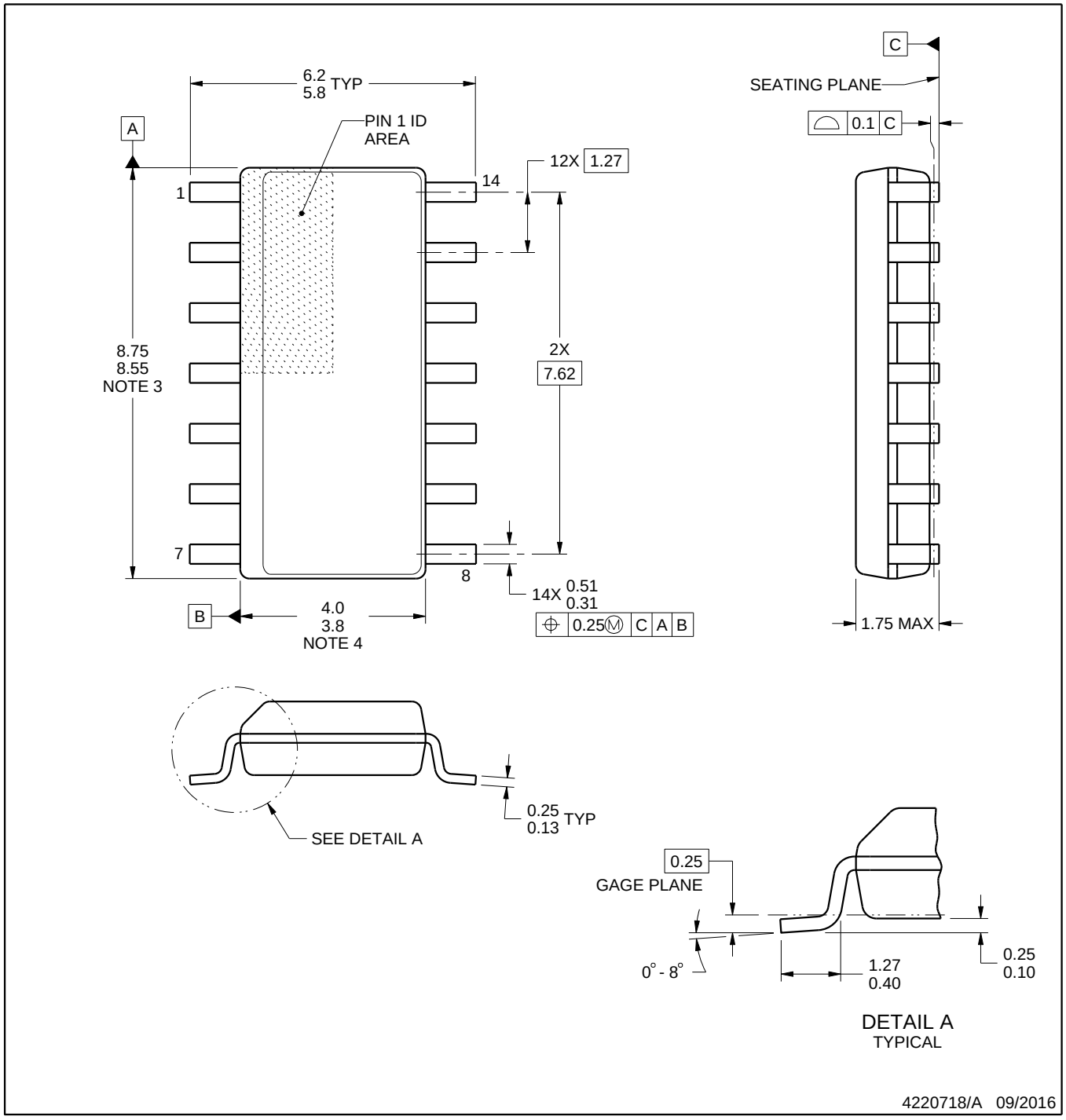
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2825DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV4825DR	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV4825PWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



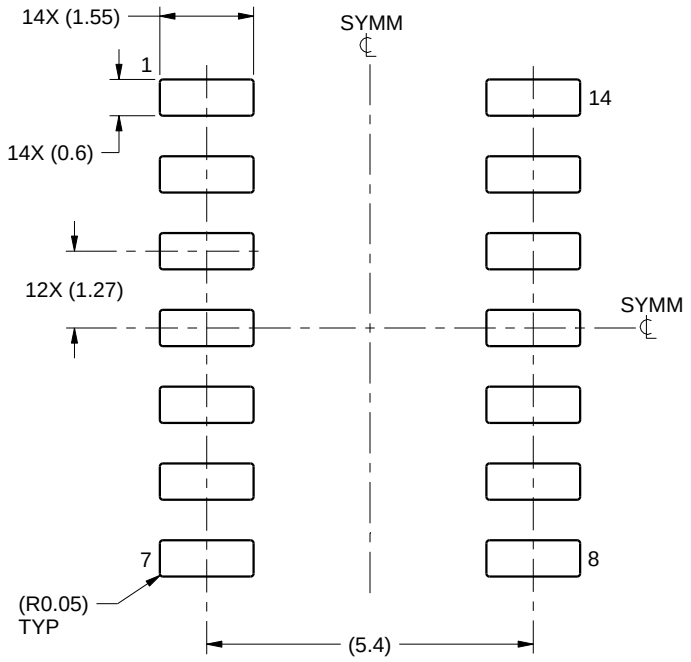
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2825DR	SOIC	D	8	3000	353.0	353.0	32.0
TLV4825DR	SOIC	D	14	3000	340.5	336.1	32.0
TLV4825PWR	TSSOP	PW	14	3000	353.0	353.0	32.0

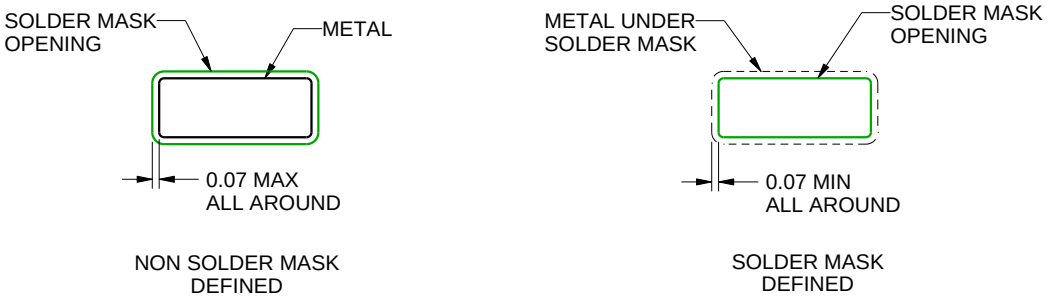


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X

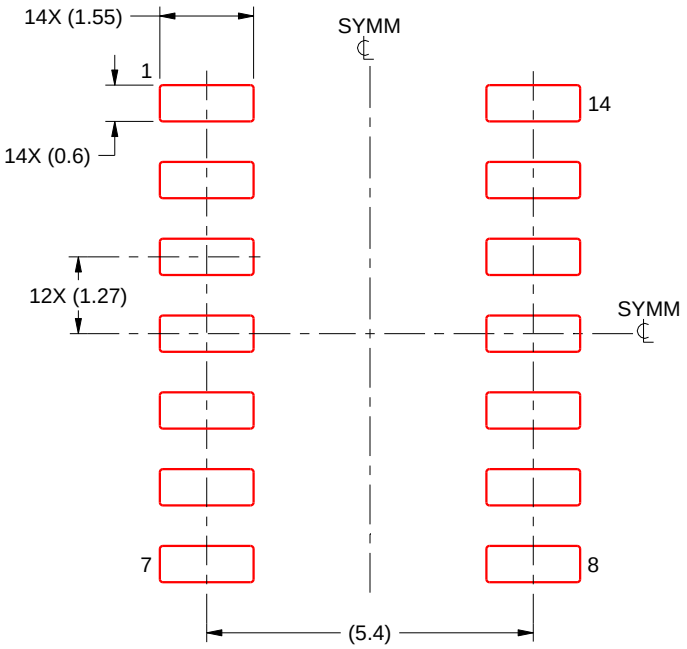


SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

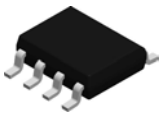


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

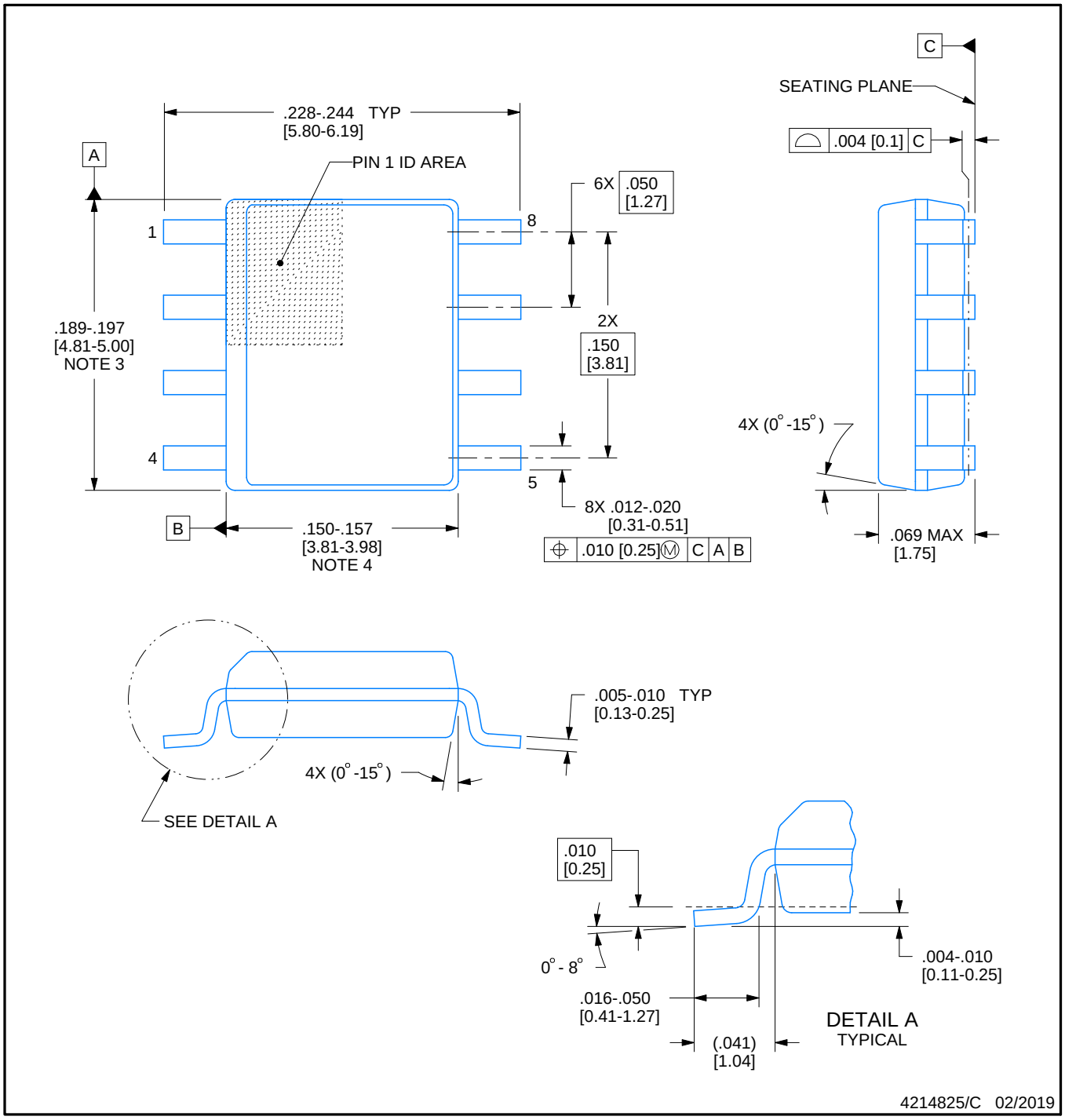


PACKAGE OUTLINE

D0008A

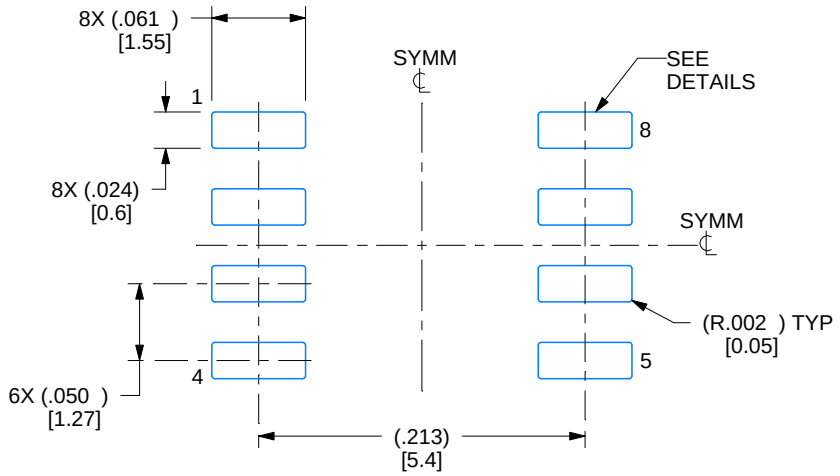
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

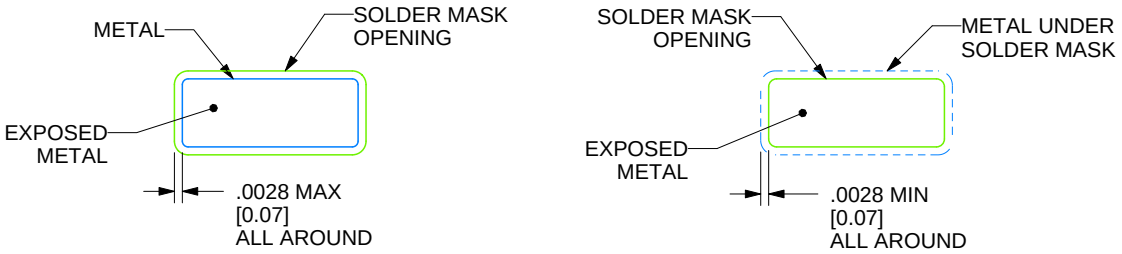


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

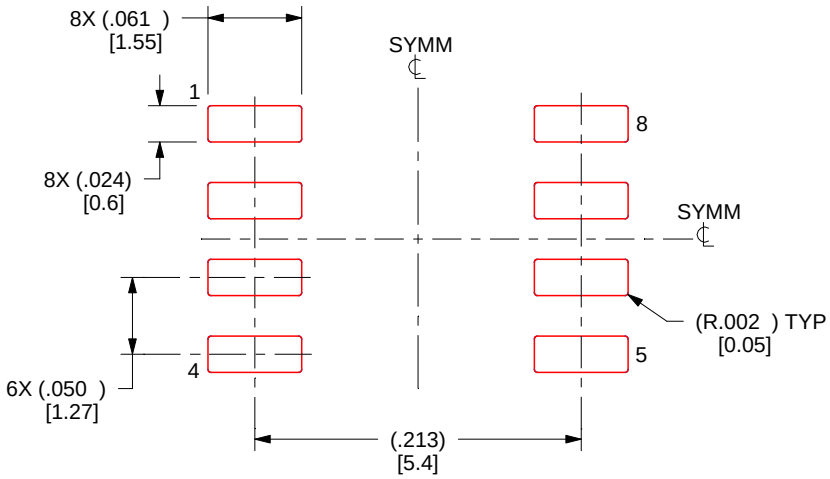


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



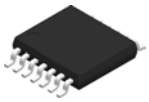
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

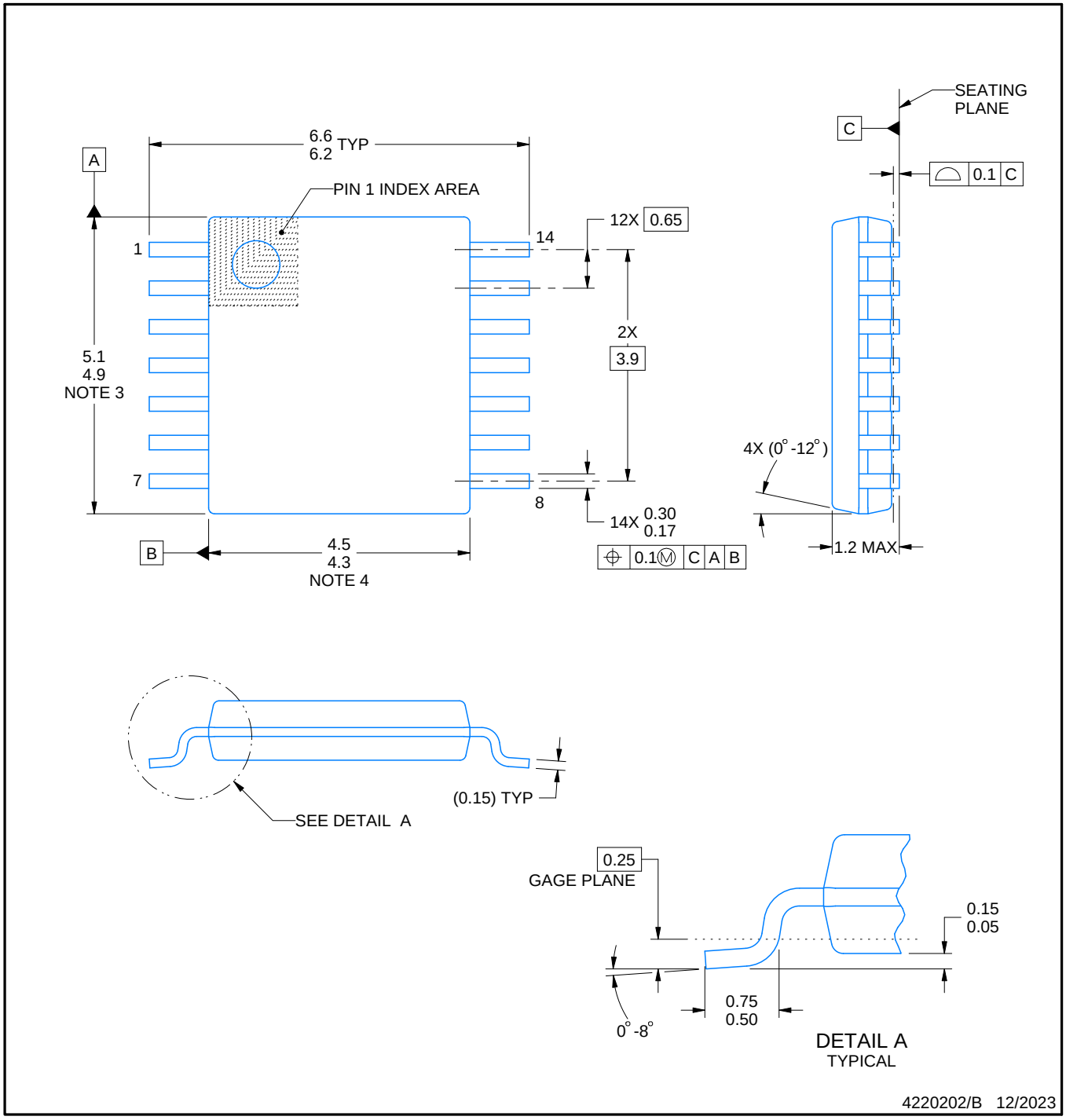
PW0014A



PACKAGE OUTLINE

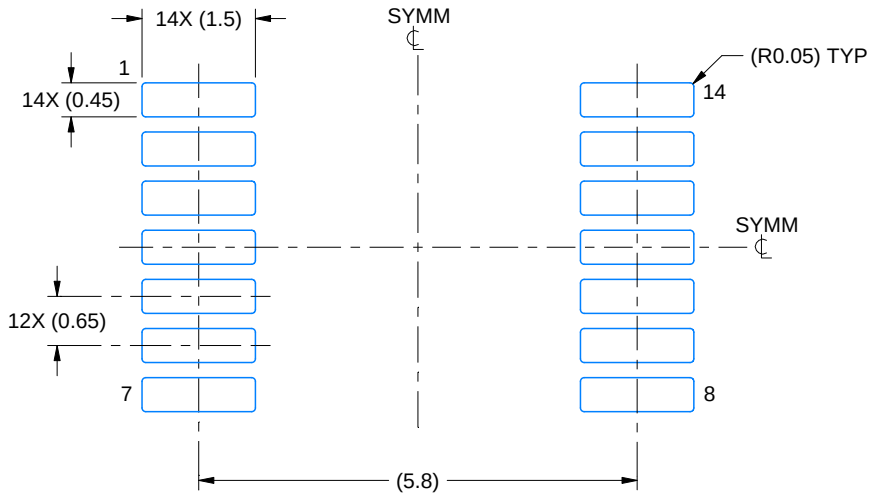
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

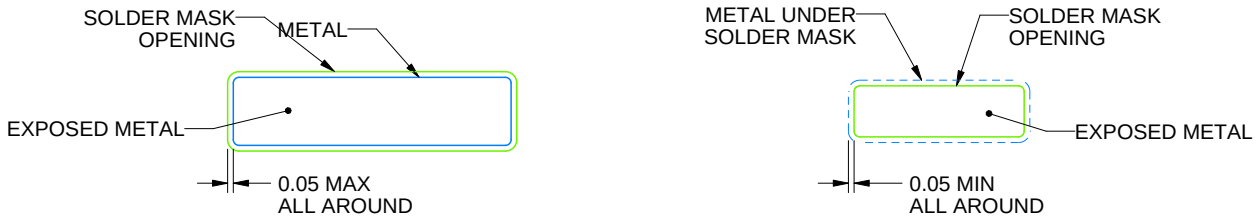


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

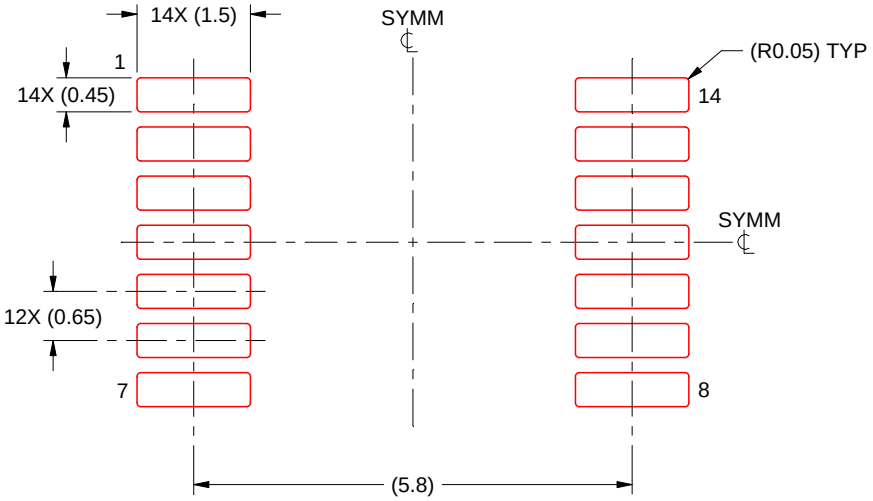
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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