2.7V TO 5.5V LOW-POWER DUAL 10-BIT DIGITAL-TO-ANALOG CONVERTER WITH INTERNAL REFERENCE AND POWER DOWN

FEATURES

- Dual 10-Bit Voltage Output DAC
- Programmable Internal Reference
- Programmable Settling Time:
  - 0.8μs in Fast Mode
  - 2.8μs in Slow Mode
- Compatible With TMS320 and SPI™ Serial Ports
- Differential Nonlinearity <0.1LSB Typ
- Monotonic Over Temperature

APPLICATIONS

- Digital Servo Control Loops
- Digital Offset and Gain Adjustment
- Industrial Process Control
- Machine and Motion Control Devices
- Mass Storage Devices

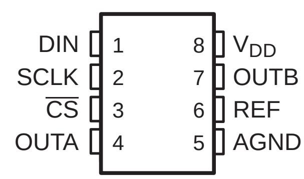
DESCRIPTION

The TLV5637 is a dual 10-bit voltage output DAC with a flexible 3-wire serial interface. The serial interface allows glueless interface to TMS320 and SPI™, QSPI™, and Microwire™ serial ports. It is programmed with a 16-bit serial string containing 2 control and 10 data bits.

The resistor string output voltage is buffered by a x2 gain rail-to-rail output buffer. The buffer features a Class AB output stage to improve stability and reduce settling time. The programmable settling time of the DAC allows the designer to optimize speed versus power dissipation. With its on-chip programmable precision voltage reference, the TLV5637 simplifies overall system design.

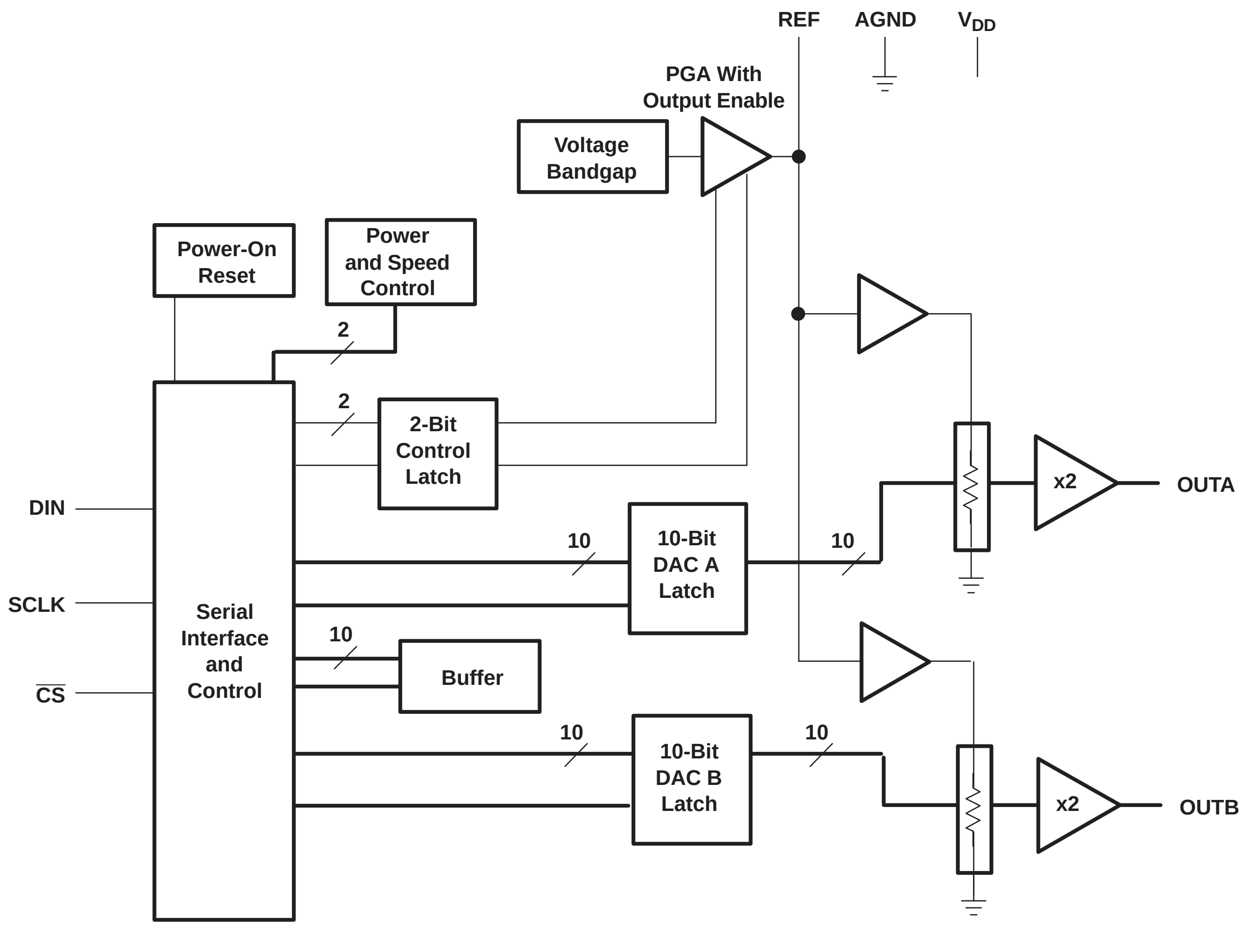
Because of its ability to source up to 1mA, the reference can also be used as a system reference. Implemented with a CMOS process, the device is designed for single supply operation from 2.7V to 5.5V. It is available in an 8-pin SOIC package to reduce board space in standard commercial and industrial temperature ranges.

D PACKAGE
(TOP VIEW)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O/P	DESCRIPTION
AGND	5	P	Ground
$\overline{CS}$	3	I	Chip select. Digital input active low, used to enable/disable inputs
DIN	1	I	Digital serial data input
OUTA	4	I	DAC A analog voltage output
OUTB	7	O	DAC B analog voltage output
REF	6	I/O	Analog reference voltage input/output
SCLK	2	I	Digital serial clock input
V_{DD}	8	P	Positive power supply

ABSOLUTE MAXIMUM RATINGS[1]

Over operating free-air temperature range (unless otherwise noted).

		UNIT
Supply voltage (V_{DD} to AGND)		7V
Reference input voltage range		–0.3 V to V_{DD} + 0.3V
Digital input voltage range		–0.3 V to V_{DD} + 0.3V
Operating free-air temperature range, T_A	TLV5637C	0°C to +70°C
	TLV5637I	–40°C to +85°C
Storage temperature range, T_{stg}		–65°C to +150°C
Lead temperature 1,6mm (1/16 inch) from case for 10 seconds		+260°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	V_{DD} = 5 V	4.5	5	5.5	V
	V_{DD} = 3 V	2.7	3	3.3	V
Power on threshold voltage, POR		0.55		2	V
High-level digital input voltage, V_{IH}	DV_{DD} = 2.7 V	2			V
	DV_{DD} = 5.5 V	2.4			
Low-level digital input voltage, V_{IL}	DV_{DD} = 2.7 V			0.6	V
	DV_{DD} = 5.5 V			1	
Reference voltage, V_{ref} to REF terminal	V_{DD} = 5 V (see [1])	AGND	2.048	V_{DD}–1.5	V
Reference voltage, V_{ref} to REF terminal	V_{DD} = 3 V (see [1])	AGND	1.024	V_{DD}–1.5	V
Load resistance, R_L		2			kΩ
Load capacitance, C_L				100	pF
Clock frequency, f_{CLK}				20	MHz
Operating free-air temperature, T_A	TLV5637C	0		+70	°C
	TLV5637I	–40		+85	

(1) Due to the x2 output buffer, a reference input voltage ≥ (V_{DD} - 0.4V)/2 causes clipping of the transfer function. The output buffer of the internal reference must be disabled, if an external reference is used.

ELECTRICAL CHARACTERISTICS

Over recommended operating conditions (unless otherwise noted).

POWER SUPPLY								
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{DD}	Power supply current	No load, All inputs = AGND or V_{DD}, DAC latch = 0x800	V_{DD} = 5V, Int. ref.	Fast		4.2	7	mA
				Slow		2	3.6	mA
			V_{DD} = 3V, Int. ref.	Fast		3.7	6.3	mA
				Slow		1.7	3.0	mA
			V_{DD} = 5V, Ext. ref.	Fast		3.8	6.3	mA
				Slow		1.7	3.0	mA
			V_{DD} = 3V, Ext. ref.	Fast		3.4	5.7	mA
				Slow		1.4	2.6	mA
	Power-down supply current					0.01	10	µA
PSRR	Power supply rejection ratio	Zero scale, See (1)				65		dB
		Full scale, See (2)				65		

(1) Power supply rejection ratio at zero scale is measured by varying V_{DD} and is given by: PSRR = 20 log [(E_{ZS}(V_{DD}max) – E_{ZS}(V_{DD}min))/V_{DD}max]
(2) Power supply rejection ratio at full scale is measured by varying V_{DD} and is given by: PSRR = 20 log [(E_G(V_{DD}max) – E_G(V_{DD}min))/V_{DD}max]

STATIC DAC SPECIFICATIONS						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		10			bits
INL	Integral nonlinearity, end point adjusted	See (1)		±0.4	±1	LSB
DNL	Differential nonlinearity	See (2)		±0.1	±0.5	LSB
E_{ZS}	Zero-scale error (offset error at zero scale)	See (3)			±24	mV
E_{ZS}TC	Zero-scale-error temperature coefficient	See (4)		10		ppm/°C
E_G	Gain error	See (5)			±0.6	% full scale V
E_GT_C	Gain error temperature coefficient	See (6)		10		ppm/°C
OUTPUT SPECIFICATIONS						
V_O	Output voltage	R_L = 10kΩ	0		V_{DD}–0.4	V
	Output load regulation accuracy	V_O= 4.096V, 2.048V, R_L= 2 kΩ			±0.25	% full scale V

(1) The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors. Tested from code 32 to 4095.
(2) The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
(3) Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
(4) Zero-scale-error temperature coefficient is given by: E_{ZS} TC = [E_{ZS} (T_{max}) – E_{ZS} (T_{min})]/V_{ref}× 10^6/(T_{max}– T_{min}).
(5) Gain error is the deviation from the ideal output (2V_{ref}– 1LSB) with an output load of 10 k excluding the effects of the zero-error.
(6) Gain temperature coefficient is given by: E_G TC = [E_G(T_{max}) – E_G (T_{min})]/V_{ref}× 10^6/(T_{max}– T_{min}).

ELECTRICAL CHARACTERISTICS (Continued)

over recommended operating conditions (unless otherwise noted)

REFERENCE PIN CONFIGURED AS OUTPUT (REF)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ref(OUTL)}$	Low reference voltage		1.003	1.024	1.045	V
$V_{ref(OUTH)}$	High reference voltage	V_{DD} > 4.75V	2.027	2.048	2.069	V
$I_{ref(source)}$	Output source current				1	mA
$I_{ref(sink)}$	Output sink current		1			mA
	Load capacitance				100	pF
PSRR	Power supply rejection ratio			65		dB

REFERENCE PIN CONFIGURED AS INPUT (REF)							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I	Input voltage			0		V_{DD}–1.5	V
R_I	Input resistance				10		MΩ
C_I	Input capacitance				5		pF
	Reference input bandwidth	REF = 0.2V_{PP} + 1.024V dc	Fast		1.3		MHz
			Slow		525		kHz
	Reference feedthrough	REF = 1V_{PP} at 1 kHz + 1.024V dc, See (1)			80		dB

(1) Reference feedthrough is measured at the DAC output with an input code = 0x000.

DIGITAL INPUTS						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current	$V_I = V_{DD}$			1	µA
I_{IL}	Low-level digital input current	V_I = 0V	1			µA
C_i	Input capacitance			8		pF

ELECTRICAL CHARACTAERISTICS (CONTINUED)

over recommended operating conditions (unless otherwise noted)

ANALOG OUTPUT DYNAMIC PERFORMANCE								
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{s(FS)}$	Output settling time, full scale	R_L = 10kΩ, C_L = 100pF,	See (1)	Fast		0.8	2.4	μs
				Slow		2.8	5.5	
$t_{s(CC)}$	Output settling time, code to code	R_L = 10kΩ, C_L = 100pF,	See (2)	Fast		0.4	1.2	μs
				Slow		0.8	1.6	
SR	Slew rate	R_L = 10kΩ, C_L = 100pF,	See (3)	Fast		12		V/μs
				Slow		1.8		
	Glitch energy	DIN = 0 to 1, f_{CLK} = 100kHz,	$\overline{CS}$ = V_{DD}			5		nV-S
SNR	Signal-to-noise ratio	f_s = 480kSPS, f_{out} = 1kHz, R_L = 10kΩ, C_L = 100pF			53	56		dB
S/(N+D)	Signal-to-noise + distortion				50	54		
THD	Total harmonic distortion					61	50	
SFDR	Spurious free dynamic range				51	62		

(1) Settling time is the time for the output signal to remain within ±0.5LSB of the final measured value for a digital input code change of 0x020 to 0xFDF or 0xFDF to 0x020 respectively. Not tested, assured by design.
(2) Settling time is the time for the output signal to remain within ± 0.5LSB of the final measured value for a digital input code change of one count. Not tested, assured by design.
(3) Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full-scale voltage.

DIGITAL INPUT TIMING REQUIREMENTS

		MIN	NOM	MAX	UNIT
$t_{su(CS-CK)}$	Setup time, $\overline{CS}$ low before first negative SCLK edge	10			ns
$t_{su(C16-CS)}$	Setup time, 16th negative SCLK edge (when D0 is sampled) before $\overline{CS}$ rising edge	10			ns
t_{wH}	SCLK pulse width high	25			ns
t_{wL}	SCLK pulse width low	25			ns
$t_{su(D)}$	Setup time, data ready before SCLK falling edge	10			ns
$t_{h(D)}$	Hold time, data held valid after SCLK falling edge	5			ns

PARAMETER MEASUREMENT INFORMATION

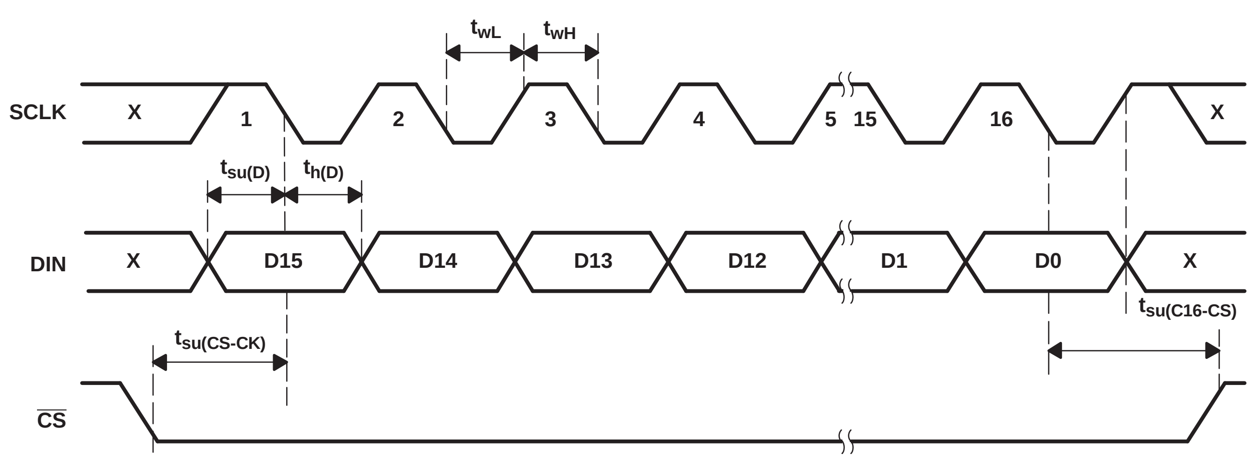


Figure 1. Timing Diagram

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

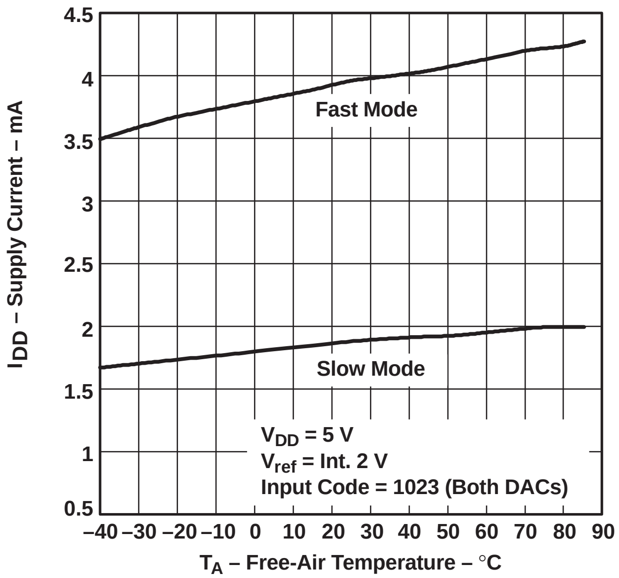


Figure 2.

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

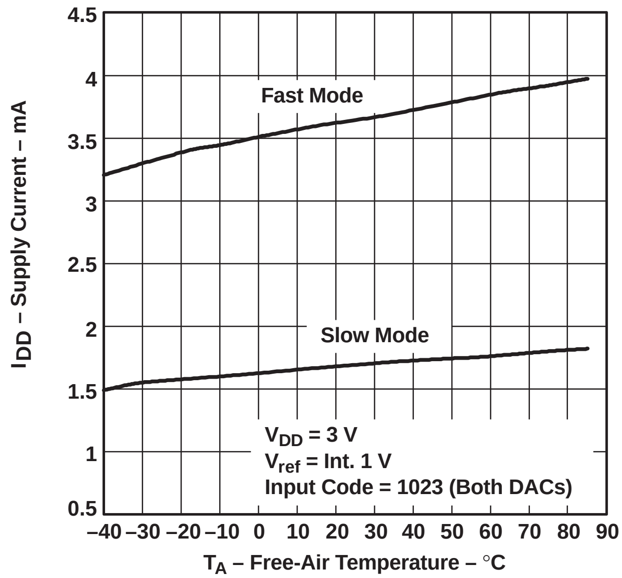


Figure 3.

POWER DOWN SUPPLY CURRENT
vs
TIME

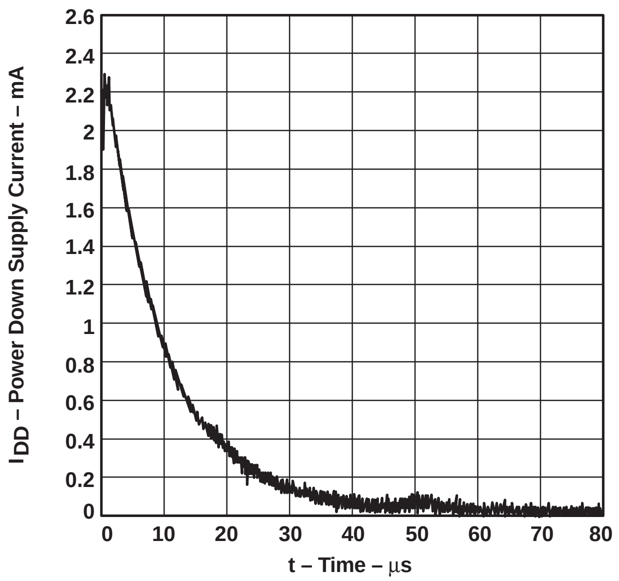


Figure 4.

OUTPUT VOLTAGE
vs
LOAD CURRENT

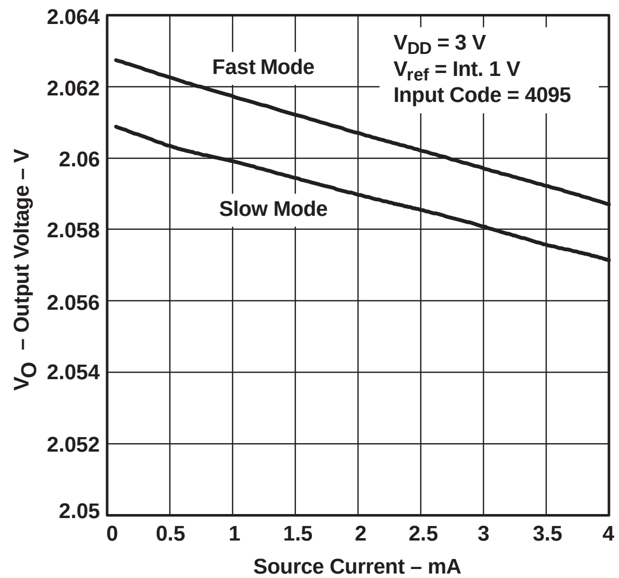


Figure 5.

TYPICAL CHARACTERISTICS (continued)

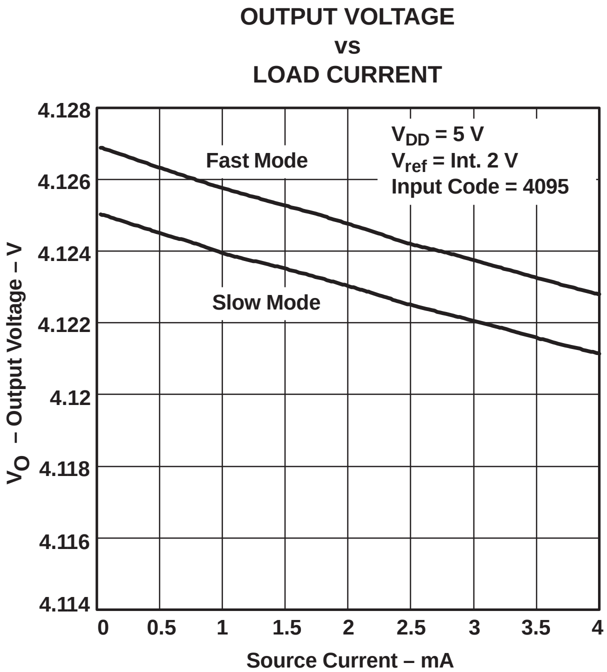


Figure 6.

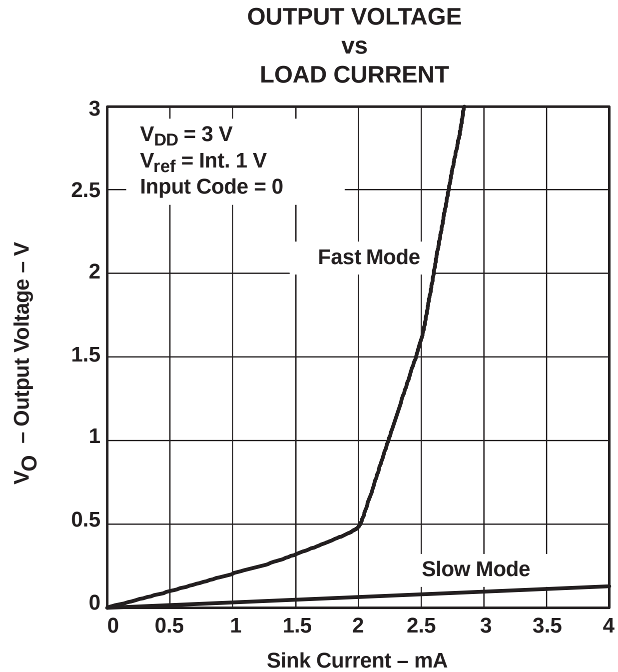


Figure 7.

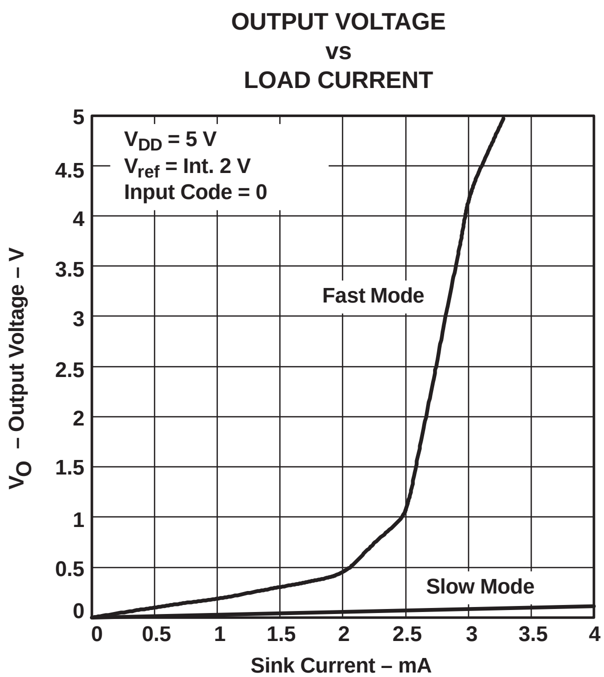


Figure 8.

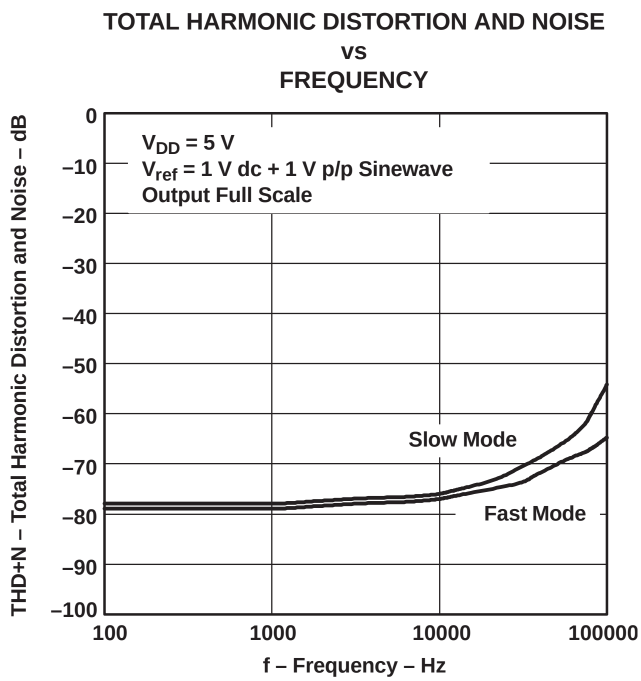


Figure 9.

TYPICAL CHARACTERISTICS (continued)

TOTAL HARMONIC DISTORTION vs FREQUENCY

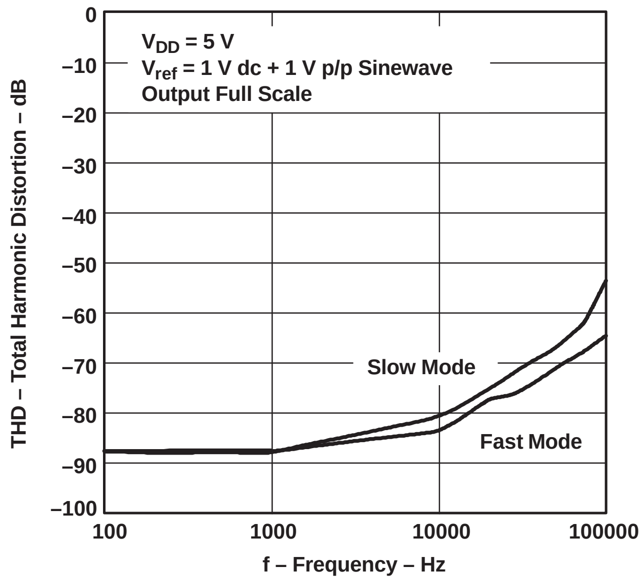


Figure 10.

INTEGRAL NONLINEARITY ERROR

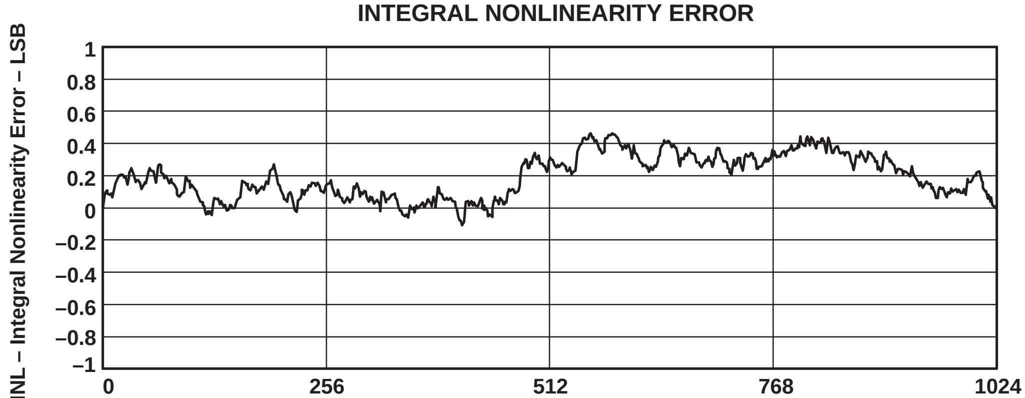


Figure 11.

DIFFERENTIAL NONLINEARITY ERROR

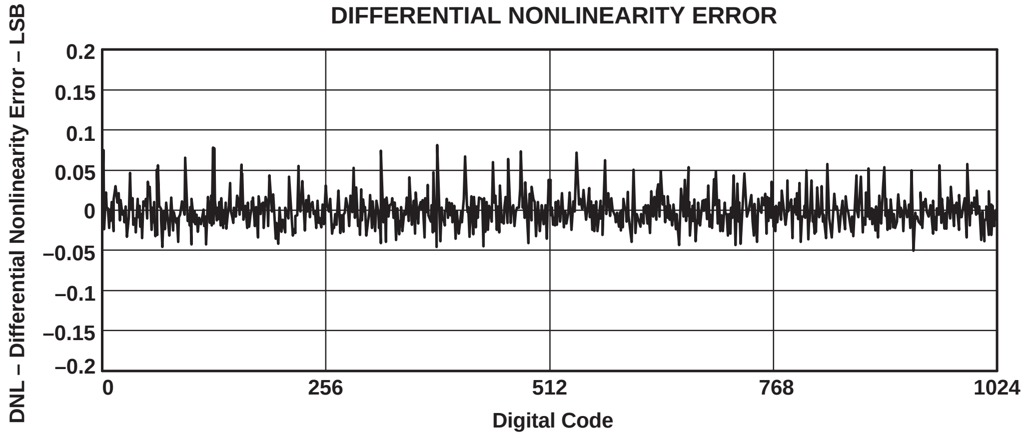


Figure 12.

APPLICATION INFORMATION

GENERAL FUNCTION

The TLV5637 is a dual 10-bit, single supply DAC, based on a resistor string architecture. It consists of a serial interface, a speed and power-down control logic, a programmable internal reference, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by reference) is given by:

$$2\ \mathrm{REF}\ \frac{\mathrm{CODE}}{0\mathrm{x}1000}\ [\mathrm{V}]$$

Where REF is the reference voltage and CODE is the digital input value in the range 0x000 to 0xFFF. Because it is a 10-bit DAC, only D11 to D2 are used. D0 and D1 are ignored. A power-on reset initially puts the internal latches to a defined state (all bits zero).

SERIAL INTERFACE

A falling edge of $\overline{\mathrm{CS}}$ starts shifting the data bit-per-bit (starting with the MSB) to the internal register on the falling edges of SCLK. After 16 bits have been transferred or $\overline{\mathrm{CS}}$ rises, the content of the shift register is moved to the target latches (DAC A, DAC B, BUFFER, CONTROL), depending on the control bits within the data word.

Figure 13 shows examples of how to connect the TLV5637 to TMS320, SPI, and Microwire.

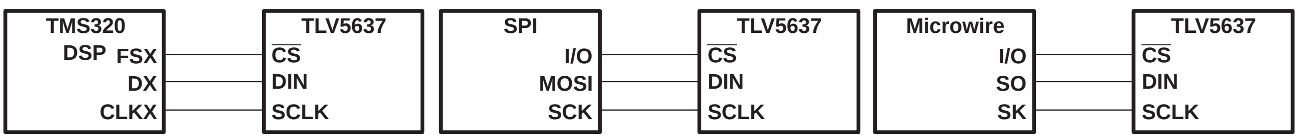


Figure 13. Three-Wire Interface

Notes on SPI and Microwire: Before the controller starts the data transfer, the software has to generate a falling edge on the I/O pin connected to $\overline{\mathrm{CS}}$. If the word width is 8 bits (SPI and Microwire), two write operations must be performed to program the TLV5637. After the write operation(s), the holding registers or the control register are updated automatically on the 16th positive clock edge.

SERIAL CLOCK FREQUENCY AND UPDATE RATE

The maximum serial clock frequency is given by:

$$f_{sclkmax} = \frac{1}{(t_{whmin} + t_{wlmin})} = 20\mathrm{MHz}$$

The maximum update rate is:

$$f_{updatemax} = \frac{1}{16\ (t_{whmin} + t_{wlmin})} = 1.25\mathrm{MHz}$$

Note that the maximum update rate is just a theoretical value for the serial interface, as the settling time of the TLV5637 has to be considered as well.

APPLICATION INFORMATION (continued)

DATA FORMAT

The 16-bit data word for the TLV5637 consists of two parts:

- Program bits (D15..D12)
- New data (D11..D0)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R1	SPD	PWR	R0	12 Data bits											

SPD: Speed control bit	1 → fast mode	0 → slow mode
PWR: Power control bit	1 → power down	0 → normal operation

The following table lists the possible combination of the register select bits:

Register Select Bits

R1	R0	REGISTER
0	0	Write data to DAC B and BUFFER
0	1	Write data to BUFFER
1	0	Write data to DAC A and update DAC B with BUFFER content
1	1	Write data to control register

The meaning of the 12 data bits depends on the register. If one of the DAC registers or the BUFFER is selected, then the 12 data bits determine the new DAC value:

Data Bits: DAC A, DAC B and BUFFER

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
New DAC Value										0	0

If control is selected, then D1, D0 of the 12 data bits are used to program the reference voltage:

Data Bits: CONTROL

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	REF1	REF0
X: don't care											

REF1 and REF0 determine the reference source and, if internal reference is selected, the reference voltage.

APPLICATION INFORMATION

REFERENCE BITS

REF1	REF0	REFERENCE
0	0	External
0	1	1.024V
1	0	2.048V
1	1	External

CAUTION:

If external refeence voltage is applied to the REF pin, external reference MUST be selected.

EXAMPLES OF OPERATION:

1. Set DAC A output, select fast mode, select internal reference at 2.048V:

a. Set reference voltage to 2.048V (CONTROL register)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0

b. Write new DAC A value and update DAC A output:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	New DAC A output value										0	0

The DAC A output is updated on the rising clock edge after D0 is sampled.

To output data consecutively using the same DAC configuration, it is not necessary to program the CONTROL register again.

2. Set DAC B output, select fast mode, select external reference:

a. Select external reference (CONTROL register):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0

b. Write new DAC B value to BUFFER and update DAC B output:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	New BUFFER content and DAC B output value										0	0

The DAC A output is updated on the rising clock edge after D0 is sampled.

To output data consecutively using the same DAC configuration, it is not necessary to program the CONTROL register again.

1. Set DAC A value, set DAC B value, update both simultaneously, select slow mode, select internal reference at 1.024V:

a. Set reference voltage to 1.024V (CONTROL register):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1

b. Write data for DAC B to BUFFER:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	New DAC B value										0	0

c. Write new DAC A value and update DAC A and B simultaneously:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	New DAC A value										0	0

Both outputs are updated on the rising clock edge after D0 from the DAC A data word is sampled.

2. Set power down mode:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X
X = Don't care															

LINEARITY, OFFSET, AND GAIN ERROR USING SINGLE ENDED SUPPLIES

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset, the output voltage may not change with the first code, depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0V.

The output voltage then remains at zero until the input code value produces a sufficiently positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 14.

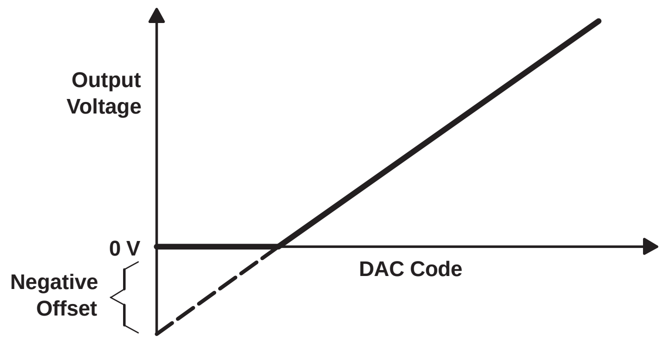


Figure 14. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage.

DEFINITIONS OF SPECIFICATIONS AND TERMINOLOGY

Integral Nonlinearity (INL)

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

Differential Nonlinearity (DNL)

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

Zero-Scale Error (E_{ZS})

Zero-scale error is defined as the deviation of the output from 0V at a digital input value of 0.

GAIN ERROR (E_G)

Gain error is the error in slope of the DAC transfer function.

SIGNAL-TO-NOISE RATIO + DISTORTION (S/N+D)

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

Spurious free dynamic range is the difference between the rms value of the output signal and the rms value of the spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from B Revision (January 2004) to C Revision	Page
• Changed —moved package option table from front page.	3

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV5637CD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	5637C
TLV5637CD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	5637C
TLV5637CDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	5637C
TLV5637CDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	5637C
TLV5637ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5637I
TLV5637ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5637I
TLV5637IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5637I
TLV5637IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	5637I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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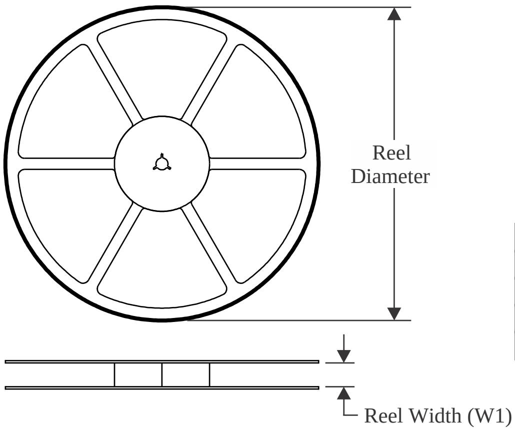
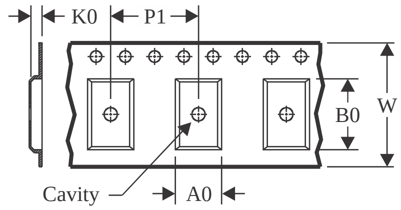
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

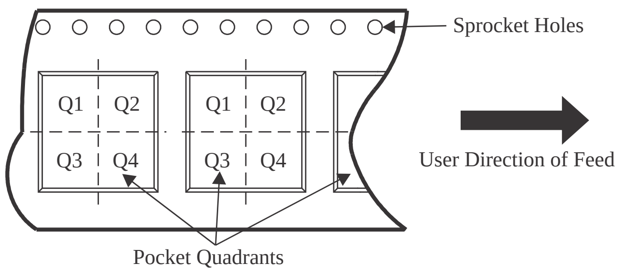


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

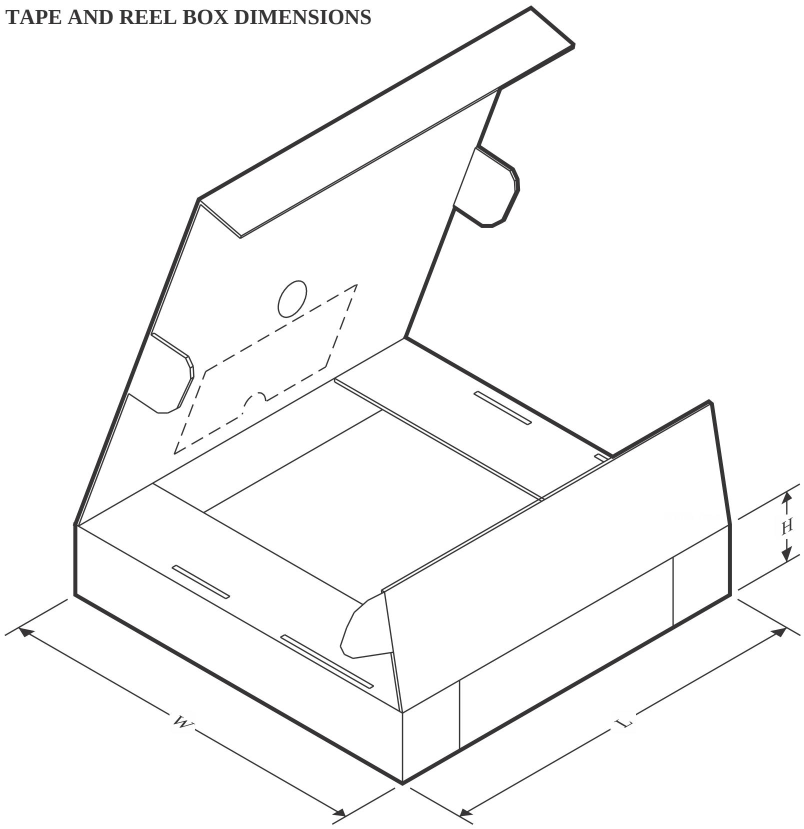
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV5637CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV5637IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

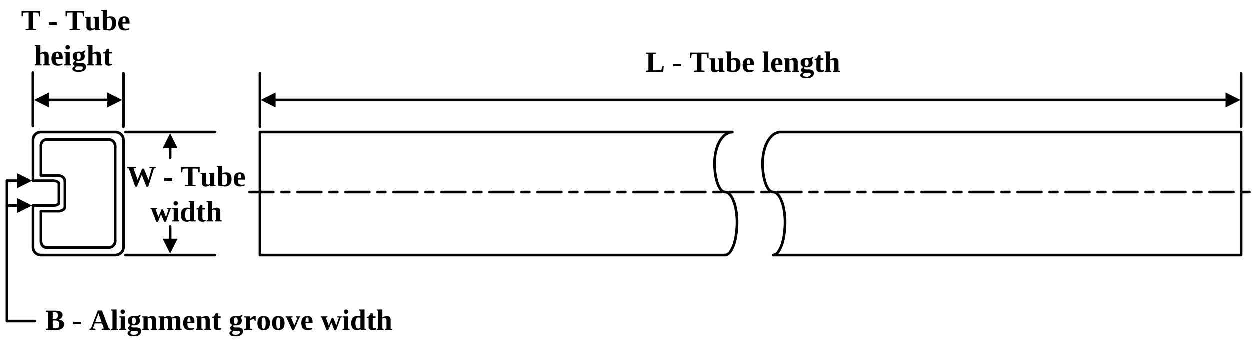
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

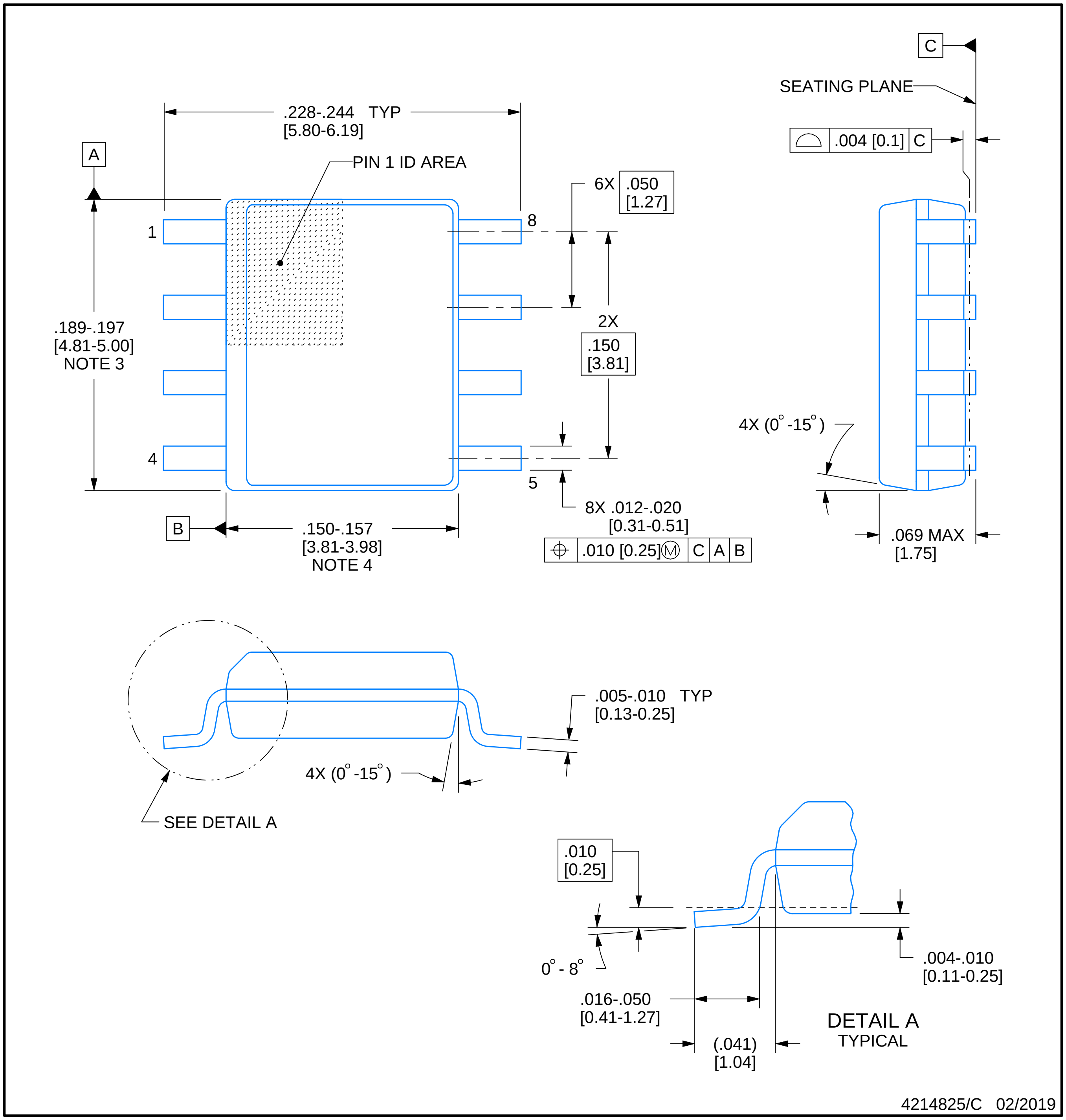
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV5637CDR	SOIC	D	8	2500	350.0	350.0	43.0
TLV5637IDR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



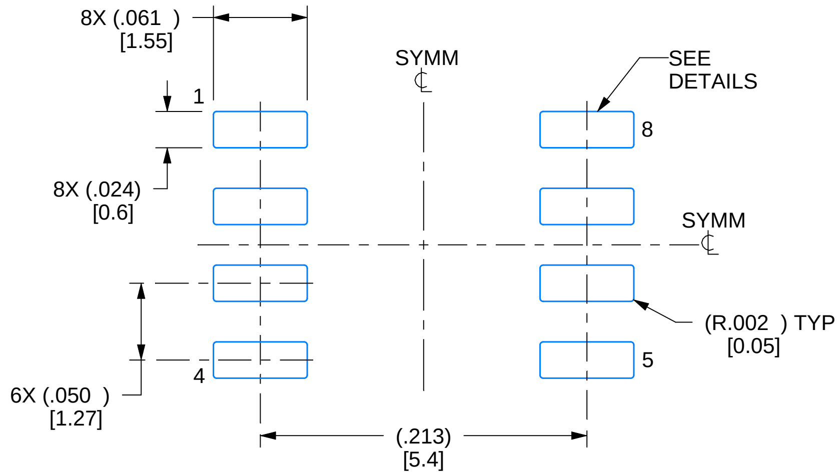
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV5637CD	D	SOIC	8	75	505.46	6.76	3810	4
TLV5637CD.A	D	SOIC	8	75	505.46	6.76	3810	4
TLV5637ID	D	SOIC	8	75	505.46	6.76	3810	4
TLV5637ID.A	D	SOIC	8	75	505.46	6.76	3810	4

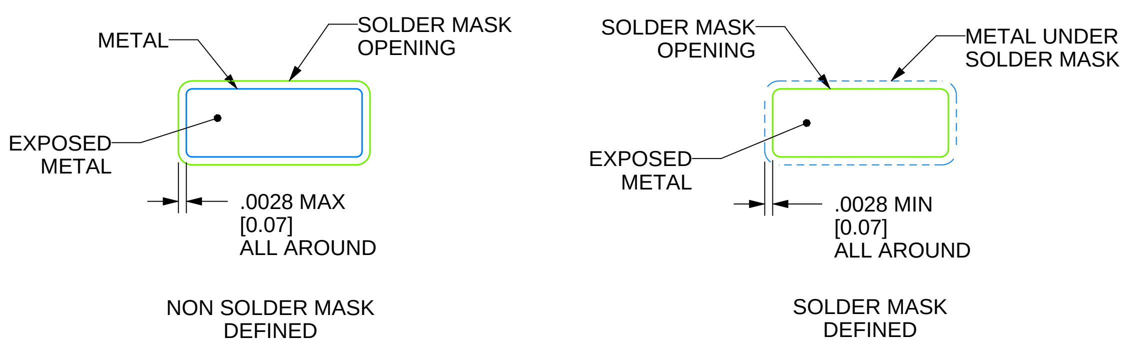


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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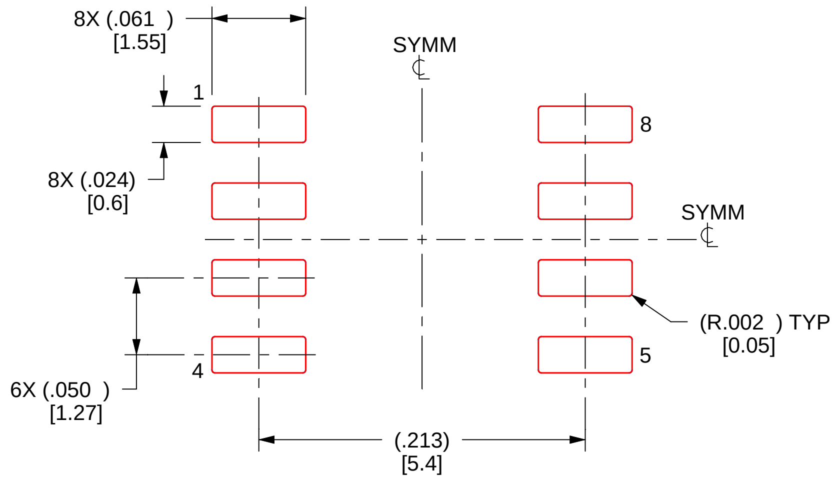
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.