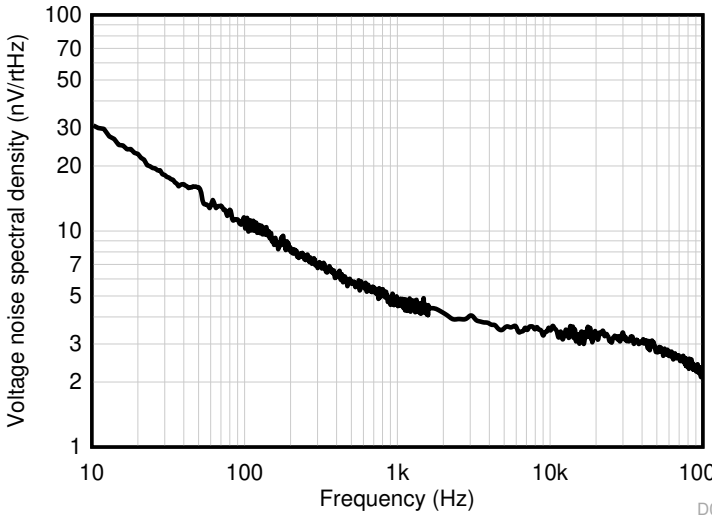
TLV6741, TLV6742, TLV6744 10-MHz, Low Broadband Noise, RRO, Operational Amplifier

1 Features

- Low broadband noise: 3.5 nV/√Hz
- Gain bandwidth: 10 MHz
- Low input bias current: ±3 pA
- Low offset voltage: 0.15 mV
- Low offset voltage drift: ±0.2 µV/°C
- Rail-to-rail output
- Unity-gain stable
- Low I_Q:
  - TLV6741: 890 µA/ch
  - TLV6742/4: 990 µA/ch
- Wide supply range:
  - TLV6741: 2.25 V to 5.5 V
  - TLV6742/4: 1.7 V to 5.5 V
- Robust EMIRR performance: 71 dB at 2.4 GHz

2 Applications

- Solid state drive
- Wearables (non-medical)
- Professional audio amplifier (rack mount)
- Transimpedance Amplifier Circuit
- Test and measurement
- Motor drives
- Pressure transmitter
- Lab and field instrumentation
- Bridge amplifier circuit
- Gaming applications



Noise Spectral Density vs Frequency

3 Description

The TLV674x family includes single (TLV6741), dual (TLV6742), and quad-channel (TLV6744) general-purpose CMOS operational amplifiers (op amp) that provide a low noise figure of 3.5 nV/√Hz and a wide bandwidth of 10 MHz. The low noise and wide bandwidth make the TLV674x family of devices attractive for a variety of precision applications that require a good balance between cost and performance. Additionally, the input bias current of the TLV674x family supports applications with high source impedance.

The robust design of the TLV674x family provides ease-of-use to the circuit designer due to its unity-gain stability, integrated RFI/EMI rejection filter, no phase reversal in overdrive conditions and high electrostatic discharge (ESD) protection (2-kV HBM). Additionally, the resistive open-loop output impedance makes them easy to stabilize with much higher capacitive loads.

This op amp family is optimized for low-voltage operation as low as 2.25 V (±1.125 V) for the TLV6741 and 1.7 V (±0.85 V) for the TLV6742 and TLV6744. All of the devices operate up to 5.5 V (±2.75 V), and are specified over the temperature range of –40°C to 125°C.

The single-channel TLV6741 is available in a small-size SC70-5 package. The dual-channel TLV6742 is available in multiple package options including a tiny 1.5 mm × 2.0 mm X2QFN package.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
TLV6741	SC70 (5)	1.25 mm × 2.00 mm
TLV6742	SOIC (8)	3.91 mm × 4.90 mm
	TSSOP (8)	3.00 mm × 4.40 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	SOT-23 (8)	1.60 mm × 2.90 mm
	WSON (8)	2.00 mm × 2.00 mm
TLV6742S	X2QFN (10)	1.50 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (February 2021) to Revision I (August 2021) — **Page**

- Removed preview tag from TLV6742 VSSOP in *Device Information* section....1
- Removed preview tag to VSSOP (DGK) in *Device Comparison Table* section....4

Changes from Revision G (April 2020) to Revision H (February 2021) — **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document....1
- Removed preview tag from TLV6742S X2QFN in *Device Information* section....1
- Removed preview note from X2QFN for TLV6742S in *Pin Configuration and Functions* section....5
- Removed Table of TLV6741 Graphs and Table of TLV6742 Graphs tables from the *Specifications* section....12
- Removed *Related Links* section from the *Device and Documentation Support* section....39

Changes from Revision F (January 2020) to Revision G (April 2020) — **Page**

- Added end equipment links in *Application* section....1
- Deleted preview tags for TSSOP, SOT-23, WSON, and X2QFN packages in *Device Information* section....1
- Deleted VSSOP (8) package in *Device Information* section....1
- Added preview tag to TLV6742S X2QFN in *Device Information* section....1
- Deleted VSSOP (DGK) in *Device Comparison Table* section....4
- Added preview tag to X2QFN (RUG) in *Device Comparison Table* section....4
- Deleted DGK package in pinout drawing for TLV6742 package in *Pin Configuration and Functions* section....5
- Deleted DGK VSSOP in *Thermal Information for Dual Channel* section....7
- Added shutdown electrical characteristic information....9
- Deleted example layout for VSSOP-8 (DGK) package in *Layout Example* section....37

Changes from Revision E (December 2019) to Revision F (January 2020) — **Page**

- Deleted TLV6744 product folder link from the data sheet page header....1

Changes from Revision D (January 2019) to Revision E (December 2019) **Page**

- Added I_Q definition for TLV6742 and TLV744 in *Features* section....1
- Added EMIRR, Supply Range, I_Q, and Offset Voltage Drift to *Features* section.... 1
- Changed Noise Spectral Density vs Frequency plot on front page to the TLV6742 and TLV6744 noise plot.... 1
- Changed wording of *Description* section to incorporate release of TLV6742 and TLV6744 devices 1
- Changed TLV6742 packages in *Device Information* 1
- Added *Device Comparison Table* section....4
- Added note regarding single supply operation to Pin Functions: TLV6741 table.... 5
- Added pin out drawings for TLV6742 packages in *Pin Configuration and Functions* section....5
- Added pin functions for TLV6742 packages.... 5
- Added X2QFN Package Drawing and Pin Functions for TLV6742S in *Pin Configuration and Functions* section 5
- Added TLV6742 typical characteristic graphs in the *Specifications* section.... 12
- Changed wording throughout *Detailed Description* section to incorporate addition of TLV6742 and TLV6744 devices....26
- Added *EMI Rejection* section with description information to *Detailed Description* section.... 27
- Added *Electrical Overstress* section and diagram to *Detailed Description* section.... 28
- Added *Typical Specification and Distributions* section to *Detailed Description* section.... 29
- Added *Shutdown Function* section with description for TLV6742S to *Detailed Description* section....30
- Added *Packages With an Exposed Thermal Pad* section to *Detailed Description* section....30
- Changed wording in *Application and Implementation* section to include the addition of TLV6742 and TLV6744 32
- Added TLV6742 and TLV6744 information to *Power Supply Recommendations* section.... 35
- Added dual channel layout example in the *Layout* section....37

Changes from Revision C (October 2017) to Revision D (January 2019) **Page**

- Changed Operating temperature from 125 to 150 in *Absolute Maximum Ratings* 7
- Added Junction temperature spec to *Absolute Maximum Ratings* 7

Changes from Revision B (October 2017) to Revision C (October 2017) **Page**

- Added test conditions to input offset voltage parameter in *Electrical Characteristics* table....9
- Changed typical input current noise density value from 2 fA√HZ to 23 fA√Hz.... 9
- Changed total supply voltage total from 5V to 5.5V in *Electrical Characteristics* condition statement.... 9
- Deleted "Vs = 2.25 V to 5.5 V" test conditions for common-mode rejection ratio parameter in *Electrical Characteristics* 9
- Deleted "C_L = 0" test condition from Figure 7-25 and Figure 7-26, Figure 7-27 and Figure 7-28 12
- Changed voltage step from 5 V to 2 V in Figure 7-32 12

Changes from Revision A (September 2017) to Revision B (October 2017) **Page**

- Changed Human-body model (HBM) value from: ±1000 to ±3000 and Charged-device mode (CDM) value from ±250 to ±1000....7

Changes from Revision * (June 2017) to Revision A (September 2017) **Page**

- Changed device document status from: Advance Information to: Production Data.... 1

5 Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE LEADS						
		SOIC D	SC-70 DCK	VSSOP DGK	WSON DSG	TSSOP PW	SOT-23 DDF	X2QFN RUG
TLV6741	1	—	5	—	—	—	—	—
TLV6742	2	8	—	8	8	8	8	—
TLV6742S		—	—	—	—	—	—	10

6 Pin Configuration and Functions

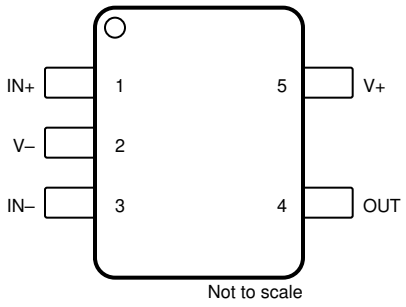


Figure 6-1. TLV6741 DCK Package
5-Pin SC70
Top View

Table 6-1. Pin Functions: TLV6741

PIN		I/O	DESCRIPTION
NAME	NO.		
IN+	1	I	Noninverting input
IN–	3	I	Inverting input
OUT	4	O	Output
V+	5	—	Positive (highest) supply
V–	2	—	Negative (lowest) supply or ground (for single-supply operation)

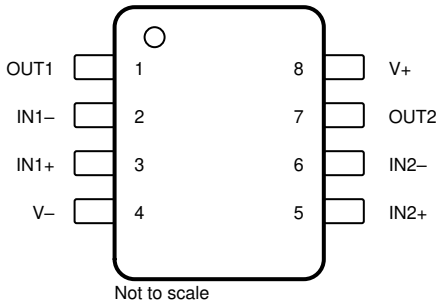
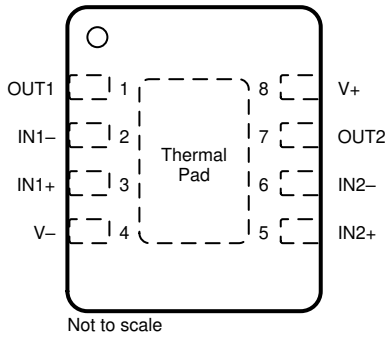


Figure 6-2. TLV6742 D, DGK, PW, and DDF Package
8-Pin SOIC, VSSOP, TSSOP, and SOT-23
Top View



Connect thermal pad to V–. See Section 8.3.8 for more information.

Figure 6-3. TLV6742 DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View

Table 6-2. Pin Functions: TLV6742

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2

Table 6-2. Pin Functions: TLV6742 (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
V–	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	—	Positive (highest) supply

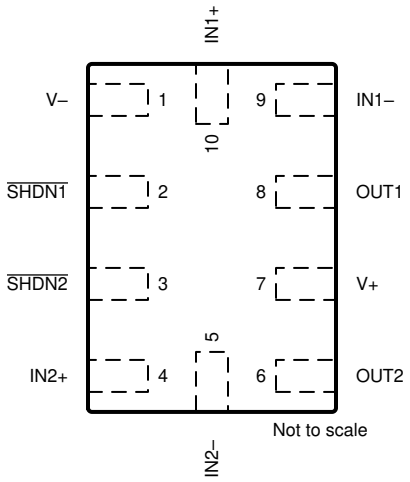


Figure 6-4. TLV6742S RUG Package
10-Pin X2QFN
Top View

Table 6-3. Pin Functions: TLV6742S

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	9	I	Inverting input, channel 1
IN1+	10	I	Noninverting input, channel 1
IN2–	5	I	Inverting input, channel 2
IN2+	4	I	Noninverting input, channel 2
OUT1	8	O	Output, channel 1
OUT2	6	O	Output, channel 2
$\overline{\text{SHDN1}}$	2	I	Shutdown: low = amp disabled, high = amp enabled. Channel 1. See Section 8.3.7 for more information.
$\overline{\text{SHDN2}}$	3	I	Shutdown: low = amp disabled, high = amp enabled. Channel 2. See Section 8.3.7 for more information.
V–	1	I or —	Negative (lowest) supply or ground (for single-supply operation)
V+	7	I	Positive (highest) supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	6	V
Signal input pins	Common-mode voltage (3)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage (3) (4)		V_S + 0.2	V
	Current (3)	–10	10	mA
Output short-circuit (2)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operating the device beyond the ratings listed under *Absolute Maximum Ratings* will cause permanent damage to the device. These are stress ratings only, based on process and design limitations, and this device has not been designed to function outside the conditions indicated under *Recommended Operating Conditions*. Exposure to any condition outside *Recommended Operating Conditions* for extended periods, including absolute-maximum-rated conditions, may affect device reliability and performance.
(2) Short-circuit to ground, one amplifier per package.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(4) Differential input voltages greater than 0.25 V applied continuously can result in a shift to the input offset voltage above the maximum specification of this parameter. The magnitude of this effect increases as the ambient operating temperature rises.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	**TLV6741:** Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±3000	V
		TLV6742: Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	
		All Devices: Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–) , for TLV6742 and TLV6744	1.7(1)	5.5	V
V_S	Supply voltage, (V+) – (V–), for TLV6741 only	2.25	5.5	V
V_I	Input voltage range	(V–)	(V+) – 1.2	V
T_A	Specified temperature	–40	125	°C

(1) Operation between 1.7V and 1.8V is only recommened for T_A = 0 - 85 ℃

7.4 Thermal Information for Single Channel

THERMAL METRIC (1)		TLV6741 DCK (SC70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	240.9	℃/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	151.7	℃/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64	℃/W
ψ_{JT}	Junction-to-top characterization parameter	34.8	℃/W
ψ_{JB}	Junction-to-board characterization parameter	63.3	℃/W

7.4 Thermal Information for Single Channel (continued)

THERMAL METRIC (1)		TLV6741	UNIT
		DCK (SC70)	
		5 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report SPRA953C.

7.5 Thermal Information for Dual Channel

THERMAL METRIC (1)		TLV6742, TLV6742S						UNIT
		D (SOIC)	DDF (SOT-23-8)	DSG (WSON)	PW (TSSOP)	DGK (VSSOP)	RUG (X2QFN)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	131.1	153.8	78.2	185.6	177.0	140.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.2	80.2	97.5	74.5	68.6	52.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	74.5	73.1	44.6	116.3	98.7	69.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	24.4	6.6	4.7	12.6	12.4	1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	73.3	72.7	44.6	114.6	97.1	67.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	19.8	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953C.

7.6 Electrical Characteristics

TLV6742/4 Specifications: V_S = (V+) – (V–) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.
TLV6741 Specifications: V_S = (V+) – (V–) = 5.5 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
OFFSET VOLTAGE								
V_{OS}	Input offset voltage	V_S = 5.0 V				±0.15	±1.0	mV
			T_A = –40°C to 125°C	TLV6742/4(3)			±1.2	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to 125°C	TLV6741(2)		±0.35		µV/°C
				TLV6742/4(3)		±0.2		
PSRR	Input offset voltage versus power supply	V_{CM} = V–		TLV6741(2)		±0.32	±6.3	µV/V
		V_{CM} = V–		TLV6742/4(3)		±0.7	±5.8	
	Channel separation	f = 20 kHz				130		dB
INPUT BIAS CURRENT								
I_B	Input bias current			TLV6741(2)		±10		pA
				TLV6742/4(3)		±3		
I_{OS}	Input offset current			TLV6741(2)		±10		pA
				TLV6742/4(3)		±0.5		
NOISE								
E_N	Input voltage noise	f = 0.1 to 10 Hz				1.2		μV_{PP}
						0.227		μV_{RMS}
e_N	Input voltage noise density	f = 10 Hz		TLV6742/4(3)		30		nV/√Hz
		f = 1 kHz		TLV6741(2)		5.0		
				TLV6742/4(3)		4.6		
		f = 10 kHz		TLV6741(2)		3.7		
				TLV6742/4(3)		3.5		
i_N	Input current noise	f = 1 kHz				23		fA/√Hz
INPUT VOLTAGE RANGE								
V_{CM}	Common-mode voltage range				(V–)		(V+) -1.2	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 1.2 V		TLV6741(2)	95	120		dB
		V_S = 1.8 V, (V–) < V_{CM} < (V+) – 1.2 V		TLV6742/4(3)	87	100		
		V_S = 5.5, (V–) < V_{CM} < (V+) – 1.2 V			94	110		
INPUT CAPACITANCE								
Z_{ID}	Differential					10 || 6		MΩ || pF
Z_{ICM}	Common-mode					10 || 6		GΩ || pF
OPEN-LOOP GAIN								
A_{OL}	Open-loop voltage gain	(V–) + 40 mV < V_O < (V+) – 40 mV, R_L = 10 kΩ to V_S/2		TLV6741(2)		125		dB
		(V–) + 150 mV < V_O < (V+) – 150 mV, R_L = 2 kΩ to V_S/2			110	130		
		V_S= 1.8 V, (V–) + 150 mV < V_O < (V+) – 150 mV, R_L = 2 kΩ to V_S/2		TLV6742/4(3)	107	120		
		V_S= 5.5 V, (V–) + 150 mV < V_O < (V+) – 150 mV, R_L = 2 kΩ to V_S/2				140		
		V_S = 1.8 V, (V–) + 40m V < V_O < (V+) – 40 mV, R_L = 10 kΩ to V_S/2			110	120		
		V_S = 5.5 V, (V–) + 40m V < V_O < (V+) – 40 mV, R_L = 10 kΩ to V_S/2				140		

7.6 Electrical Characteristics (continued)

TLV6742/4 Specifications: V_S = (V+) – (V–) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.
TLV6741 Specifications: V_S = (V+) – (V–) = 5.5 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE								
GBW	Gain-bandwidth product					10		MHz
SR	Slew rate	V_S = 5.5 V, G = +1, C_L = 20 pF				4.5		V/µs
t_S	Settling time	To 0.1%, V_S = 5.5 V, V_{STEP} = 2 V, G = +1, CL = 20pF				0.65		µs
		To 0.01%, V_S = 5.5 V, V_{STEP} = 2 V, G = +1, CL = 20pF				1.2		
	Phase margin	G = +1, R_L = 10kΩ, C_L = 20 pF				55		°
	Overload recovery time	V_{IN} × gain > V_S				0.2		µs
THD+N	Total harmonic distortion + noise	V_S = 5.5 V, V_{CM} = 2.5 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz, R_L = 10 kΩ		TLV6741[2]		0.00035%		
				TLV6742/4[3]		0.00015%		
EMIRR	Electro-magnetic interference rejection ratio	f = 1 GHz		TLV6742/4[3]		51		dB
OUTPUT								
	Voltage output swing from rail	Positive/Negative rail headroom	V_S = 5.5 V, R_L = 10k	TLV6741[2]		8	10	mV
		Positive rail headroom	V_S = 5.5 V, R_L = no load	TLV6742/4[3]			7	
			V_S = 5.5 V, R_L = 2 kΩ				35	
			V_S = 5.5 V, R_L = 10 kΩ			5	14	
		Negative rail headroom	V_S = 5.5 V, R_L = no load				7	
			V_S = 5.5 V, R_L = 2 kΩ				35	
			V_S = 5.5 V, R_L = 10 kΩ			5	14	
I_{SC}	Short-circuit current			TLV6742/4[3]		±68		mA
C_{LOAD}	Capacitive load drive					See Figure 7-58		
Z_O	Open-loop output impedance	f = 10 MHz, I_O = 0 A		TLV6741[2]		160		Ω
		f = 2 MHz, I_O = 0 A		TLV6742/4[3]		165		
POWER SUPPLY								
I_Q	Quiescent current per amplifier	V_S = 5.5 V, I_O = 0 A		TLV6741[2]		890		µA
			T_A = –40°C to 125°C				1100	
				TLV6742/4[3]		990	1200	
			T_A = –40°C to 125°C				1250	
	Turn-On Time	At T_A = 25°C, V_S = 5.5 V, V_S ramp rate > 0.3 V/µs		TLV6742/4[3]		10		µs

7.6 Electrical Characteristics (continued)

TLV6742/4 Specifications: V_S = (V+) – (V–) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.
TLV6741 Specifications: V_S = (V+) – (V–) = 5.5 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SHUTDOWN							
I_{QSD}	Quiescent current per amplifier	All amplifiers disabled, $\overline{SHDN}$ = V–			1	3.5	µA
Z_{SHDN}	Output impedance during shutdown	Amplifier disabled			10 || 6		GΩ || pF
V_{IH}	Logic high threshold voltage (amplifier enabled)			(V–) + 1.1 V			V
V_{IL}	Logic low threshold voltage (amplifier disabled)					(V–) + 0.2 V	
t_{ON}	Amplifier enable time (full shutdown) (1)	G = +1, V_{CM} = V-, V_O = 0.1 × V_S/2			15		µs
	Amplifier enable time (partial shutdown)(1)	G = +1, V_{CM} = V-, V_O = 0.1 × V_S/2			8		
t_{OFF}	Amplifier disable time (1)	V_{CM} = V-, V_O = V_S/2			3		
	$\overline{SHDN}$ pin input bias current (per pin)	(V+) ≥ $\overline{SHDN}$ ≥ (V–) + 0.9 V			0.4		µA
		(V–) ≤ $\overline{SHDN}$ ≤ (V–) + 0.7 V			0.25		

(1) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.
(2) This electrical characteristic only applies to the single-channel, TLV6741
(3) This electrical characteristic only applies to the dual-channel TLV6742 and quad-channel TLV6744

7.7 TLV6741: Typical Characteristics

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

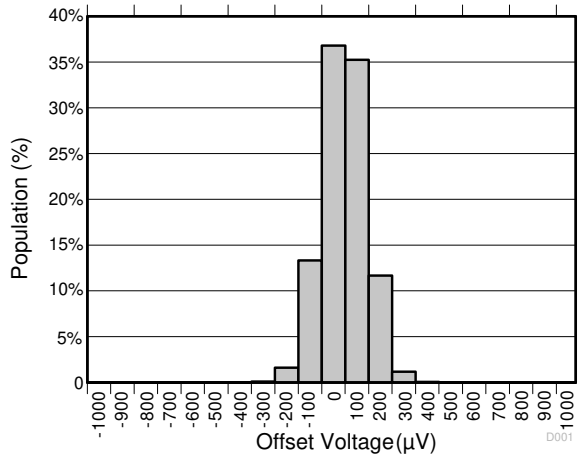


Figure 7-1. Offset Voltage Production Distribution

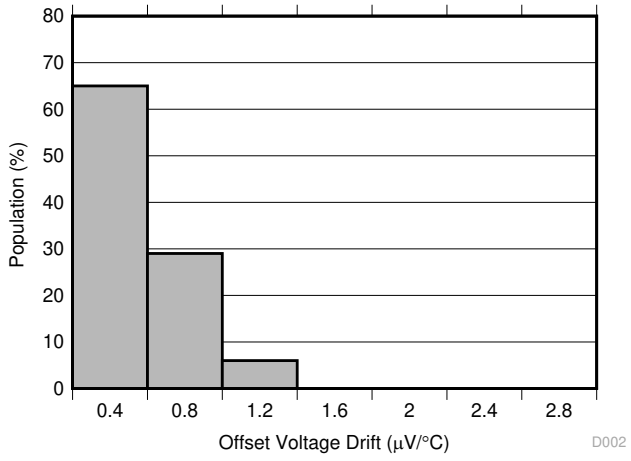


Figure 7-2. Offset Voltage Drift Distribution

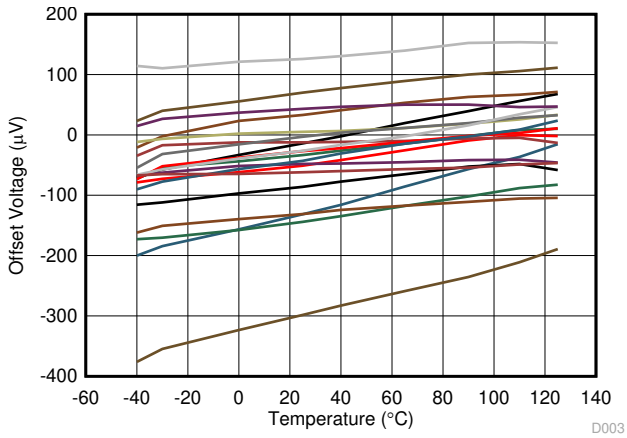


Figure 7-3. Offset Voltage vs Temperature

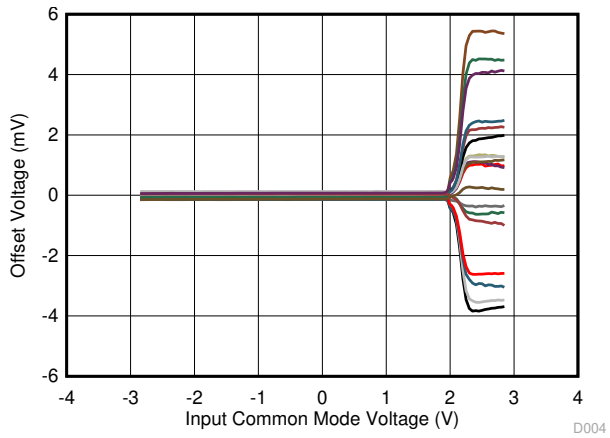


Figure 7-4. Offset Voltage vs Common-Mode Voltage

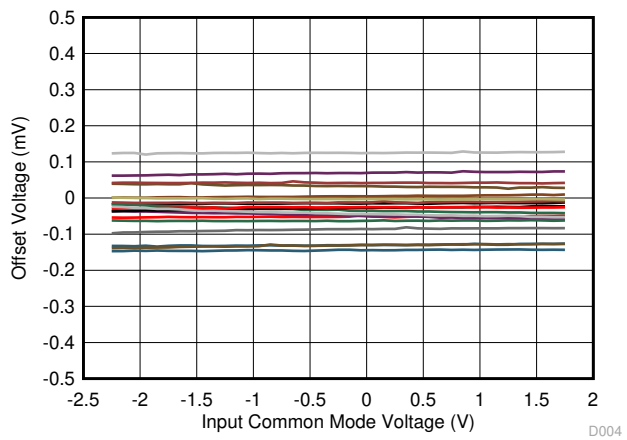


Figure 7-5. Offset Voltage vs Common-Mode Voltage

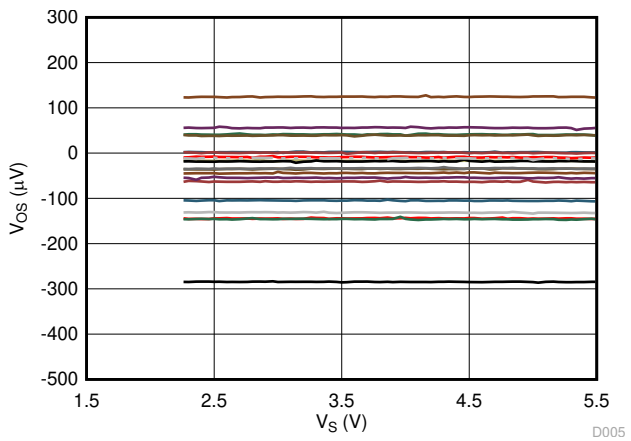


Figure 7-6. Offset Voltage vs Power Supply

7.7 TLV6741: Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

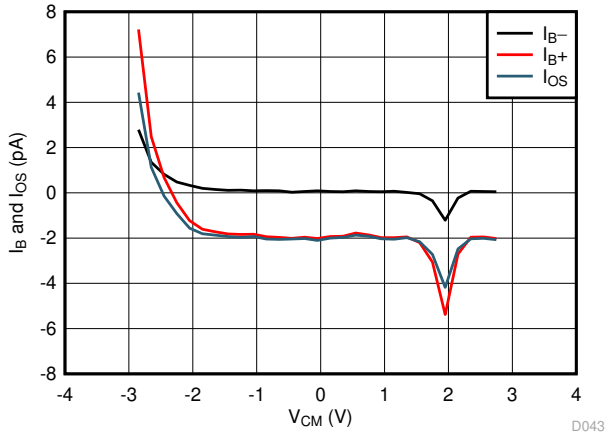


Figure 7-7. I_B and I_{OS} vs Common-Mode Voltage

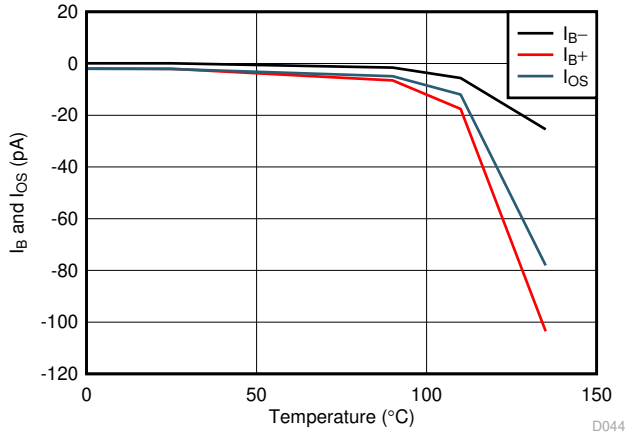
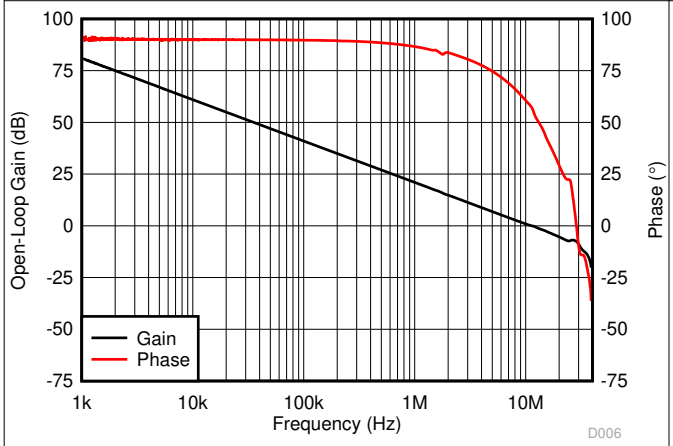


Figure 7-8. I_B and I_{OS} vs Temperature



C_L = 10 pF

Figure 7-9. Open-Loop Gain and Phase vs Frequency

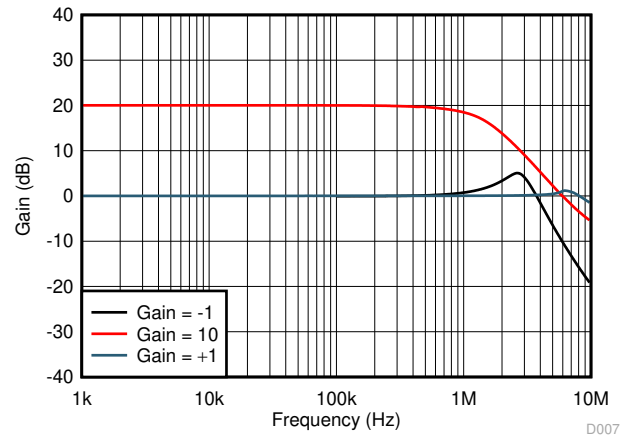


Figure 7-10. Closed-Loop Gain vs Frequency

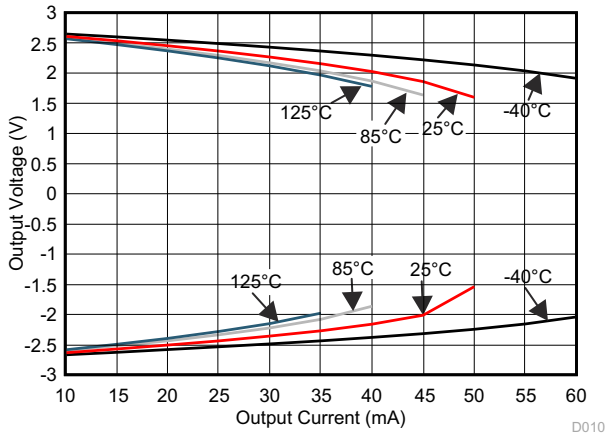


Figure 7-11. V_O vs I Sourcing and Sinking

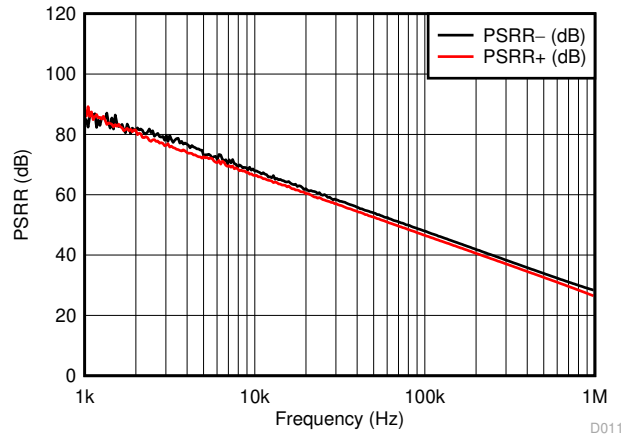


Figure 7-12. PSRR vs Frequency (Referred to Input)

7.7 TLV6741: Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

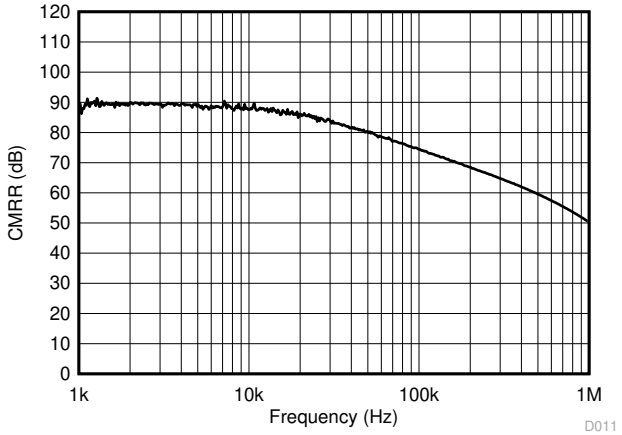
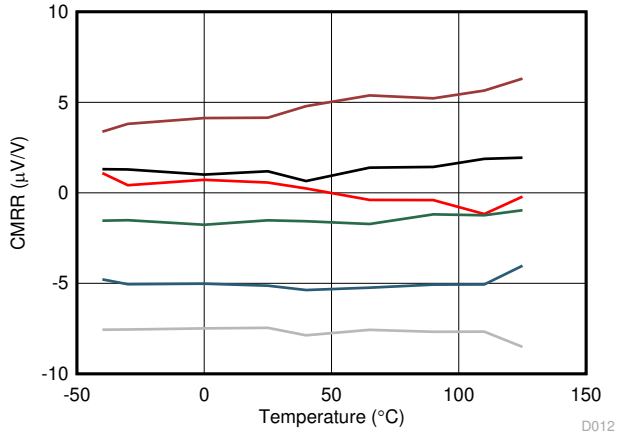


Figure 7-13. CMRR vs Frequency (Referred to Input)



V_S = 5.5 V, T_A = –40°C to 125°C, V_{CM} = 0 V to 4.3 V

Figure 7-14. CMRR vs Temperature

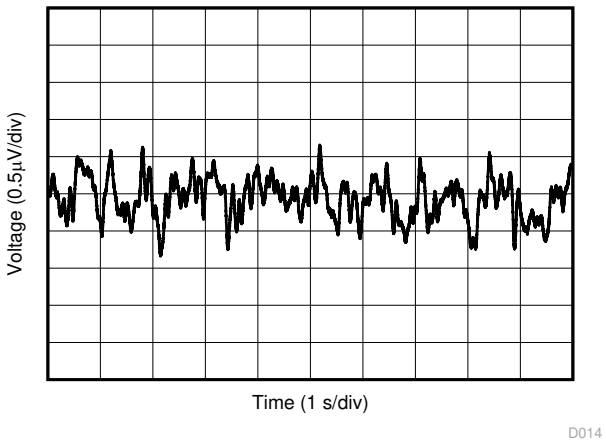


Figure 7-15. 0.1-Hz to 10-Hz Flicker Noise

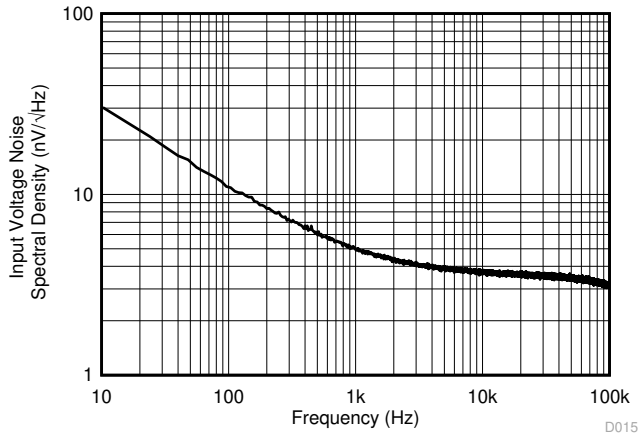
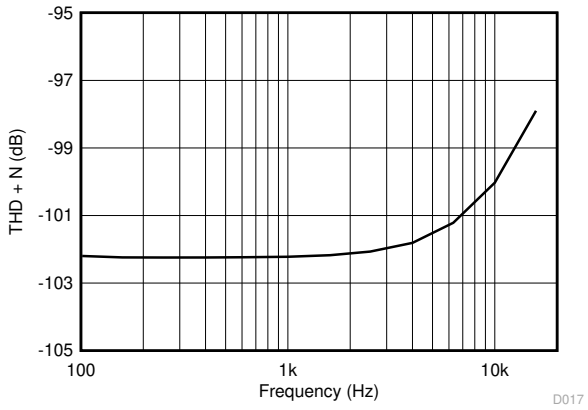
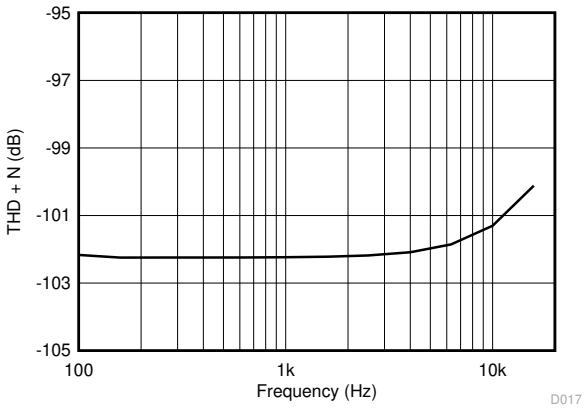


Figure 7-16. Input Voltage Noise Spectral Density vs Frequency



V_S = 5.5 V, V_{ICM} = 2.5 V, R_L = 2 kΩ,
Gain = 1, BW = 80 kHz, V_{OUT} = 0.5 Vrms

Figure 7-17. THD + N vs Frequency

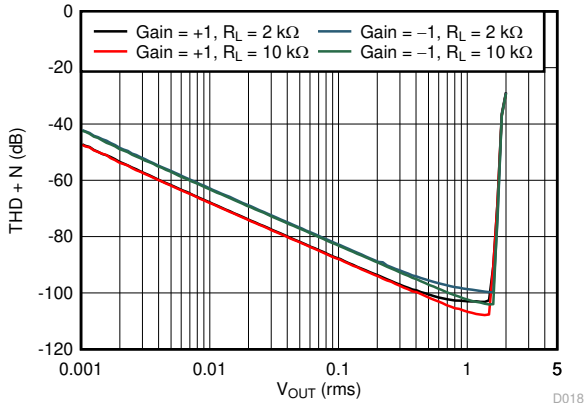


V_S = 5.5 V, V_{ICM} = 2.5 V, R_L = 10 kΩ,
Gain = 1, BW = 80 kHz, V_{OUT} = 0.5 Vrms

Figure 7-18. THD + N vs Frequency

7.7 TLV6741: Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.



V_S = 5.5 V, V_{ICM} = 2.5 V,
BW = 80 kHz, V_{OUT} = 0.5 Vrms

Figure 7-19. THD + N vs Amplitude

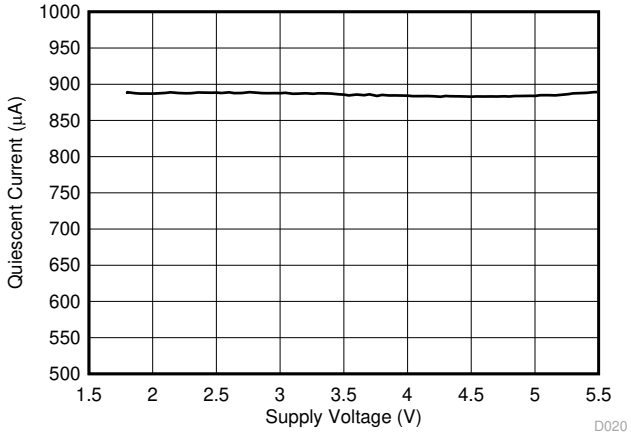


Figure 7-20. Quiescent Current vs Supply Voltage

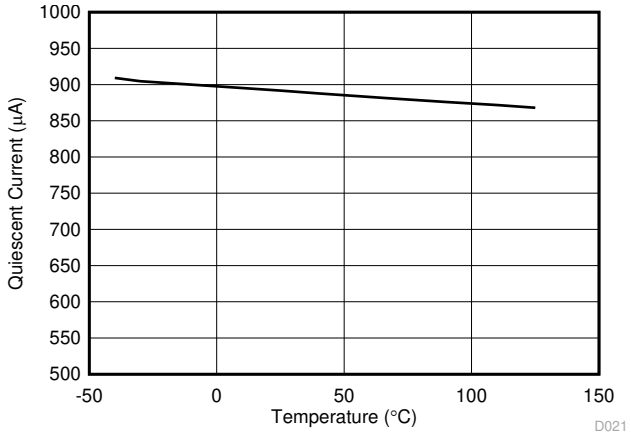
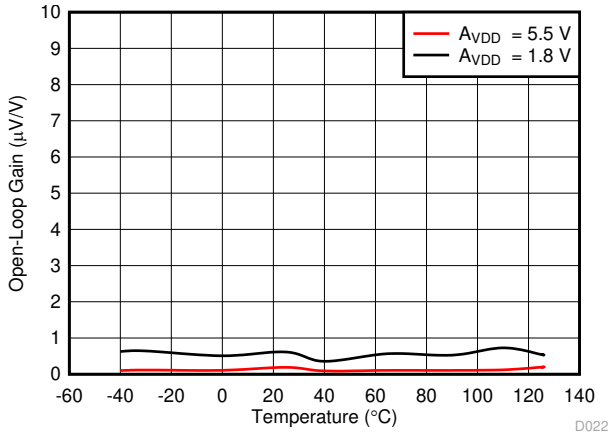


Figure 7-21. Quiescent Current vs Temperature



R_L = 2 kΩ

Figure 7-22. Open-Loop Gain vs Temperature

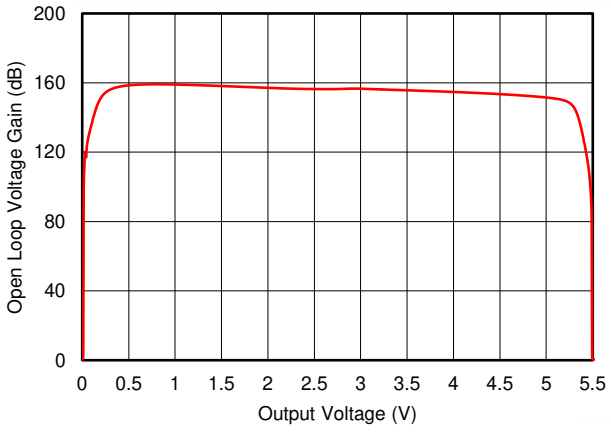
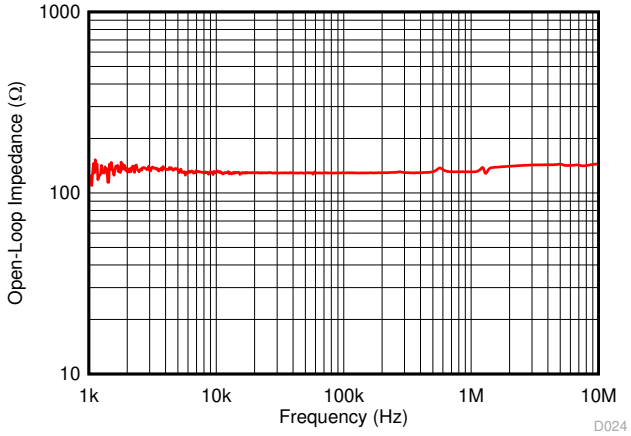


Figure 7-23. Open-Loop Gain vs Output Voltage

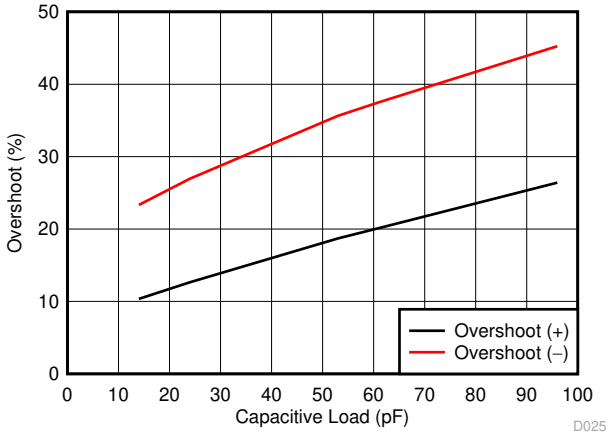


A_{VDD} = 5.5 V, V_{ICM} = V_{OCM} = 2.75 V

Figure 7-24. Open-Loop Output Impedance vs Frequency

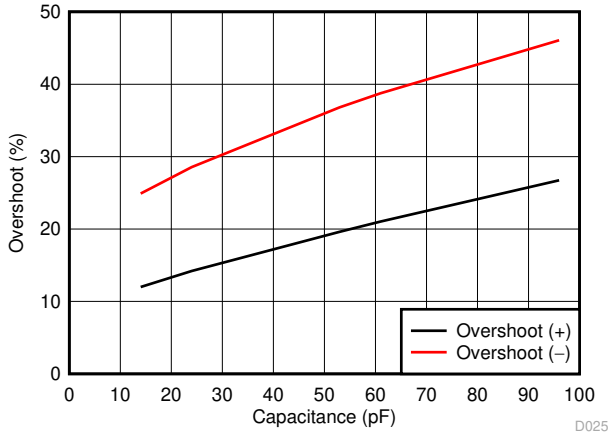
7.7 TLV6741: Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.



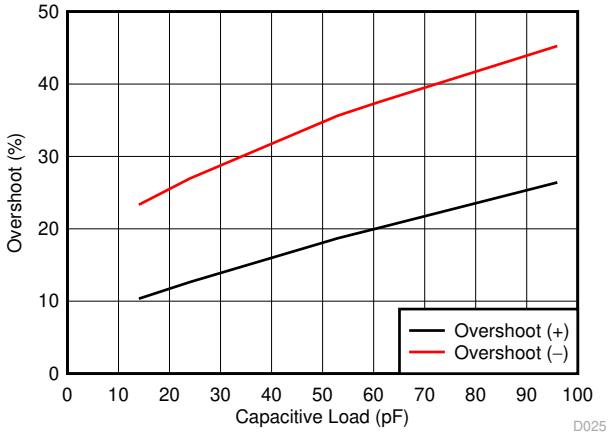
V_S = 5.5 V, V_{ICM} = 2.75 V,
V_{OCM} = 2.75 V, G = 1, 100-mV output step

Figure 7-25. Small-Signal Overshoot vs Load Capacitance



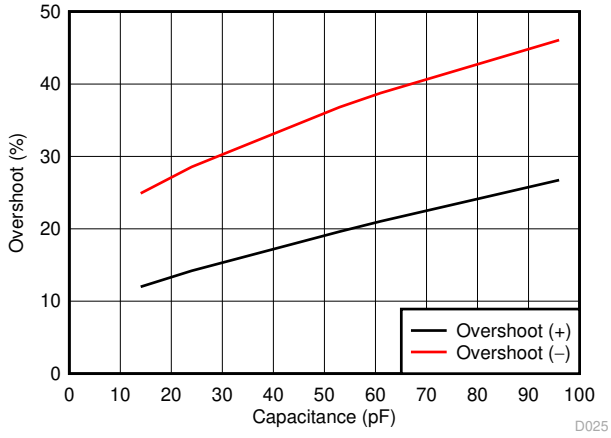
V_S = 1.8 V, V_{ICM} = 0.9 V
V_{OCM} = 0.9 V, G = 1, 100-mV output step

Figure 7-26. Small-Signal Overshoot vs Load Capacitance



V_S = 5.5 V, V_{ICM} = 2.75 V,
V_{OCM} = 2.75 V, Gain = –1, 100-mV output step

Figure 7-27. Small-Signal Overshoot vs Load Capacitance



V_S = 1.8 V, V_{ICM} = 0.9 V
V_{OCM} = 0.9 V, Gain = –1, 100-mV output step

Figure 7-28. Small-Signal Overshoot vs Load Capacitance

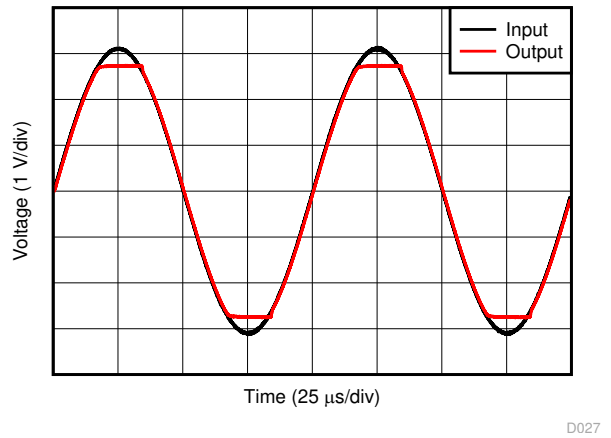


Figure 7-29. No Phase Reversal

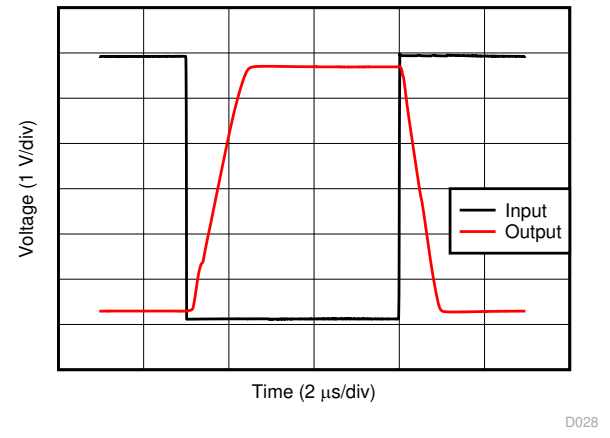
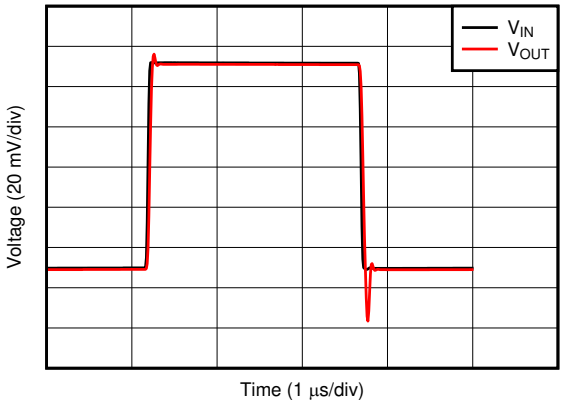


Figure 7-30. Overload Recovery

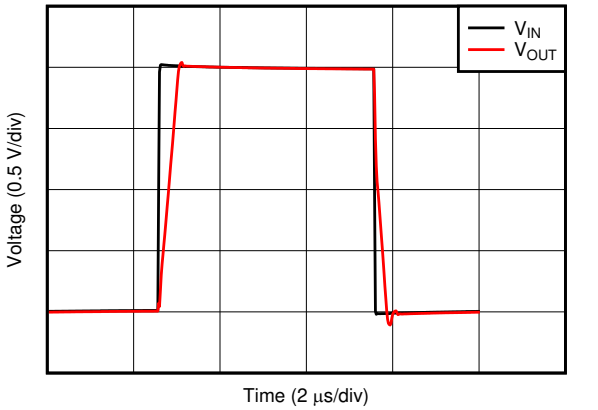
7.7 TLV6741: Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.



V_S = 1.8 V, V_{ICM} = 0.9 V, V_{OCM} = 0.9 V
C_L = 30 pF, Gain = 1, V_{IN} = 100-mVpp

Figure 7-31. Small-Signal Step Response

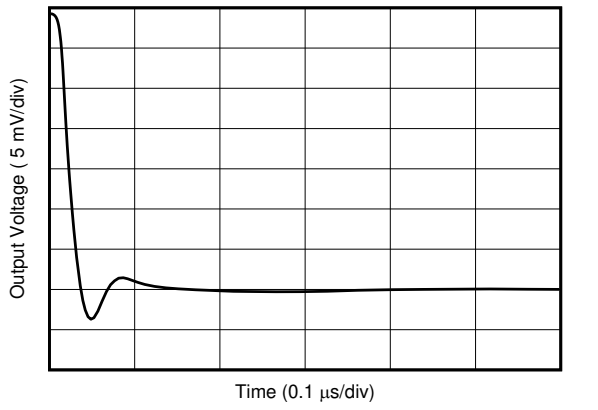


V_S = 5.5 V, V_{OCM} = 2.75 V, C_L = 10 pF
V_{ICM} = 2.75 V, Gain = 1, 2-V step

Figure 7-32. Large Signal Step Response

V_S = 5.5 V, V_{ICM} = 2.75 V, V_{OCM} = 2.75 V
C_L = 0, Gain = 1, 5-V step

Figure 7-33. Large Signal Settling Time (Positive)



V_S = 5.5 V, V_{ICM} = 2.75 V, V_{OCM} = 2.75 V
C_L = 0, Gain = 1, 5-V step

Figure 7-34. Large Signal Settling Time (Negative)

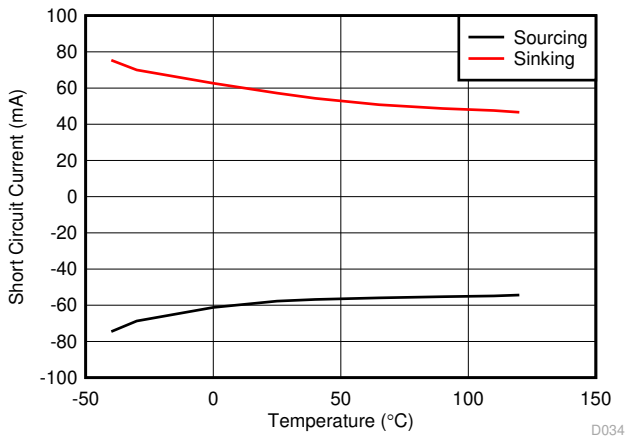
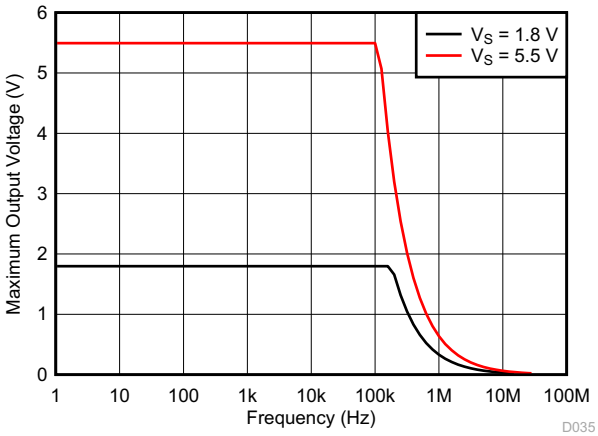


Figure 7-35. Short-Circuit Current vs Temperature



V_{ICM} = V_S / 2, V_{OCM} = V_S / 2,
C_L = 10 pF, Gain = 1

Figure 7-36. Maximum Output Voltage vs Frequency

7.7 TLV6741: Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

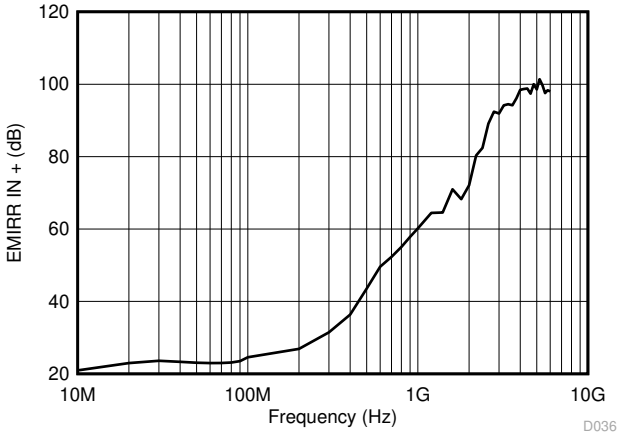
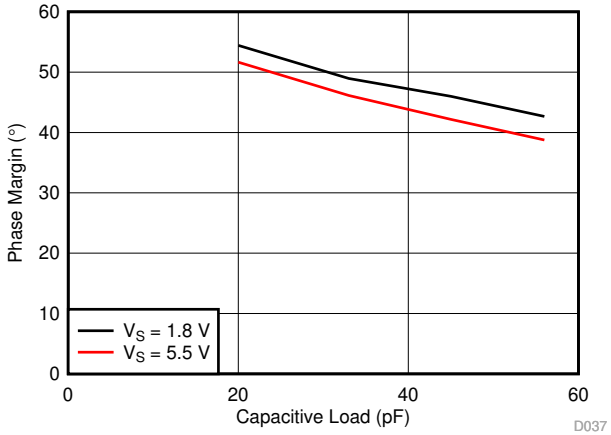


Figure 7-37. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

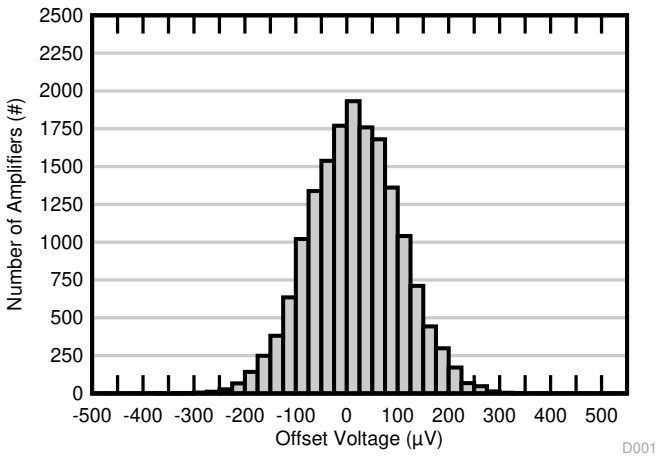


V_{ICM} = V_{OCM} = V_S / 2

Figure 7-38. Phase Margin vs Capacitive Load

7.8 TLV6742: Typical Characteristics

at T_A = 25°C, V_S = ±2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.



V_{CM} = V–

Figure 7-39. Offset Voltage Production Distribution

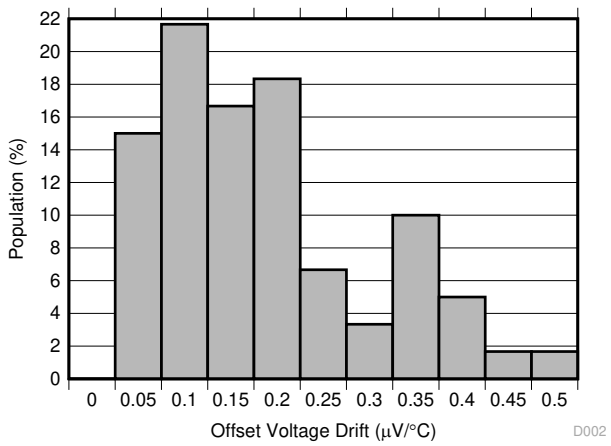
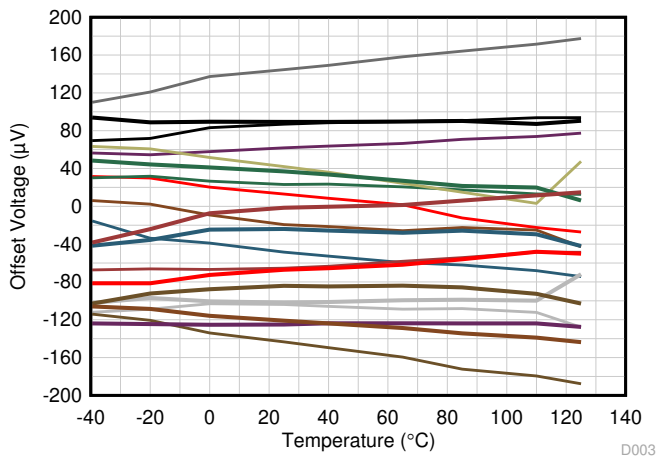


Figure 7-40. Offset Voltage Drift Distribution

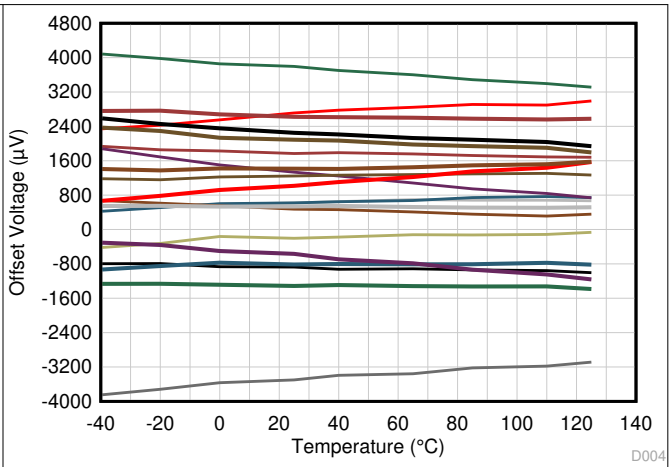
7.8 TLV6742: Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.



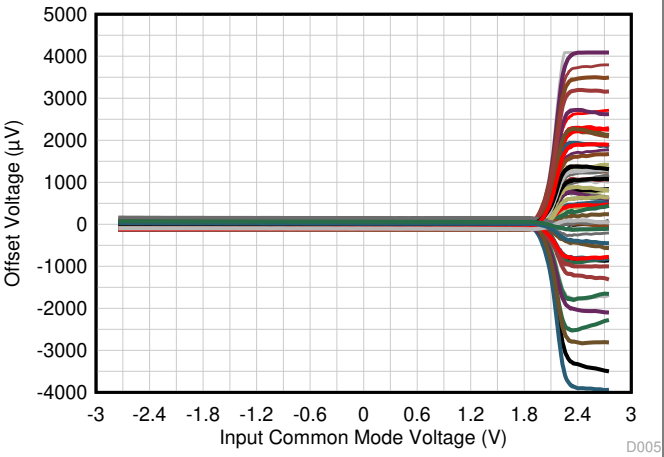
V_{CM} = V–

Figure 7-41. Offset Voltage vs Temperature (PMOS Input Pair)



V_{CM} = V+

Figure 7-42. Offset Voltage vs Temperature (NMOS Input Pair)



Over full common-mode voltage range

Figure 7-43. Offset Voltage vs Common-Mode Voltage (Full Range)

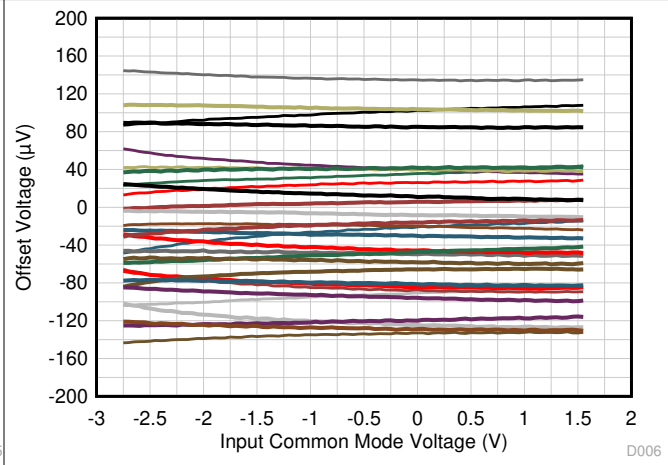


Figure 7-44. Offset Voltage vs Common-Mode Voltage (PMOS Input Pair)

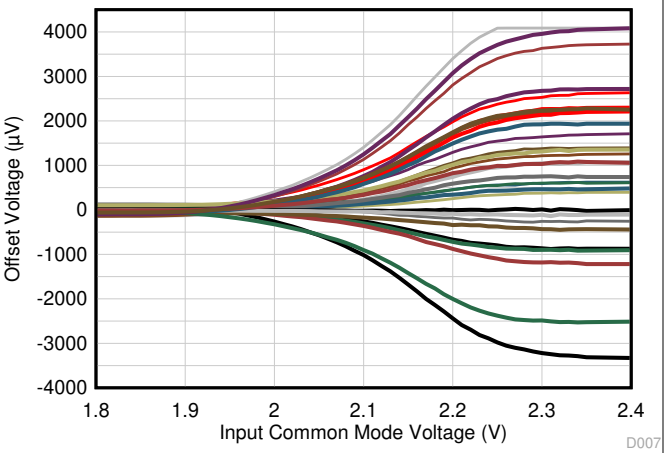


Figure 7-45. Offset Voltage vs Common-Mode Voltage (Transition Region)

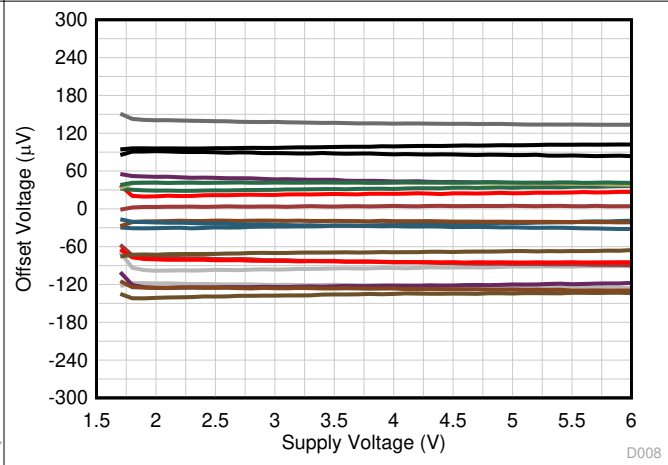


Figure 7-46. Offset Voltage vs Power Supply

7.8 TLV6742: Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

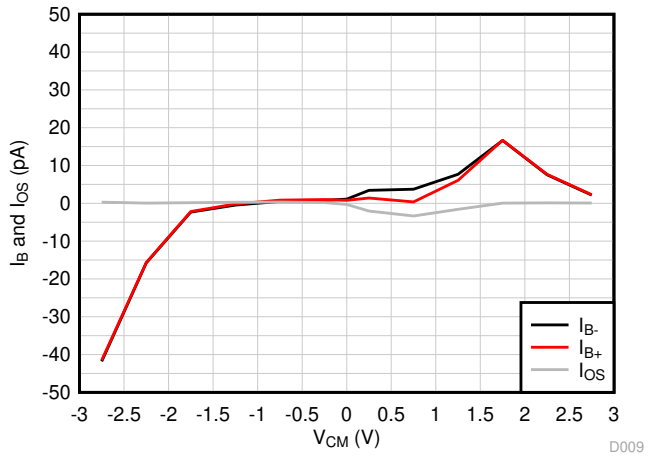


Figure 7-47. I_B and I_{OS} vs Common-Mode Voltage

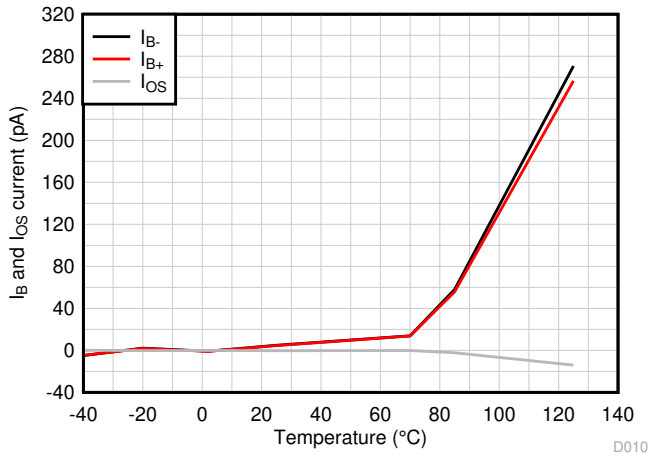


Figure 7-48. I_B and I_{OS} vs Temperature

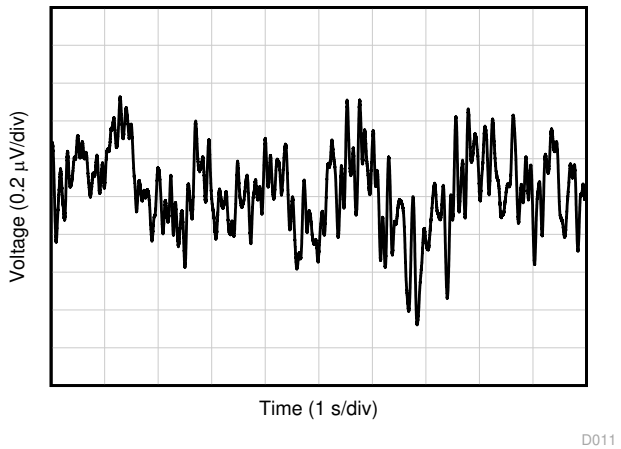


Figure 7-49. 0.1-Hz to 10-Hz Flicker Noise

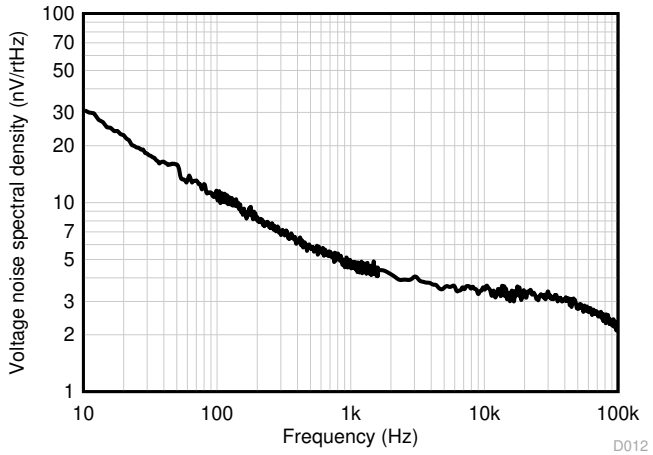


Figure 7-50. Input Voltage Noise Spectral Density vs Frequency

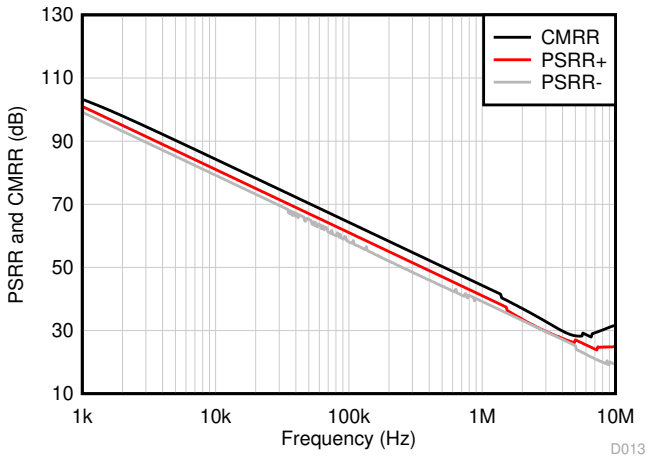
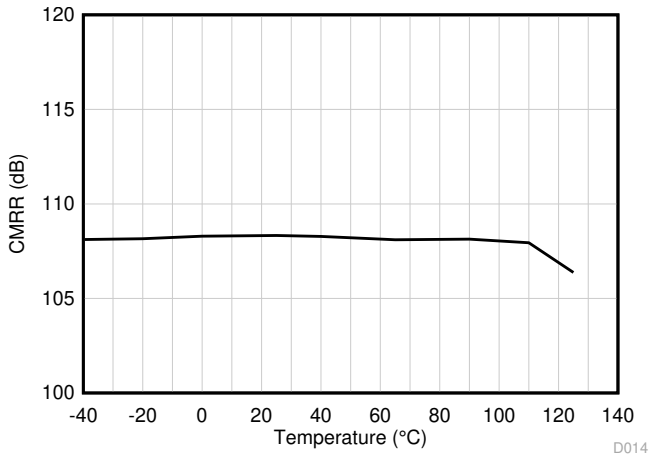


Figure 7-51. CMRR and PSRR vs Frequency (Referred to Input)

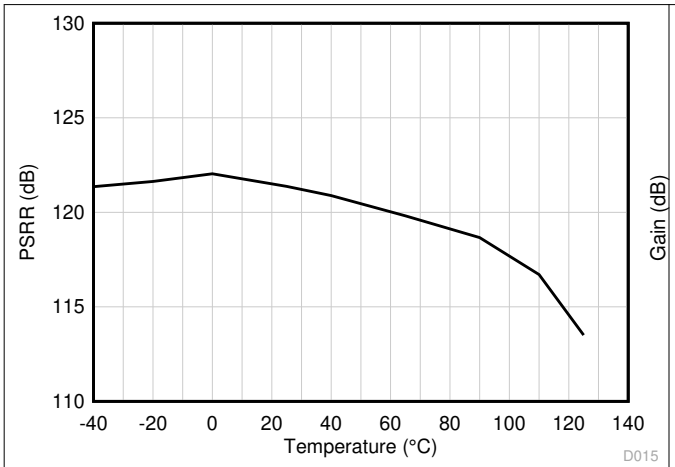


V_S = 5.5 V, V_{CM} = V– to (V+) – 1.2 V

Figure 7-52. CMRR vs Temperature

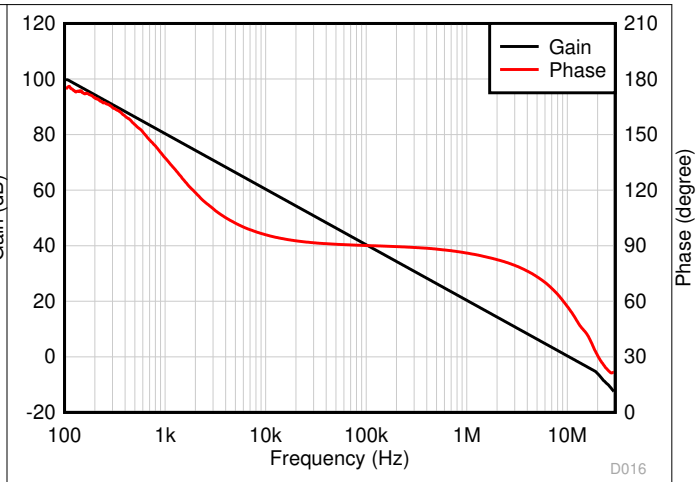
7.8 TLV6742: Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.



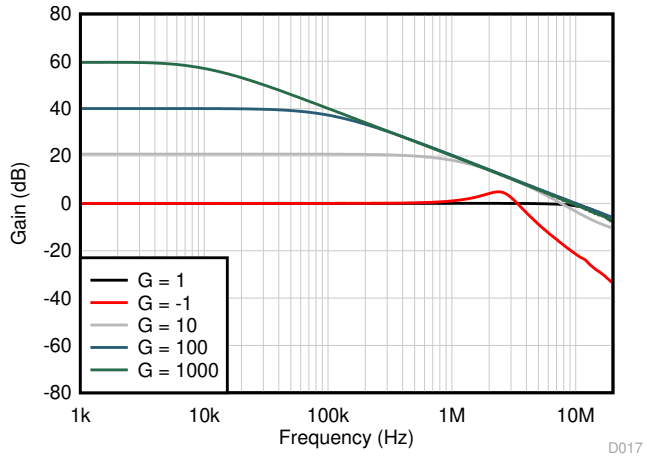
V_{CM} = V–

Figure 7-53. PSRR vs Temperature



C_L = 10 pF

Figure 7-54. Open-Loop Gain and Phase vs Frequency



C_L = 10 pF

Figure 7-55. Closed-Loop Gain vs Frequency

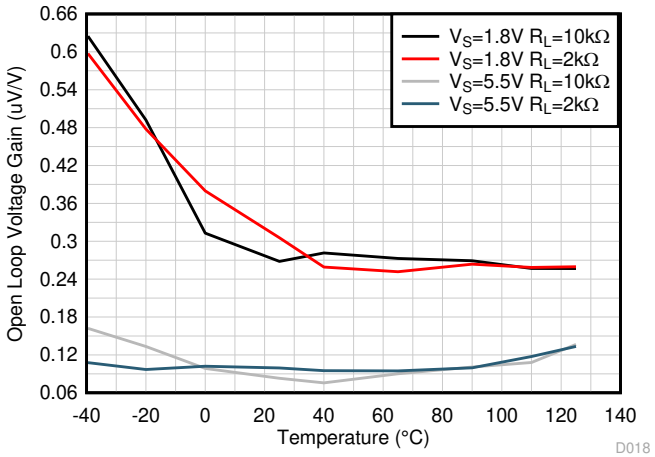


Figure 7-56. Open-Loop Gain vs Temperature

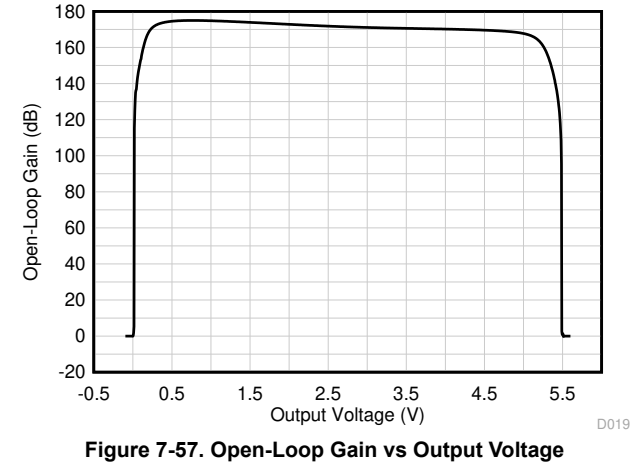


Figure 7-57. Open-Loop Gain vs Output Voltage

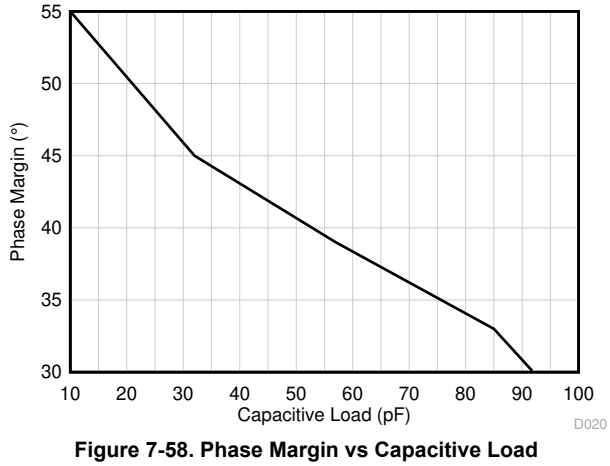


Figure 7-58. Phase Margin vs Capacitive Load

7.8 TLV6742: Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

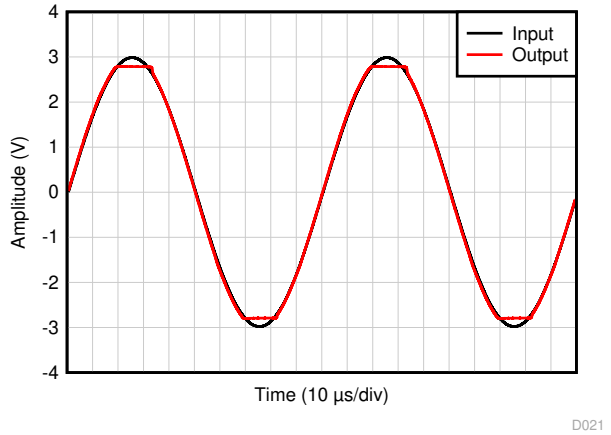
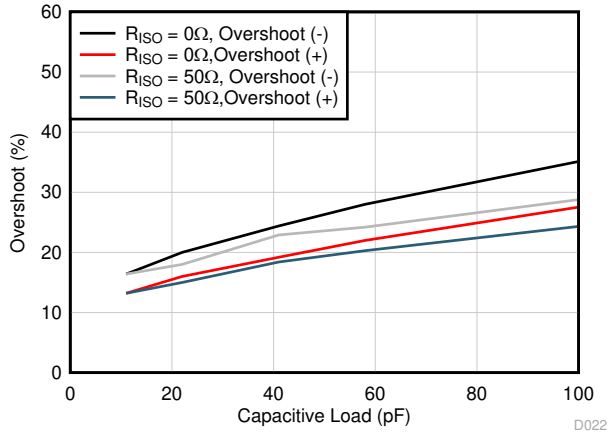
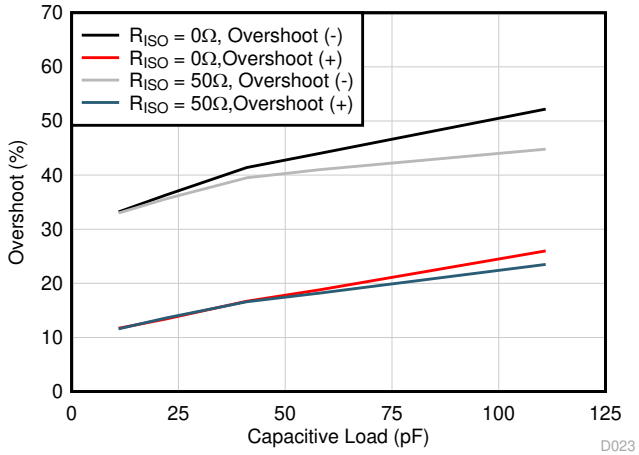


Figure 7-59. No Phase Reversal



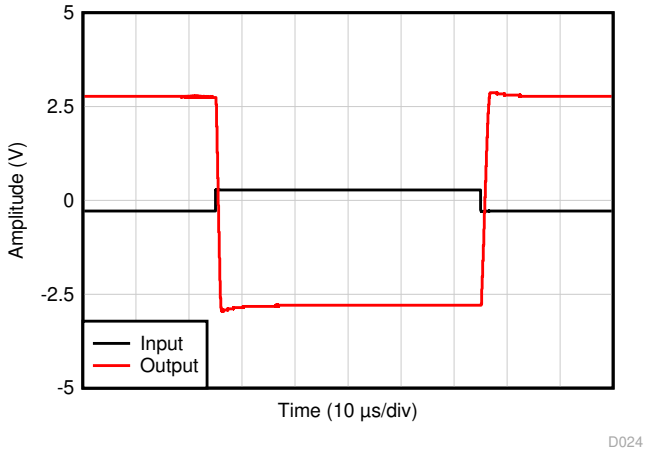
V_{CM} = V_S / 2, R_L = 1 kΩ
Gain = –1, 100-mV output step

Figure 7-60. Small-Signal Overshoot vs Load Capacitance



V_{CM} = V_S / 2, R_L = 1 kΩ
Gain = +1, 100-mV output step

Figure 7-61. Small-Signal Overshoot vs Load Capacitance

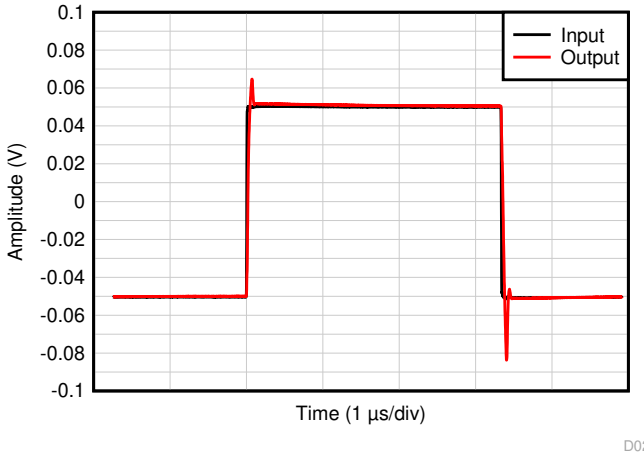


V_{IN}=0.6 Vpp, G = –10, V_{IN} × gain > V_S

Figure 7-62. Overload Recovery

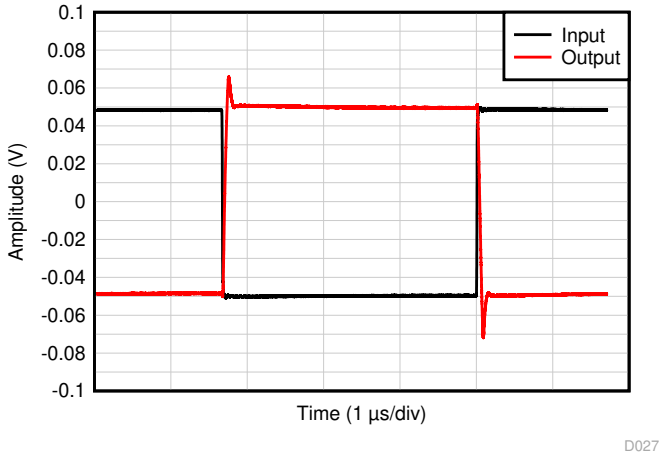
7.8 TLV6742: Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.



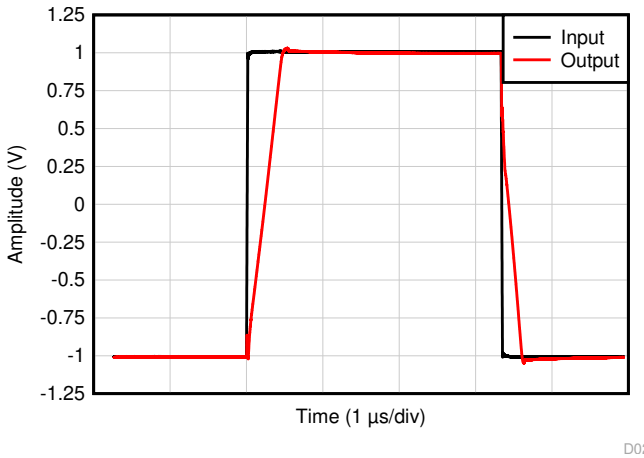
C_L = 20 pF, Gain = 1, V_{IN} = 100-mVpp , R_L = 1 kΩ

Figure 7-63. Small-Signal Step Response



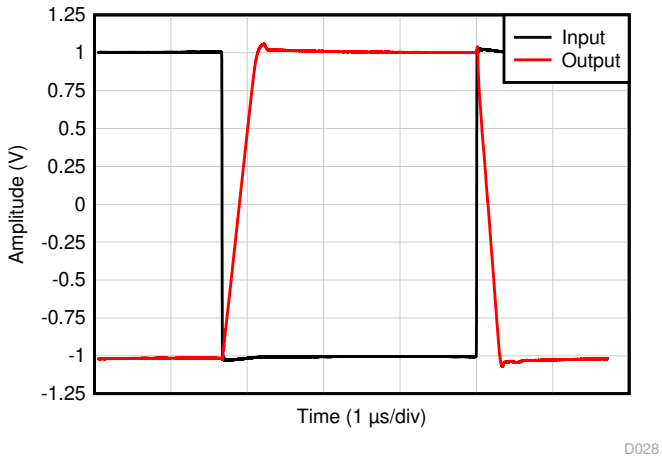
C_L = 20 pF, Gain = –1, V_{IN} = 100-mVpp, R_L = 1 kΩ

Figure 7-64. Small-Signal Step Response



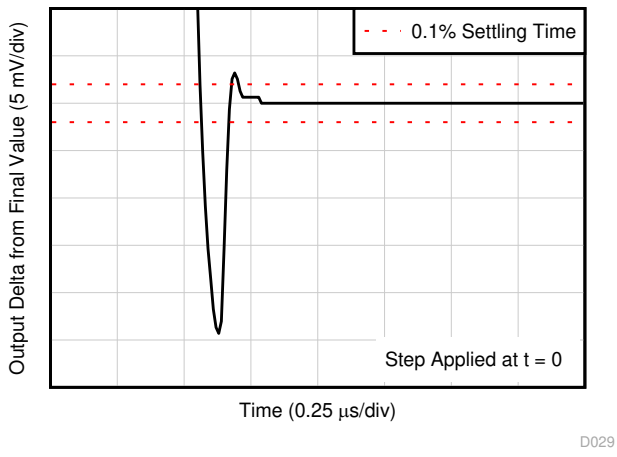
C_L = 20 pF, Gain = +1, V_{IN} = 2-V step, R_L = 1 kΩ

Figure 7-65. Large Signal Step Response



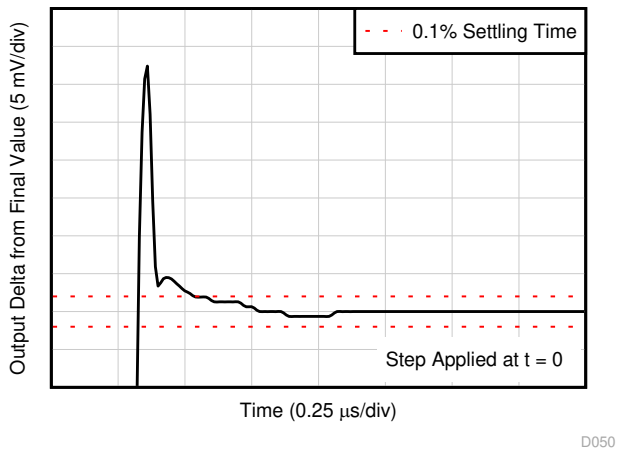
C_L = 20 pF, Gain = –1, V_{IN} = 2-V step, R_L = 1 kΩ

Figure 7-66. Large Signal Step Response



C_L = 20 pF, Gain = 1, V_{IN} = 2-V step

Figure 7-67. Large Signal Settling Time (Positive)

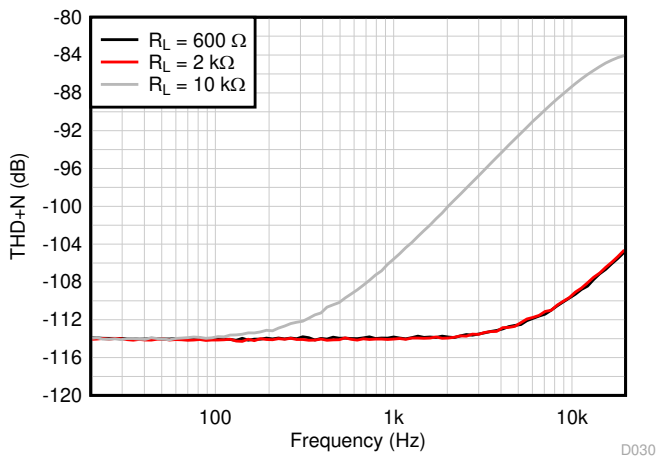


C_L = 20 pF, Gain = –1, V_{IN} = 2-V step

Figure 7-68. Large Signal Settling Time (Negative)

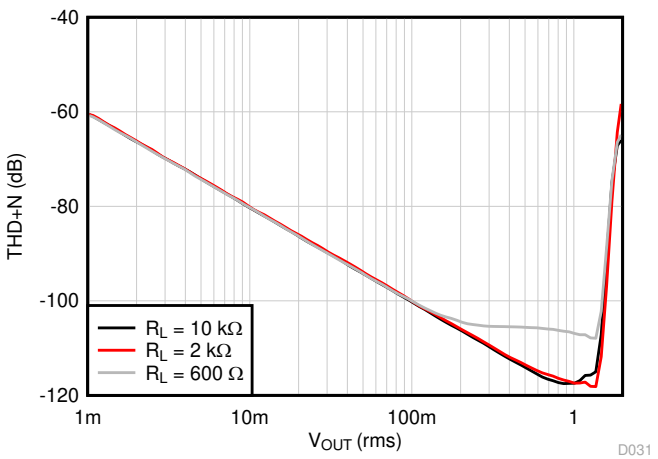
7.8 TLV6742: Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.



V_{CM} = 2.5 V
Gain = +1, BW = 80 kHz, V_{OUT} = 0.5 Vrms

Figure 7-69. THD + N vs Frequency



V_{CM} = 2.5 V
BW = 80 kHz

Figure 7-70. THD + N vs Amplitude

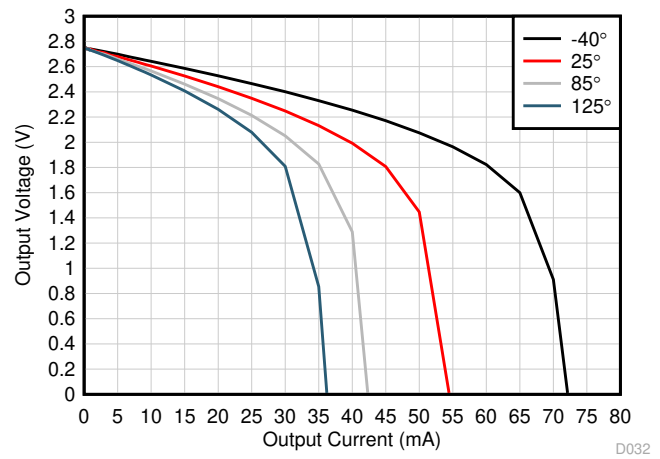


Figure 7-71. V_{OUT} vs Sourcing Current

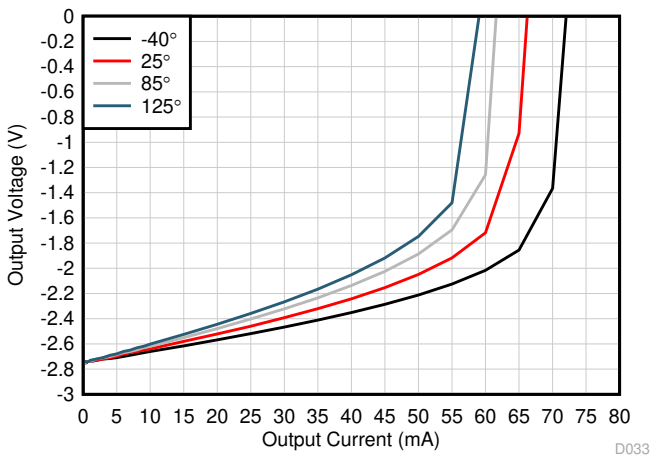
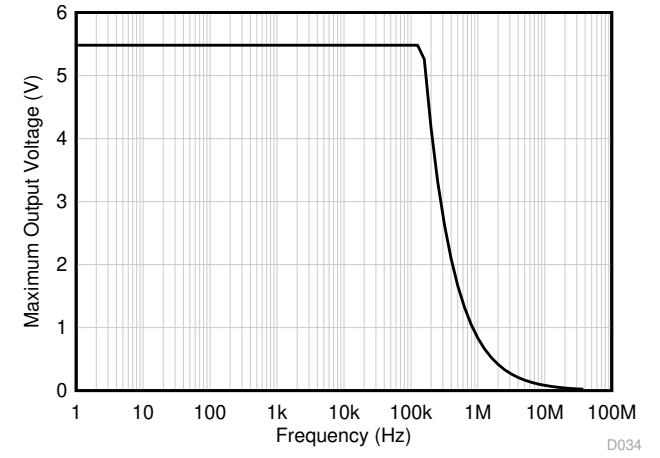


Figure 7-72. V_{OUT} vs Sinking Current



C_L = 10 pF, Gain = +1, V_S= 5.5 V

Figure 7-73. Maximum Output Voltage vs Frequency

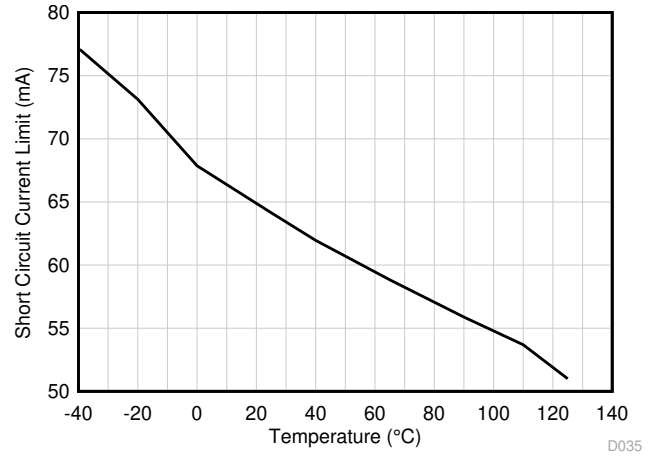


Figure 7-74. Short-Circuit Current vs Temperature

7.8 TLV6742: Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

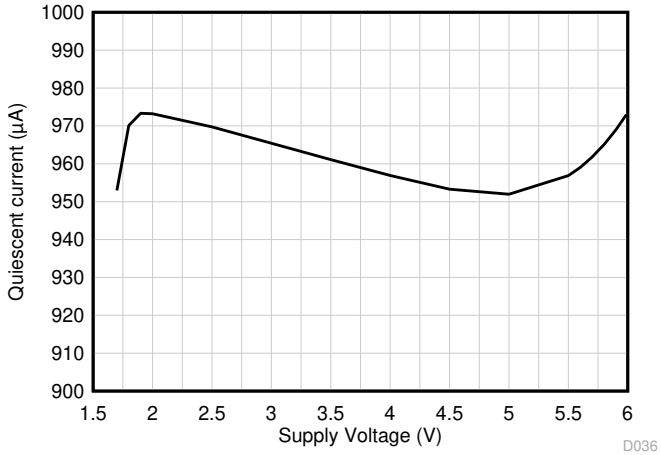


Figure 7-75. Quiescent Current vs Supply Voltage

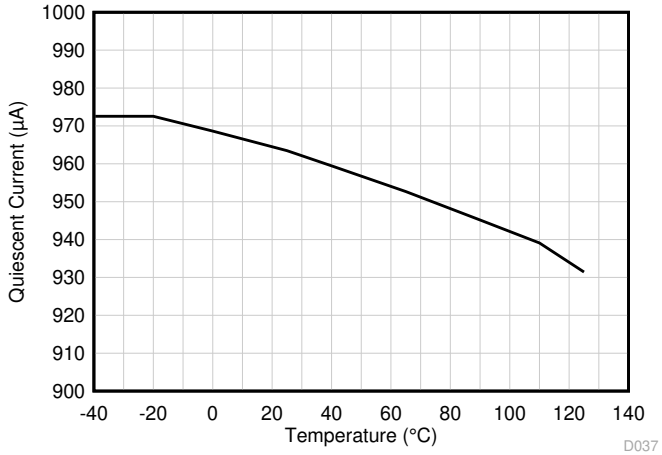


Figure 7-76. Quiescent Current vs Temperature

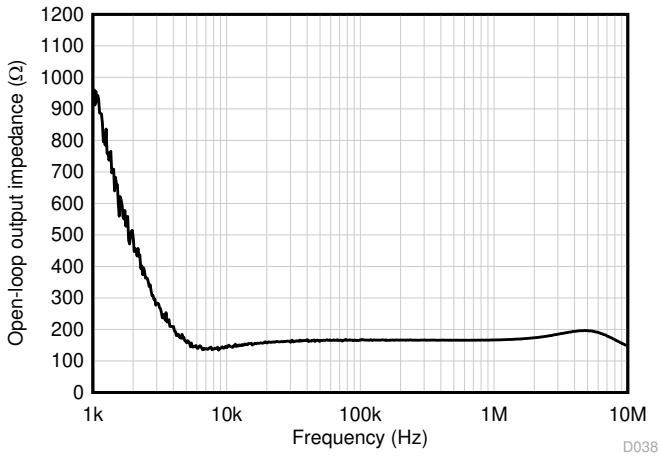
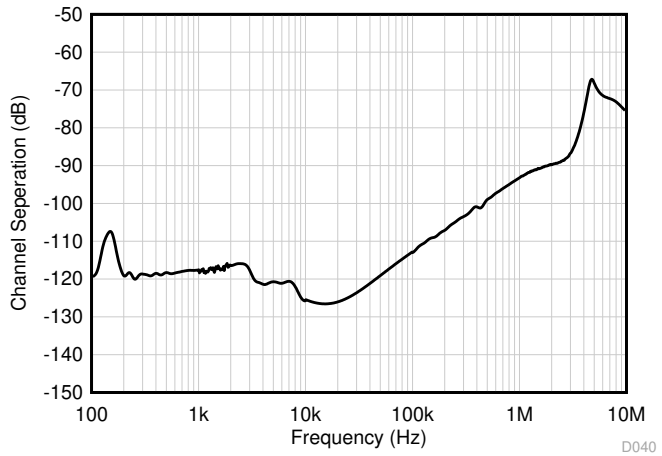


Figure 7-77. Open-Loop Output Impedance vs Frequency



A_{VDD} = 5.5 V, V_{ICM} = V_{OCM} = 2.75 V

Figure 7-78. Channel Separation vs Frequency

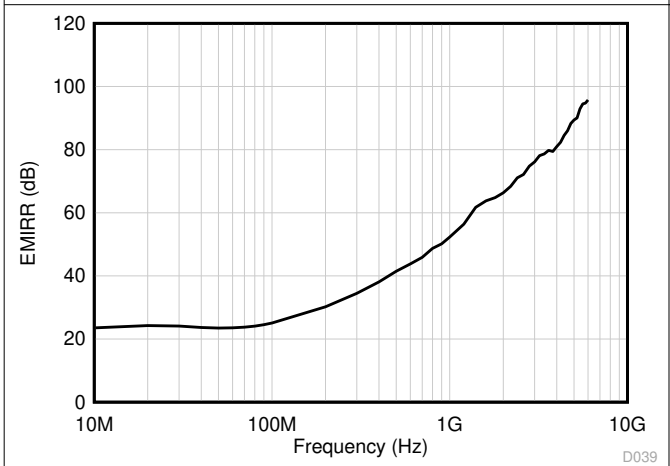
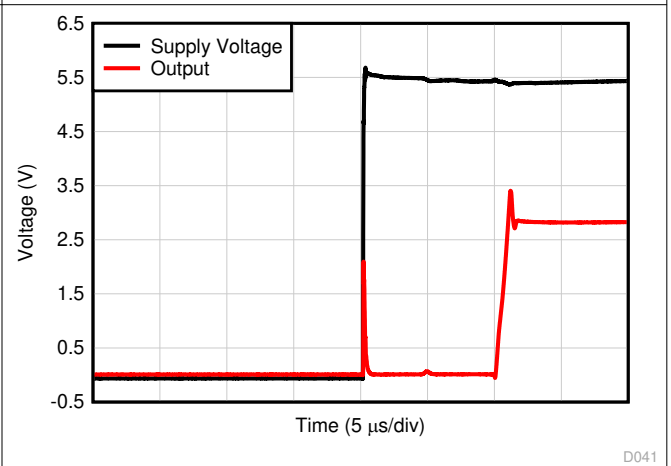


Figure 7-79. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency



V_S = 0 to 5.5 V, V_{OUT} = 0 to 2.75 V

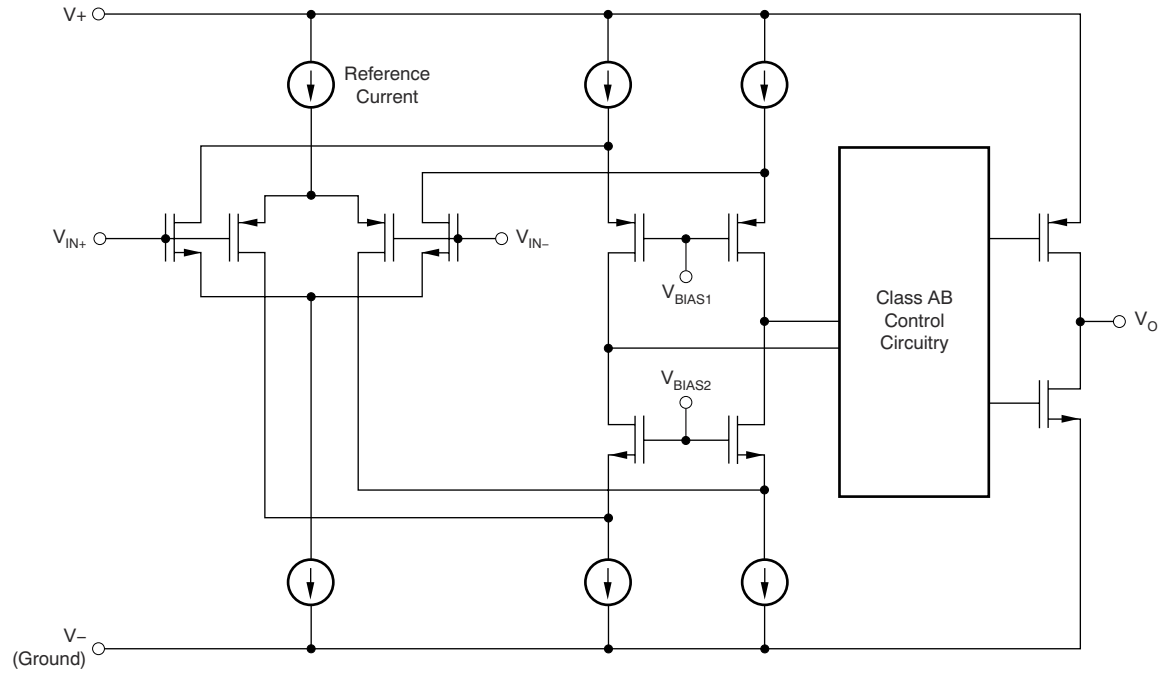
Figure 7-80. Turn-On Time

8 Detailed Description

8.1 Overview

The TLV674x family is an ultra low-noise, rail-to-rail output operational amplifier family. These devices operate from a supply voltage of 2.25 V to 5.5 V (TLV6741) and 1.7 V to 5.5 V (TLV6742 and TLV6744), are unity-gain stable, and suitable for a wide range of general-purpose applications. The input common-mode voltage range includes the negative rail and allows the TLV674x op amp family to be used in most single-supply applications. Rail-to-rail output swing significantly increases dynamic range, especially in low-supply applications, and makes it suitable for many audio applications as well as driving sampling analog-to-digital converters (ADCs).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 THD+ Noise Performance

TLV674x operational amplifier family has excellent distortion characteristics. TLV6742 and TLV6744 THD + Noise is below 0.00015% (G = +1, V_O = 1 V_{RMS}, V_{CM} = 1.8 V, V_S = 5.5 V) throughout the audio frequency range, 20 Hz to 20 kHz with a 10-kΩ load. TLV6741 THD + Noise is below 0.00035% (G = +1, V_O = 1 V_{RMS}, V_{CM} = 2.5 V, V_S = 5.5 V) throughout the audio frequency range, 20 Hz to 20 kHz, with a 10-kΩ load. Broadband noise of 3.5 nV/√ Hz (TLV6742/4) and 3.7 nV/√ Hz (TLV6741) is extremely low for a 10-MHz general purpose amplifier.

8.3.2 Operating Voltage

The TLV674x operational amplifier family is fully specified and assured for operation from 1.7 V to 5.5 V (TLV6742/4) and 2.25 V to 5.5 V (TLV6741). In addition, many specifications apply from –40°C to 125°C. Power-supply pins should be bypassed with 0.1-µF ceramic capacitors.

8.3.3 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TLV674x devices deliver a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10-kΩ, the output swings to within a few mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails, see Figure 7-11.

8.3.4 EMI Rejection

The TLV674x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV674x benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 8-1 shows the results of this testing on the TLV674x. Table 8-1 shows the EMIRR IN+ values for the TLV674x at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

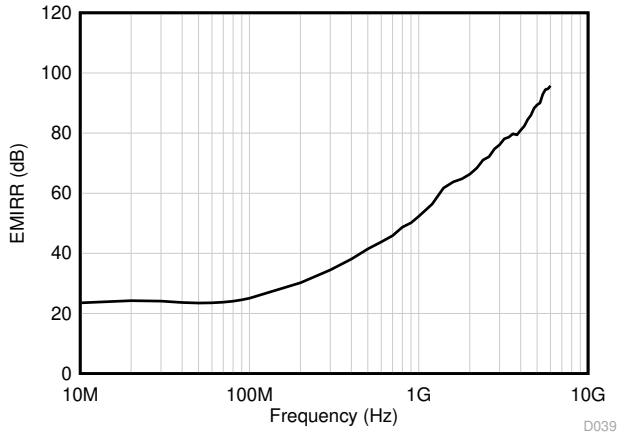


Figure 8-1. EMIRR Testing

Table 8-1. TLV674x EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	59.5 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	68.9 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	77.8 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	78.0 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.8 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	87.6 dB

8.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 8-2 shows an illustration of the ESD circuits contained in the TLV674x (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

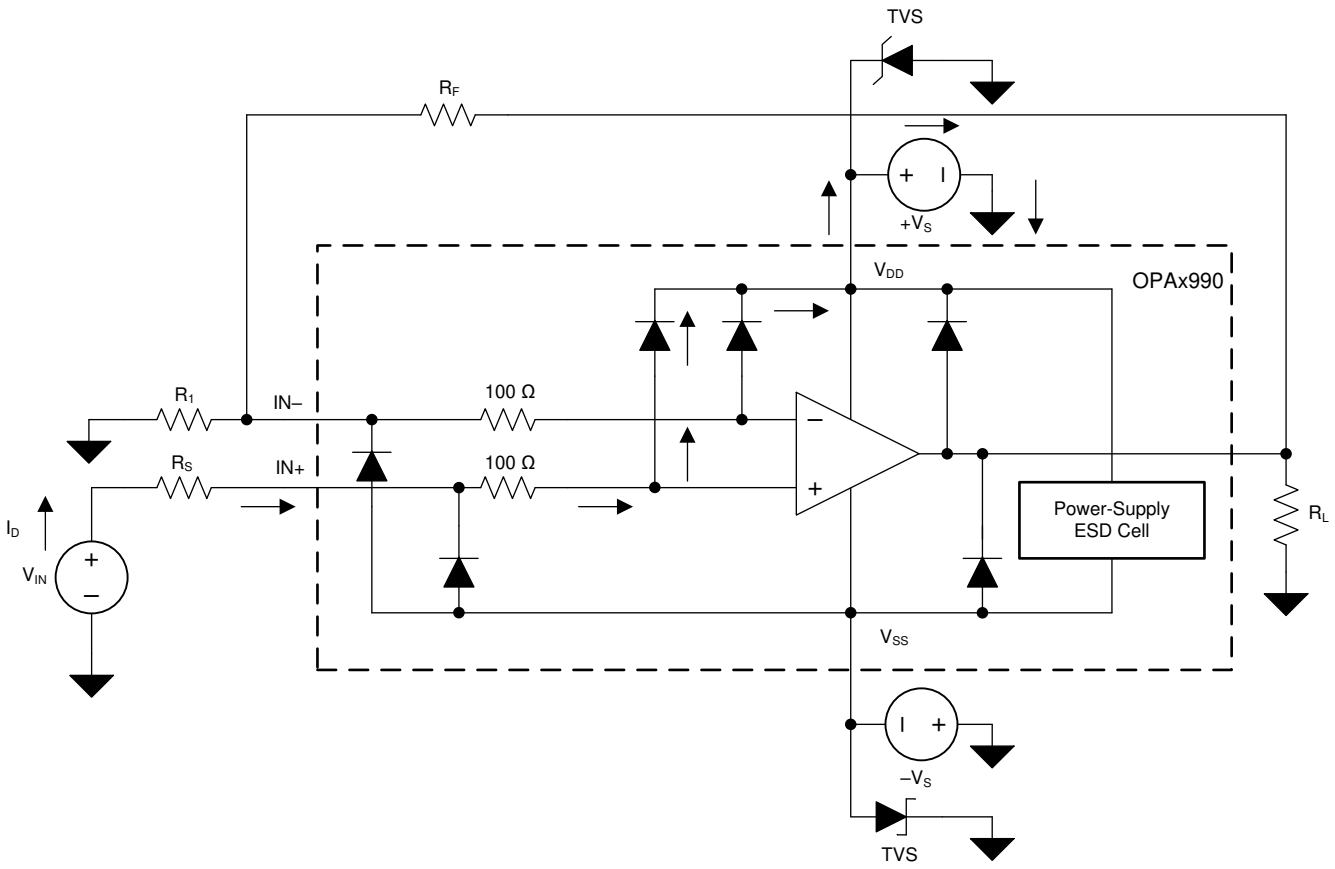


Figure 8-2. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example; 1 kV, 100 ns), whereas an EOS event is long in duration and lower voltage (for example; 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressor (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

The TLV674x family incorporates internal electrostatic discharge (ESD) protection circuits on all pins, as shown above. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in Section 7.1. Figure 8-3 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

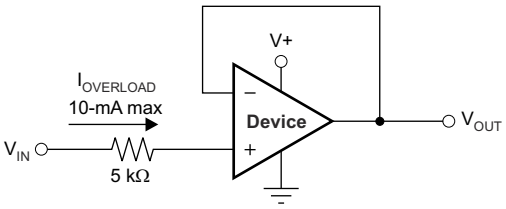


Figure 8-3. Input Current Protection

8.3.6 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier in order to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier will exhibit some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian* ("bell curve"), or *normal*, distributions and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in Section 7.6.

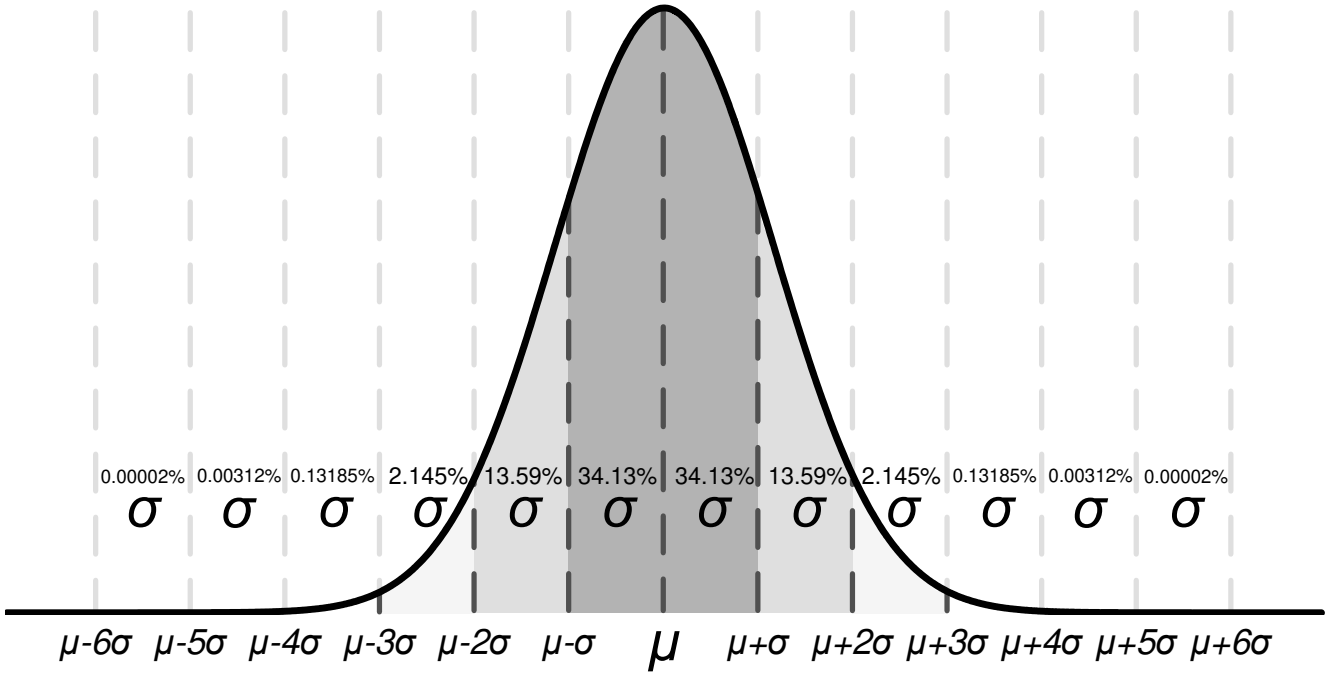


Figure 8-4. Ideal Gaussian Distribution

Figure 8-4 shows an example distribution, where *μ*, or *mu*, is the mean of the distribution, and where *σ*, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from *μ–σ* to *μ+σ*).

Depending on the specification, values listed in the *typical* column of Section 7.6 are represented in different ways. As a general rule of thumb, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near

zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) in order to most accurately represent the typical value.

You can use this chart to calculate approximate probability of a specification in a unit; for example, for TLV6742, the typical input voltage offset is 150 μV, so 68.2% of all TLV6742 devices are expected to have an offset from –150 μV to 150 μV.

Specifications with a value in the minimum or maximum column are assured by TI, and units outside these limits will be removed from production material. For example, the TLV6742 device has a maximum offset voltage of 1.0 mV at 25°C, and even though this corresponds to 5 σ (≈1 in 1.7 million units), which is extremely unlikely, TI assures that any unit with a larger offset than 1.0 mV will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for your application, and design worst-case conditions using this value. For example, the 6σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and could be an option as a wide guardband to design a system around. In this case, the TLV6742 does not have a maximum or minimum for offset voltage drift, but based on Figure 7-40 and the typical value of 0.2 μV/°C in Section 7.6, it can be calculated that the 6-σ value for offset voltage drift is about 1.0 μV/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should be used only to estimate the performance of a device.

8.3.7 Shutdown Function

The TLV674xS devices feature $\overline{\text{SHDN}}$ pins that disable the op amp, placing it into a low-power standby mode. In this mode, the op amp typically consumes less than 1 μA. The $\overline{\text{SHDN}}$ pins are active-low, meaning that shutdown mode is enabled when the input to the $\overline{\text{SHDN}}$ pin is a valid logic low.

The $\overline{\text{SHDN}}$ pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 800 mV (typical) above the negative rail. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure optimal shutdown behavior, the $\overline{\text{SHDN}}$ pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V– and V– + 0.2 V. A valid logic high is defined as a voltage between V– + 1.2 V and V+. The shutdown pin must either be connected to a valid high or a low voltage or driven, and not left as an open circuit. There is ***no*** internal pull-up to enable the amplifier.

The $\overline{\text{SHDN}}$ pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled, and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 15 μs for full shutdown of all channels; disable time is 3 μs. When disabled, the output assumes a high-impedance state. This architecture allows the TLV674xS to be operated as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 10-kΩ load to midsupply (V_S / 2) is required. If using the TLV674xS without a load, the resulting turnoff time is significantly increased.

8.3.8 Packages With an Exposed Thermal Pad

The TLV674x family is available in packages such as the WSON-8 (DSG) which feature an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must either be connected to V– or left floating. Attaching the thermal pad to a potential other than V– is not allowed, and performance of the device is not assured when doing so.

8.4 Device Functional Modes

The TLV674x family has a single functional mode. The TLV6742 and TLV6744 are powered on as long as the power-supply voltage is between 1.7 V (±0.85 V) and 5.5 V (±2.75 V).The TLV6741 is powered on as long as the power-supply voltage is between 2.25 V (±1.125 V) and 5.5 V (±2.75 V).

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV674x family features 10-MHz bandwidth and 4.5-V/µs slew rate with only 890-µA (TLV6741), 990-µA (TLV6742/4) of supply current per channel, providing good AC performance at very-low-power consumption. DC applications are well served with a very-low input noise voltage of 3.5 nV /vHz (TLV6742/4), 3.7 nV / vHz (TLV6741) at 10 kHz, low input bias current, and a typical input offset voltage of 0.15 mV.

9.2 Single-Supply Electret Microphone Preamplifier With Speech Filter

Electret microphones are commonly used in portable electronics because of their small size, low cost, and relatively good signal-to-noise ratio (SNR). The small package size, low operating voltage and excellent AC performance of the TLV674x family make it an excellent choice for preamplifier circuits for electret microphones. The circuit shown in Figure 9-1 is a single-supply preamplifier circuit for electret microphones, highlighting the TLV6741 device.

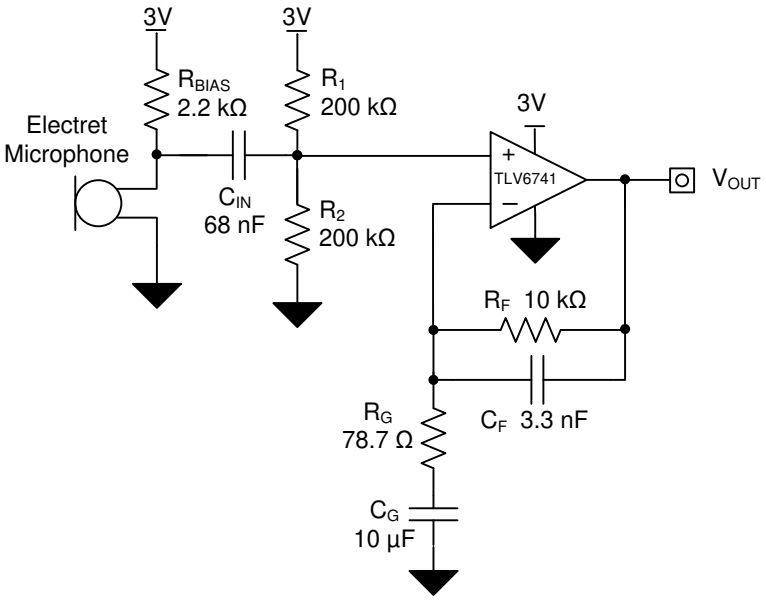


Figure 9-1. Microphone Preamplifier

9.2.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 3 V
- Input: 7.93 mV_{RMS} (0.63 Pa with a –38 dB SPL microphone)
- Output: 1 V_{RMS}
- Bandwidth: 300 Hz to 3 kHz

9.2.2 Detailed Design Procedure

The transfer function defining the relationship between V_{OUT} and the AC input signal is shown in Equation 1:

$$V_{OUT} = V_{IN\_AC} \times \left(1 + \frac{R_F}{R_G}\right) \quad (1)$$

The required gain can be calculated based on the expected input signal level and desired output level as shown in Equation 2:

$$G_{OPA} = \frac{V_{OUT}}{V_{IN\_AC}} = \frac{1V_{RMS}}{7.93mV_{RMS}} = 126\frac{V}{V} \quad (2)$$

Select a standard 10-kΩ feedback resistor and calculate R_G.

$$R_G = \frac{R_F}{G_{OPA} - 1} = \frac{10k\Omega}{126\frac{V}{V} - 1} = 80\Omega \rightarrow 78.7\Omega \text{ (closest standard value)} \quad (3)$$

To minimize the attenuation in the desired passband from 300 Hz to 3 kHz, set the upper (f_H) and lower (f_L) cutoff frequencies outside of the desired bandwidth as:

f_L = 200 Hz (4)

and

f_H = 5 kHz (5)

Select C_G to set the f_L cutoff frequency using Equation 6:

$$C_G = \frac{1}{2 \times \pi \times R_G \times f_L} = \frac{1}{2 \times \pi \times 78.7\Omega \times 200Hz} = 10.11\mu F \rightarrow 10\mu F \quad (6)$$

Select C_F to set the f_H cutoff frequency using Equation 7:

$$C_F = \frac{1}{2 \times \pi \times R_F \times f_H} = \frac{1}{2 \times \pi \times 10k\Omega \times 5kHz} = 3.18nF \rightarrow 3.3nF \text{ (Standard Value)} \quad (7)$$

The input signal cutoff frequency should be set low enough such that low-frequency sound waves still pass through. Therefore select C_{IN} to achieve a 30-Hz cutoff frequency (f_{IN}) using Equation 8:

$$C_{IN} = \frac{1}{2 \times \pi \times (R_1 \parallel R_2) \times f_{IN}} = \frac{1}{2 \times \pi \times 100k\Omega \times 30Hz} = 53nF \rightarrow 68nF \text{ (Standard Value)} \quad (8)$$

The measured transfer function for the microphone preamplifier circuit is shown in Figure 9-2 and the measured THD+N performance of the microphone preamplifier circuit is shown in Figure 9-3.

9.2.3 Application Curves

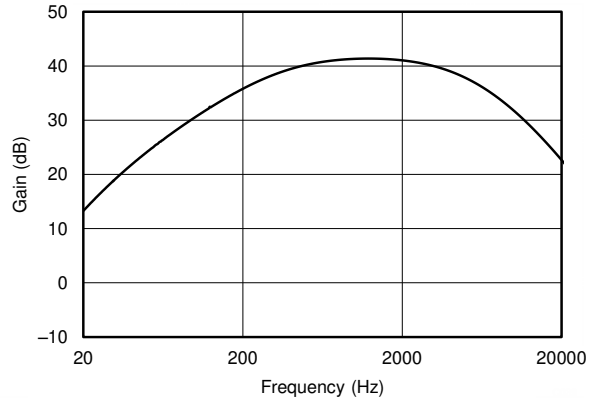


Figure 9-2. Gain vs Frequency

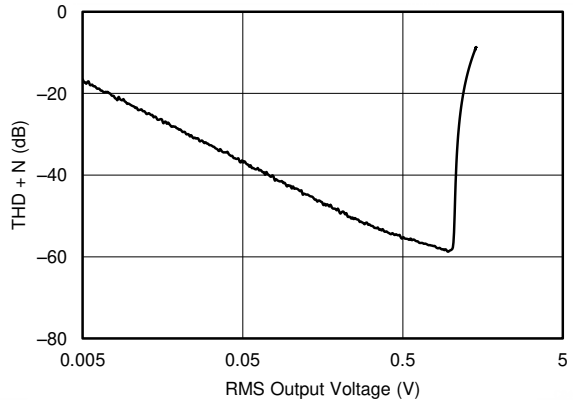


Figure 9-3. THD + N vs RMS Output Voltage

10 Power Supply Recommendations

The TLV6742 and TLV6744 devices are specified for operation from 1.7 V to 5.5 V (±0.85 V to ±2.75 V). The TLV6741 device is specified for operation from 2.25 V to 5.5 V (±1.125 V to ±2.75 V). Many specifications of the TLV674x family apply from –40°C to 125°C.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see Section 7.1).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see Section 11.1.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in Figure 11-1.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

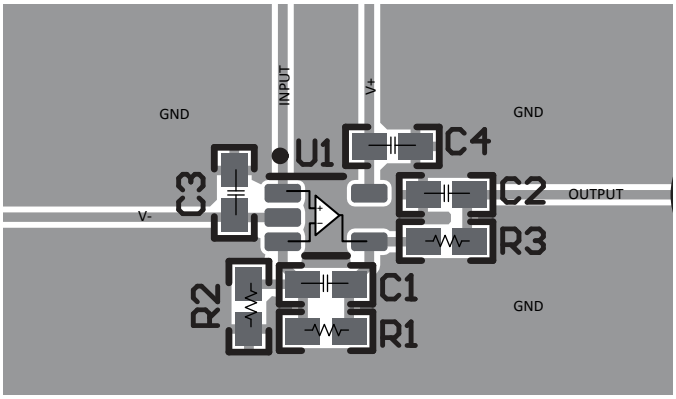


Figure 11-1. Operational Amplifier Board Layout for Noninverting Configuration

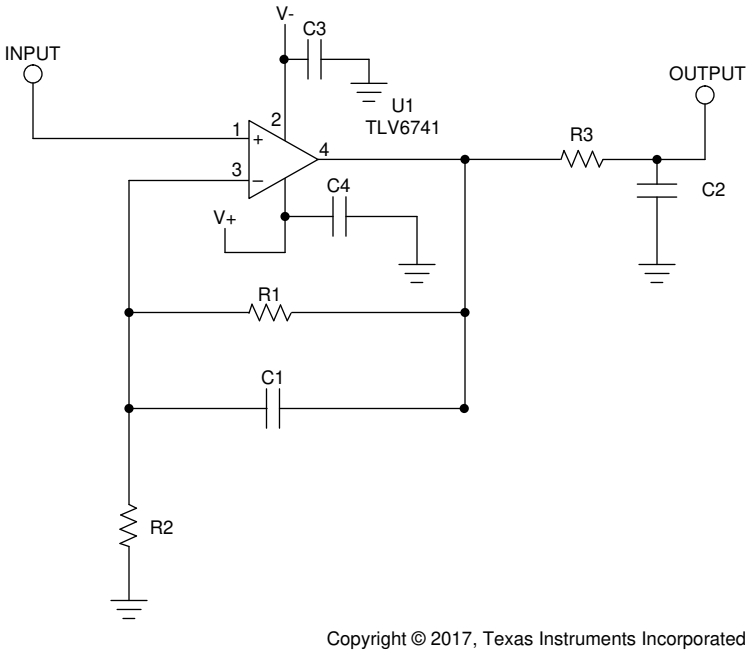


Figure 11-2. Schematic Used for Layout Example

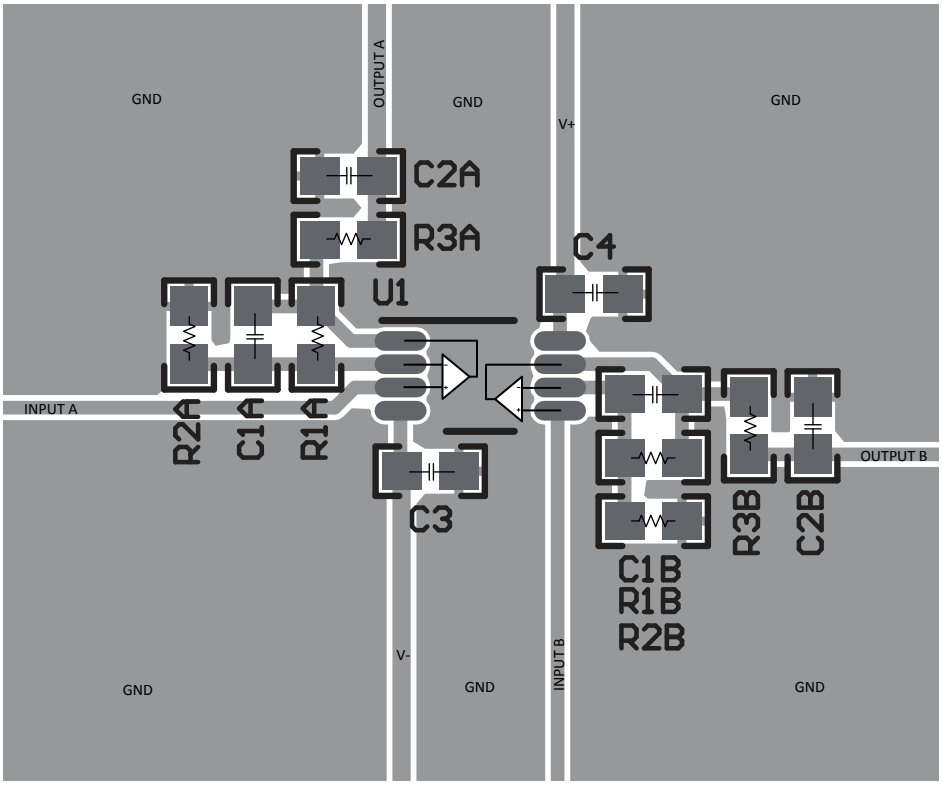


Figure 11-3. Example Layout for VSSOP-8 (DGK) Package

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *QFN/SON PCB Attachment*.
- *Quad Flatpack No-Lead Logic Packages*.
- *EMI Rejection Ratio of Operational Amplifiers*.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV6741DCKR	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	18E
TLV6741DCKR.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	18E
TLV6741DCKRG4	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	18E
TLV6741DCKRG4.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	18E
TLV6741DCKT	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	18E
TLV6741DCKT.A	Active	Production	SC70 (DCK) | 5	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	18E
TLV6742IDDFR	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T42D
TLV6742IDDFR.A	Active	Production	SOT-23-THIN (DDF) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T42D
TLV6742IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2H8T
TLV6742IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2H8T
TLV6742IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T6742D
TLV6742IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T6742D
TLV6742IDSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	D42S
TLV6742IDSGR.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	D42S
TLV6742IDSGRG4	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D42S
TLV6742IDSGRG4.A	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	D42S
TLV6742IPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T6742P
TLV6742IPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T6742P
TLV6742SIRUGR	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	HHF
TLV6742SIRUGR.A	Active	Production	X2QFN (RUG) | 10	3000 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	HHF

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

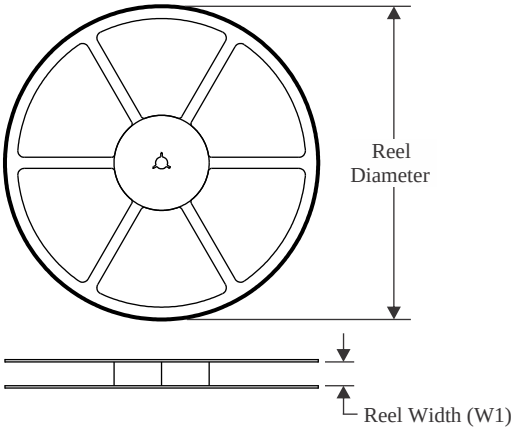
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

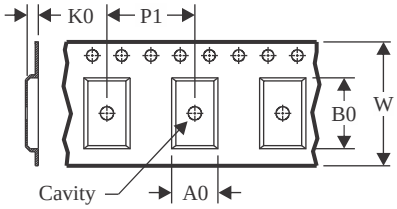
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

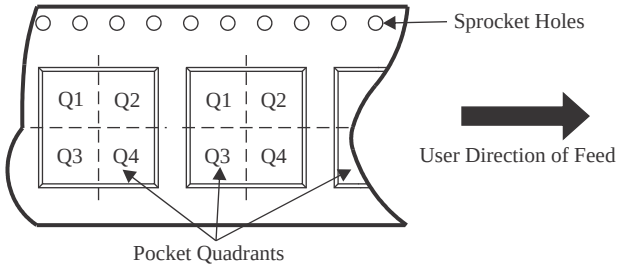


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

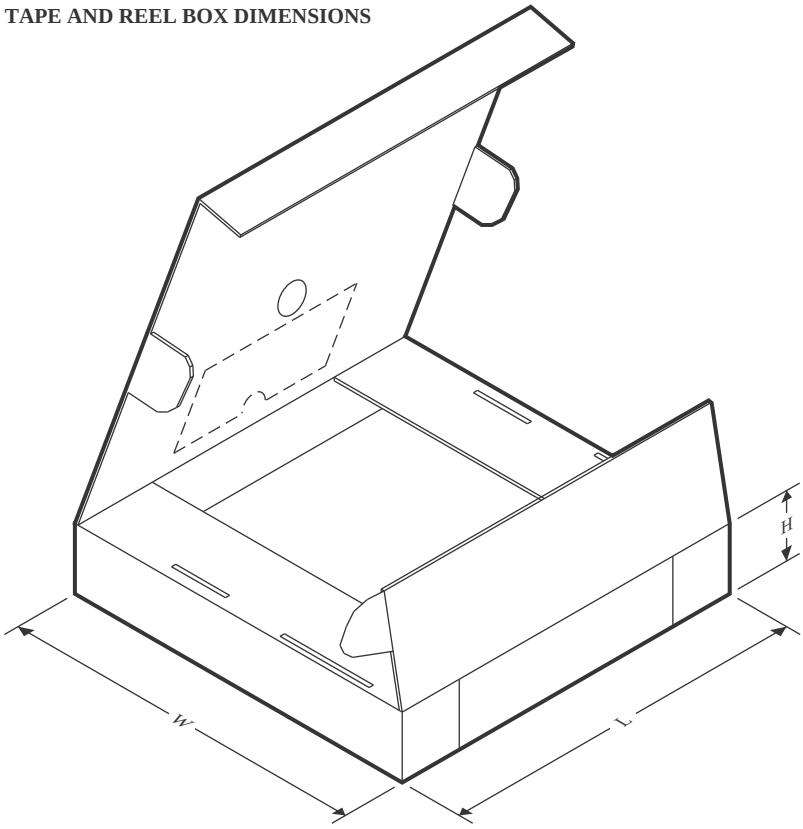
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV6741DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
TLV6741DCKRG4	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV6741DCKT	SC70	DCK	5	250	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
TLV6741DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV6742IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV6742IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV6742IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV6742IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV6742IDSGRG4	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV6742IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV6742SIRUGR	X2QFN	RUG	10	3000	178.0	8.4	1.75	2.25	0.56	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV6741DCKR	SC70	DCK	5	3000	208.0	191.0	35.0
TLV6741DCKRG4	SC70	DCK	5	3000	190.0	190.0	30.0
TLV6741DCKT	SC70	DCK	5	250	208.0	191.0	35.0
TLV6741DCKT	SC70	DCK	5	250	190.0	190.0	30.0
TLV6742IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV6742IDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV6742IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV6742IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV6742IDSGRG4	WSON	DSG	8	3000	210.0	185.0	35.0
TLV6742IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLV6742SIRUGR	X2QFN	RUG	10	3000	205.0	200.0	33.0

GENERIC PACKAGE VIEW

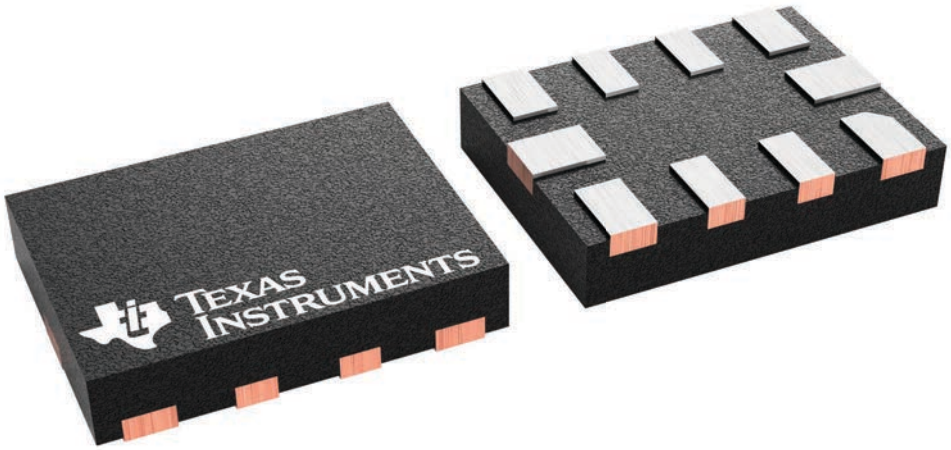
RUG 10

X2QFN - 0.4 mm max height

1.5 x 2, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



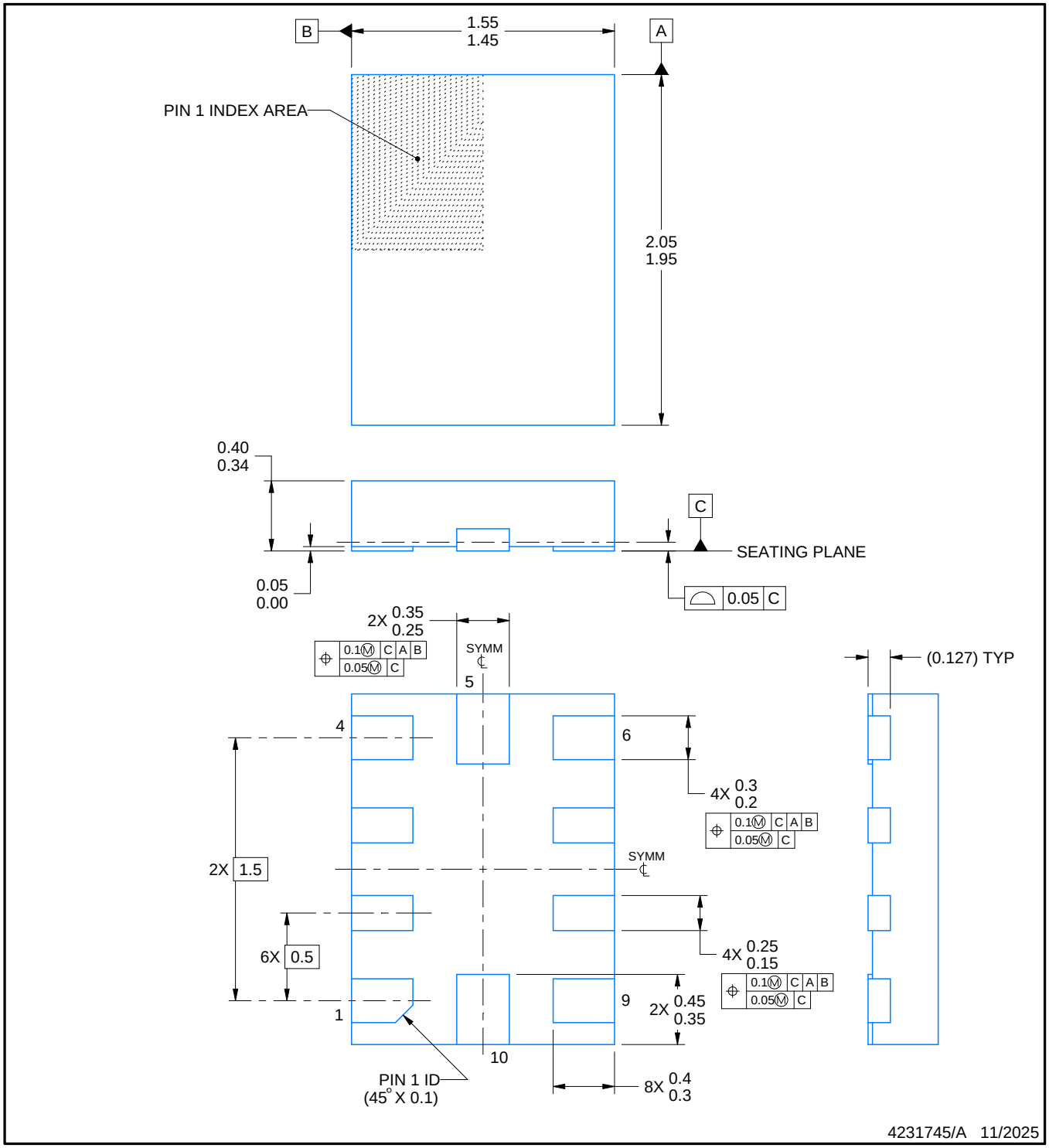
4231768/A

RUG0010A

PACKAGE OUTLINE

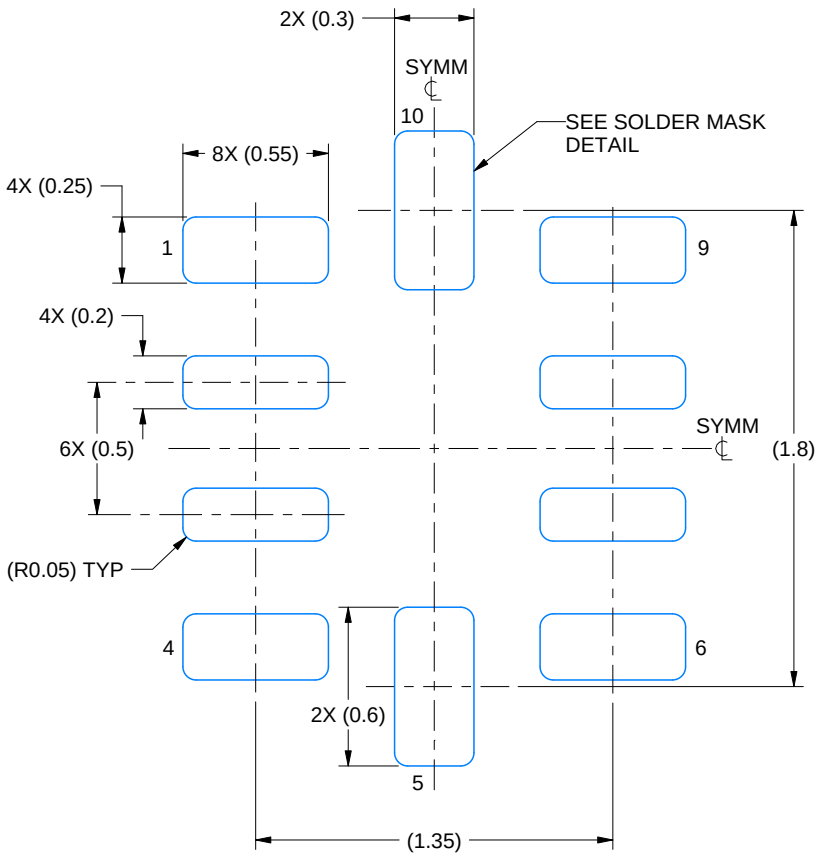
X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

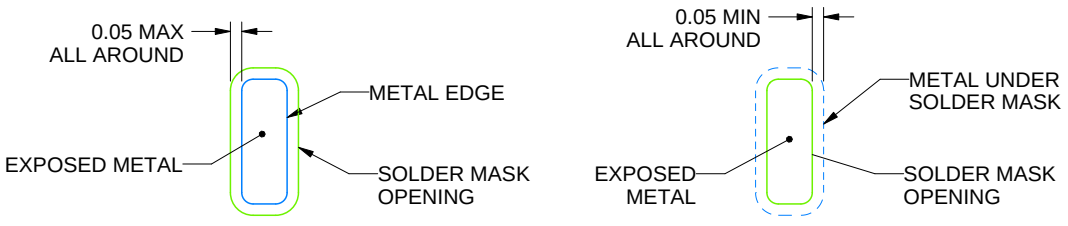


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 35X

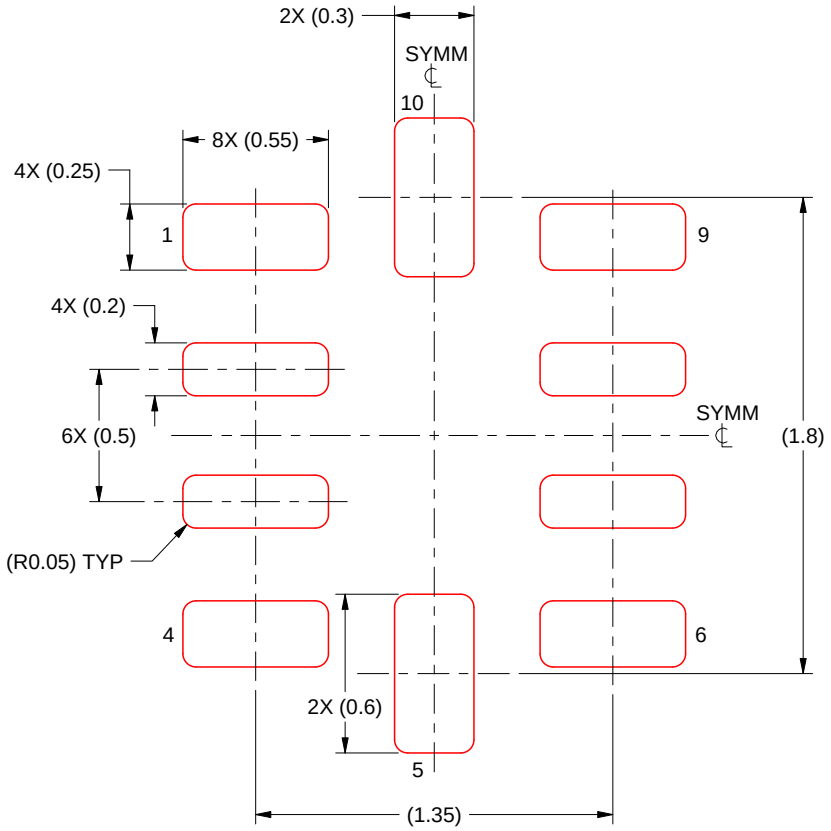


SOLDER MASK DETAILS

4231745/A 11/2025

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 35X

4231745/A 11/2025

NOTES: (continued)

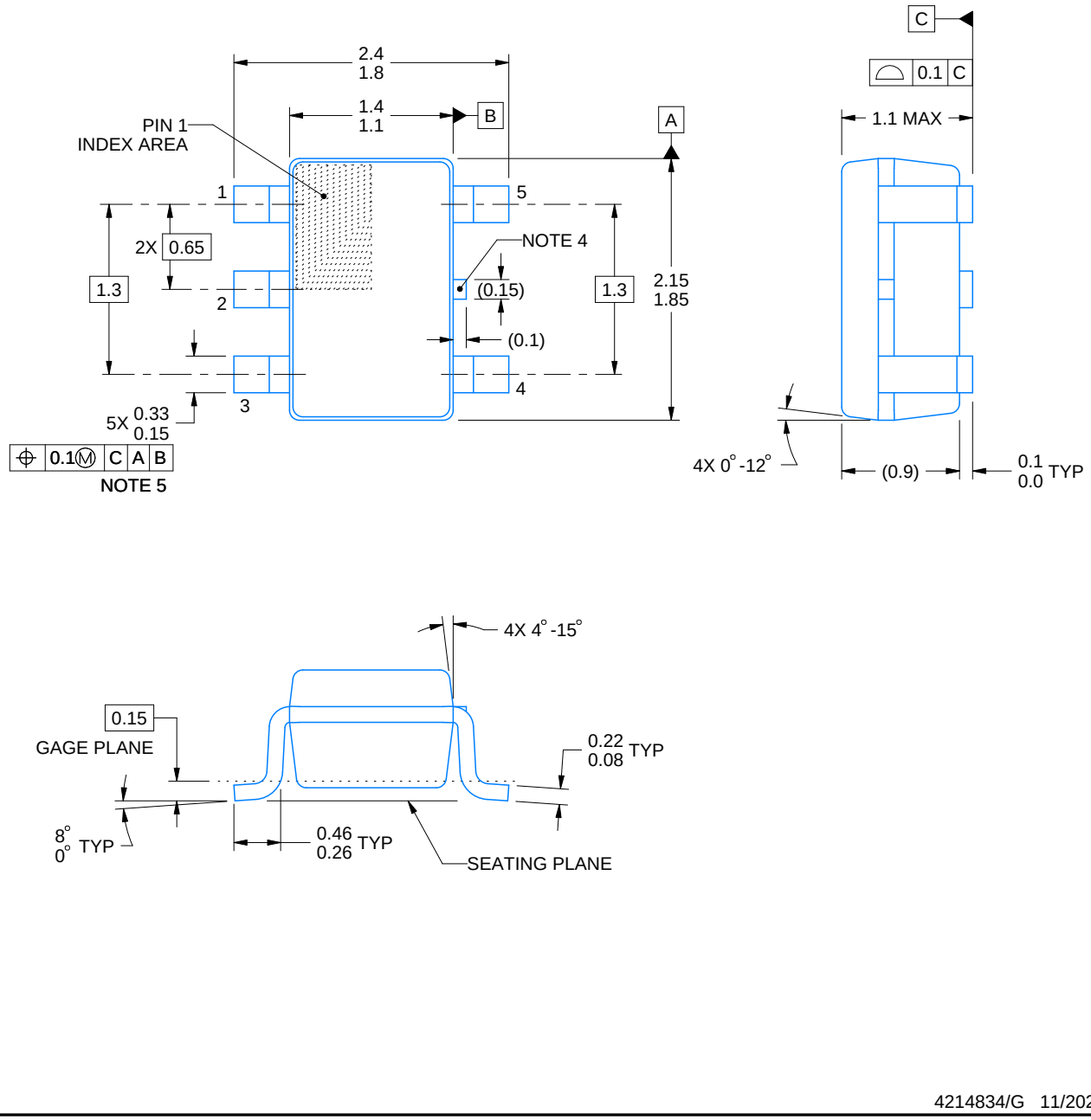
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

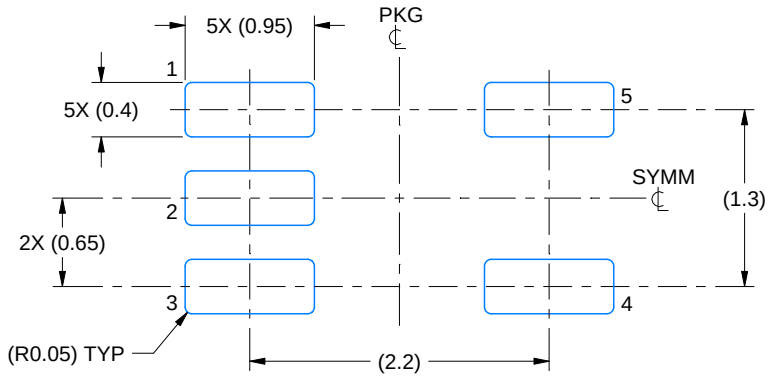
SMALL OUTLINE TRANSISTOR



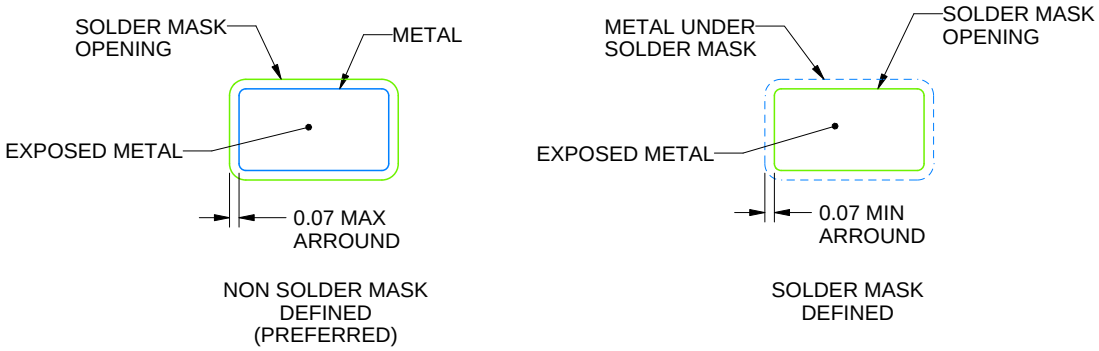
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

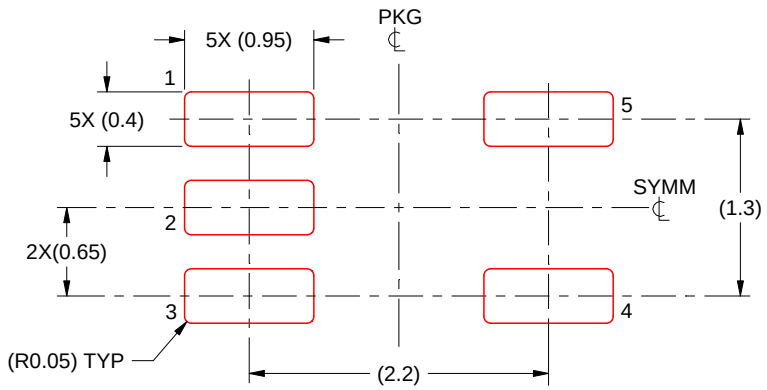


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

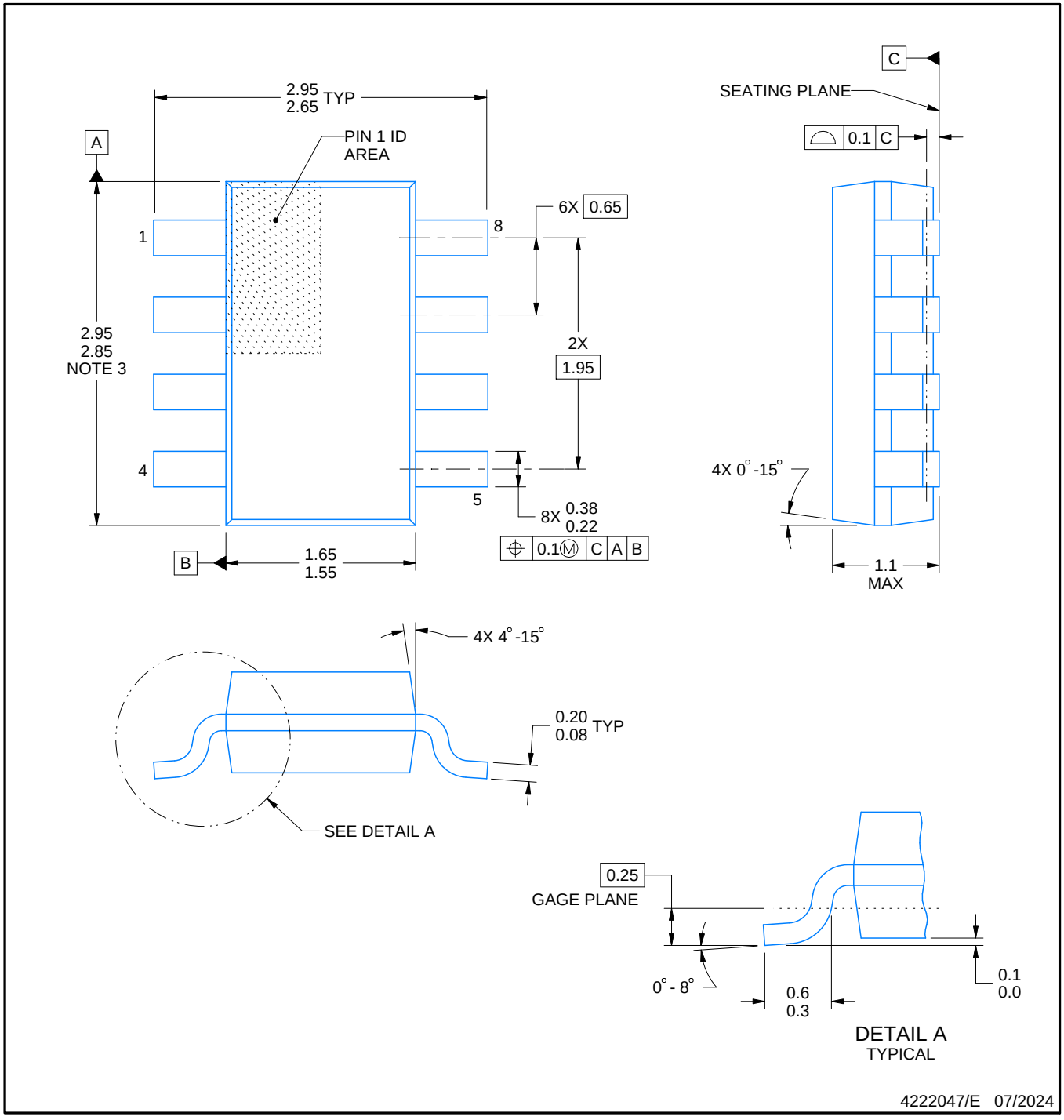
9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDF0008A

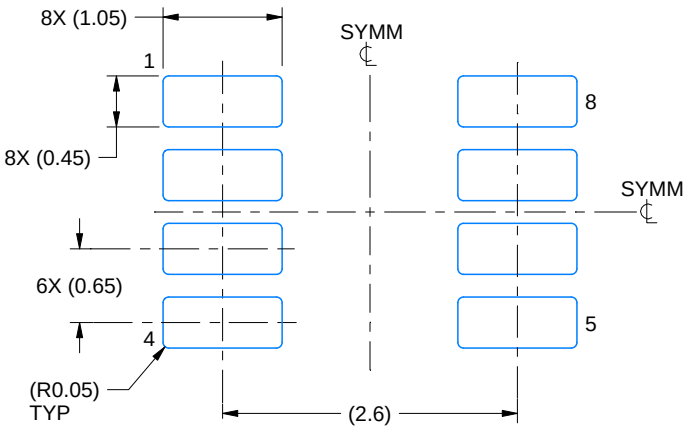
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

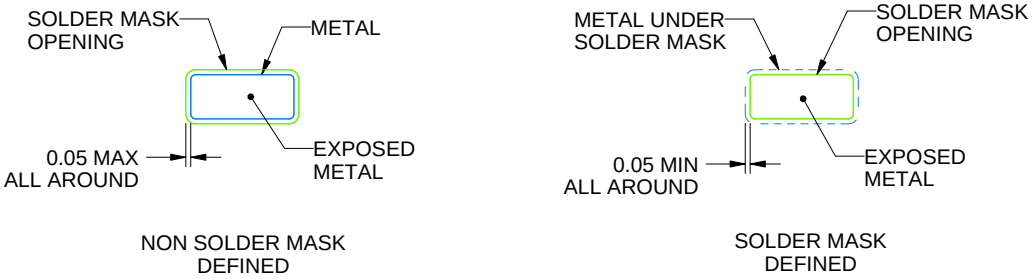


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

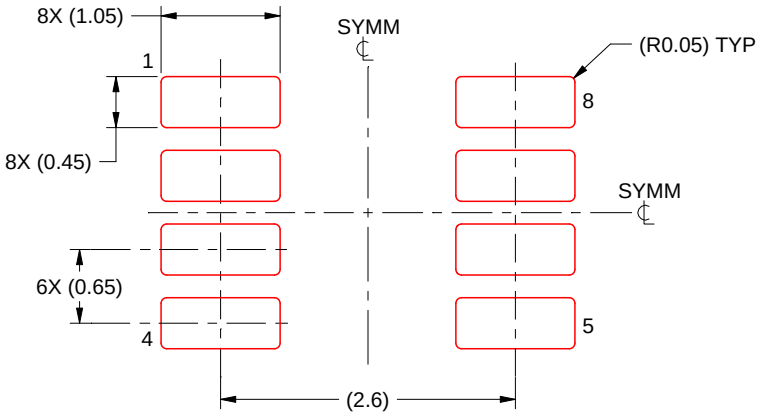
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

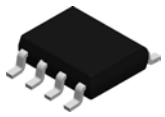


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

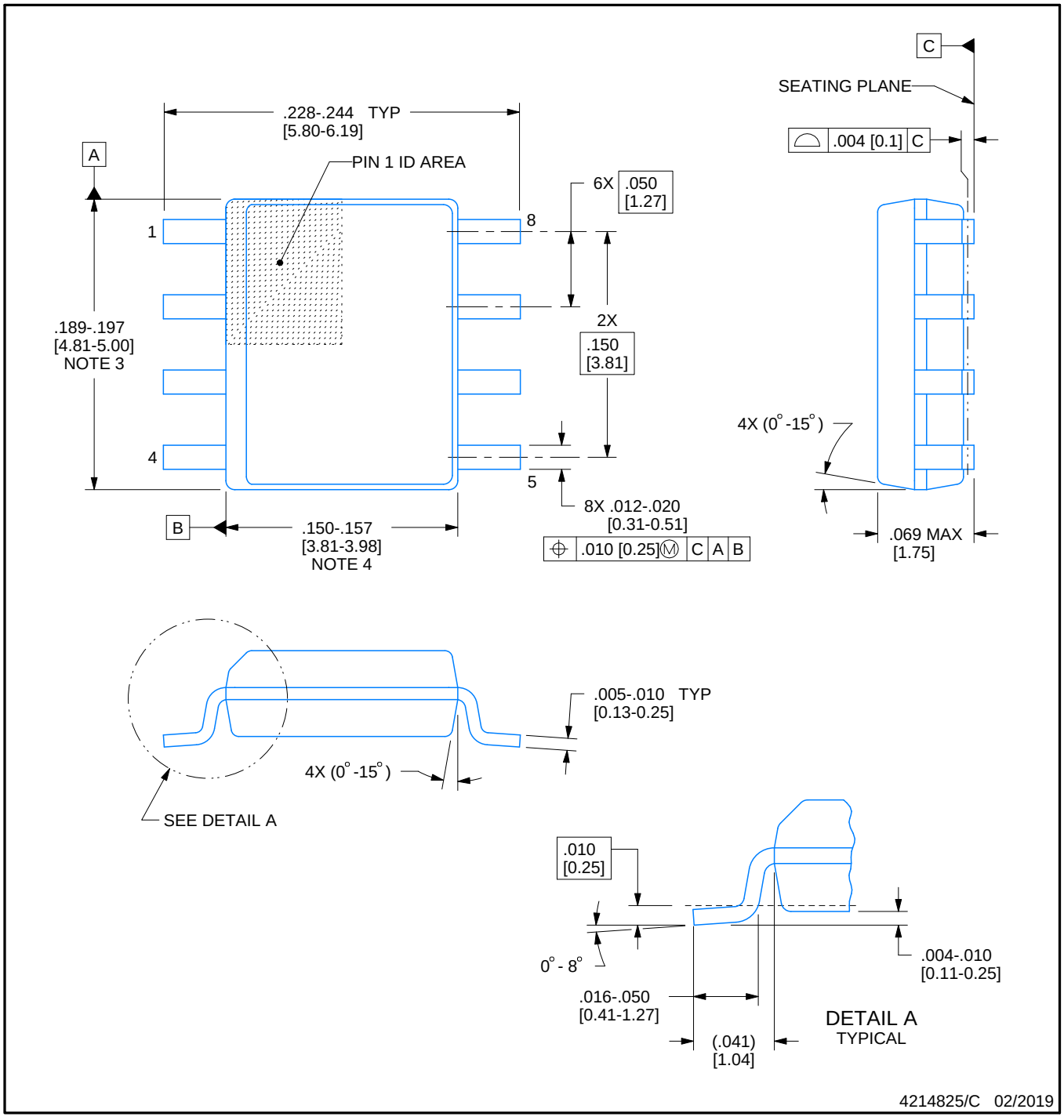


PACKAGE OUTLINE

D0008A

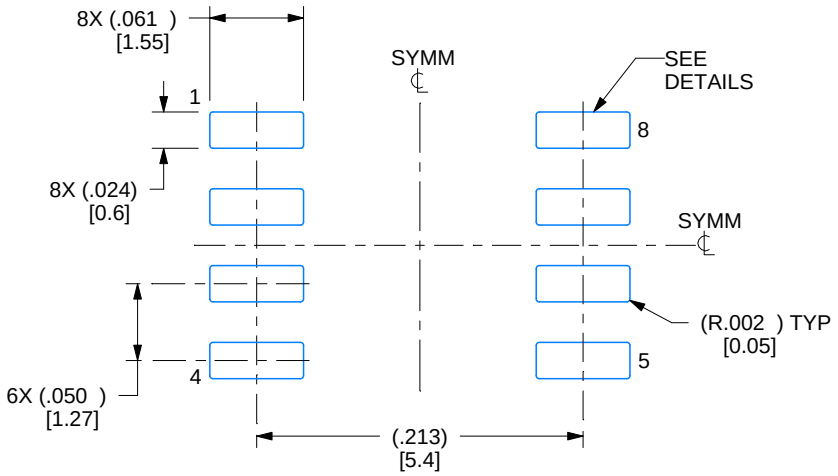
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

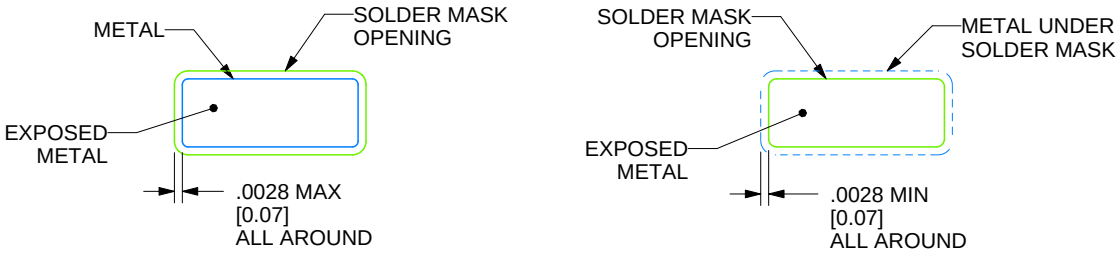


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

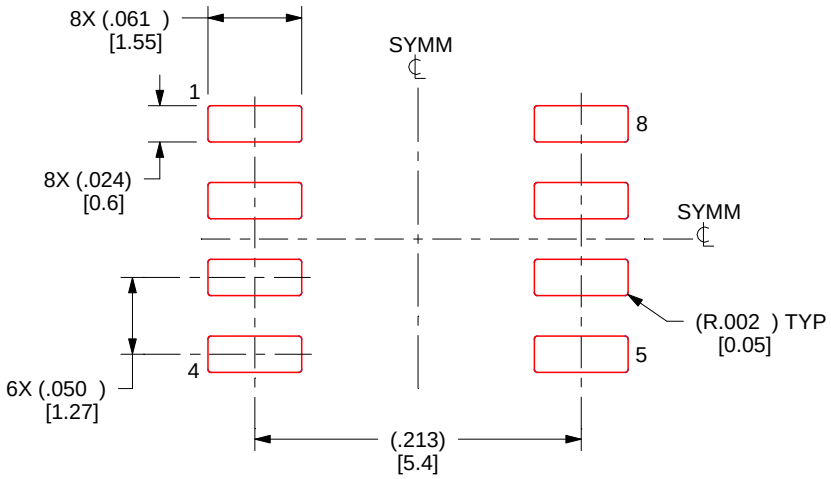
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

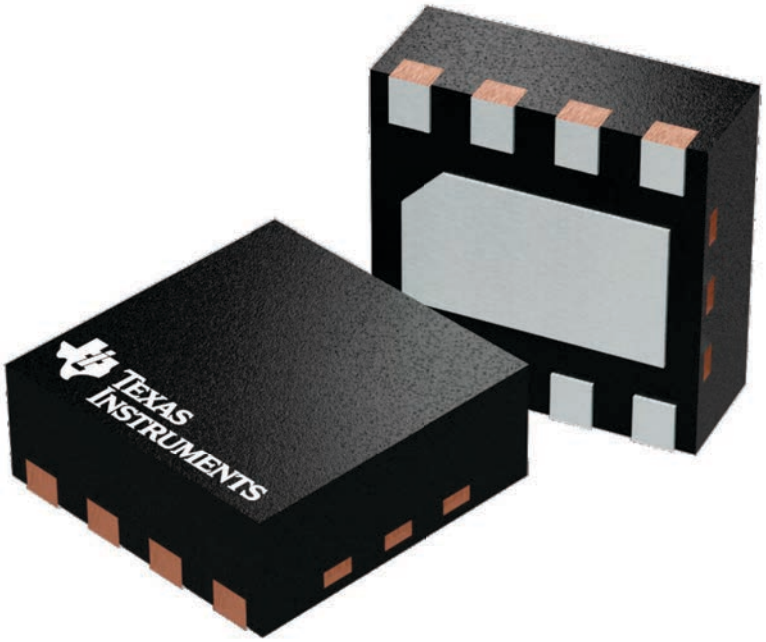
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



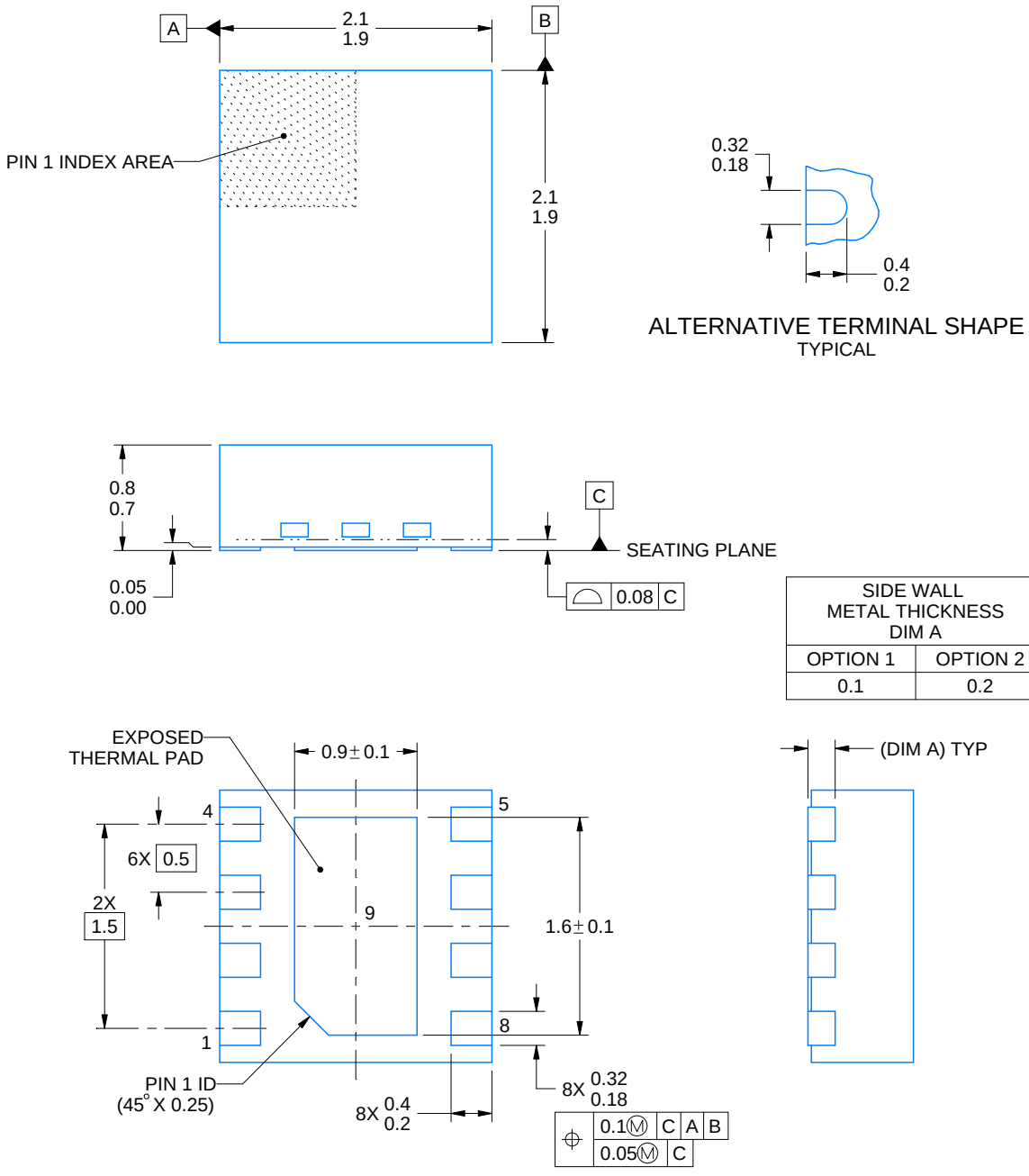
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

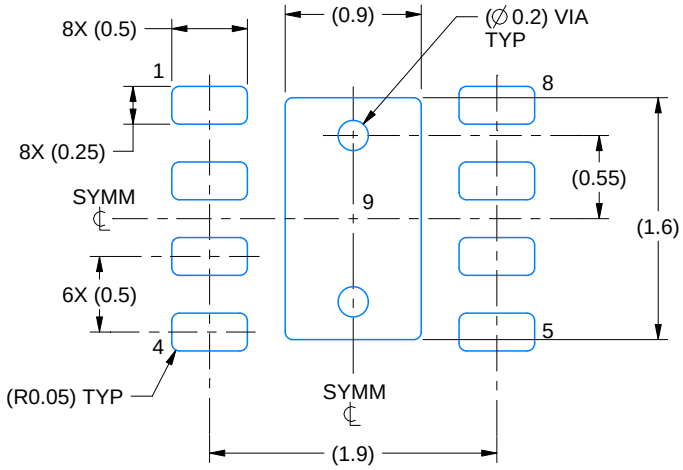
PLASTIC SMALL OUTLINE - NO LEAD



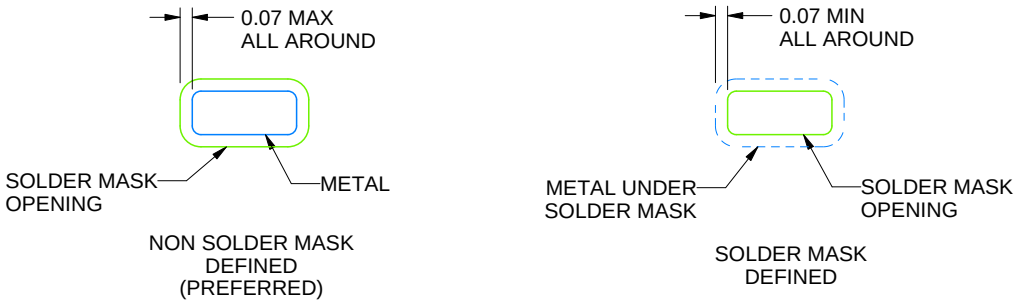
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

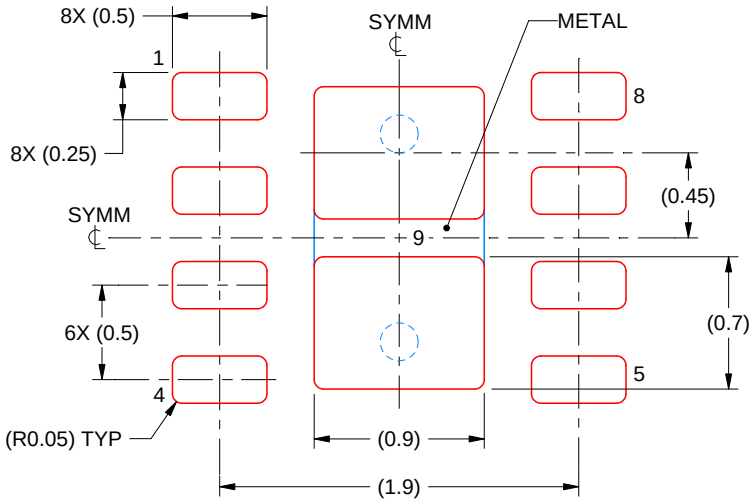


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

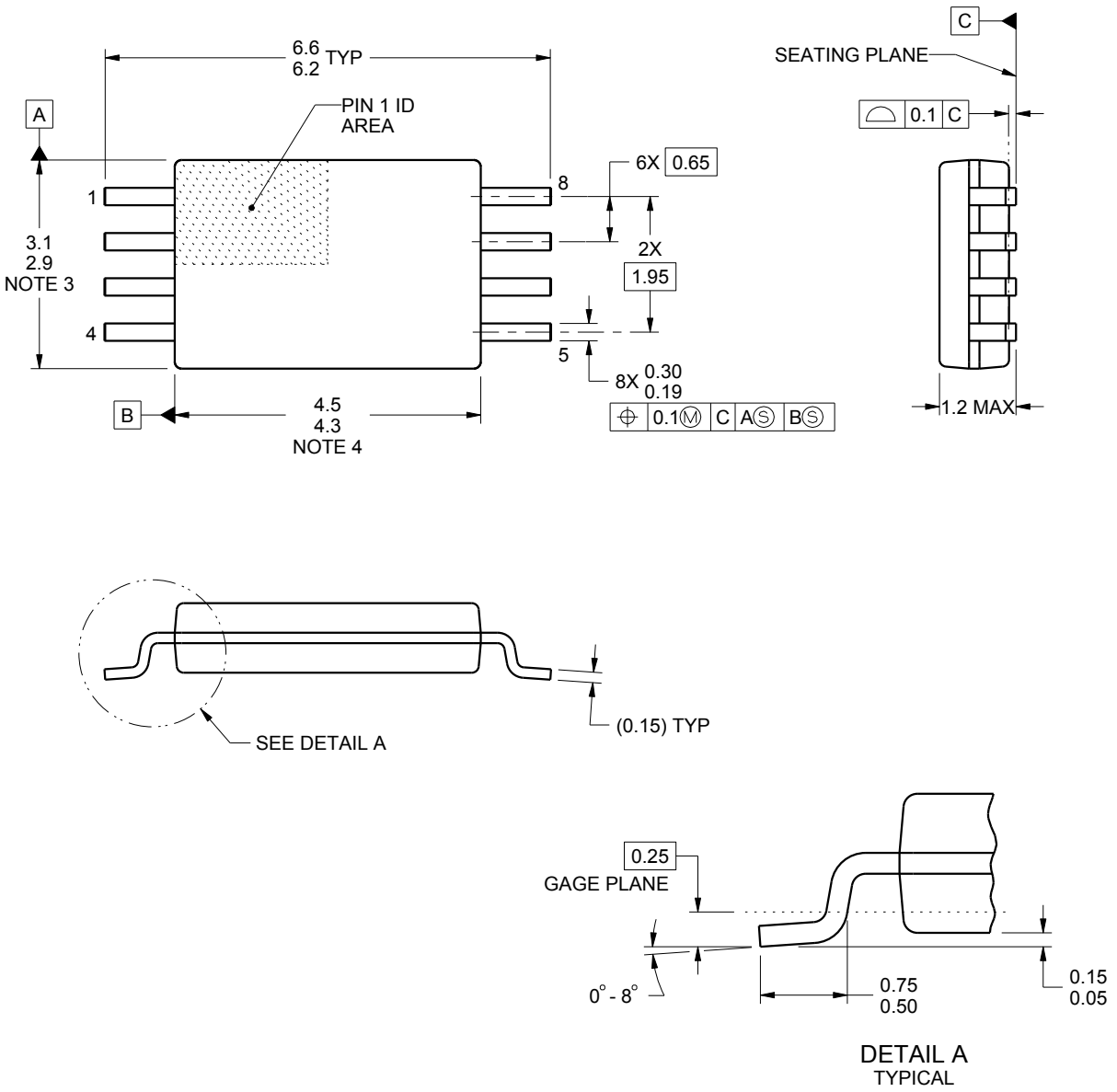
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0008A

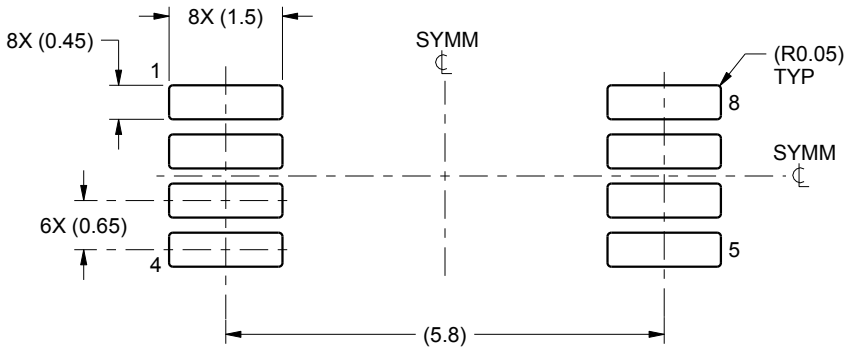
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

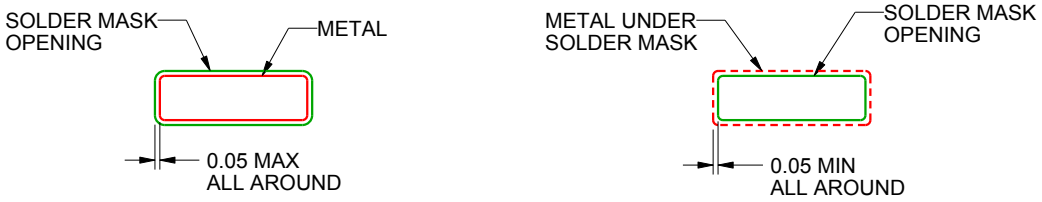


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

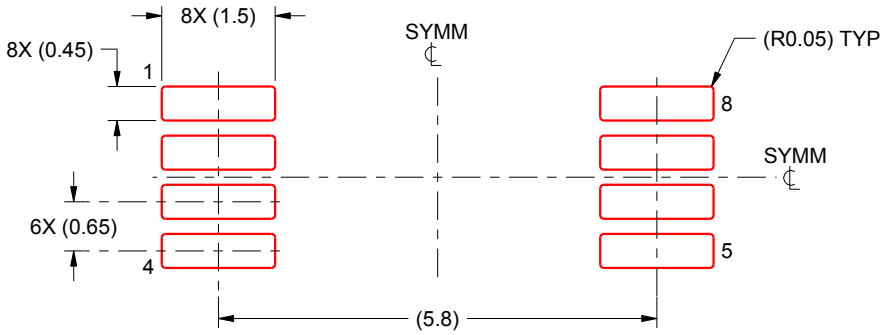


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

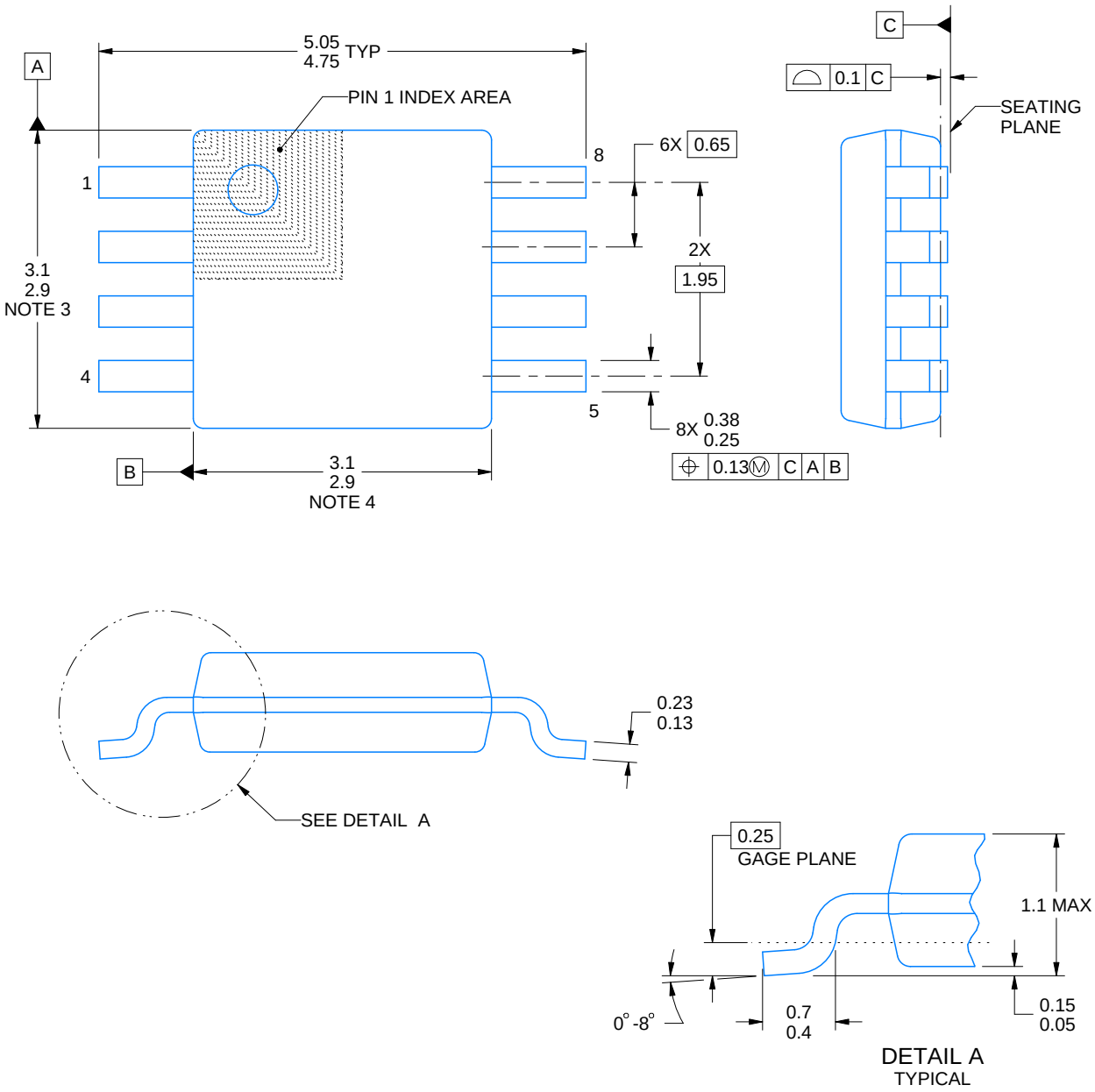
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

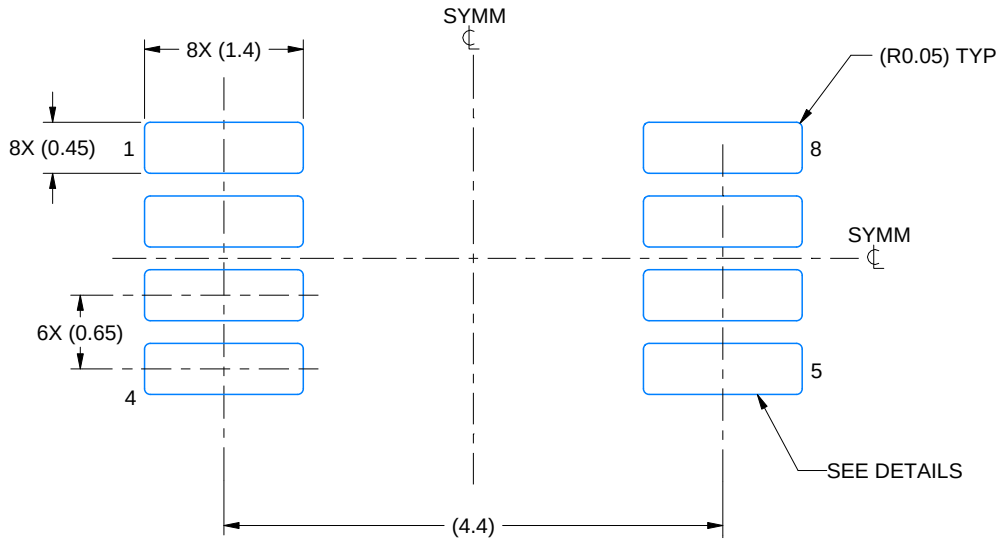
SMALL OUTLINE PACKAGE



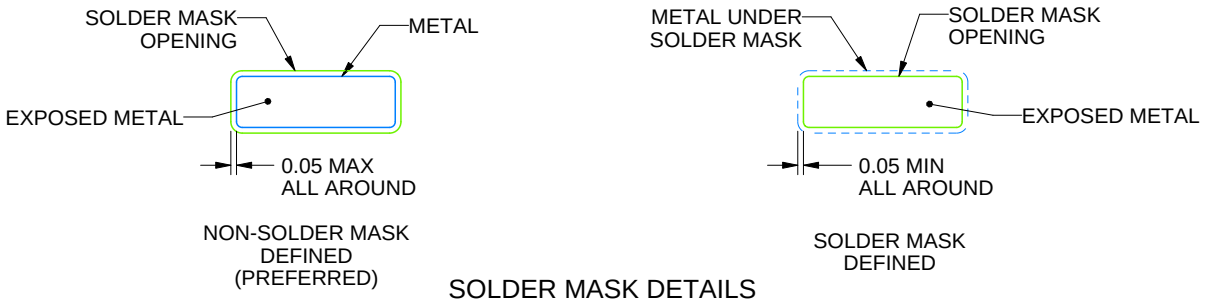
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

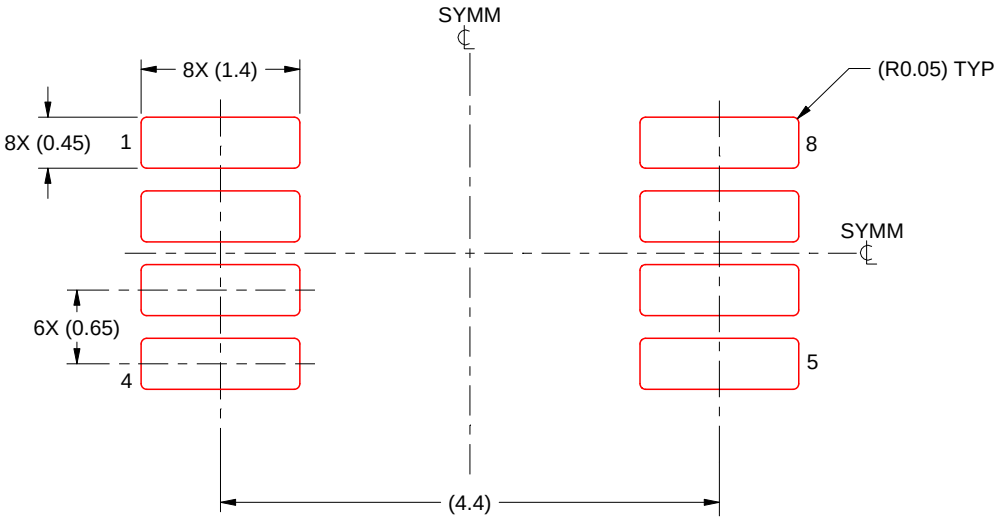


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025