# TLV758P 500-mA, High-Accuracy, Adjustable LDO in a Small Size Package

## 1 Features

- Input voltage range: 1.5 V to 6.0 V
- Adjustable output voltage:
  - 0.55 V to 5.5 V
- Low dropout:
  - 130 mV (max) at 500 mA (3.3 $V_{OUT}$)
- High output accuracy: 0.7% (typical) and 1% (maximum over temperature)
- $I_Q$: 25 µA (typical)
- Built-in soft-start with monotonic $V_{OUT}$ rise
- Packages:
  - 2-mm × 2-mm WSON-6 (DRV)
  - SOT23-5 (DBV)
- Active output discharge

## 2 Applications

- Gaming consoles
- Home theaters and entertainment
- PC and notebooks
- Connected peripherals and printers
- Rack and server power
- Thermostats
- Retail automation and payment

## 3 Description

The TLV758P is an adjustable 500-mA low-dropout (LDO) regulator . This device is available in a small, 6-pin, 2-mm × 2-mm WSON package and a 5-pin SOT23 package and consumes very low quiescent current and provides fast line and load transient performance. The TLV758P features an ultra-low dropout of 130 mV at 500 mA that can help improve the power efficiency of the system.

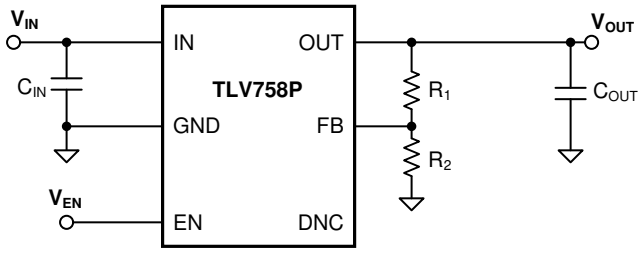
The TLV758P is optimized for a wide variety of applications by supporting an input voltage range from 1.5 V to 6.0 V and an externally adjustable output range of 0.55 V to 5.5 V. The low output voltage enables this LDO to power the modern microcontrollers with lower core voltages.

The TLV758P is stable with small ceramic output capacitors, allowing for a small overall solution size. A precision band-gap and error amplifier provides high accuracy of 0.7% (max) at 25°C and 1% (max) over temperature (85°C). This device includes integrated thermal shutdown, current limit, and undervoltage lockout (UVLO) features. The TLV758P has an internal foldback current limit that helps reduce the thermal dissipation during short-circuit events.

**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| TLV758P | DRV (WSON, 6) | 2 mm × 2 mm |
| | DBV (SOT-23, 5) | 2.9 mm × 2.8 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Typical Application**

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# 4 Pin Configuration and Functions

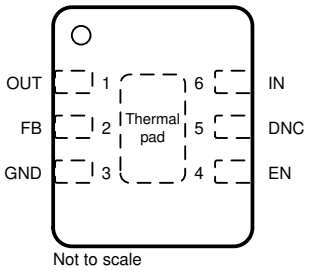



**Figure 4-1. DRV Package, 6-Pin Adjustable WSON (Top View)**

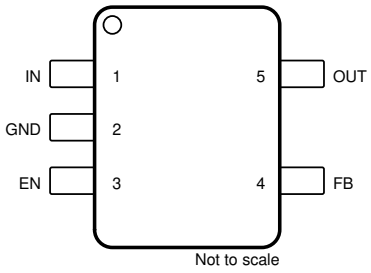



**Figure 4-2. DBV Package, 5-Pin Adjustable SOT-23 (Top View)**

**Table 4-1. Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| DNC | 5 | — | Do not connect |
| EN | 4 | Input | Enable pin. Drive EN greater than $V_{EN(HI)}$ to turn on the regulator. Drive EN less than $V_{EN(LO)}$ to put the LDO into shutdown mode. |
| FB | 2 | — | This pin is used as an input to the control loop error amplifier and is used to set the output voltage of the LDO. |
| GND | 3 | — | Ground pin |
| IN | 6 | Input | Input pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to ground as listed in the *Recommended Operating Conditions* table and the *Input and Output Capacitor Selection* section. Place the input capacitor as close to the output of the device as possible. |
| OUT | 1 | Output | Regulated output voltage pin. A capacitor is required from OUT to ground for stability. For best transient response, use the nominal recommended value or larger ceramic capacitor from OUT to ground; see the *Recommended Operating Conditions* table and the *Input and Output Capacitor Selection* section. Place the output capacitor as close to output of the device as possible. |
| Thermal pad | Pad | — | Connect the thermal pad to a large area GND plane for improved thermal performance. |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage | Supply, $V_{IN}$ | –0.3 | 6.5 | V |
| | Enable, $V_{EN}$ | –0.3 | 6.5 | |
| | Feedback, $V_{FB}$ | –0.3 | 2 | |
| | Output, $V_{OUT}$ | –0.3 | $V_{IN}$ + 0.3(2) | |
| Temperature | Operating junction, $T_J$ | –40 | 150 | °C |
| | Storage, $T_{stg}$ | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is $V_{IN}$ + 0.3V or 6.5 V, whichever is smaller.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage | 1.5 | | 6.0 | V |
| $V_{OUT}$ | Output voltage | 0.55 | | 5.5 | V |
| $I_{OUT}$ | Output current | 0 | | 500 | mA |
| $C_{IN}$ | Input capacitor | 1 | | | µF |
| $C_{OUT}$ | Output capacitor(1) | 1 | | 220 | µF |
| $V_{EN}$ | Enable voltage(2) | 0 | | 6.0 | V |
| $f_{EN}$ | Enable toggle frequency | | | 10 | kHz |
| $T_J$ | Junction temperature | –40 | | 125 | °C |

(1) Minimum derated capacitance of 0.47 µF is required for stability.
(2) If $V_{EN}$ > $V_{IN,}$ when $V_{EN}$ > $V_{UVLO}$ rising (min), the input pin (IN) must sink 1 mA of current to avoid the device being turn on with floating input pin.

## 5.4 Thermal Information

| THERMAL METRIC(1) | | TLV758P | | UNIT |
|---|---|---|---|---|
| | | DBV (SOT-23) | DRV (WSON) | |
| | | 5 PINS | 6 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 176.9 | 80.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 95.3 | 98.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 45.0 | 44.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 21.0 | 6.1 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 44.8 | 45.0 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | 20.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

## 5.5 Electrical Characteristics

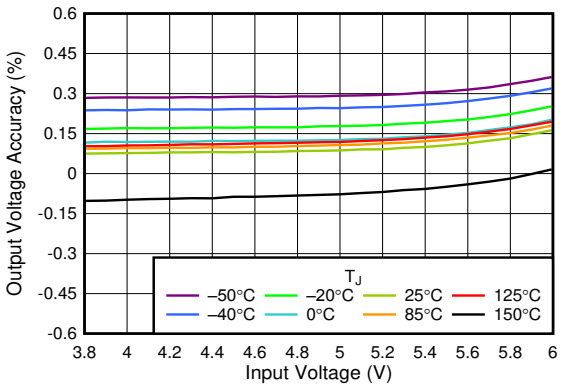
at operating temperature range ($T_J$ = –40°C to +125°C),$V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted); all typical values are at $T_J$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{FB}$ | Feedback voltage | $T_J$ = 25°C | | | 0.55 | | V |
| | Output accuracy(1) | $T_J$ = 25°C | | –0.7% | | 0.7% | |
| | | –40°C ≤ $T_J$ ≤ +85°C | | –1% | | 1% | |
| | | –40°C ≤ $T_J$ ≤ +125°C | | –1.5% | | 1.5% | |
| | Line regulation | $V_{OUT(NOM)}$ + 0.5 V(2) ≤ $V_{IN}$ ≤ 6.0 V | | | 2 | 7.5 | mV |
| | Load regulation | 0.1 mA ≤ $I_{OUT}$ ≤ 500 mA, $V_{IN}$ ≥ 2.0 V | | | 0.030 | | V/A |
| $I_{GND}$ | Ground current | $I_{OUT}$ = 0 mA | $T_J$ = 25°C | 10 | 25 | 31 | µA |
| $I_{GND}$ | Ground current | | –40°C ≤ $T_J$ ≤ +125°C | | | 35 | µA |
| $I_{SHDN}$ | Shutdown current | $V_{EN}$ ≤ 0.3 V, 1.5 V ≤ $V_{IN}$ ≤ 6.0 V | | | 0.1 | 1 | µA |
| $I_{FB}$ | Feedback pin current | | | | 0.01 | 0.1 | µA |
| $I_{CL}$ | Output current limit | $V_{IN}$ = $V_{OUT(NOM)}$ + 1.0 V | $V_{OUT}$ = $V_{OUT(NOM)}$ – 0.2 V, $V_{OUT}$ < 1.5 V | 530 | 720 | 865 | mA |
| | | | $V_{OUT}$ = 0.9 V × $V_{OUT(NOM)}$, $V_{OUT}$ ≥ 1.5 V | 530 | 720 | 865 | |
| $I_{SC}$ | Short-circuit current limit | $V_{IN}$ = $V_{OUT(NOM)}$ + 1.0 V | $V_{OUT}$ = 0 V | | 350 | | mA |
| $V_{DO}$ | Dropout voltage | $I_{OUT}$ = 500 mA, –40°C ≤ $T_J$ ≤ +125°C, $V_{OUT}$ = 0.95 × $V_{OUT(NOM)}$ | 0.65 V ≤ $V_{OUT}$ < 0.8 V | | 720 | 880 | mV |
| | | | 0.8 V ≤ $V_{OUT}$ < 1.0 V | | 585 | 750 | |
| | | | 1.0 V ≤ $V_{OUT}$ < 1.2 V | | 420 | 570 | |
| | | | 1.2 V ≤ $V_{OUT}$ < 1.5 V | | 285 | 400 | |
| | | | 1.5 V ≤ $V_{OUT}$ < 1.8 V | | 180 | 235 | |
| | | | 1.8 V ≤ $V_{OUT}$ < 2.5 V | | 140 | 185 | |
| | | | 2.5 V ≤ $V_{OUT}$ < 3.3 V | | 102 | 140 | |
| | | | 3.3 V ≤ $V_{OUT}$ ≤ 5.5 V | | 95 | 130 | |
| PSRR | Power-supply rejection ratio | $V_{IN}$ = $V_{OUT(NOM)}$ + 1.0 V, $I_{OUT}$ = 50 mA | f = 1 kHz | | 50 | | dB |
| | | | f = 100 kHz | | 45 | | |
| | | | f = 1 MHz | | 30 | | |
| $V_n$ | Output noise voltage | BW = 10 Hz to 100 kHz, $V_{OUT}$ = 0.9 V | | | 53 | | $µV_{RMS}$ |
| $V_{UVLO}$ | Undervoltage lockout | $V_{IN}$ rising | | 1.21 | 1.33 | 1.47 | V |
| | | $V_{IN}$ falling | | 1.17 | 1.29 | 1.42 | V |
| $V_{UVLO, HYST}$ | Undervoltage lockout hysteresis | $V_{IN}$ Hysteresis | | | 40 | | mV |
| $t_{STR}$ | Start-up time | From EN low-to-high transition to $V_{OUT}$ = $V_{OUT(NOM)}$ × 95% | | | 500 | | µs |
| $V_{EN(HI)}$ | EN pin high voltage | | | 1.0 | | | V |
| $V_{EN(LO)}$ | EN pin low voltage | | | | | 0.3 | V |
| $I_{EN}$ | Enable pin current | $V_{IN}$ = EN = 6.0 V | | | 10 | | nA |
| $R_{PULL DOWN}$ | Pulldown resistance | $V_{IN}$ = 6.0 V | | | 95 | | Ω |
| $T_{SD}$ | Thermal shutdown | Shutdown, temperature increasing | | | 170 | | °C |
| | | Reset, temperature decreasing | | | 155 | | |

(1) When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included
(2) $V_{IN}$ = 1.5 V for $V_{OUT}$ < 1.0 V.

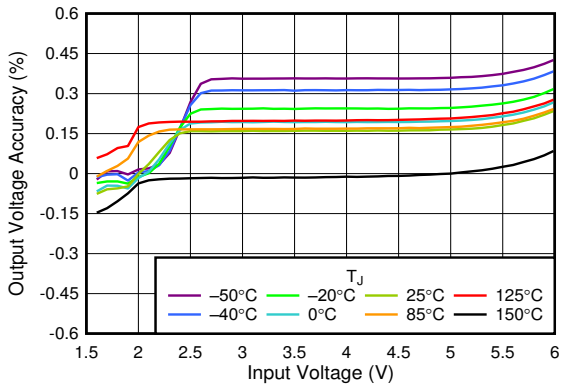
## 5.6 Typical Characteristics

at operating temperature range $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)



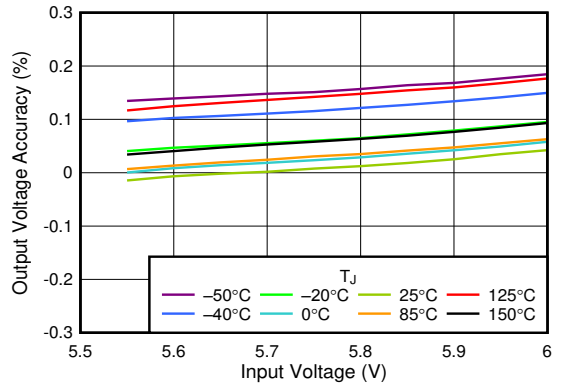

$V_{OUT}$ = 3.3 V, $I_{OUT}$ = 1 mA

**Figure 5-1. 3.3-V Line Regulation vs $V_{IN}$**




$V_{OUT}$ = 0.55 V, $I_{OUT}$ = 1 mA

**Figure 5-2. 0.55-V Line Regulation vs $V_{IN}$**




$V_{OUT}$ = 5.5 V, $I_{OUT}$ = 1 mA

**Figure 5-3. 5.5-V Line Regulation vs $V_{IN}$**

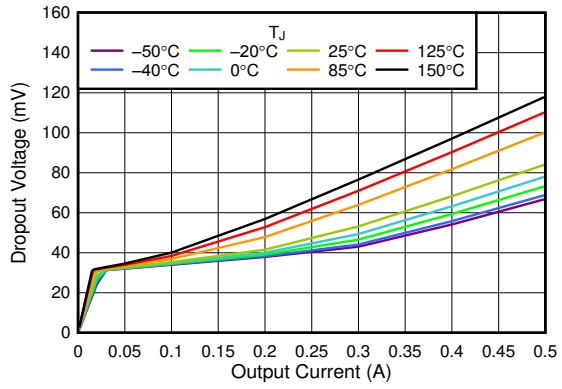



**Figure 5-4. 3.3-V Dropout Voltage vs $I_{OUT}$**

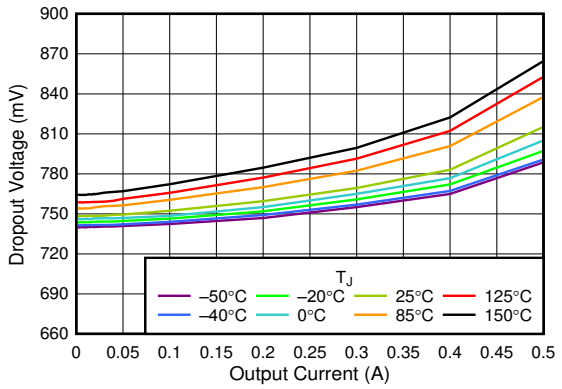



**Figure 5-5. 0.55-V Dropout Voltage vs $I_{OUT}$**

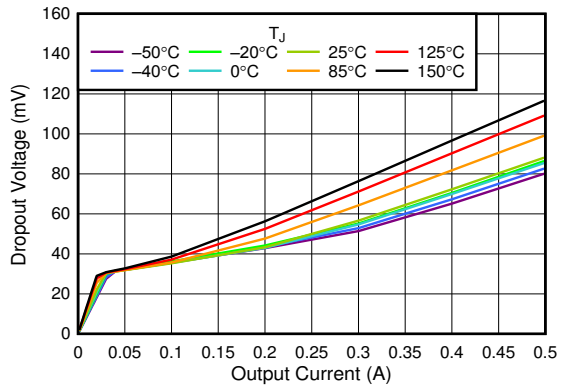
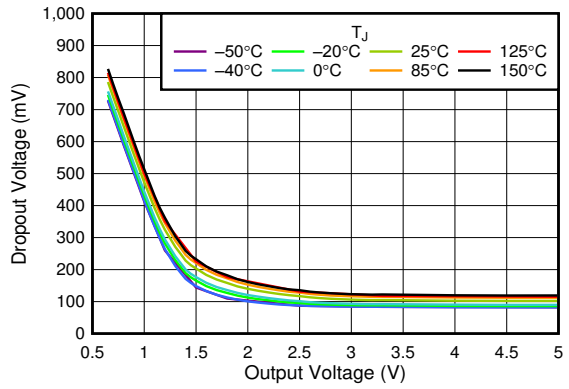



**Figure 5-6. 5.5-V Dropout Voltage vs $I_{OUT}$**

## 5.6 Typical Characteristics (continued)

at operating temperature range $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)




$I_{OUT}$ = 500 mA

**Figure 5-7. $V_{DO}$ vs $V_{OUT}$**

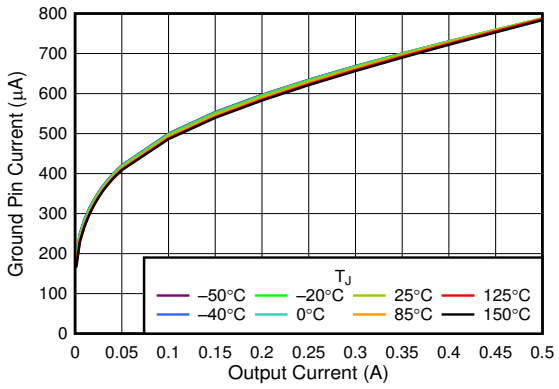
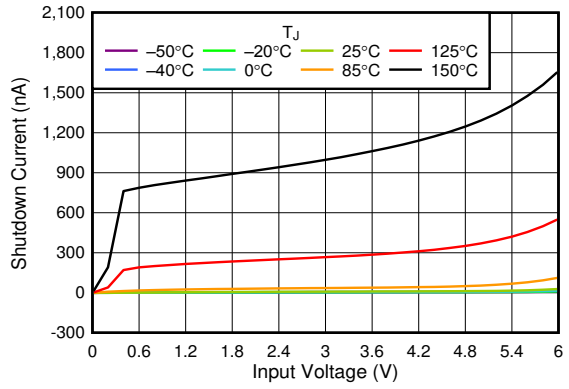
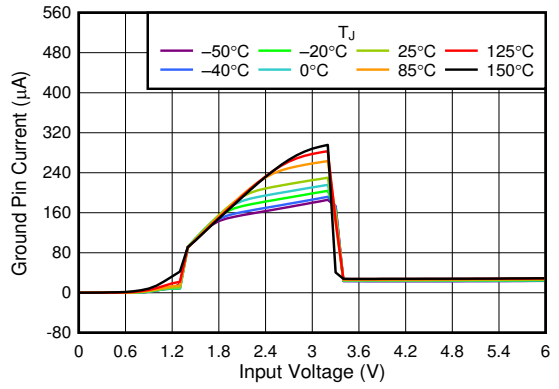



**Figure 5-8. $I_{GND}$ vs $I_{OUT}$**



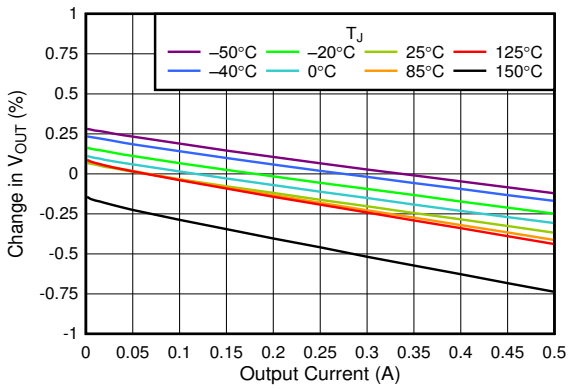

$V_{EN}$ = 0 V

**Figure 5-9. $I_{SHDN}$ vs $V_{IN}$**



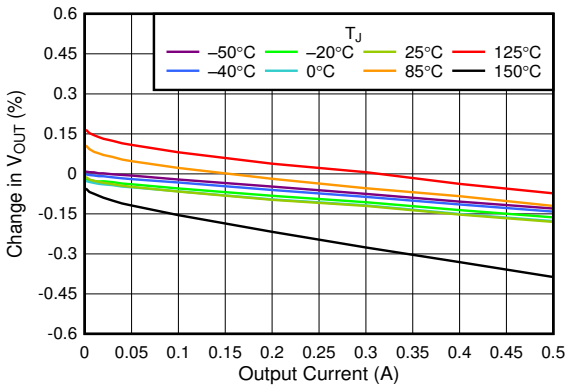

$V_{OUT}$ = 3.3 V, $I_{OUT}$ = 0 mA

**Figure 5-10. $I_Q$ vs $V_{IN}$**




$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V

**Figure 5-11. 3.3-V Load Regulation vs $I_{OUT}$**

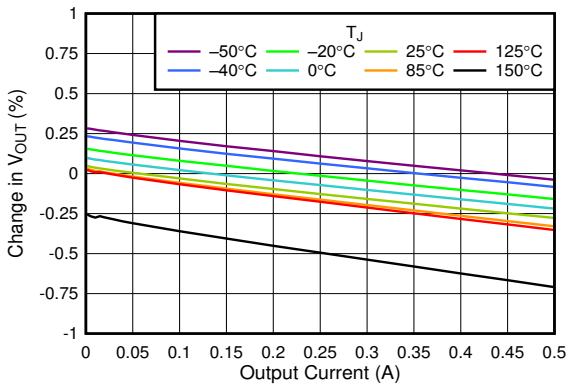



$V_{IN}$ = 2 V, $V_{OUT}$ = 0.55 V

**Figure 5-12. 0.55-V Load Regulation vs $I_{OUT}$**

## 5.6 Typical Characteristics (continued)

at operating temperature range $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)




$V_{IN}$ = 6 V, $V_{OUT}$ = 5.5 V

**Figure 5-13. 5.5-V Load Regulation vs $I_{OUT}$**

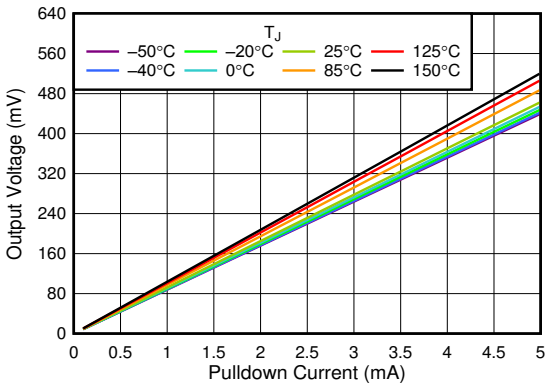



**Figure 5-14. $V_{OUT}$ vs $I_{OUT}$ Pulldown Resistor**

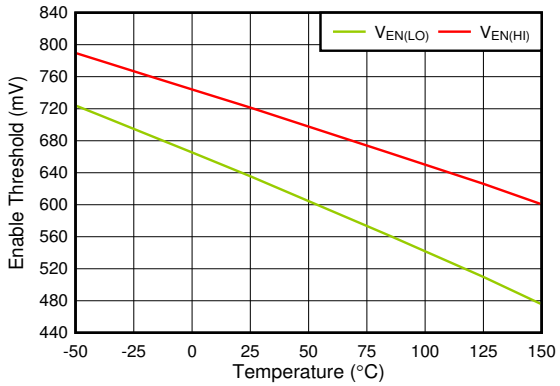
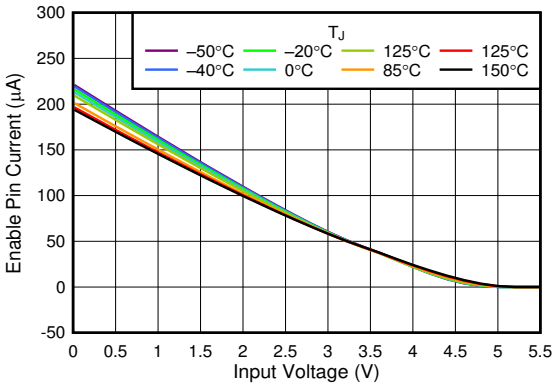



**Figure 5-15. $V_{EN(HI)}$ and $V_{EN(LO)}$ vs Temperature**




$V_{EN}$ = 5.5 V

**Figure 5-16. $I_{EN}$ vs $V_{IN}$**

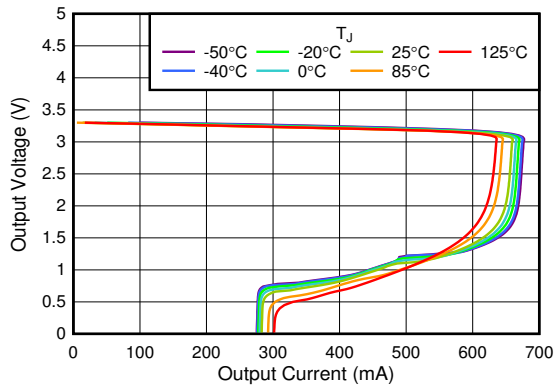
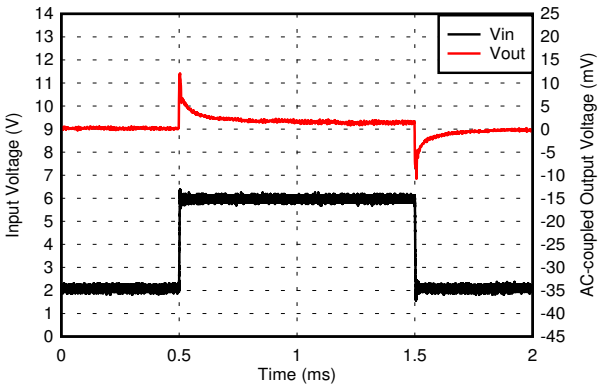



**Figure 5-17. 3.3-V Foldback Current Limit vs $I_{OUT}$**

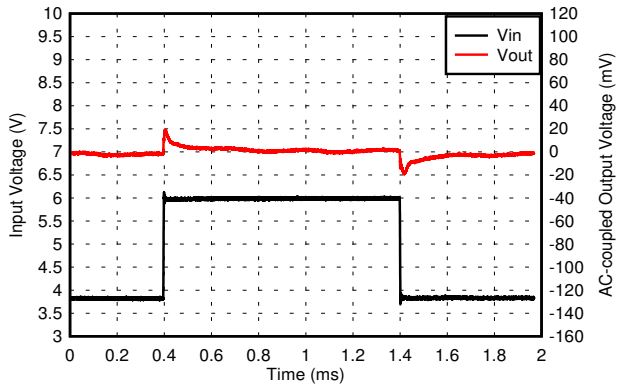



$V_{OUT}$ = 0.55 V, $I_{OUT}$ = 1 mA, $V_{IN}$ slew rate = 1 V/µs

**Figure 5-18. 0.55-V Line Transient**

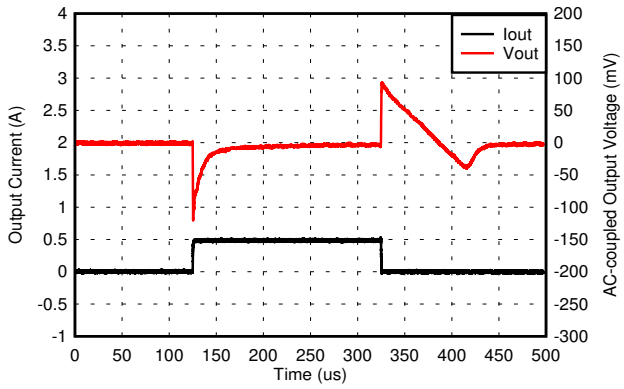
## 5.6 Typical Characteristics (continued)

at operating temperature range $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)



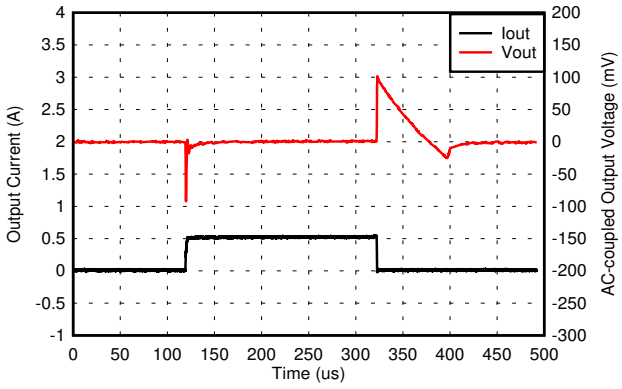

$V_{OUT}$ = 3.3 V, $I_{OUT}$ = 1 mA, $V_{IN}$ slew rate = 1 V/µs

**Figure 5-19. 3.3-V Line Transient**



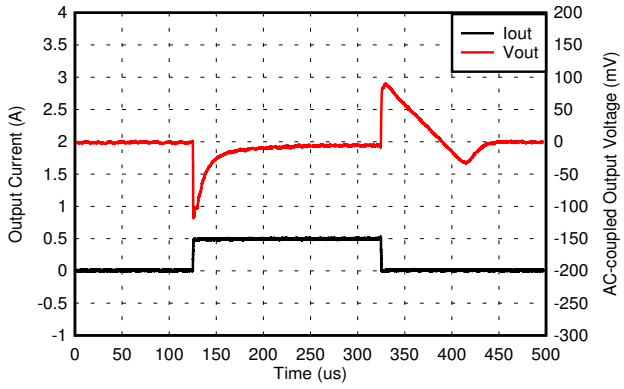

$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ slew rate = 1 A/µs

**Figure 5-20. 3.3-V, 1-mA to 500-mA Load Transient**



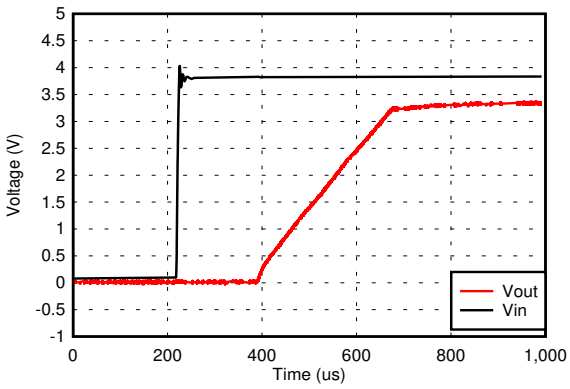

$V_{IN}$ = 2 V, $V_{OUT}$ = 0.55 V, $I_{OUT}$ slew rate = 1 A/µs

**Figure 5-21. 0.55-V, 1-mA to 500-mA Load Transient**



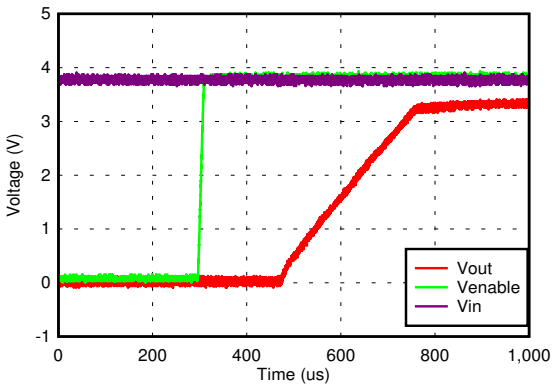

$V_{IN}$ = 5.5 V, $V_{OUT}$ = 5 V, $I_{OUT}$ slew rate = 1 A/µs

**Figure 5-22. 5-V, 1-mA to 500-mA Load Transient**




$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 1 mA

**Figure 5-23. $V_{IN}$ Power-Up**

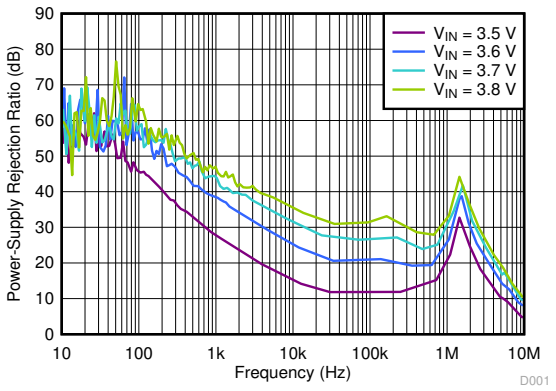



$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 1 mA

**Figure 5-24. Start-Up With EN**

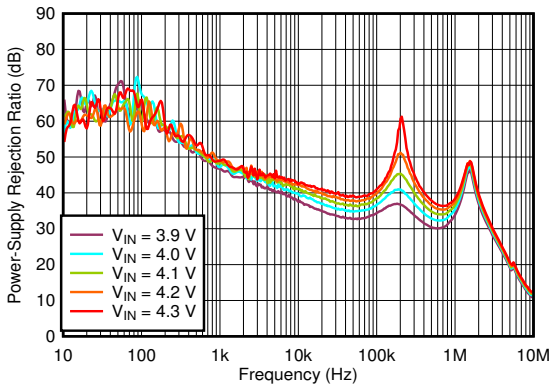
## 5.6 Typical Characteristics (continued)

at operating temperature range $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)



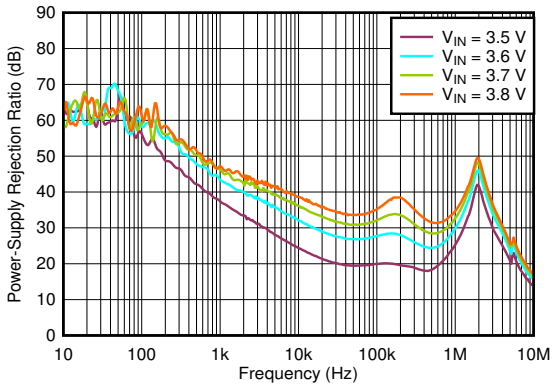

$V_{OUT}$ = 3.3 V, $I_{OUT}$ = 500 mA, $C_{OUT}$ = 2.2 µF

**Figure 5-25. PSRR vs Frequency and $V_{IN}$**



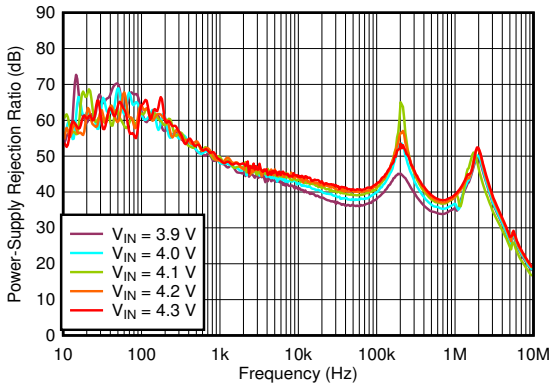

$V_{OUT}$ = 3.3 V, $I_{OUT}$ = 500 mA, $C_{OUT}$ = 2.2 µF

**Figure 5-26. PSRR vs Frequency and $V_{IN}$**



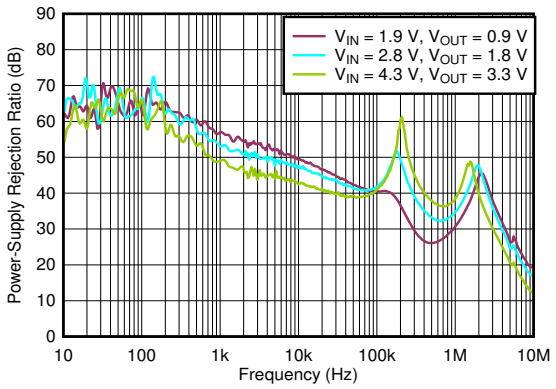

$V_{OUT}$ = 3.3 V, $I_{OUT}$ = 250 mA, $C_{OUT}$ = 2.2 µF

**Figure 5-27. PSRR vs Frequency and $V_{IN}$**



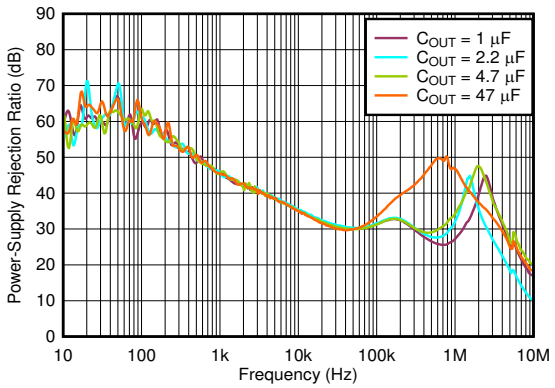

$V_{OUT}$ = 3.3 V, $I_{OUT}$ = 250 mA, $C_{OUT}$ = 2.2 µF

**Figure 5-28. PSRR vs Frequency and $V_{IN}$**




$I_{OUT}$ = 500 mA, $C_{OUT}$ = 2.2 µF

**Figure 5-29. PSRR vs Frequency**

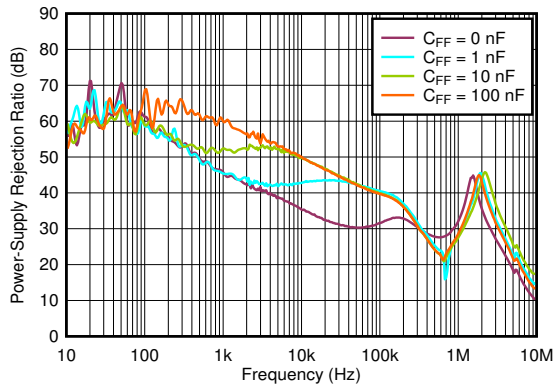



$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 500 mA

**Figure 5-30. PSRR vs Frequency and $C_{OUT}$**

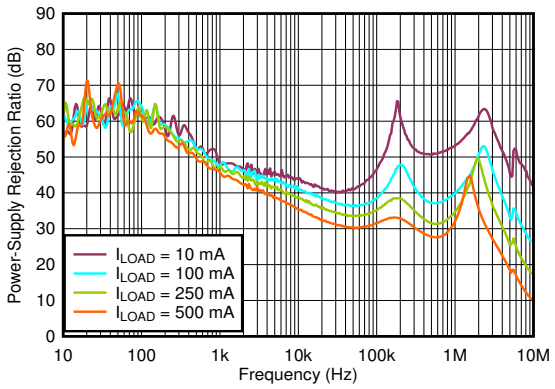
## 5.6 Typical Characteristics (continued)

at operating temperature range $T_J$ = 25°C, $V_{IN}$ = $V_{OUT(NOM)}$ + 0.5 V or 1.5 V (whichever is greater), $I_{OUT}$ = 1 mA, $V_{EN}$ = $V_{IN}$, and $C_{IN}$ = $C_{OUT}$ = 1 µF (unless otherwise noted)



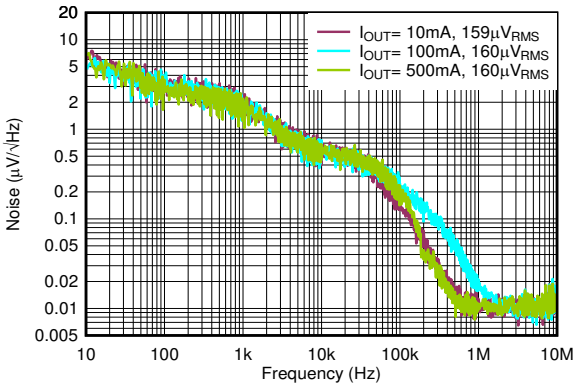

$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 500 mA

**Figure 5-31. PSRR vs Frequency and $C_{FF}$**



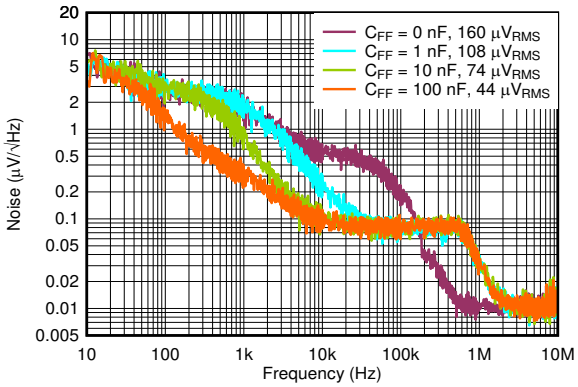

$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $C_{OUT}$ = 2.2 µF

**Figure 5-32. PSRR vs Frequency and $I_{LOAD}$**



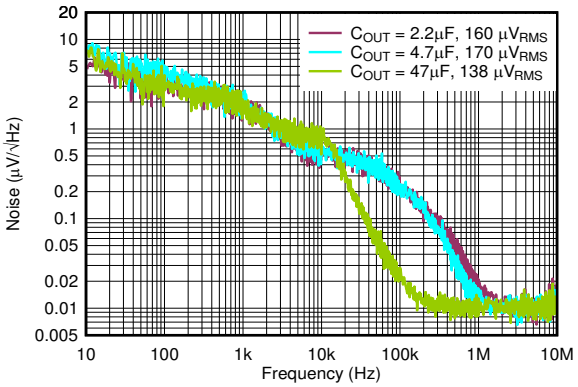

$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $C_{OUT}$ = 2.2 µF, $V_{RMS}$ BW = 10 Hz to 100 kHz

**Figure 5-33. Output Spectral Noise Density**



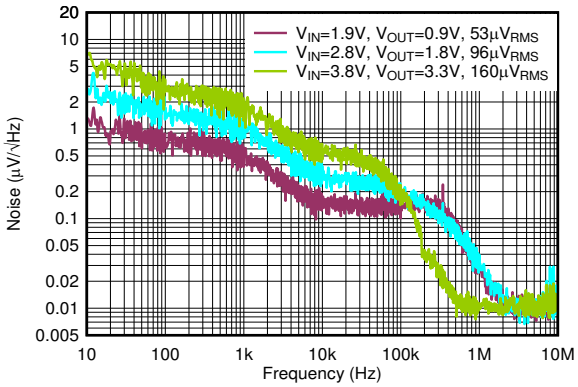

$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 500 mA, $C_{OUT}$ = 2.2 µF, $V_{RMS}$ BW = 10 Hz to 100 kHz

**Figure 5-34. Output Spectral Noise Density vs Frequency and $C_{FF}$**




$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $I_{OUT}$ = 100 mA, $C_{FF}$ = 0 µF, $V_{RMS}$ BW = 10 Hz to 100 kHz

**Figure 5-35. Output Spectral Noise Density vs Frequency and $C_{OUT}$**




$I_{OUT}$ = 500 mA, $C_{OUT}$ = 2.2 µF, $V_{RMS}$ BW = 10 Hz to 100 kHz

**Figure 5-36. Output Spectral Noise Density vs Frequency**

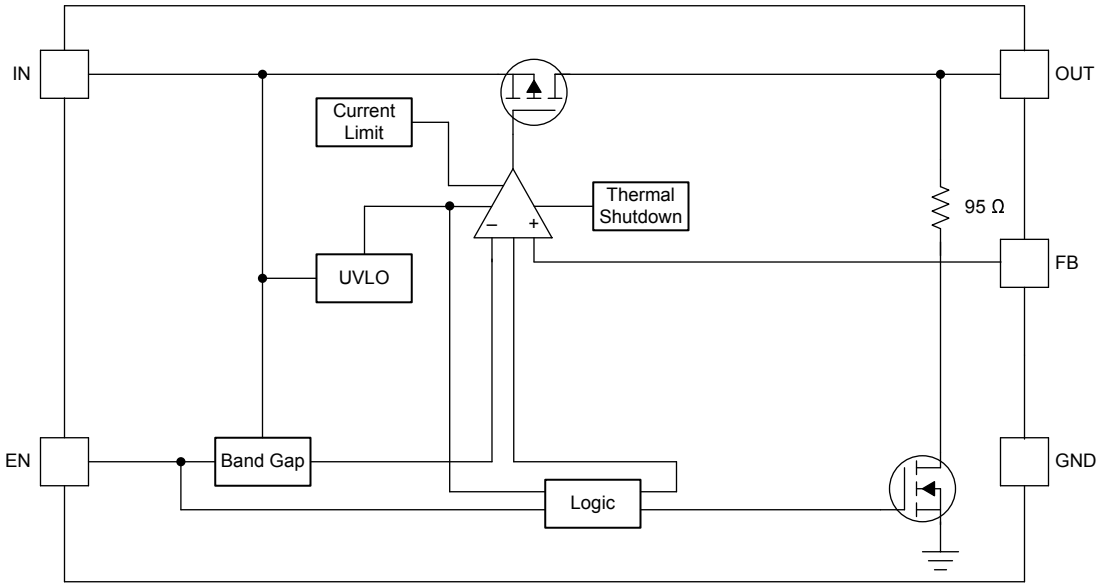
# 6 Detailed Description

## 6.1 Overview

The TLV758P low-dropout regulators (LDO) consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise and good PSRR with low dropout voltage, make this device designed for portable consumer applications.

This regulator offers foldback current limit, shutdown, and thermal protection. The operating junction temperature for this device is –40°C to +125°C.

## 6.2 Functional Block Diagram




## 6.3 Feature Description

### 6.3.1 Undervoltage Lockout (UVLO)

The TLV758P uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage ($V_{UVLO}$). This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. When $V_{IN}$ is less than $V_{UVLO}$, the output is connected to ground with a pulldown resistor ($R_{PULLDOWN}$).

### 6.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(HI)}$. Turn off the device by forcing the EN pin to drop below $V_{EN(LO)}$. If shutdown capability is not required, connect EN to IN.

The TLV758P has an internal pulldown MOSFET that connects an $R_{PULLDOWN}$ resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance ($C_{OUT}$) and the load resistance ($R_L$) in parallel with the pulldown resistor ($R_{PULLDOWN}$). Equation 1 calculates the time constant:

$$\tau = ( R_{PULLDOWN} \times R_L) / (R_{PULLDOWN} + R_L) \quad (1)$$

### 6.3.3 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brick-wall-foldback scheme. The current limit transitions from a brick-wall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brick-wall scheme limits the output current to the current limit ($I_{CL}$). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the

output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit ($I_{SC}$). $I_{CL}$ and $I_{SC}$ are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK}$ = 0.4 V × $V_{OUT(NOM)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [($V_{IN}$ – $V_{OUT}$) × $I_{CL}$]. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power [($V_{IN}$ – $V_{OUT}$) × $I_{SC}$]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

Figure 6-1 shows a diagram of the foldback current limit.

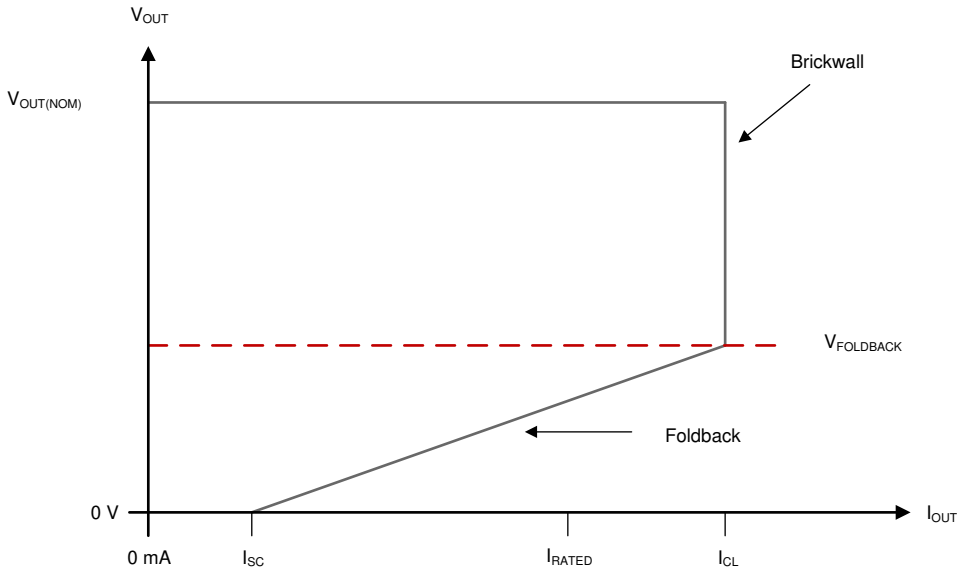



**Figure 6-1. Foldback Current Limit**

### 6.3.4 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 170°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 155°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating.

Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the ($V_{IN}$ – $V_{OUT}$) voltage and the load current. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TLV758P internal protection circuitry protects against overload conditions but is not intended to be activated in normal operation. Continuously running the TLV758P into thermal shutdown degrades device reliability.

## 6.4 Device Functional Modes

### 6.4.1 Device Functional Mode Comparison

Table 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

**Table 6-1. Device Functional Mode Comparison**

| OPERATING MODE | PARAMETER | | | |
|---|---|---|---|---|
| | $V_{IN}$ | $V_{EN}$ | $I_{OUT}$ | $T_J$ |
| Normal operation | $V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$ | $V_{EN} > V_{EN(HI)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < T_{SD(shutdown)}$ |
| Dropout operation | $V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$ | $V_{EN} > V_{EN(HI)}$ | $I_{OUT} < I_{OUT(max)}$ | $T_J < T_{SD(shutdown)}$ |
| Disabled (any true condition disables the device) | $V_{IN} < V_{UVLO}$ | $V_{EN} < V_{EN(LOW)}$ | Not applicable | $T_J > T_{SD(shutdown)}$ |

### 6.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The enable voltage has previously exceeded the enable rising threshold voltage and has not yet decreased to less than the enable falling threshold

### 6.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start-up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

### 6.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the enable pin to less than the maximum EN pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

# 7 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 7.1 Application Information

### 7.1.1 Adjustable Device Feedback Resistors

Figure 7-1 shows that the output voltage of the TLV758P can be adjusted from 0.55 V to 5.5 V by using a resistor divider network.

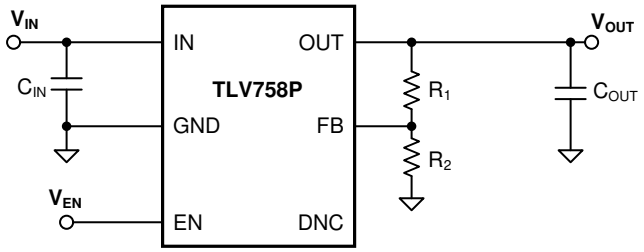



**Figure 7-1. Adjustable Operation**

The adjustable-version device requires external feedback divider resistors to set the output voltage. $V_{OUT}$ is set using the feedback divider resistors, $R_1$ and $R_2$, according to the following equation:

$$V_{OUT} = V_{FB} \times (1 + R_1 / R_2) \quad (2)$$

For this device, $V_{FB}$ = 0.55 V.

To ignore the FB pin current error term in the $V_{OUT}$ equation, set the feedback divider current to 100 times the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq V_{OUT} / (I_{FB} \times 100) \quad (3)$$

For this device, $I_{FB}$ = 10 nA.

### 7.1.2 Input and Output Capacitor Selection

The TLV758P requires an output capacitance of 0.47 µF or larger for stability. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature. When choosing a capacitor for a specific application, pay attention to the dc bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For best performance, the maximum recommended output capacitance is 220 µF.

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has a high impedance over a large range of frequencies, several input capacitors can be used in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast, rise-time load transients are anticipated, or if the device is located several inches from the input power source.

### 7.1.3 Dropout Voltage

The TLV758P uses a PMOS pass transistor to achieve low dropout. When ($V_{IN}$ – $V_{OUT}$) is less than the dropout voltage ($V_{DO}$), the PMOS pass transistor is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass transistor. $V_{DO}$ scales approximately with output current because the PMOS pass transistor behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as ($V_{IN}$ – $V_{OUT}$) approaches dropout operation.

### 7.1.4 Exiting Dropout

Some applications have transients that place the LDO into dropout, such as slower ramps on $V_{IN}$ during start-up. As with other LDOs, the output may overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up, as shown in Figure 7-2, when the slew rate and voltage levels are in the correct range. Use an enable signal to avoid this condition.

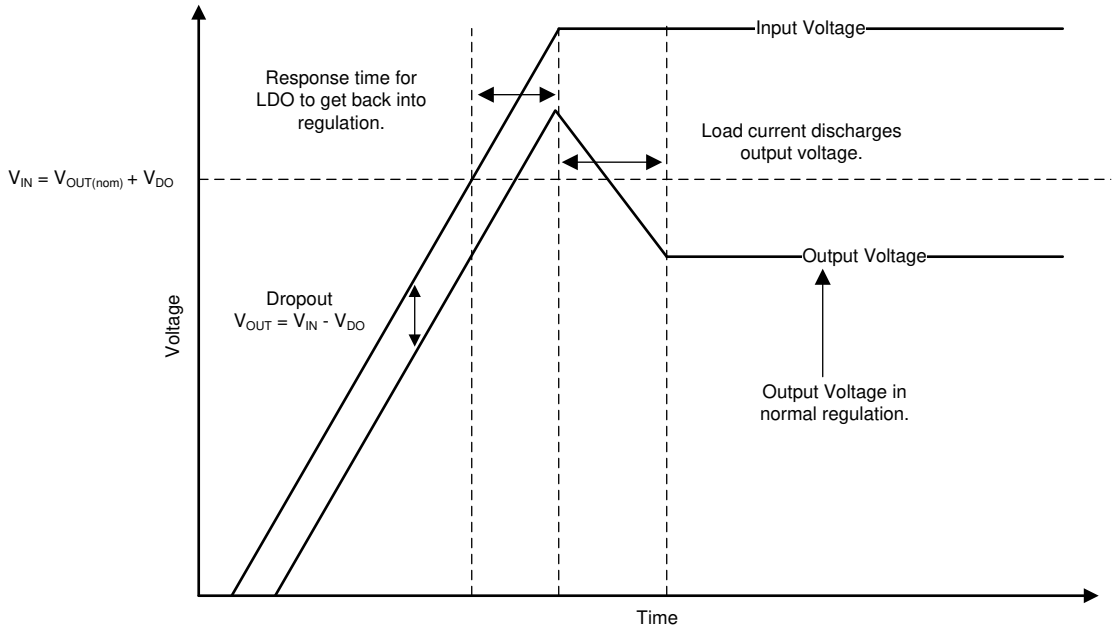



**Figure 7-2. Start-Up Into Dropout**

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass transistor and bring the gate back to the correct voltage for proper regulation. Figure 7-3 illustrates what is happening internally with the gate voltage and how overshoot can be caused during operation. When the LDO is placed in dropout, the gate voltage (VGS) is pulled all the way down to ground to give the pass transistor the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation and can cause the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.

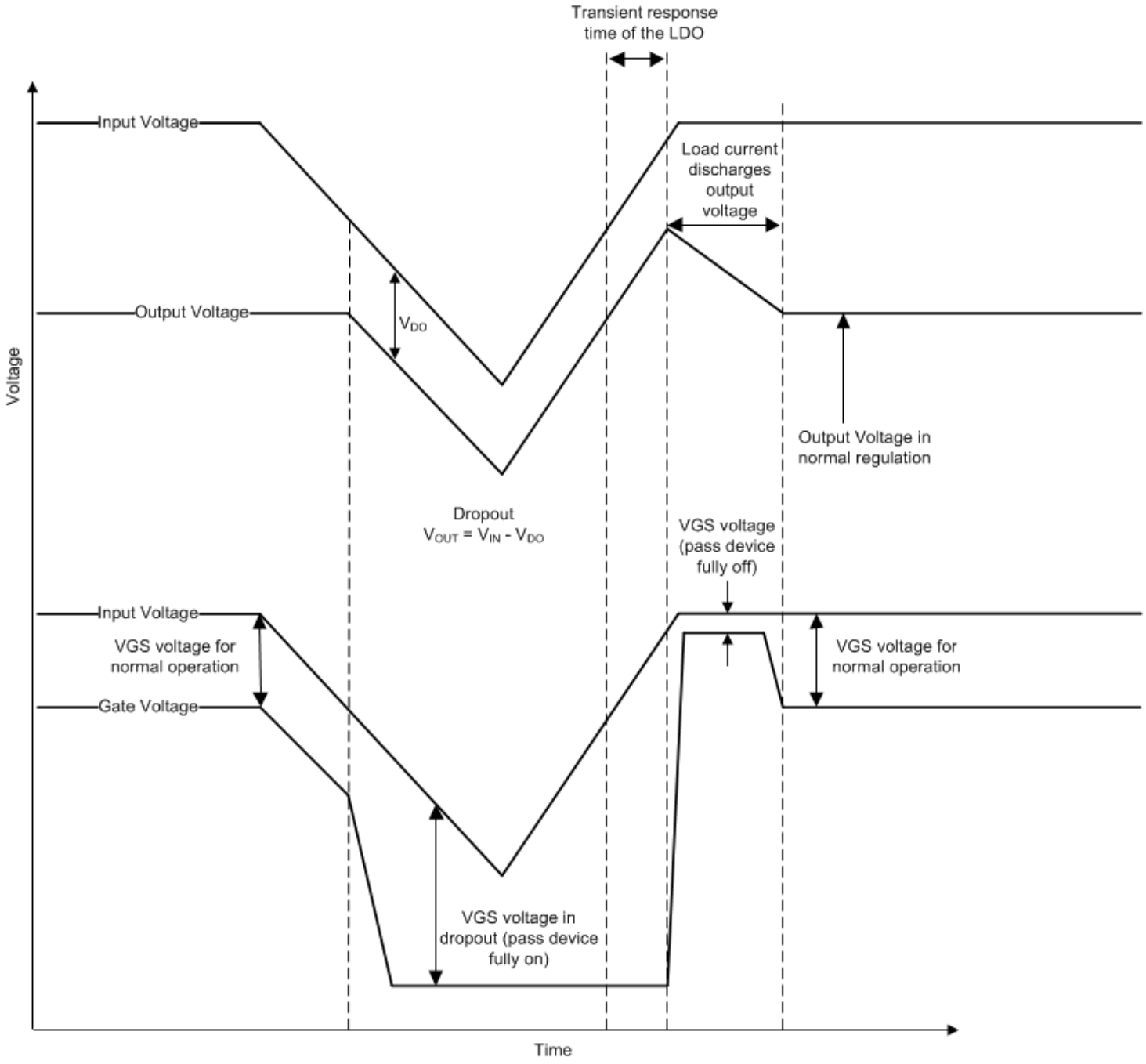



**Figure 7-3. Line Transients From Dropout**

### 7.1.5 Reverse Current

As with most LDOs, excessive reverse current can damage this device.

Reverse current flows through the body diode on the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device, as a result of one of the following conditions:

- Degradation caused by electromigration
- Excessive heat dissipation
- Potential for a latch-up condition

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} > V_{IN} + 0.3$ V:

- If the device has a large $C_{OUT}$ and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection must be used to protect the device. Figure 7-4 shows one approach of protecting the device.

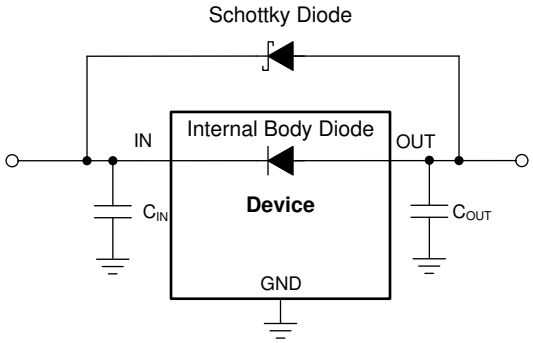



**Figure 7-4. Example Circuit for Reverse Current Protection Using a Schottky Diode**

### 7.1.6 Power Dissipation ($P_D$)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Equation 4 calculates power dissipation ($P_D$).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

**Note**

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature ($T_A$) for the device. According to Equation 5, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air ($T_A$).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (5)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

### 7.1.7 Feed-Forward Capacitor ($C_{FF}$)

For the adjustable-voltage version device, a feed-forward capacitor ($C_{FF}$) can be connected from the OUT pin to the FB pin. $C_{FF}$ improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended $C_{FF}$ values are listed in the *Recommended Operating Conditions* table. A higher capacitance $C_{FF}$ can be used; however, the start-up time increases. For a detailed description of $C_{FF}$ tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

### 7.1.8 Start-Up Sequencing

If $V_{EN}$ is greater than $V_{UVLO}$ rising (min), then the input pin (IN) must sink 1 mA of current to avoid the device being turn on with a floating input pin.

## 7.2 Typical Application

Figure 7-5 shows the typical application circuit for the TLV758P. Input and output capacitances must be at least 1 µF.

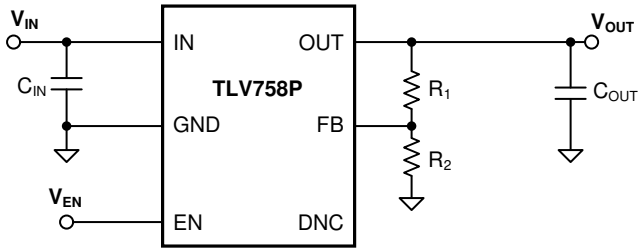



**Figure 7-5. TLV758P Typical Application**

### 7.2.1 Design Requirements

Use the parameters listed in Table 7-1 for typical linear regulator applications.

**Table 7-1. Design Parameters**

| PARAMETER | DESIGN REQUIREMENT |
|---|---|
| Input voltage | 3.8 V |
| Output voltage | 3.3 V, ±1% |
| Input current | 500 mA (maximum) |
| Output load | 500-mA DC |
| Maximum ambient temperature | 70°C |

### 7.2.2 Detailed Design Procedure

Input and output capacitors are required to achieve the output voltage transient requirements. Capacitance values of 2.2 µF are selected to give the maximum output capacitance in a small, low-cost package; see the *Input and Output Capacitor Selection* section for details.

Figure 7-1 illustrates the output voltage of the TLV758P; set the output voltage using the resistor divider.

#### *7.2.2.1 Input Current*

During normal operation, the input current to the LDO is approximately equal to the output current of the LDO. During start-up, the input current is higher as a result of the inrush current charging the output capacitor. Use Equation 6 to calculate the current through the input.

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt}\right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}}\right] \quad (6)$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
- $dV_{OUT}(t) / dt$ is the slope of the $V_{OUT}$ ramp
- $R_{LOAD}$ is the resistive load impedance

#### 7.2.2.2 Thermal Dissipation

The junction temperature can be determined using the junction-to-ambient thermal resistance ($R_{\theta JA}$) and the total power dissipation ($P_D$). Use Equation 7 to calculate the power dissipation. Multiply $P_D$ by $R_{\theta JA}$ as Equation 8 shows and add the ambient temperature ($T_A$) to calculate the junction temperature ($T_J$).

$$P_D = (I_{GND} + I_{OUT}) \times (V_{IN} - V_{OUT}) \quad (7)$$

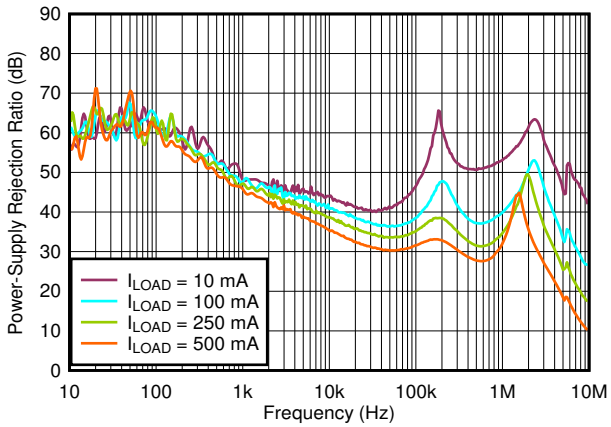
$$T_J = R_{\theta JA} \times P_D + T_A \quad (8)$$

Calculate the maximum ambient temperature as Equation 9 shows if the ($T_{J(MAX)}$) value does not exceed 125°C. Equation 10 calculates the maximum ambient temperature with a value of 104.93°C.

$$T_{A(MAX)} = T_{J(MAX)} - R_{\theta JA} \times P_D \quad (9)$$

$$T_{A(MAX)} = 125°C - 80.3°C/W \times (3.8\ V - 3.3\ V) \times (0.5\ A) = 104.93°C \quad (10)$$

### 7.2.3 Application Curve




$V_{IN}$ = 3.8 V, $V_{OUT}$ = 3.3 V, $C_{OUT}$ = 2.2 µF

**Figure 7-6. PSRR vs Frequency and $I_{LOAD}$**

## 7.3 Power Supply Recommendations

Connect a low output impedance power supply directly to the IN pin of the TLV758P.

## 7.4 Layout

### 7.4.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections, in order to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.
- Do not place a thermal via directly beneath the thermal pad of the DRV package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

### 7.4.2 Layout Examples

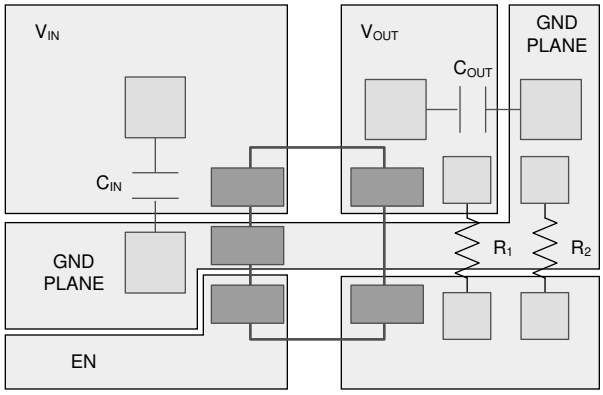



**Figure 7-7. DBV Package Layout Example**

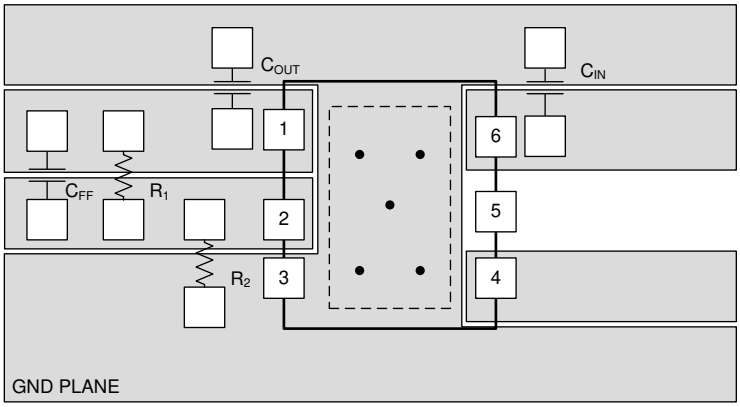



**Figure 7-8. DRV Package Layout Example**

# 8 Device and Documentation Support

## 8.1 Documentation Support

### 8.1.1 Device Nomenclature

**Table 8-1. Device Nomenclature(1)**

| PRODUCT | $V_{OUT}$ |
|---|---|
| TLV758 **xx(x)Pyyyz** | **xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). 01 is for adjustable version.<br>**P** indicates an active output discharge feature. All members of the TLV758P family actively discharge the output when the device is disabled.<br>**yyy** is the package designator.<br>**z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces). |

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

### 8.1.2 Related Documentation

For related documentation see the following:

Texas Instruments, *Pros and cons of using a feedforward capacitor with a low-dropout regulator* application note

## 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.4 Trademarks

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## 8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (March 2019) to Revision D (October 2023) | Page |
|---|---|
| • Changed DBV package from *Advance Information* to *Production Data* | 1 |
| • Added links to *Applications* section | 1 |
| • Changed 5-V to 5.5-V in title of *5.5-V Load Regulation vs* $I_{OUT}$ figure | 7 |
| • Added *Startup Sequencing* section | 20 |
| • Added *Device Nomenclature* section | 24 |

| Changes from Revision B (March 2019) to Revision C (March 2019) | Page |
|---|---|
| • Deleted thermal pad from DBV pin out drawing | 3 |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV75801PDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 1UDF | Samples |
| TLV75801PDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 125 | 1UDF | Samples |
| TLV75801PDRVR | ACTIVE | WSON | DRV | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1MHH | Samples |
| TLV75801PDRVT | ACTIVE | WSON | DRV | 6 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1MHH | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

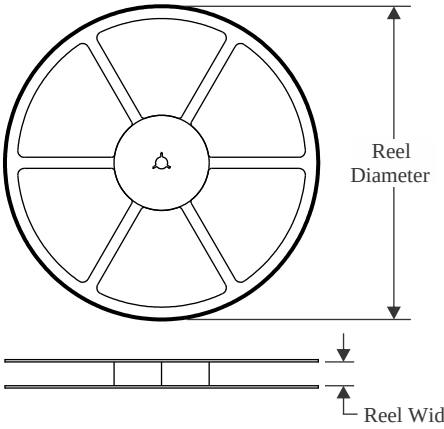
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

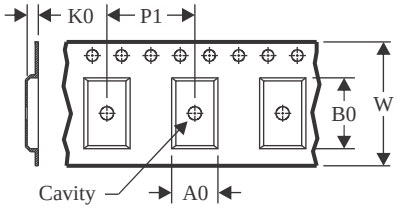
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

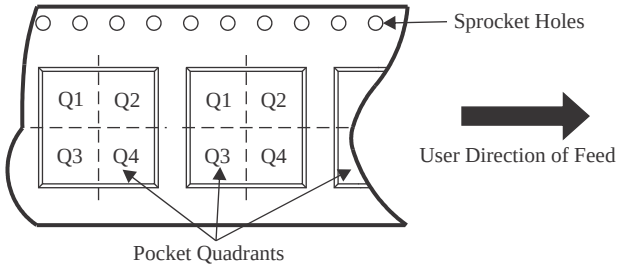



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

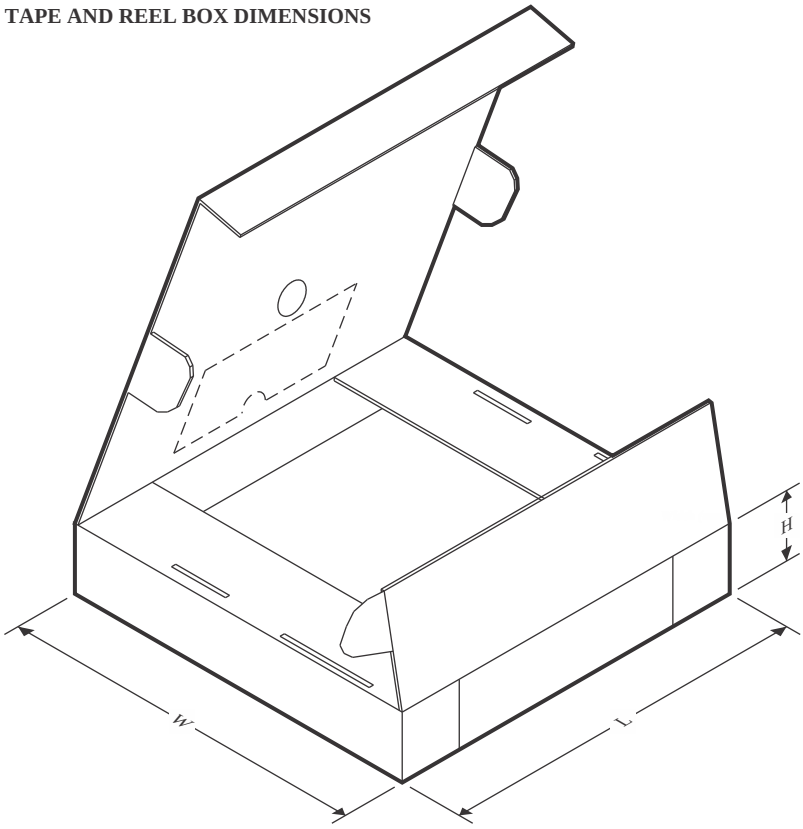
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV75801PDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV75801PDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV75801PDRVR | WSON | DRV | 6 | 3000 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |
| TLV75801PDRVT | WSON | DRV | 6 | 250 | 180.0 | 8.4 | 2.3 | 2.3 | 1.15 | 4.0 | 8.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

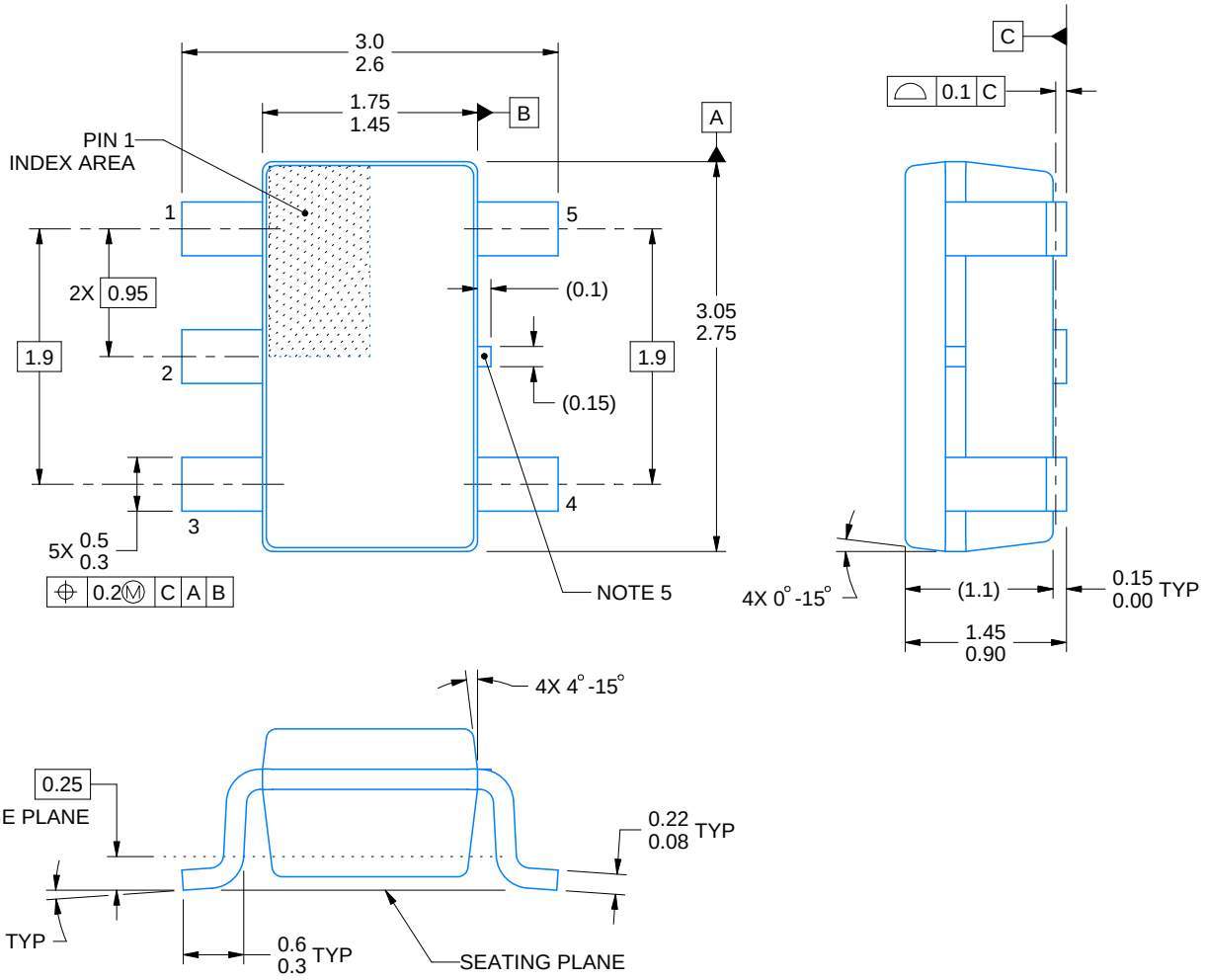
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV75801PDBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV75801PDBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |
| TLV75801PDRVR | WSON | DRV | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TLV75801PDRVT | WSON | DRV | 6 | 250 | 210.0 | 185.0 | 35.0 |

# PACKAGE OUTLINE

## DBV0005A

## SOT-23 - 1.45 mm max height

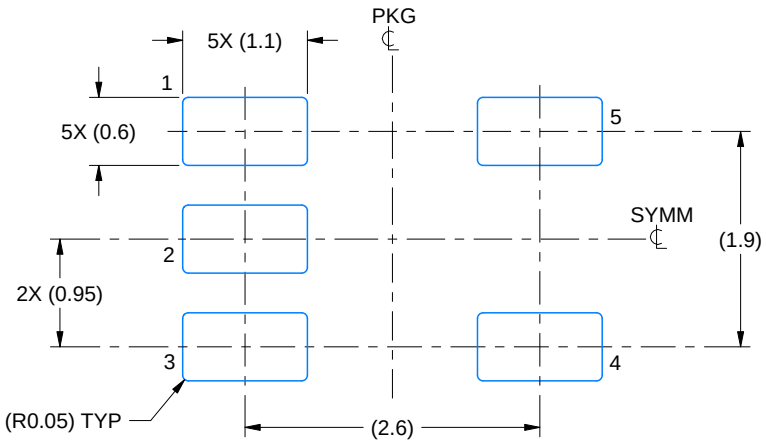
SMALL OUTLINE TRANSISTOR



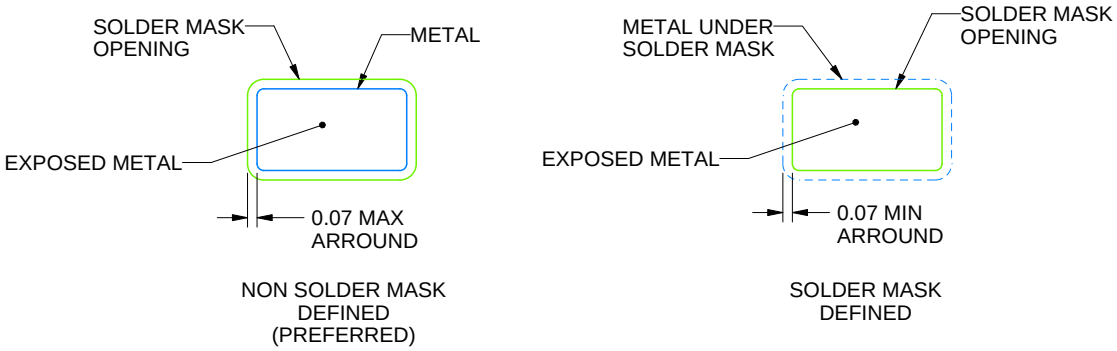

4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

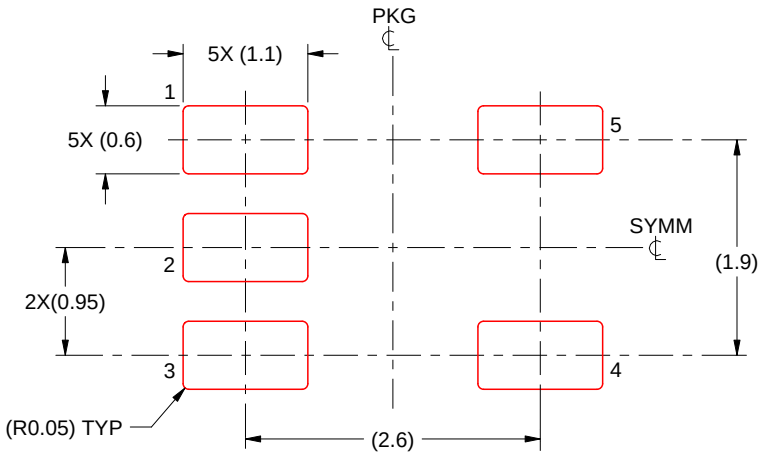



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

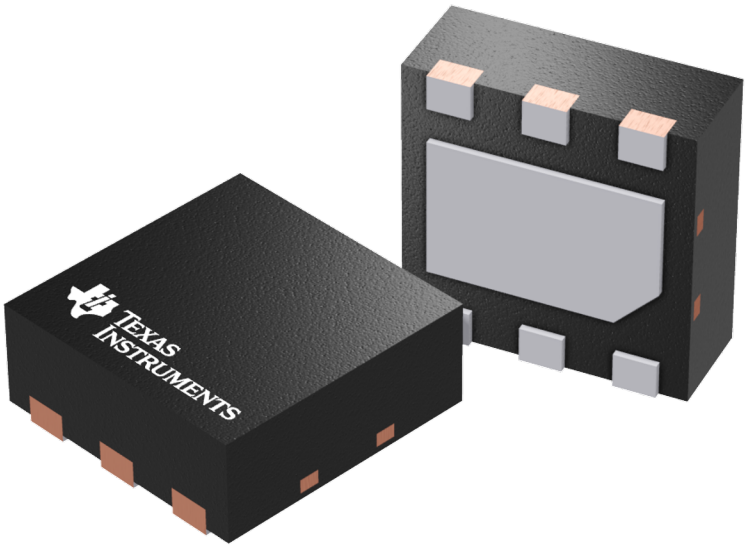
4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



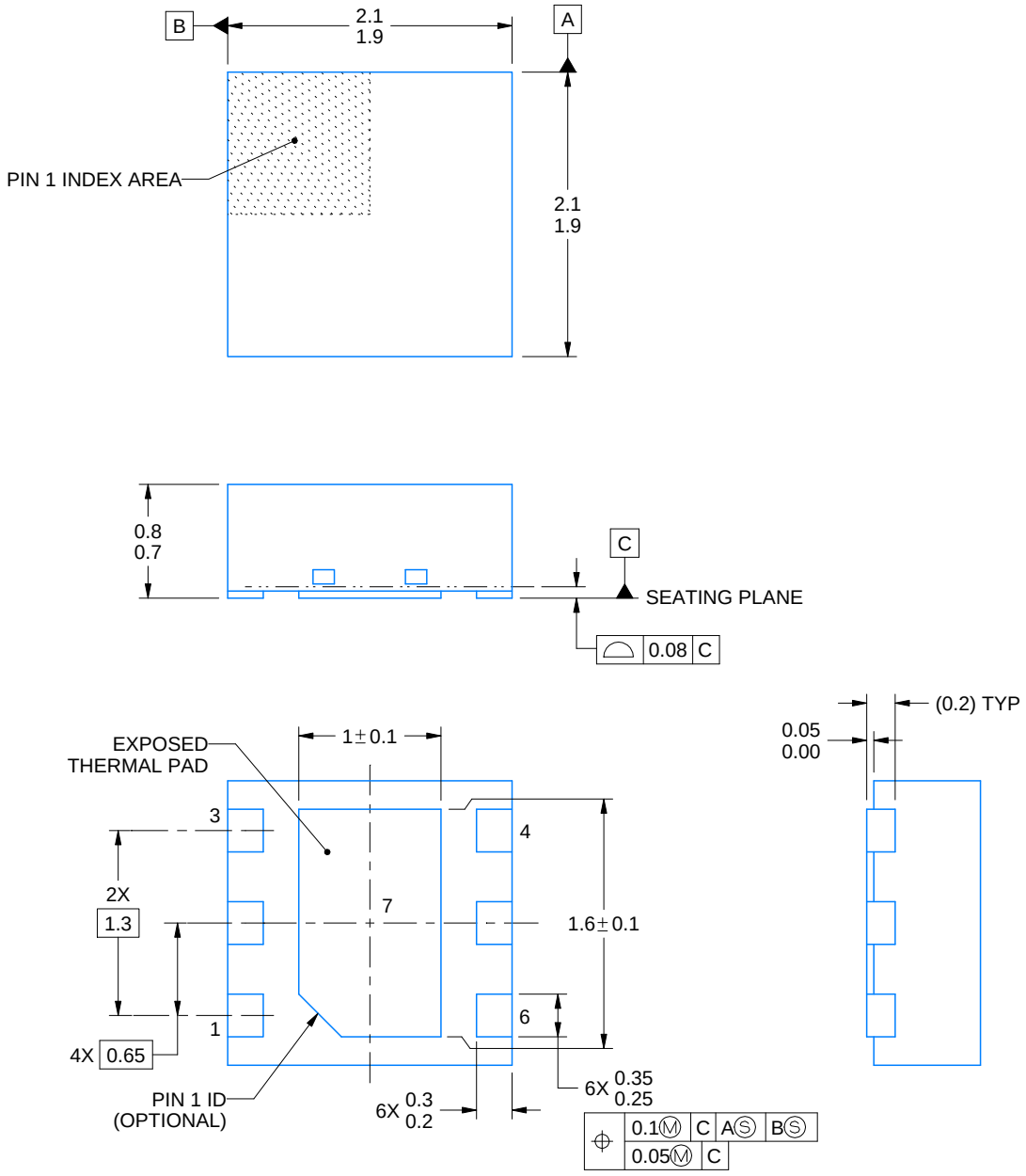

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

# PACKAGE OUTLINE

## DRV0006A

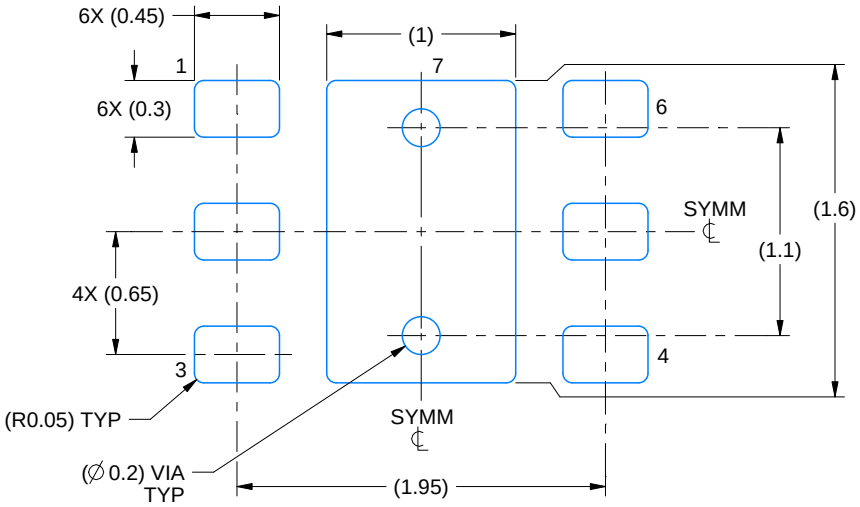
## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

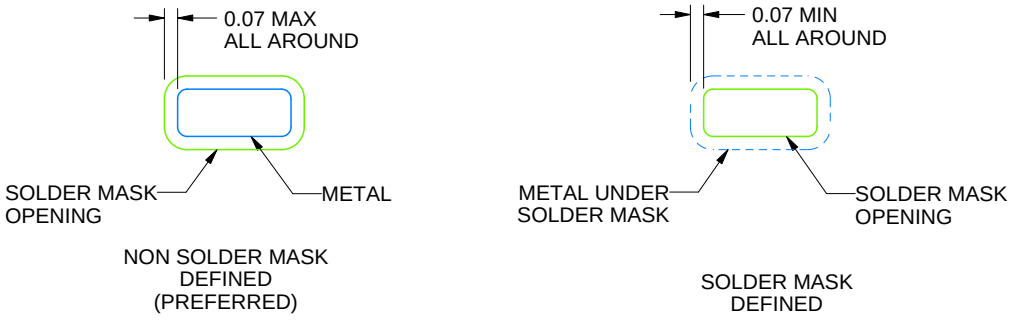



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:25X




SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

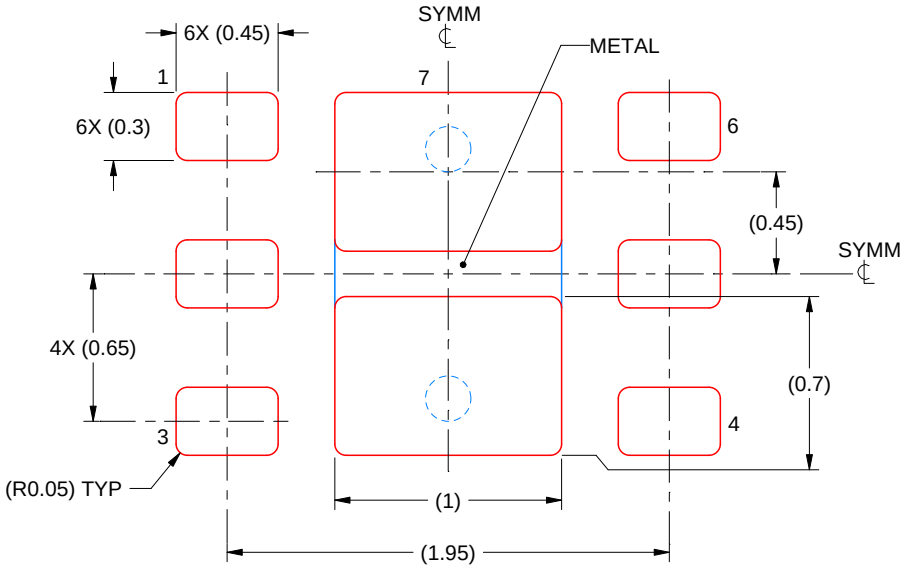
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

## DRV0006A

## WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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