TLV910x-Q1 Automotive 16V, 1MHz, Rail-to-Rail Input/Output, Low Power Op Amp

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to +125°C, T_A
- Rail-to-rail input and output
- Wide bandwidth: 1.1MHz GBW
- Low quiescent current: 120µA per amplifier
- Low offset voltage: ±300µV
- Low offset voltage drift: ±0.6µV/°C
- Low noise: 28nV/$\sqrt{Hz}$ at 10kHz
- High common-mode rejection: 110dB
- Low bias current: ±10pA
- High slew rate: 4.5V/µs
- Wide supply: ±1.35V to ±8V, 2.7V to 16V
- Robust EMIRR performance: 77dB at 1.8GHz

2 Applications

- HEV/EV battery-management system (BMS)
- HEV/EV OBC & DC/DC converter
- HEV/EV inverter & motor control
- Body control module (BCM)
- Zone control module
- Domain gateway
- 12V/48V power distribution box
- Automotive HVAC compressor module
- Electric power steering (EPS)

3 Description

The TLV910x-Q1 family (TLV9101-Q1, TLV9102-Q1, and TLV9104-Q1) is a family of 16V general purpose operational amplifiers. This family offers excellent DC precision and AC performance, including rail-to-rail input/output, low offset (±300µV, typical), low offset drift (±0.6µV/°C, typical), and 1.1MHz bandwidth.

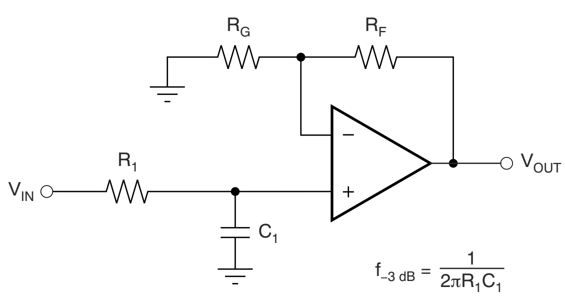
Wide differential and common-mode input-voltage range, high output current (±80mA, typical), high slew rate (4.5V/µs, typical), and low power operation (115µA, typical)make the TLV910x-Q1 a robust, low-power, high-performance operational amplifier for automotive applications.

The TLV910x-Q1 family of op amps is available in several packages, and is specified from –40°C to 125°C.

Device Information

PART NUMBER (1)	CHANNEL COUNT	PACKAGE	PACKAGE SIZE (4)
TLV9101-Q1(2)	Single	DBV (SOT-23, 5(3)	2.9mm × 2.8mm
		DCK (SC70, 5)(3)	2mm × 2.1mm
TLV9102-Q1(2)	Dual	D (SOIC, 8)(3)	4.9mm × 6mm
		DGK (VSSOP, 8)(3)	3mm × 4.9mm
TLV9104-Q1	Quad	D (SOIC, 14)(3)	8.65mm × 6mm
		PW (TSSOP, 14)	5mm × 6.4mm

(1) For all available packages, see Section 10.
(2) This device is preview only.
(3) This package is preview only.
(4) The package size (length × width) is a nominal value and includes pins, where applicable.



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

TLV910x-Q1 in a Single-Pole, Low-Pass Filter

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4 Pin Configuration and Functions

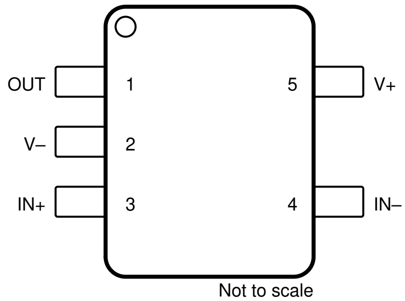


Figure 4-1. TLV9101-Q1[(1)] DBV Package 5-Pin SOT-23 Top View

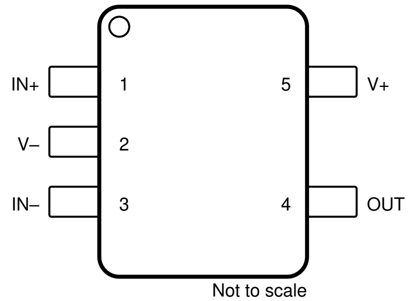


Figure 4-2. TLV9101-Q1[(1)] DCK Package 5-Pin SC70 Top View

Table 4-1. Pin Functions: TLV9101-Q1

PIN			I/O	DESCRIPTION
NAME	DBV	DCK and DRL		
+IN	3	1	I	Noninverting input
–IN	4	3	I	Inverting input
OUT	1	4	O	Output
V+	5	5	—	Positive (highest) power supply
V–	2	2	—	Negative (lowest) power supply

1. This package is preview only.

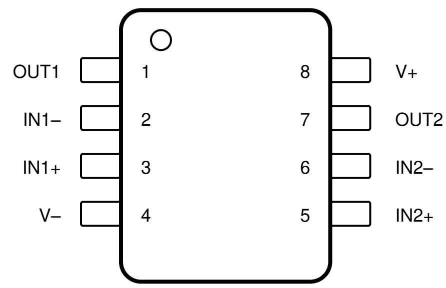


Figure 4-3. TLV9102-Q1(1) D and DGK Package 8-Pin SOIC and VSSOP Top View

Table 4-2. Pin Functions: TLV9102-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN1–	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2–	6	I	Inverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

1. This package is preview only.

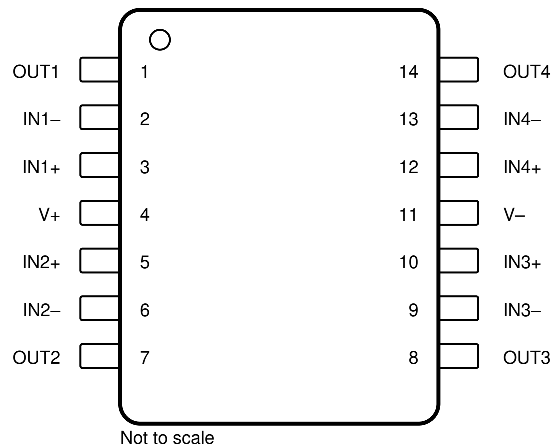


Figure 4-4. TLV9104-Q1 D[(1)] and PW Package 14-Pin SOIC[(1)] and TSSOP Top View

Table 4-3. Pin Functions: TLV9104-Q1

PIN		I/O	DESCRIPTION
NAME	SOIC and TSSOP		
IN1+	3	I	Noninverting input, channel 1
IN1–	2	I	Inverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN2–	6	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3–	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4–	13	I	Inverting input, channel 4
NC	—	—	Do not connect
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V+	4	—	Positive (highest) power supply
V–	11	—	Negative (lowest) power supply

1. This package is preview only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	20	V
Signal input pins	Common-mode voltage[(3)]	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage[(3)]		V_S + 0.2	V
	Current[(3)]	–10	10	mA
Shutdown pin voltage		V–	V+	V
Output short-circuit[(2)]		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)]	±1000	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	2.7	16	V
V_I	Input voltage range	(V–) – 0.2	(V+) + 0.2	V
T_A	Specified temperature	–40	125	°C

5.4 Thermal Information for Quad Channel

THERMAL METRIC[(1)]		TLV9104-Q1		UNIT
		D[(2)] (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.2	134.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.2	55.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.1	79.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	21.4	9.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	60.7	78.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) This package option is preview for TLV9104-Q1.

5.5 Electrical Characteristics

For V_S = (V+) – (V–) = 2.7 V to 16 V (±1.35 V to ±8 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

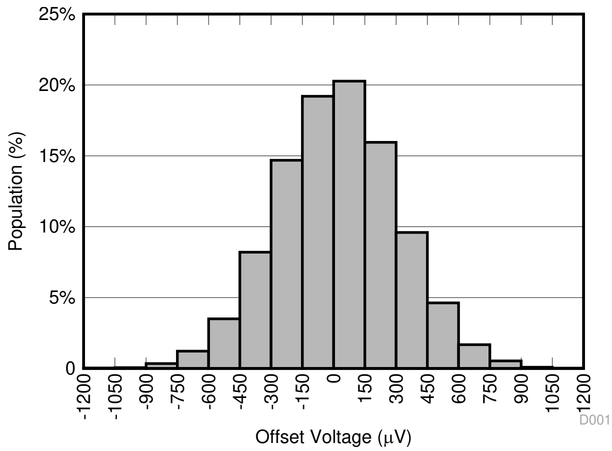
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = V–			±0.3	±1.5	mV
			T_A = –40°C to 125°C			±1.75	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to 125°C		±0.6		μV/°C
PSRR	Input offset voltage versus power supply	V_{CM} = V–	T_A = –40°C to 125°C		±0.1	±0.7	μV/V
	Channel separation	f = 0Hz			5		μV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±10		pA
I_{OS}	Input offset current				±5		pA
NOISE							
E_N	Input voltage noise	f = 0.1Hz to 10Hz			6		$μV_{PP}$
					1		$μV_{RMS}$
e_N	Input voltage noise density	f = 1kHz			30		nV/√Hz
		f = 10kHz			28		
i_N	Input current noise	f = 1kHz			2		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	V_S = 16V, (V–) – 0.1V < V_{CM} < (V+) – 2V (Main input pair)	T_A = –40°C to 125°C	90	110		dB
		V_S = 4V, (V–) – 0.1V < V_{CM} < (V+) – 2V (Main input pair)		75	95		
		V_S = 2.7 – 16V, (V+) – 1V < V_{CM} < (V+) + 0.1V (Aux input pair)			80		
		(V+) – 2V < V_{CM} < (V+) – 1V		See Offset Voltage (Transition Region) in the *Typical Characteristics* section			
INPUT CAPACITANCE							
Z_{ID}	Differential				100 || 3		MΩ || pF
Z_{ICM}	Common-mode				6 || 1		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 16V, V_{CM} = V– (V–) + 0.1V < V_O < (V+) – 0.1V	T_A = –40°C to 125°C	115	135		dB
		V_S = 4V, V_{CM} = V– (V–) + 0.1V < V_O < (V+) – 0.1V		104	125		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				1.1		MHz
SR	Slew rate	V_S = 16V, G = +1, C_L = 20pF			4.5		V/μs
t_S	Settling time	To 0.1%, V_S = 16V, V_{STEP} = 10V, G = +1, CL = 20pF			4		μs
		To 0.1%, V_S = 16V, V_{STEP} = 2V, G = +1, CL = 20pF			2		
		To 0.01%, V_S = 16V, V_{STEP} = 10V, G = +1, CL = 20pF			5		
		To 0.01%, V_S = 16V, V_{STEP} = 2V, G = +1, CL = 20pF			3		
	Phase margin	G = +1, R_L = 10kΩ, C_L = 20pF			60		°
	Overload recovery time	V_{IN} × gain > V_S			600		ns
THD+N	Total harmonic distortion + noise	V_S = 16V, V_O = $1V_{RMS}$, G = -1, f = 1kHz			0.0028%		
OUTPUT							
	Voltage output swing from rail	Positive and negative rail headroom	V_S = 16V, R_L = no load		3		mV
			V_S = 16V, R_L = 10kΩ		45	60	
			V_S = 16V, R_L = 2kΩ		200	300	
			V_S = 2.7V, R_L = no load		1		
			V_S = 2.7V, R_L = 10kΩ		5	20	
			V_S = 2.7V, R_L = 2kΩ		25	50	
I_{SC}	Short-circuit current				±80		mA
C_{LOAD}	Capacitive load drive			See Small-Signal Overshoot vs Capacitive Load in the *Typical Characteristics* section			
Z_O	Open-loop output impedance	f = 1MHz, I_O = 0A			600		Ω

For V_S = (V+) – (V–) = 2.7 V to 16 V (±1.35 V to ±8 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0A			115	150	μA
			T_A = –40°C to 125°C			160	

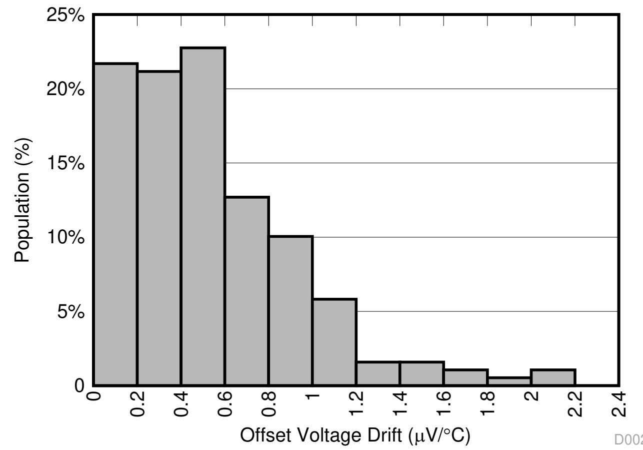
5.6 Typical Characteristics

at T_A = 25°C, V_S = ±8V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



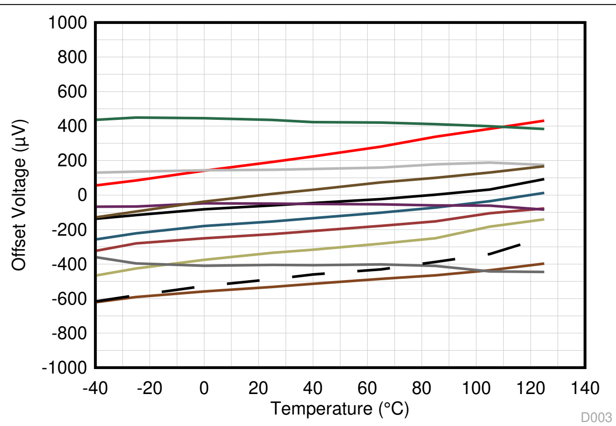
Distribution from 13, 481 amplifiers; T_A = 25°C

Figure 5-1. Offset Voltage Production Distribution



Distribution from 175 amplifiers

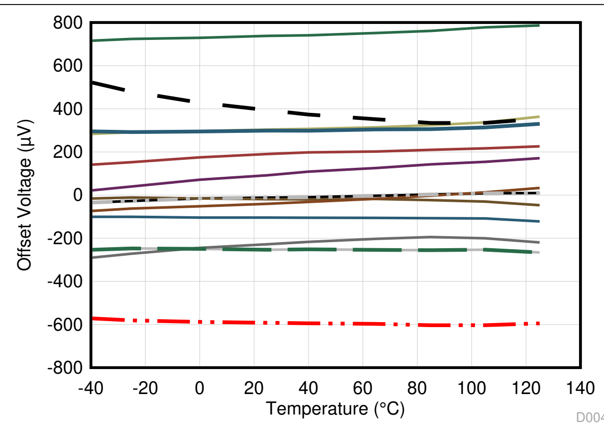
Figure 5-2. Offset Voltage Drift Distribution



V_{CM} = V+

Each color represents one sample device.

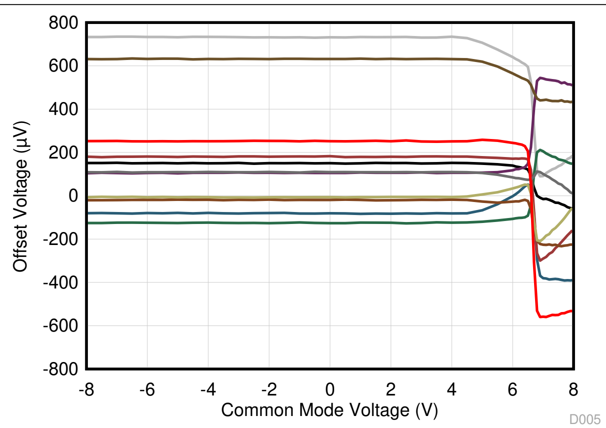
Figure 5-3. Offset Voltage vs Temperature



V_{CM} = V–

Each color represents one sample device.

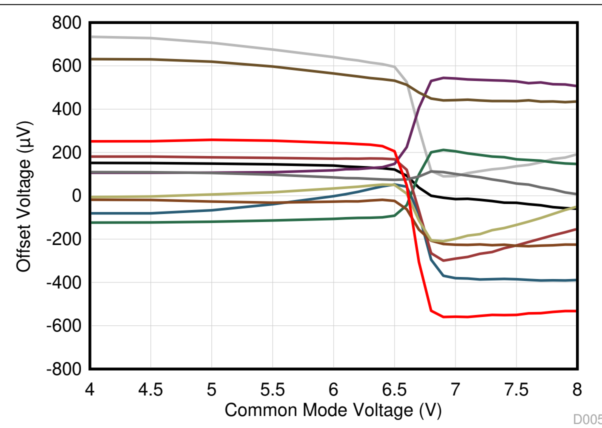
Figure 5-4. Offset Voltage vs Temperature



T_A = 25°C

Each color represents one sample device.

Figure 5-5. Offset Voltage vs Common-Mode Voltage



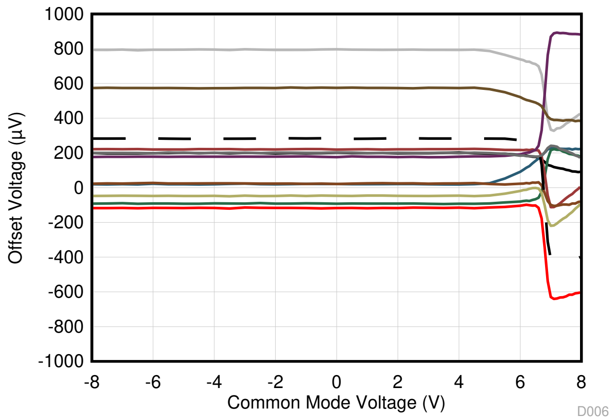
T_A = 25°C

Each color represents one sample device.

Figure 5-6. Offset Voltage vs Common-Mode Voltage (Transition Region)

5.6 Typical Characteristics (continued)

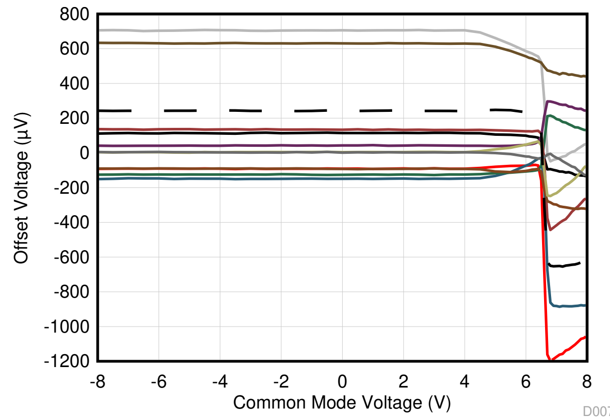
at T_A = 25°C, V_S = ±8V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



T_A = 125°C

Each color represents one sample device.

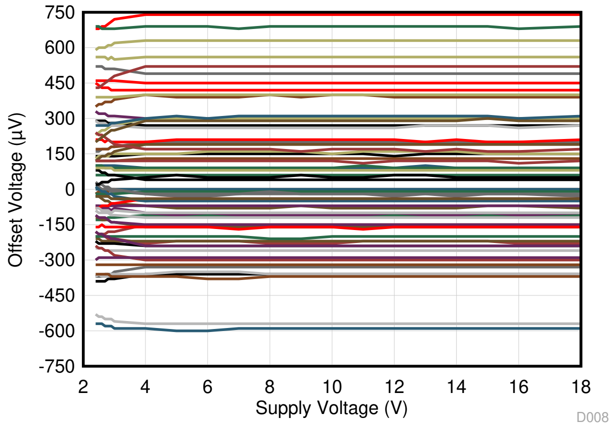
Figure 5-7. Offset Voltage vs Common-Mode Voltage



T_A = –40°C

Each color represents one sample device.

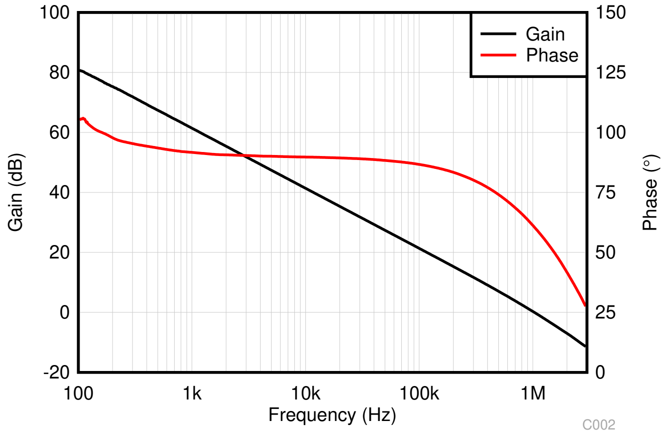
Figure 5-8. Offset Voltage vs Common-Mode Voltage



V_{CM} = V–

Each color represents one sample device.

Figure 5-9. Offset Voltage vs Power Supply



C_{LOAD} = 15pF

Figure 5-10. Open-Loop Gain and Phase vs Frequency

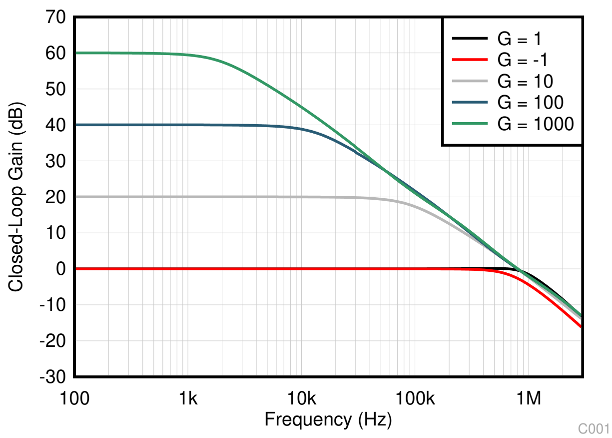


Figure 5-11. Closed-Loop Gain and Phase vs Frequency

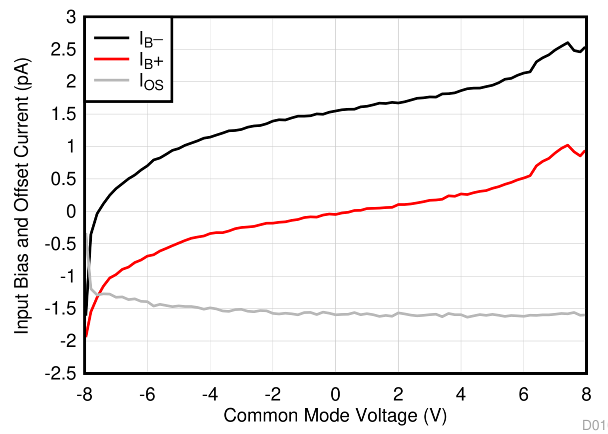


Figure 5-12. Input Bias Current vs Common-Mode Voltage

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)

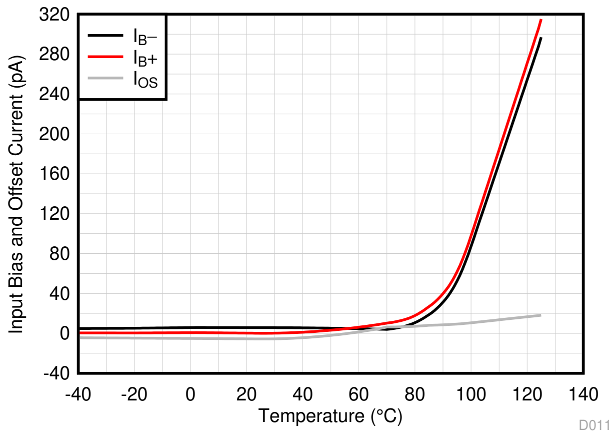


Figure 5-13. Input Bias Current vs Temperature

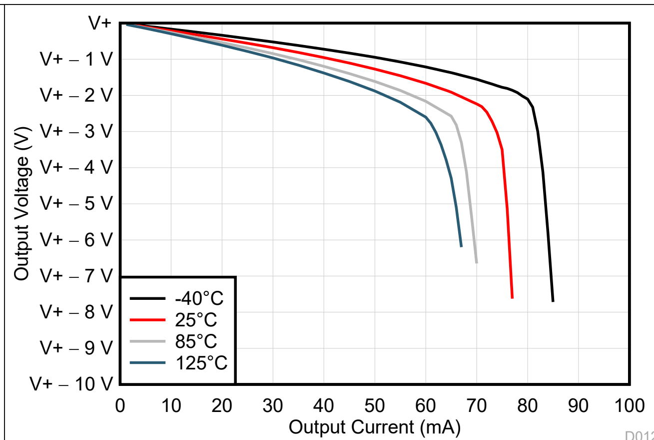


Figure 5-14. Output Voltage Swing vs Output Current (Sourcing)

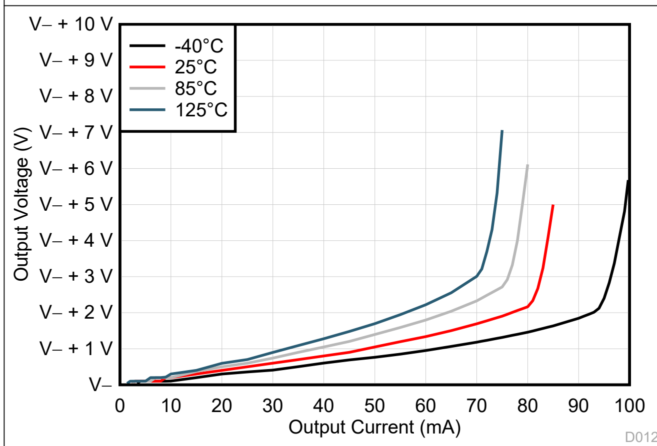
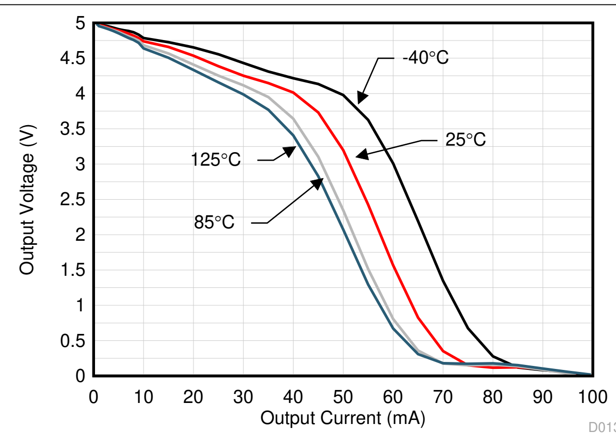
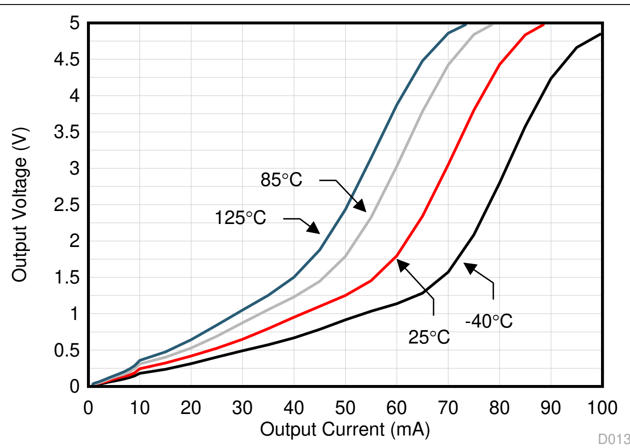


Figure 5-15. Output Voltage Swing vs Output Current (Sinking)



V_S = 5V, R_L connected to V–

Figure 5-16. Output Voltage Swing vs Output Current (Sourcing)



V_S = 5V, R_L connected to V+

Figure 5-17. Output Voltage Swing vs Output Current (Sinking)

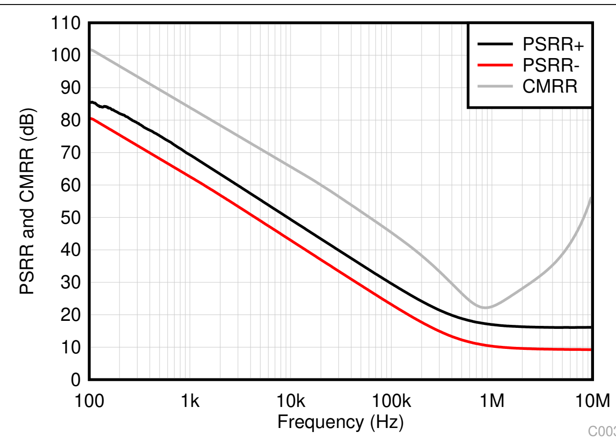
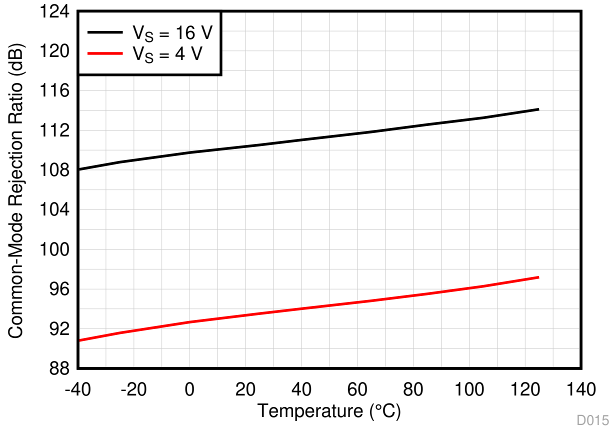


Figure 5-18. CMRR and PSRR vs Frequency

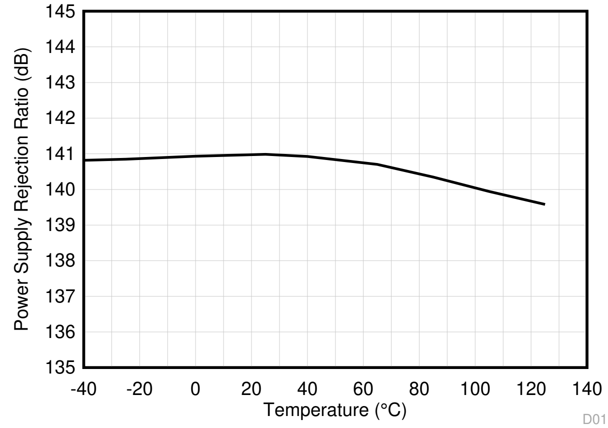
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



f = 0Hz

Figure 5-19. CMRR vs Temperature (dB)



f = 0Hz

Figure 5-20. PSRR vs Temperature (dB)

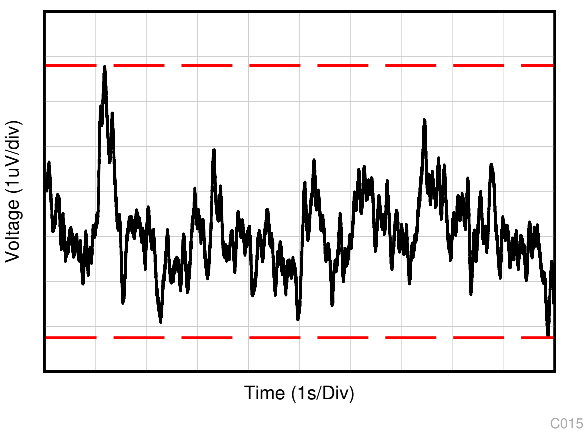


Figure 5-21. 0.1Hz to 10Hz Noise

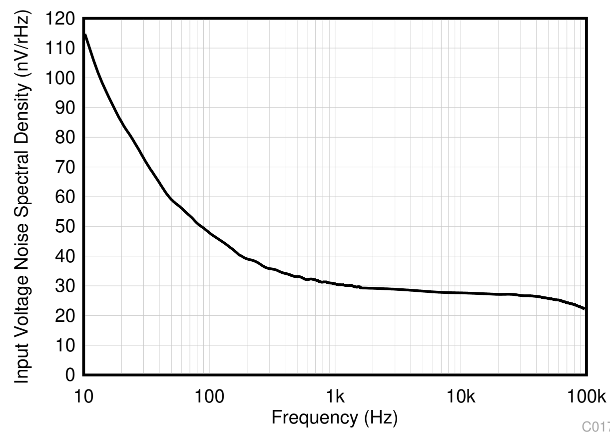
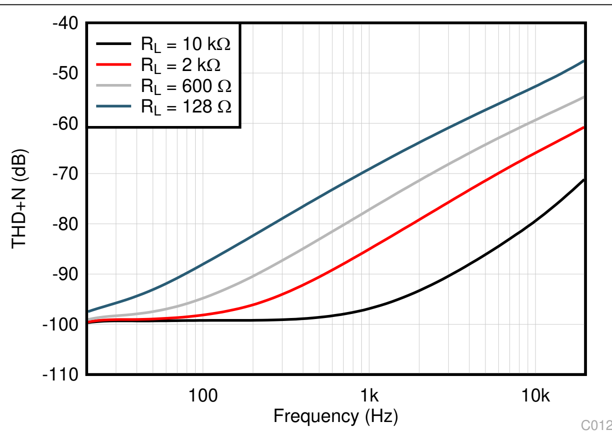
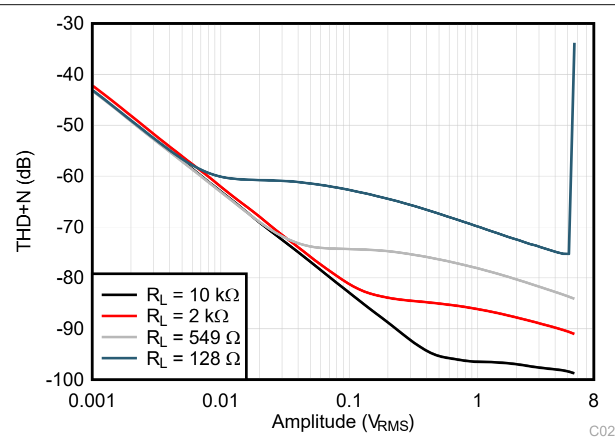


Figure 5-22. Input Voltage Noise Spectral Density vs Frequency



BW = 80kHz, V_{OUT} = 3.5V_{RMS}

Figure 5-23. THD+N Ratio vs Frequency



BW = 80kHz, f = 1kHz

Figure 5-24. THD+N vs Output Amplitude

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)

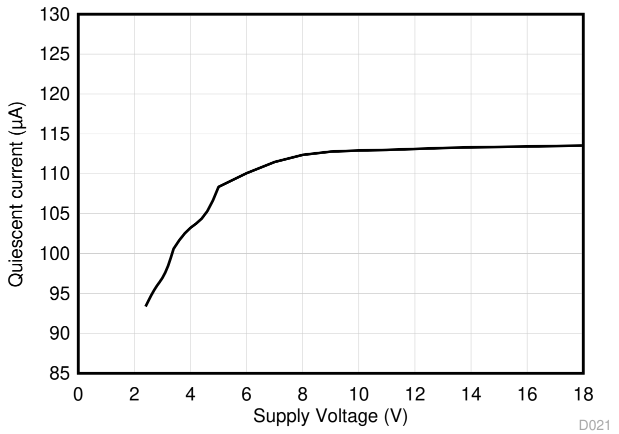


Figure 5-25. Quiescent Current per Channel vs Supply Voltage

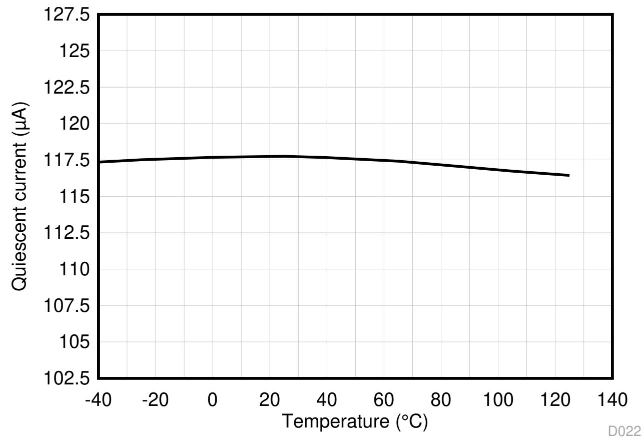


Figure 5-26. Quiescent Current per Channel vs Temperature

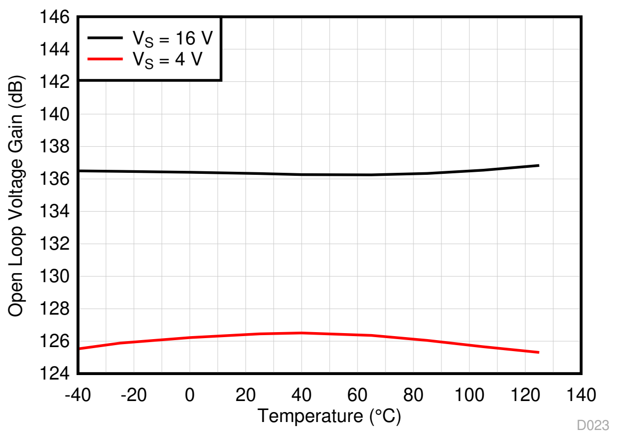


Figure 5-27. Open-Loop Voltage Gain vs Temperature (dB)

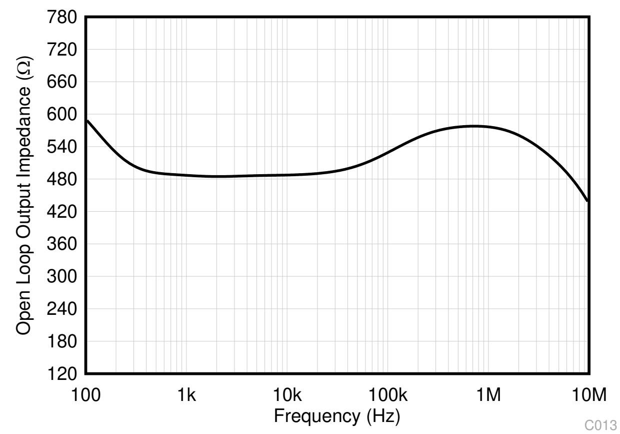
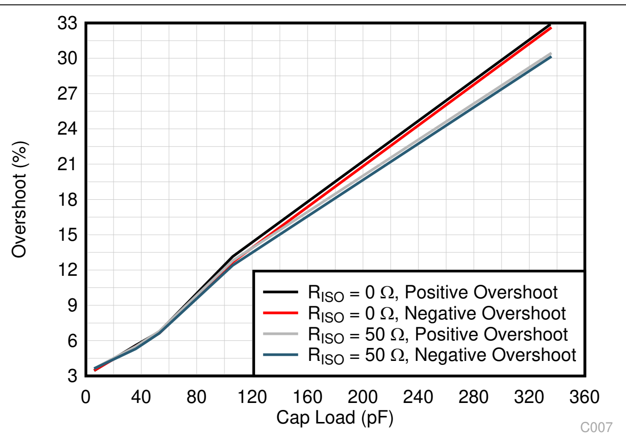
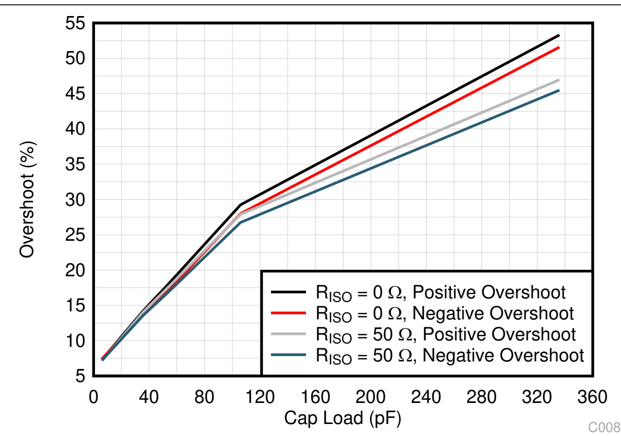


Figure 5-28. Open-Loop Output Impedance vs Frequency



G = –1, 100mV output step

Figure 5-29. Small-Signal Overshoot vs Capacitive Load

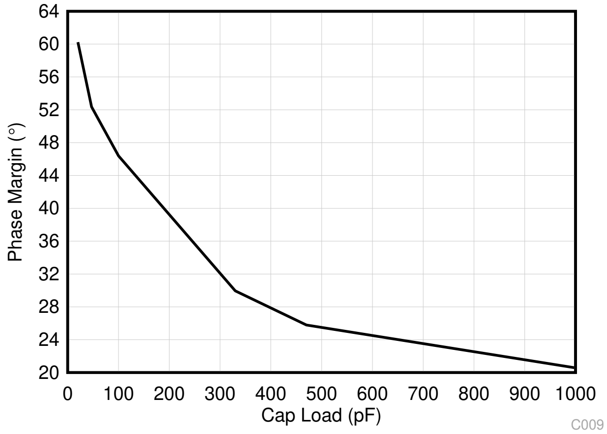


G = 1, 100mV output step

Figure 5-30. Small-Signal Overshoot vs Capacitive Load

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



G = –1, 100mV output step

Figure 5-31. Small-Signal Overshoot vs Capacitive Load

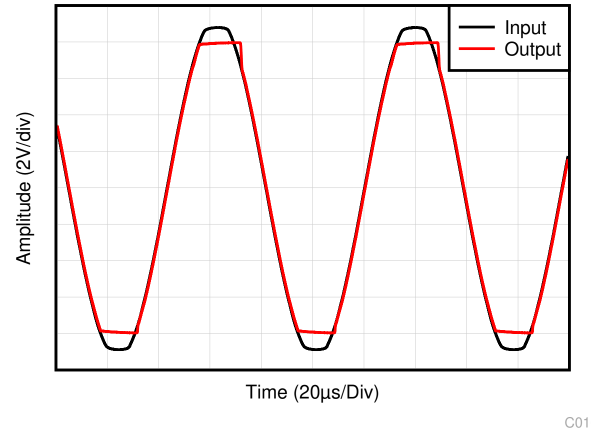
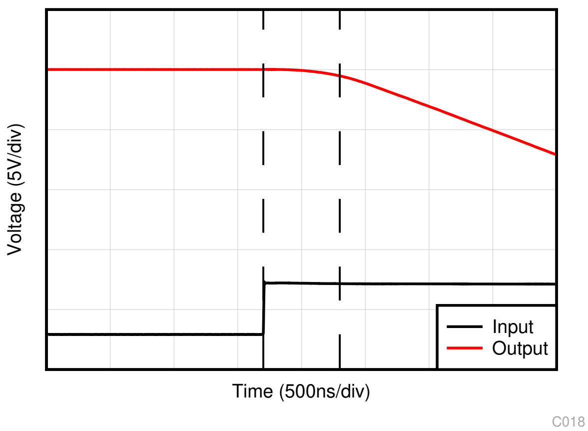
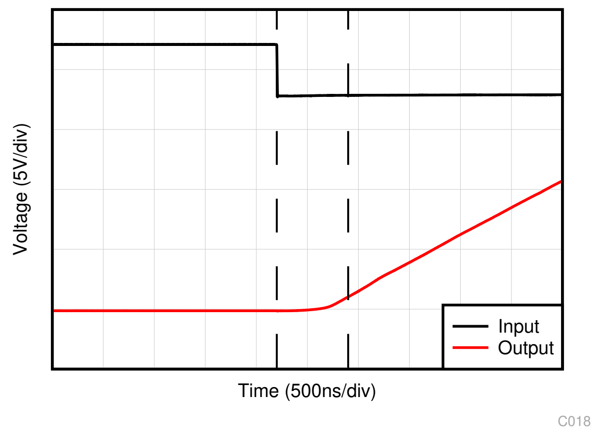


Figure 5-32. No Phase Reversal



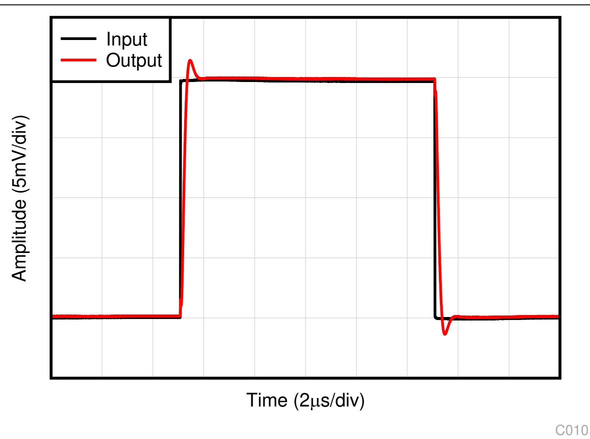
G = –10

Figure 5-33. Positive Overload Recovery



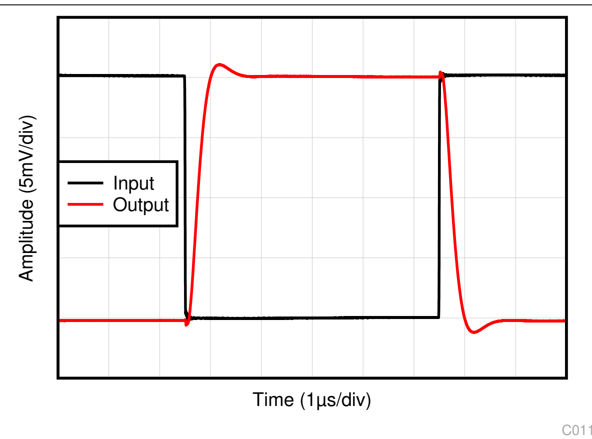
G = –10

Figure 5-34. Negative Overload Recovery



C_L = 20pF, G = 1, 20mV step response

Figure 5-35. Small-Signal Step Response

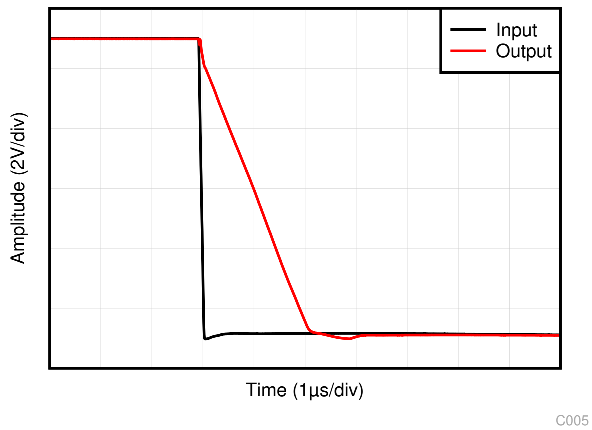


R_L = 1kΩ, C_L = 20pF, G = –1, 10mV step response

Figure 5-36. Small-Signal Step Response

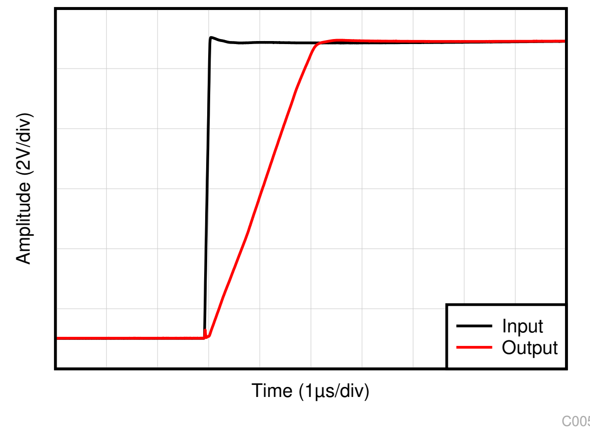
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)



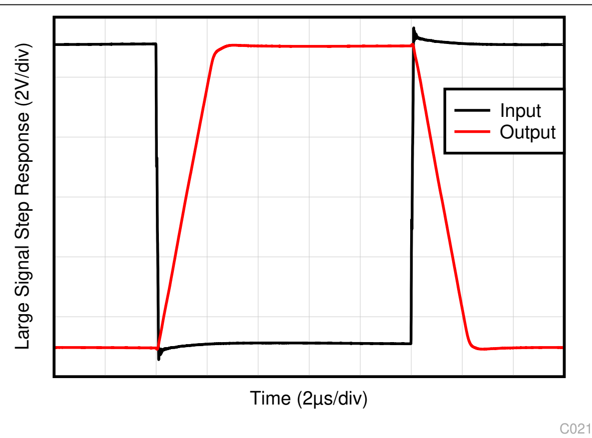
C_L = 20pF, G = 1

Figure 5-37. Large-Signal Step Response (Falling)



C_L = 20pF, G = 1

Figure 5-38. Large-Signal Step Response (Rising)



C_L = 10pF, G = –1

Figure 5-39. Large-Signal Step Response

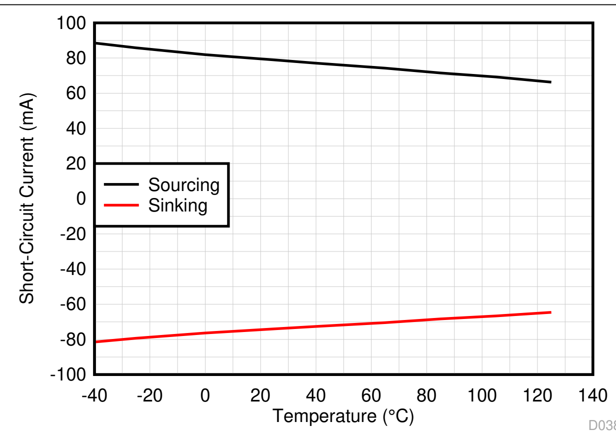


Figure 5-40. Short-Circuit Current vs Temperature

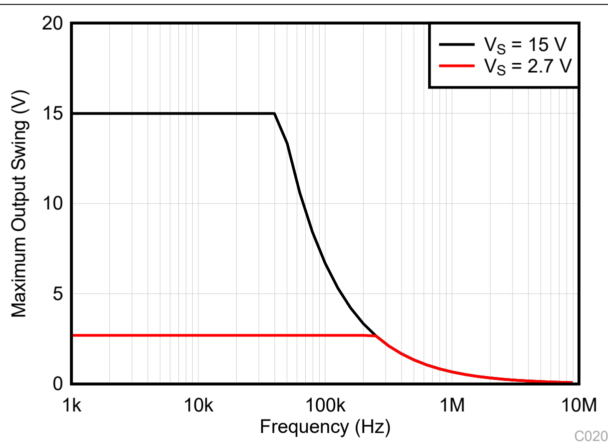


Figure 5-41. Maximum Output Voltage vs Frequency

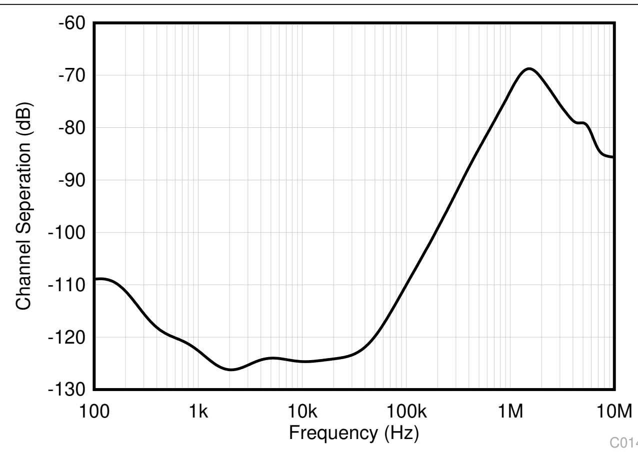


Figure 5-42. Channel Separation vs Frequency

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±8V, V_{CM} = V_S / 2, R_{LOAD} = 10kΩ connected to V_S / 2, and C_L = 100pF (unless otherwise noted)

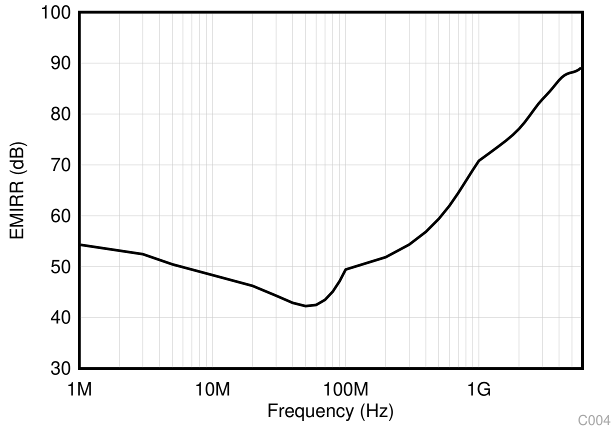


Figure 5-43. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

6 Detailed Description

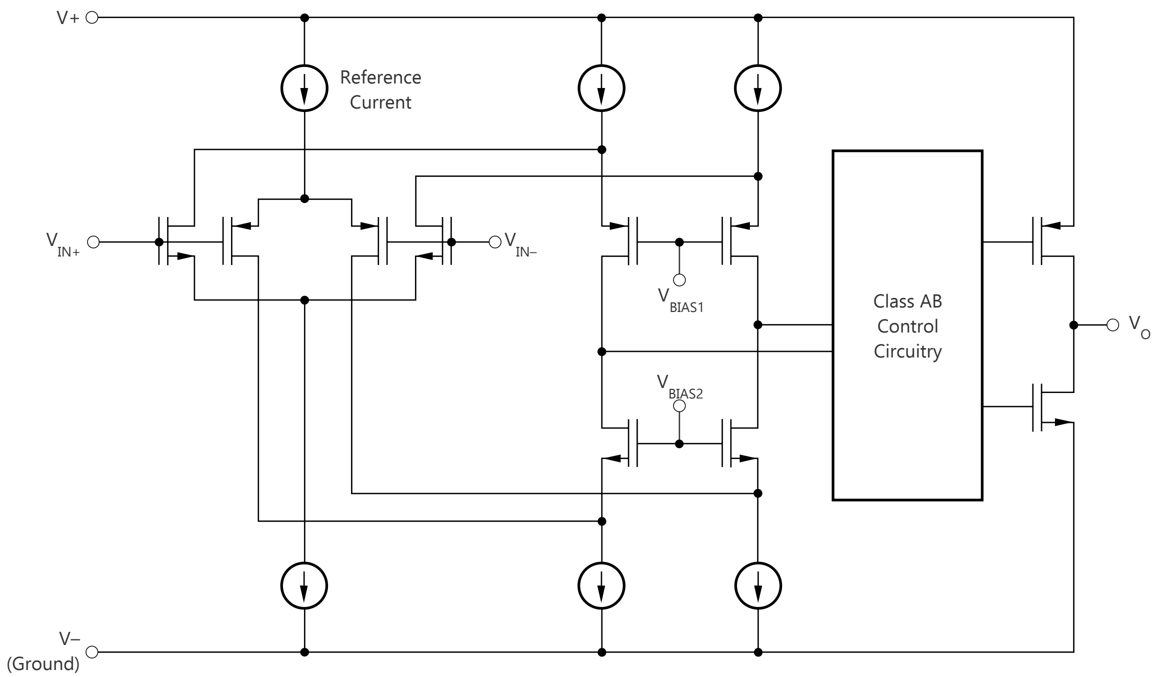
6.1 Overview

The TLV910x-Q1 family (TLV9101-Q1, TLV9102-Q1, and TLV9104-Q1) is a family of 16V general purpose operational amplifiers.

These devices offer excellent DC precision and AC performance, including rail-to-rail input/output, low offset (±300μV, typical), low offset drift (±0.6μV/°C, typical), and 1.1MHz bandwidth.

Wide differential and common-mode input-voltage range, high output current (±80mA), high slew rate (4.5V/μs), low power operation (120μA, typical), and shutdown functionality make the TLV910x-Q1 a robust, low-power, high-performance operational amplifier for industrial applications.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 EMI Rejection

The TLV910x-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques, and the TLV910x-Q1 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10MHz to 6GHz. Figure 6-1 shows the results of this testing on the TLV910x-Q1. Table 6-1 shows the EMIRR IN+ values for the TLV910x-Q1 at particular frequencies commonly encountered in real-world applications. Table 6-1 lists applications that can be centered on or operated near the particular frequency shown. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance of op amps and is available for download from www.ti.com.

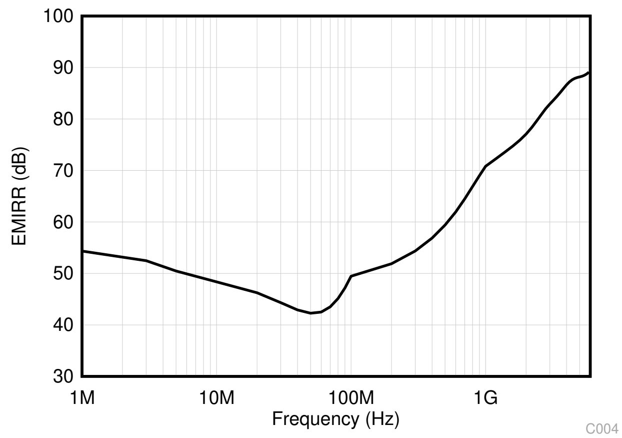


Figure 6-1. TLV910x-Q1 EMIRR Testing

Table 6-1. TLV910x-Q1 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	59.5dB
900MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6GHz), GSM, aeronautical mobile, UHF applications	68.9dB
1.8GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1GHz to 2GHz)	77.8dB
2.4GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2GHz to 4GHz)	78.0dB
3.6GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.8dB
5GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4GHz to 8GHz)	87.6dB

6.3.2 Phase Reversal Protection

The TLV910x-Q1 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The TLV910x-Q1 is a rail-to-rail input op amp, therefore the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal. Instead, the output limits into the appropriate rail. Figure 6-2 shows this performance.

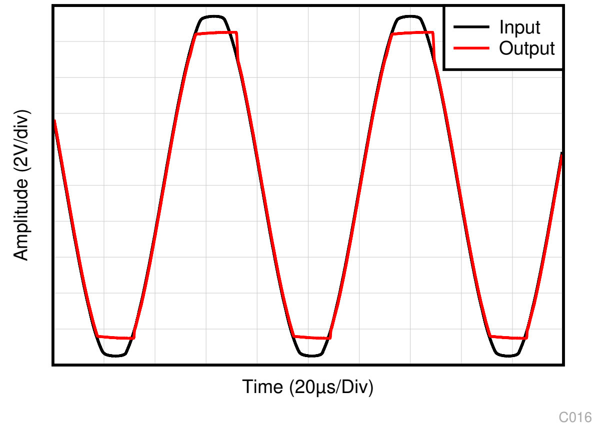


Figure 6-2. No Phase Reversal

6.3.3 Thermal Protection

The internal power dissipation of any amplifier causes the internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the TLV910x-Q1 is 150°C. Exceeding this temperature causes damage to the device. The TLV910x-Q1 has a thermal protection feature that prevents damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 140°C. Figure 6-3 shows an application example for the TLV9101-Q1 that has significant self heating (154°C) because of the power dissipation (0.39W). Thermal calculations indicate that for an ambient temperature of 100°C, the device junction temperature must reach 154°C. The actual device, however, turns off the output drive to maintain a safe junction temperature. Figure 6-3 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3V. When self heating causes the device junction temperature to increase above 140°C, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor RL.

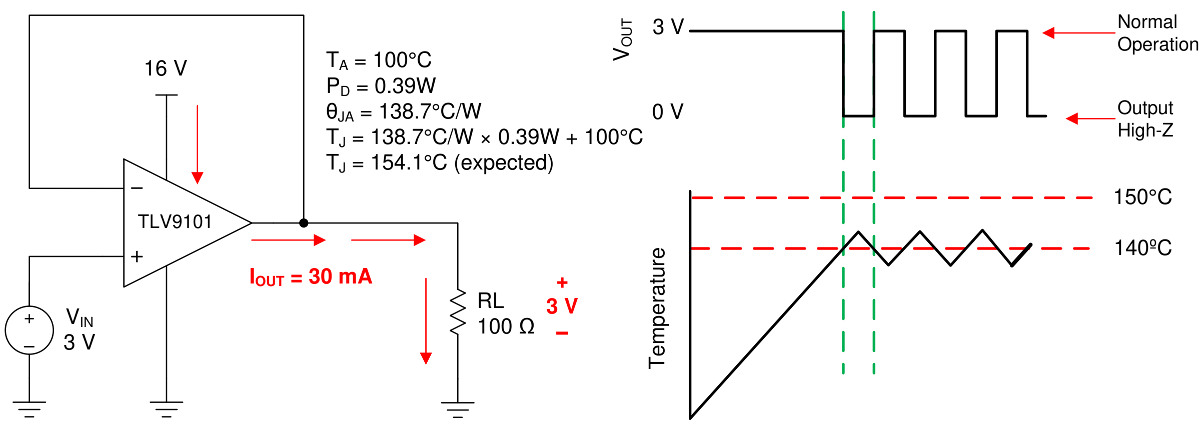


Figure 6-3. Thermal Protection

6.3.4 Capacitive Load and Stability

The TLV910x-Q1 features a resistive output stage capable of driving moderate capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive large capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads (see Figure 6-4 and Figure 6-5). The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation.

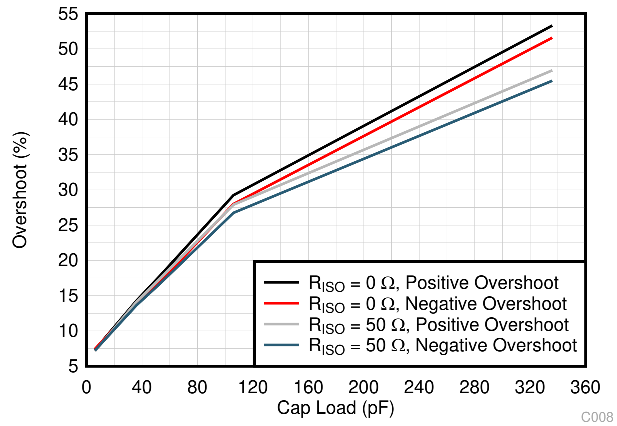


Figure 6-4. Small-Signal Overshoot vs Capacitive Load (100mV Output Step, G = 1)

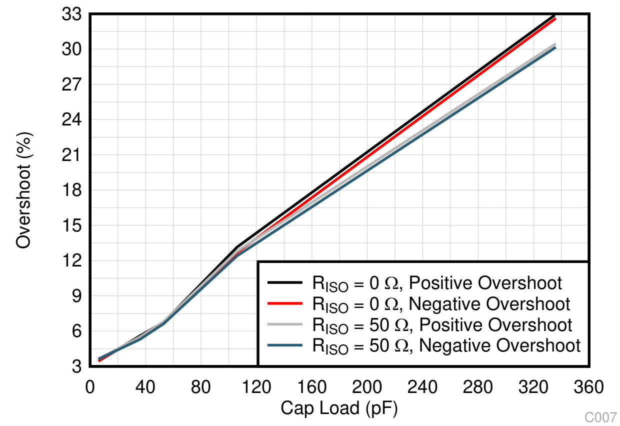


Figure 6-5. Small-Signal Overshoot vs Capacitive Load (100mV Output Step, G = –1)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small (10 Ω to 20 Ω) resistor, R_{ISO}, in series with the output, as shown in Figure 6-6. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. The high capacitive load drive of the TLV910x-Q1 is designed for applications like reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in Figure 6-6 uses an isolation resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin.

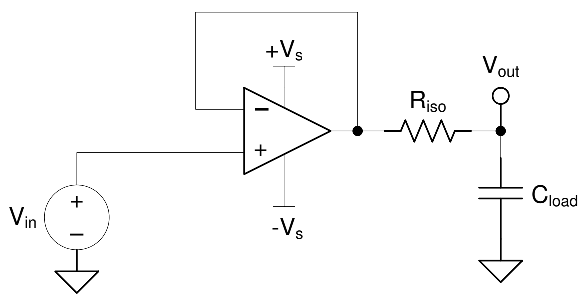


Figure 6-6. Extending Capacitive Load Drive With the TLV9101-Q1

6.3.5 Common-Mode Voltage Range

The TLV910x-Q1 is a 16V, true rail-to-rail input operational amplifier with an input common-mode range that extends 100mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in Figure 6-7. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1V to 100mV above the positive supply. The P-channel pair is active for inputs from 100mV below the negative supply to approximately (V+) – 2V. There is a small transition region, typically (V+) –2V to (V+) – 1V in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance can be degraded compared to operation outside this region. To achieve best performance with the TLV910x-Q1 family, avoid this transition region when possible.

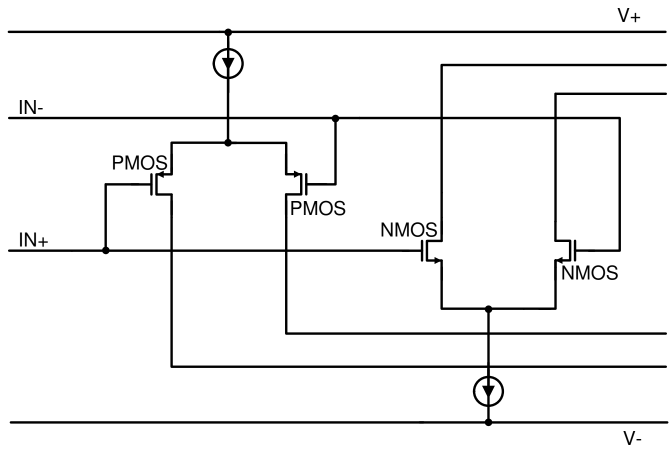


Figure 6-7. Rail-to-Rail Input Stage

6.3.6 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 6-8 shows an illustration of the ESD circuits contained in the TLV910x-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

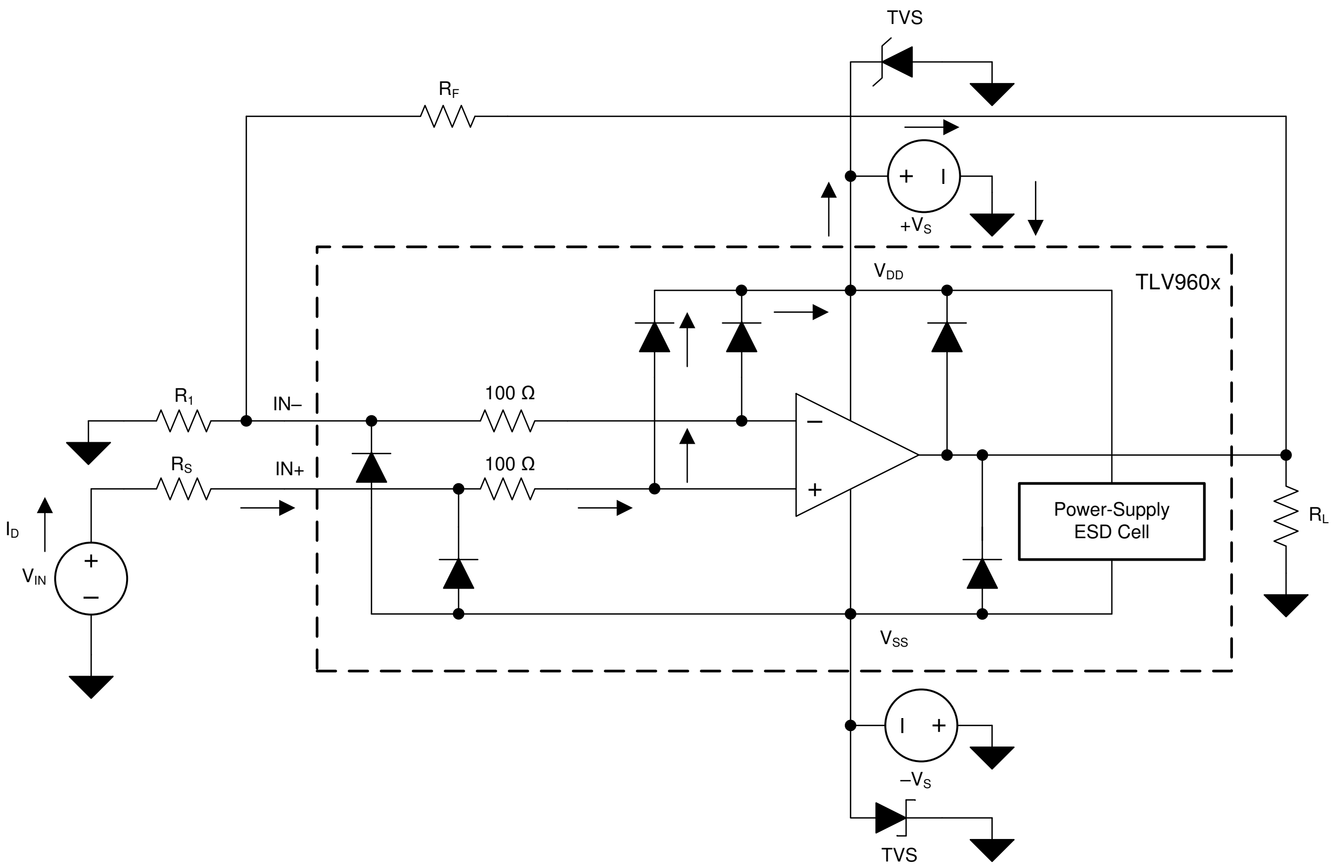


Figure 6-8. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example, 1kV, 100ns), whereas an EOS event is long duration and lower voltage (for example, 50V, 100ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

6.3.7 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV910x-Q1 is approximately 1µs.

6.3.8 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier exhibits some amount of deviation from the expected value, like the input offset voltage of an amplifier. These deviations often follow *Gaussian* ("bell curve"), or *normal* distributions, and circuit designers can leverage this information to guardband a system, even when there is not a minimum or maximum specification in *Electrical Characteristics*.

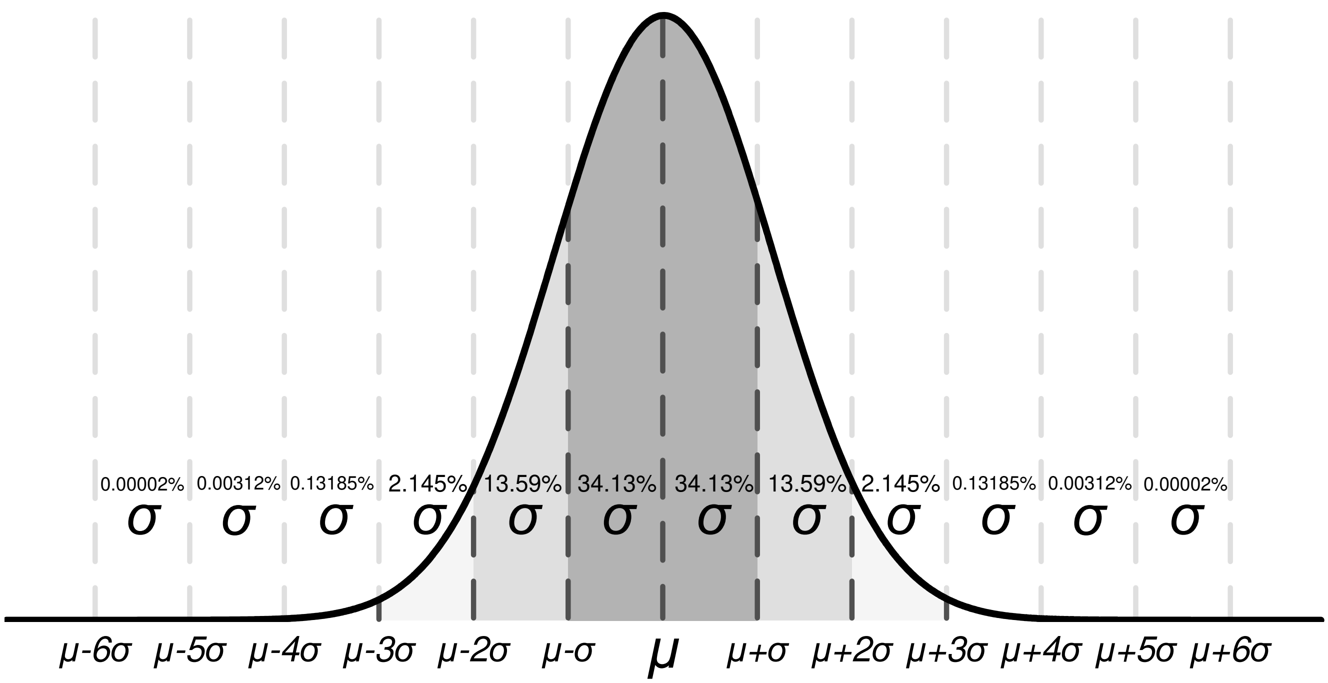


Figure 6-9. Gaussian Distribution

Figure 6-9 shows an example distribution, where μ, or *mu*, is the mean of the distribution, and where σ, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu-\sigma$ to $\mu+\sigma$).

Depending on the specification, values listed in the *typical* column of *Electrical Characteristics* are represented in different ways. As a general rule, if a specification naturally has a nonzero mean (for example, gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) to most accurately represent the typical value.

You can use this chart to calculate approximate probability of a specification in a unit; for example, for TLV910x-Q1, the typical input voltage offset is 300μV, so 68.2% of all TLV910x-Q1 devices are expected to have an offset from –300μV to +300μV. At 4 σ (±1200μV), 99.9937% of the distribution has an offset voltage less than ±1200μV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are specified by TI, and units outside these limits are removed from production material. For example, the TLV910x-Q1 family has a maximum offset voltage of 1.5mV at 25°C, and even though this corresponds to 5σ (≈1 in 1.7 million units), which is extremely unlikely, TI removes any unit with larger offset than 1.5mV from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for your application, and design worst-case conditions using this value. For example, the 6σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance and can be an option as a wide guardband to design a system around. In this case, the TLV910x-Q1 family does not have a maximum or minimum for offset voltage drift, but based on Figure 5-2 and the typical value of 0.6μV/°C in *Electrical Characteristics*, the 6-σ value for offset voltage drift is about 3.6μV/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot specify the performance of a device. This information is intended to be used only to estimate the performance of a device.

6.4 Device Functional Modes

The TLV910x-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 2.7V (±1.35V). The maximum power supply voltage for the TLV910x-Q1 is 16V (±8V).

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLV910x-Q1 family offers excellent DC precision and DC performance. These devices operate up to 16V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 1.1MHz bandwidth and high output drive. These features make the TLV910x-Q1 a robust, high-performance operational amplifier for high-voltage automotive applications.

7.2 Typical Applications

7.2.1 Low-Side Current Measurement

Figure 7-1 shows the TLV910x-Q1 configured in a low-side current sensing application. For a full analysis of the circuit shown in Figure 7-1 including theory, calculations, simulations, and measured data, see TI Precision Design TIPD129, *0A to 1A Single-Supply Low-Side Current-Sensing Solution*.

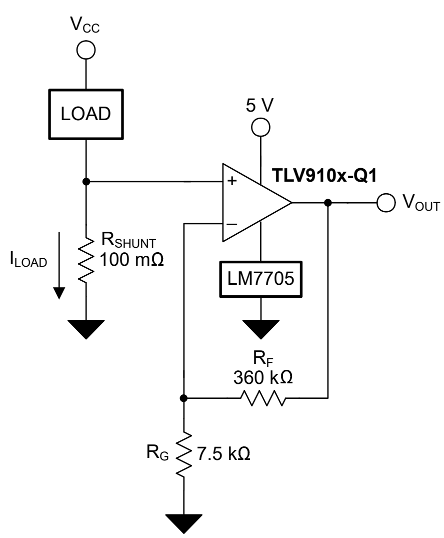


Figure 7-1. TLV910x-Q1 in a Low-Side, Current-Sensing Application

7.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0A to 1A
- Output voltage: 4.9V
- Maximum shunt voltage: 100mV

7.2.1.2 Detailed Design Procedure

Use Equation 1 to calculate the transfer function of the circuit in Figure 7-1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \text{Gain} \tag{1}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0A to 1A. To keep the shunt voltage below 100mV at maximum load current, use Equation 2 to calculate the largest shunt resistor allowed.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100\text{ mV}}{1\text{ A}} = 100\text{ m}\Omega \tag{2}$$

Using Equation 2, R_{SHUNT} is calculated to be 100mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV910x-Q1 to produce an output voltage of 0V to 4.9V. Use Equation 3 to calculate the gain required for the TLV910x-Q1 to produce the necessary output voltage is calculated using.

$$\text{Gain} = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \tag{3}$$

Equation 3 calculates the required gain as 49V/V, which is set with resistors R_F and R_G. Equation 4 is used to size the resistors, R_F and R_G, to set the gain of the TLV910x-Q1 to 49V/V.

$$\text{Gain} = 1 + \frac{(R_F)}{(R_G)} \tag{4}$$

With R_F as 360kΩ, Equation 4 calculates R_G as 7.5kΩ. This example has the R_F and R_G as 360kΩ and 7.5kΩ because these values are the standard resistor values that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. Figure 7-2 shows the measured transfer function of the circuit shown in Figure 7-1.

7.2.1.3 Application Curve

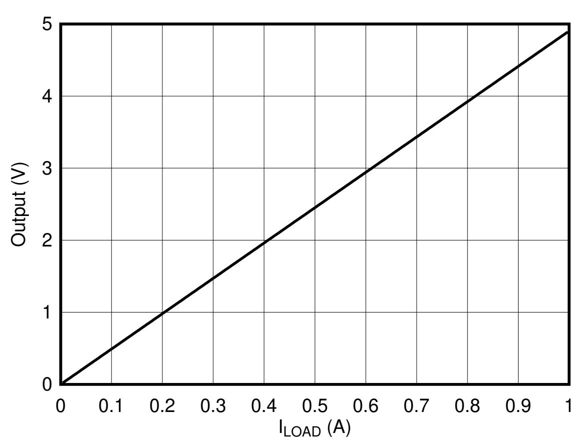


Figure 7-2. Low-Side, Current-Sense, Transfer Function

7.3 Power Supply Recommendations

The TLV910x-Q1 is specified for operation from 2.7V to 16V (±1.35V to ±8V), and many specifications apply from –40°C to 125°C.

> **CAUTION**
>
> Supply voltages larger than 20V can permanently damage the device. See *Absolute Maximum Ratings*.

Place 0.1µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. See *Layout* for more information.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  – Connect low-ESR, 0.1µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 7-4, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example

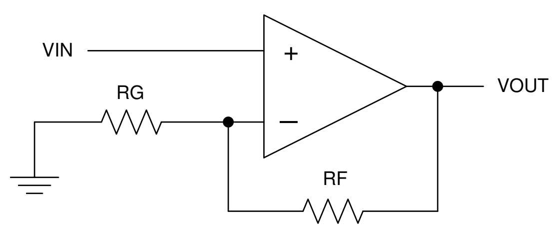


Figure 7-3. Schematic Representation

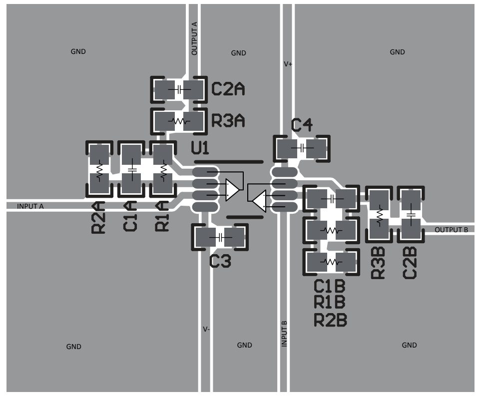


Figure 7-4. Example Layout for VSSOP-8 (DGK) Package

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional DC, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

8.2 Documentation Support

8.2.1 Related Documentation

Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV9104QPWRQ1	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9104PW
TLV9104QPWRQ1.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9104PW

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV9104-Q1 :

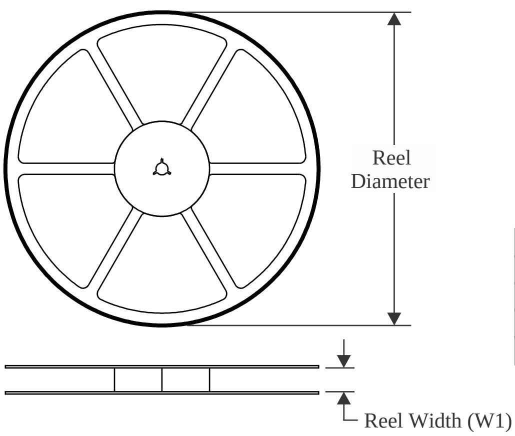
- Catalog : TLV9104

NOTE: Qualified Version Definitions:

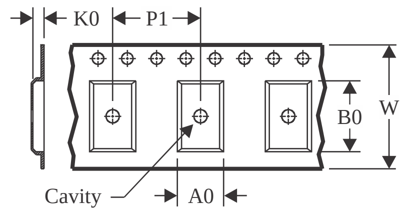
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

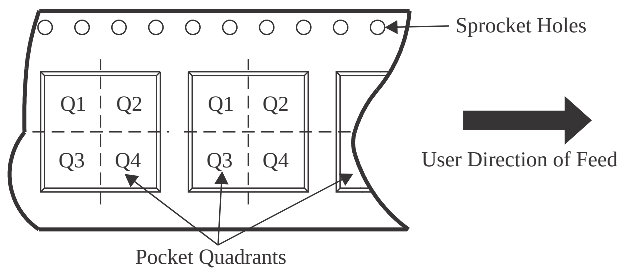


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

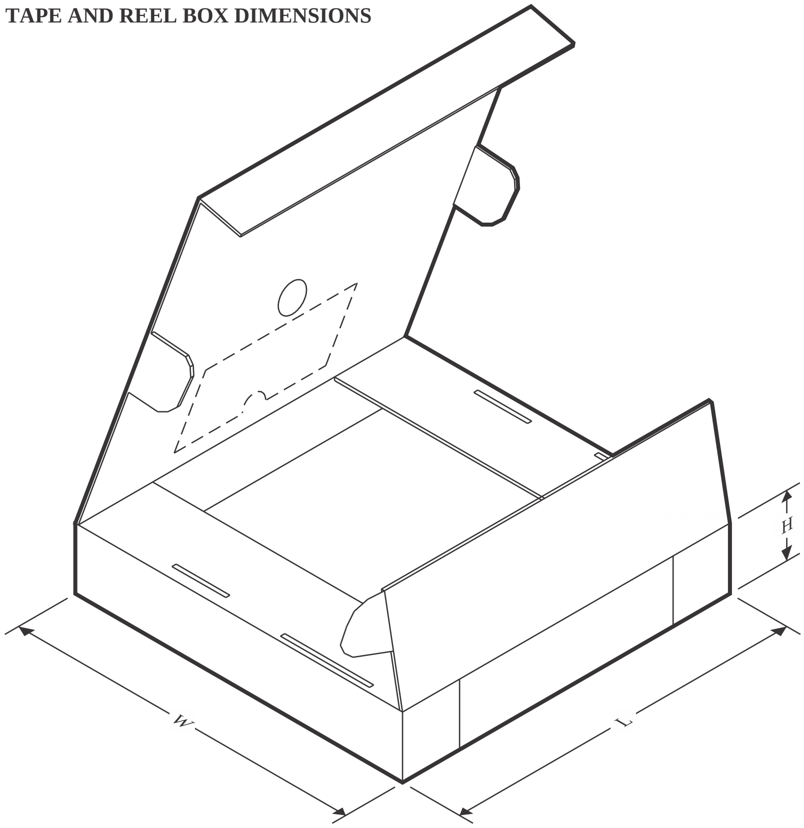
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

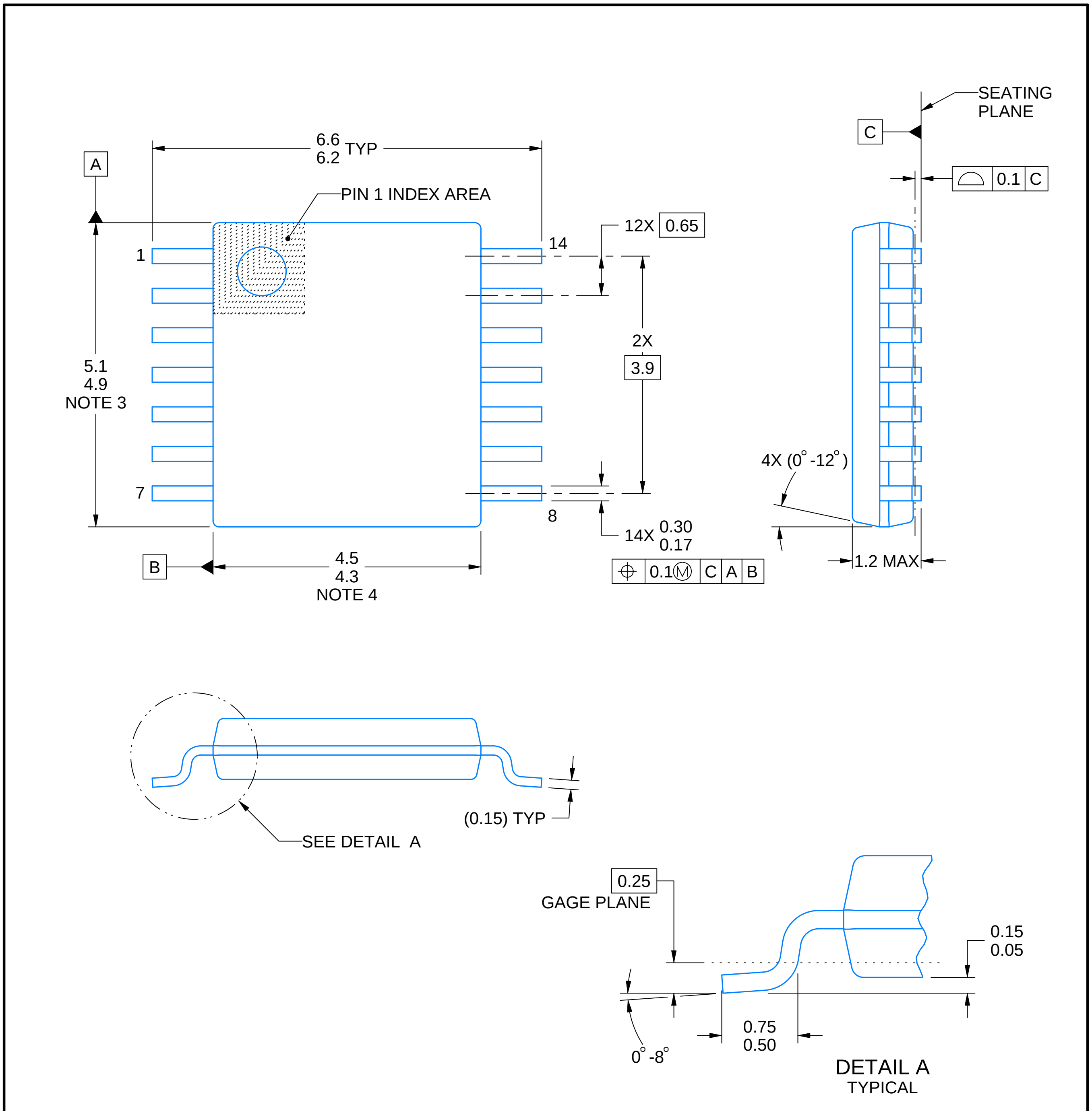
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9104QPWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9104QPWRQ1	TSSOP	PW	14	3000	353.0	353.0	32.0



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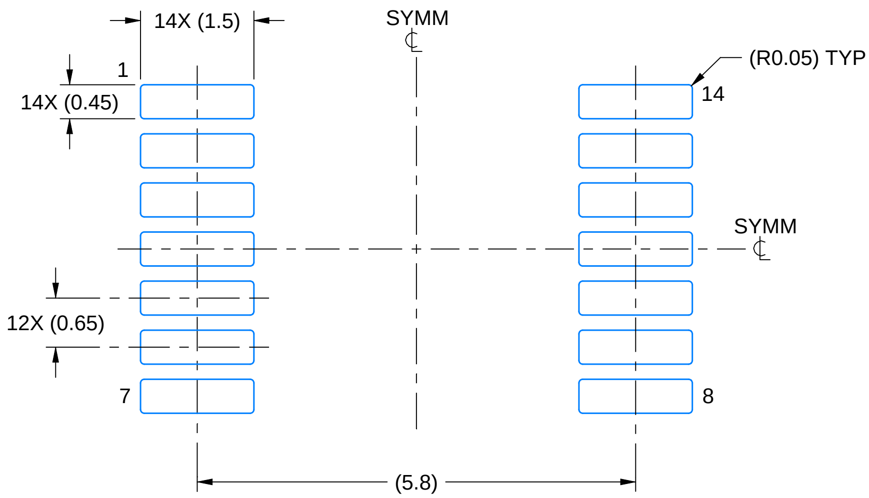
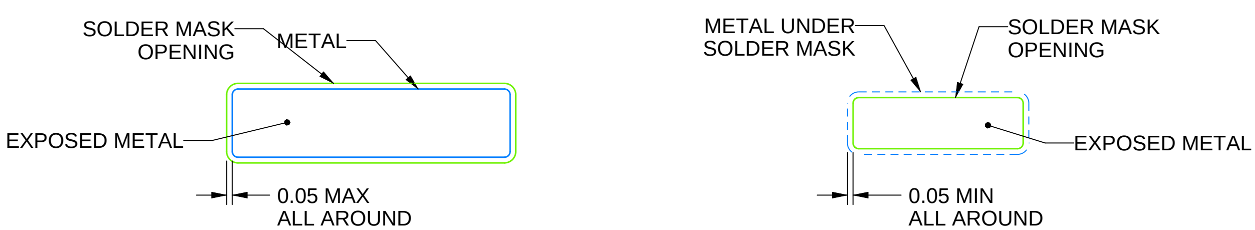
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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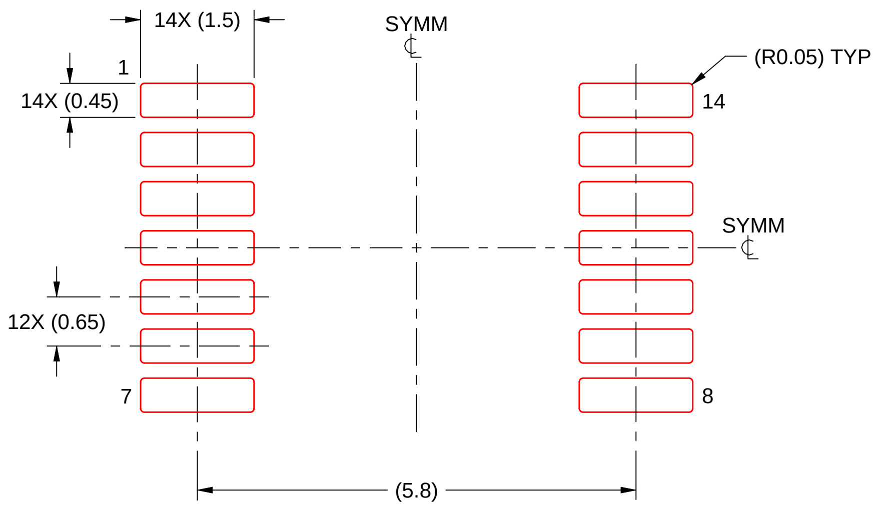
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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