TLV9351-Q1, TLV9352-Q1, TLV9354-Q1
SBOSA34E – JANUARY 2021 – REVISED MARCH 2024

TLV935x-Q1 3.5MHz, 40V, RRO, MUX-Friendly Automotive Operational Amplifier for Cost-Sensitive Systems

1 Features

- Low offset voltage: ±350µV
- Low offset voltage drift: ±1.5µV/°C
- Low noise: 15nV/√Hz at 1kHz
- High common-mode rejection: 110dB
- Low bias current: ±10pA
- Rail-to-rail output
- MUX-friendly/comparator inputs
  - Amplifier operates with differential inputs up to supply rail
  - Amplifier can be used in open-loop or as comparator
- Wide bandwidth: 3.5MHz GBW
- High slew rate: 20V/µs
- Low quiescent current: 600µA per amplifier
- Wide supply: ±2.25V to ±20V, 4.5V to 40V
- Robust EMIRR performance: EMI/RFI filters on input pins

2 Applications

- Optimized for AEC-Q100 grade 1 applications
- Infotainment and cluster
- Passive safety
- Body electronics and lighting
- HEV/EV inverter and motor control
- On-board (OBC) and wireless changer
- Powertrain current sensor
- Advanced driver assistance systems (ADAS)
- Single-supply, low-side current sensing

3 Description

The TLV935x-Q1 family (TLV9351-Q1, TLV9352-Q1, and TLV9354-Q1) is a family of 40V cost-optimized automotive operational amplifiers.

These devices offer strong DC and AC specifications, including rail-to-rail output, low offset (±350µV, typical), low offset drift (±1.5µV/°C, typical), and 3.5MHz bandwidth.

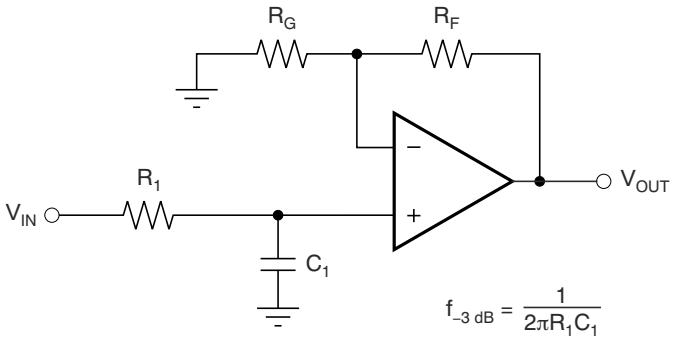
Unique features such as differential input-voltage range to the supply rail, high output current (±60mA), and high slew rate (20V/µs) make the TLV935x-Q1 a robust operational amplifier for high-voltage, cost-sensitive applications.

The TLV935x-Q1 family of op amps is available in standard packages and is specified from –40°C to 125°C.

Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)	PACKAGE SIZE(2)
TLV9351-Q1	Single	DBV (SOT-23, 5)	2.9mm × 2.8mm
		DCK (SC70, 5)	2.0mm × 2.1mm
TLV9352-Q1	Dual	D (SOIC, 8)	4.9mm × 6mm
		PW (TSSOP, 8)	3mm × 6.4mm
		DGK (VSSOP, 8)	3mm × 4.9mm
TLV9354-Q1	Quad	D (SOIC, 14)	8.65mm × 6mm
		DYY (SOT-23, 14)	4.2mm × 3.26mm
		PW (TSSOP, 14)	5mm × 6.4mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TLV935x-Q1 in a Single-Pole, Low-Pass Filter

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

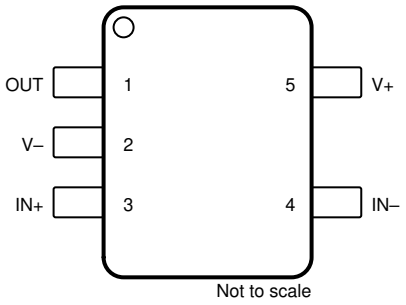


Figure 4-1. TLV9351-Q1 DBV Package, 5-Pin SOT-23 (Top View)

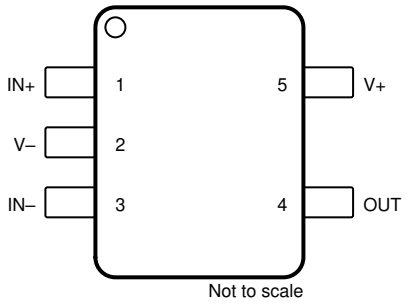


Figure 4-2. TLV9351-Q1 DCK Package, 5-Pin SC70 (Top View)

Table 4-1. Pin Functions: TLV9351-Q1

PIN			TYPE[1]	DESCRIPTION
NAME	DBV	DCK		
IN+	3	1	I	Noninverting input
IN–	4	3	I	Inverting input
OUT	1	4	O	Output
V+	5	5	—	Positive (highest) power supply
V–	2	2	—	Negative (lowest) power supply

(1) I = input, O = output

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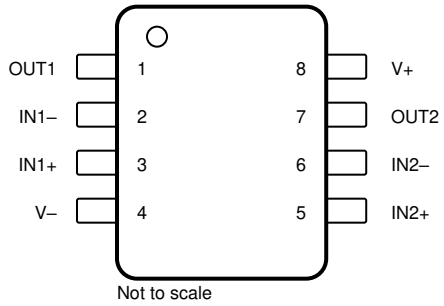


Figure 4-3. TLV9352-Q1 D, PW and DGK Package, 8-Pin SOIC, TSSOP and VSSOP (Top View)

Table 4-2. Pin Functions: TLV9352-Q1

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN2+	5	I	Noninverting input, channel 1
IN1–	2	I	Inverting input, channel 1
IN2–	6	I	Inverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

(1) I = input, O = output

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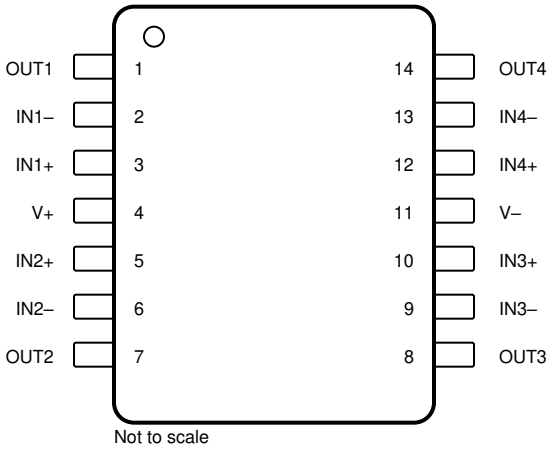


Figure 4-4. TLV9354-Q1 D, DYY, and PW Package, 14-Pin SOIC, SOT-23, and TSSOP (Top View)

Table 4-3. Pin Functions: TLV9354-Q1

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IN1+	3	I	Noninverting input, channel 1
IN2+	5	I	Noninverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN1–	2	I	Inverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN3–	9	I	Inverting input, channel 3
IN4–	13	I	Inverting input, channel 4
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V+	4	—	Positive (highest) power supply
V–	11	—	Negative (lowest) power supply

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	42	V
Signal input pins	Common-mode voltage (3)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage(3)		V_S + 0.2	V
	Current (3)	–10	10	mA
Output short-circuit (2)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings,* the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Short-circuit to ground, one amplifier per package.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	4.5	40	V
V_I	Input voltage range	(V–) – 0.1	(V+) – 2	V
T_A	Specified ambient temperature	–40	125	°C

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5.4 Thermal Information for Single Channel

THERMAL METRIC (1)		TLV9351-Q1		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.4	202.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.2	101.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.6	47.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.8	18.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.3	47.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Thermal Information for Dual Channel

THERMAL METRIC (1)		TLV9352-Q1			UNIT
		D (SOIC)	DGK (VSSOP)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	132.6	176.5	185.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.4	68.1	74.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.1	98.2	115.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.0	12.0	12.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	75.4	96.7	114.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.6 Thermal Information for Quad Channel

THERMAL METRIC (1)		TLV9354-Q1			UNIT
		D (SOIC)	DYY (SOT-23)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	101.4	110.7	118	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.6	55.9	47.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.3	35.3	60.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.5	2.3	6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.9	35.1	60.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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5.7 Electrical Characteristics

For V_S = (V+) – (V–) = 4.5 V to 40 V (±2.25 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_{CM} = V–			±0.35	±1.8	mV
			T_A = –40°C to 125°C			±2	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to 125°C		±1.5		µV/°C
PSRR	Input offset voltage versus power supply	V_{CM} = V–	T_A = –40°C to 125°C		±2	±5	µV/V
	Channel separation	f = 0 Hz			5		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±10		pA
I_{OS}	Input offset current				±10		pA
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			2		μV_{PP}
					0.33		μV_{RMS}
e_N	Input voltage noise density	f = 1 kHz			15		nV/√Hz
		f = 10 kHz			14		
i_N	Input current noise	f = 1 kHz			2		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) – 0.2		(V+) – 2	V
CMRR	Common-mode rejection ratio	V_S = 40 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V (Main input pair)	T_A = –40°C to 125°C	95	110		dB
		V_S = 4.5 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V (Main input pair)		82	90		
INPUT CAPACITANCE							
Z_{ID}	Differential				100 || 3		MΩ || pF
Z_{ICM}	Common-mode				6 || 1		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 40 V, V_{CM} = V– (V–) + 0.1 V < V_O < (V+) – 0.1 V		120	130		dB
			T_A = –40°C to 125°C		127		

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5.7 Electrical Characteristics (continued)

For V_S = (V+) – (V–) = 4.5 V to 40 V (±2.25 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and $V_{O\ UT}$ = V_S / 2, unless otherwise noted.

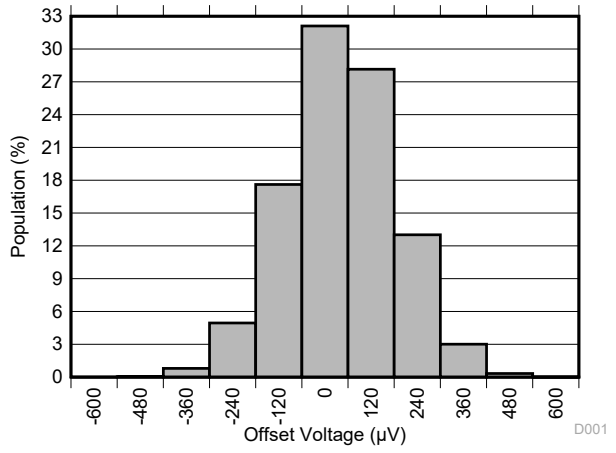
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				3.5		MHz
SR	Slew rate	V_S = 40 V, G = +1, C_L = 20 pF			20		V/µs
t_S	Settling time	To 0.01%, V_S = 40 V, V_{STEP} = 10 V , G = +1, CL = 20 pF			5		µs
		To 0.01%, V_S = 40 V, V_{STEP} = 2 V , G = +1, CL = 20 pF			4		
		To 0.1%, V_S = 40 V, V_{STEP} = 10 V , G = +1, CL = 20 pF			4		
		To 0.1%, V_S = 40 V, V_{STEP} = 2 V , G = +1, CL = 20 pF			3		
	Phase margin	G = +1, R_L = 10 kΩ			60		°
	Overload recovery time	V_{IN} × gain > V_S			600		ns
THD+N	Total harmonic distortion + noise (1)	V_S = 40 V, V_O = 1 V_{RMS}, G = 1, f = 1 kHz			0.001%		
OUTPUT							
	Voltage output swing from rail	Positive and negative rail headroom	V_S = 40 V, R_L = no load(2)		5	10	mV
			V_S = 40 V, R_L = 10 kΩ		50	55	
			V_S = 40 V, R_L = 2 kΩ		200	250	
			V_S = 4.5 V, R_L = no load(2)		1		
			V_S = 4.5 V, R_L = 10 kΩ		20	30	
			V_S = 4.5 V, R_L = 2 kΩ		40	75	
I_{SC}	Short-circuit current				±60		mA
C_{LOAD}	Capacitive load drive				300		pF
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A			600		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_{CM} = V–, I_O = 0 A			650	800	µA
			T_A = –40°C to 125°C			850	

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.
(2) Specified by characterization only.

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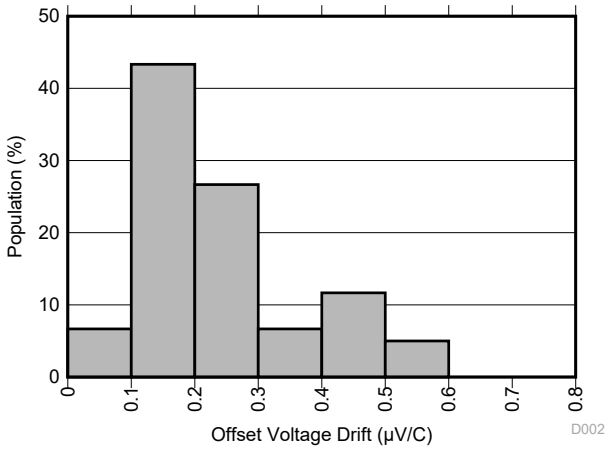
5.8 Typical Characteristics

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)



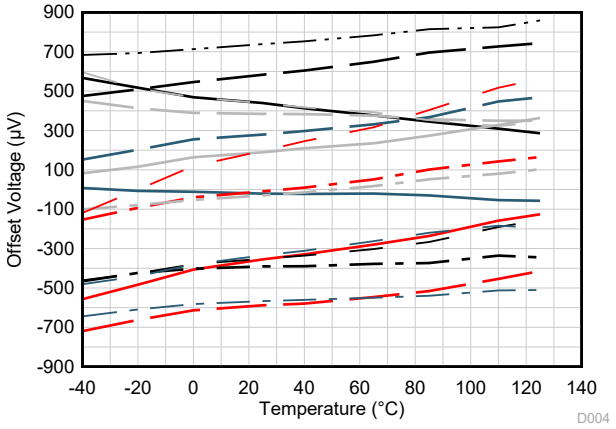
Distribution from 15462 amplifiers, T_A = 25°C

Figure 5-1. Offset Voltage Production Distribution



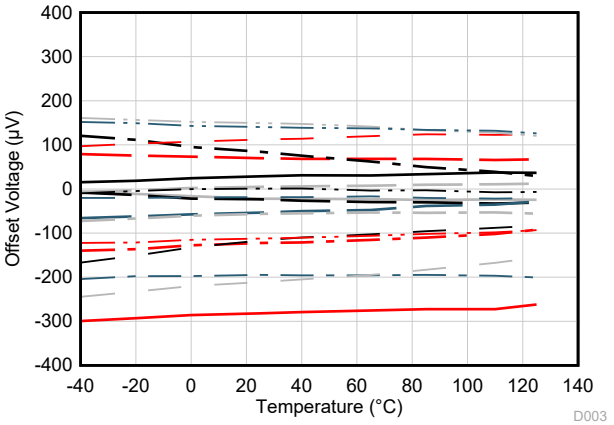
Distribution from 60 amplifiers

Figure 5-2. Offset Voltage Drift Distribution



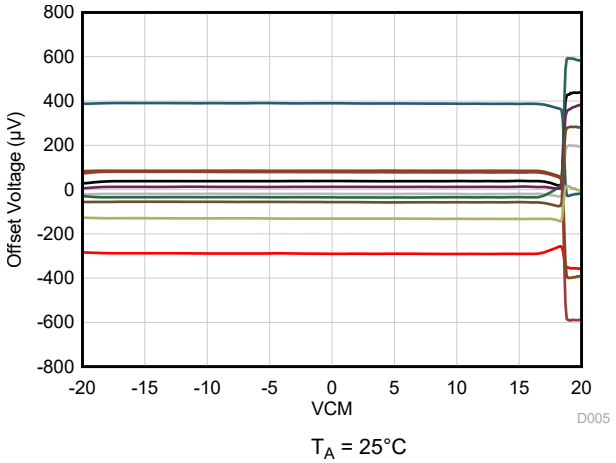
V_{CM} = V+

Figure 5-3. Offset Voltage vs Temperature



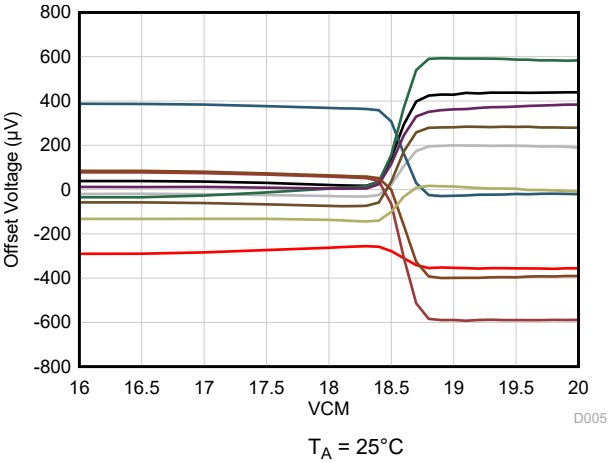
V_{CM} = V–

Figure 5-4. Offset Voltage vs Temperature



T_A = 25°C

Figure 5-5. Offset Voltage vs Common-Mode Voltage



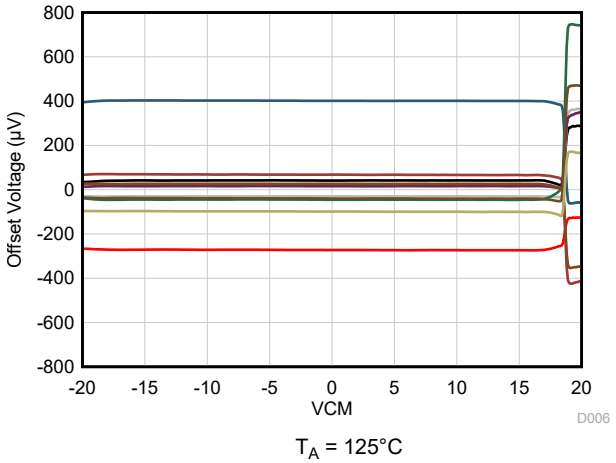
T_A = 25°C

Figure 5-6. Offset Voltage vs Common-Mode Voltage (Transition Region)

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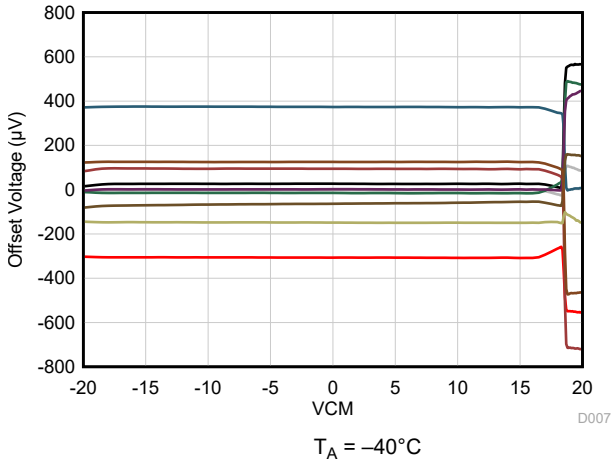
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)



T_A = 125°C

Figure 5-7. Offset Voltage vs Common-Mode Voltage



T_A = –40°C

Figure 5-8. Offset Voltage vs Common-Mode Voltage

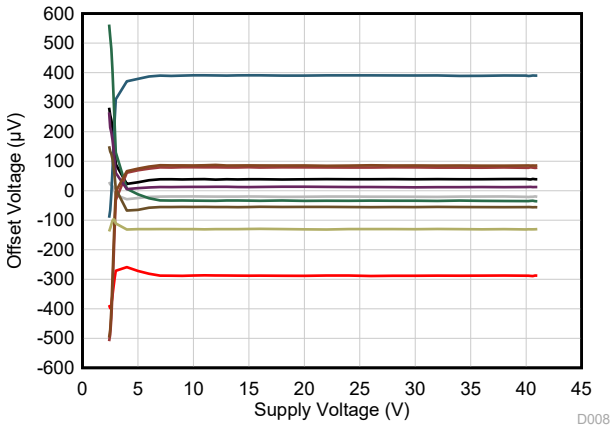
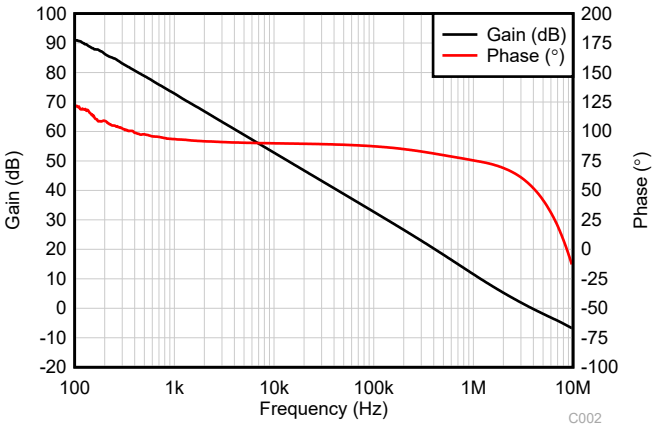


Figure 5-9. Offset Voltage vs Power Supply



C_L = 20 pF

Figure 5-10. Open-Loop Gain and Phase vs Frequency

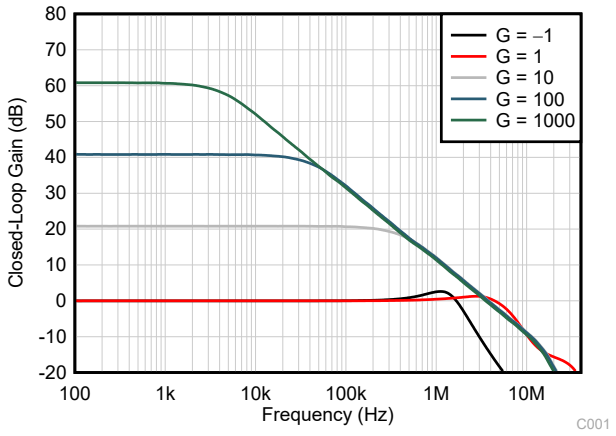


Figure 5-11. Closed-Loop Gain vs Frequency

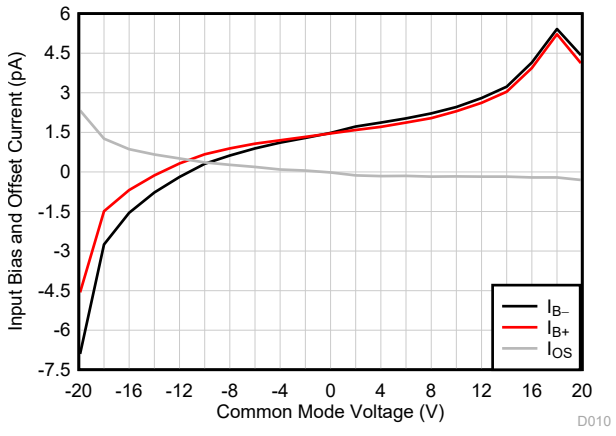


Figure 5-12. Input Bias Current vs Common-Mode Voltage

5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)

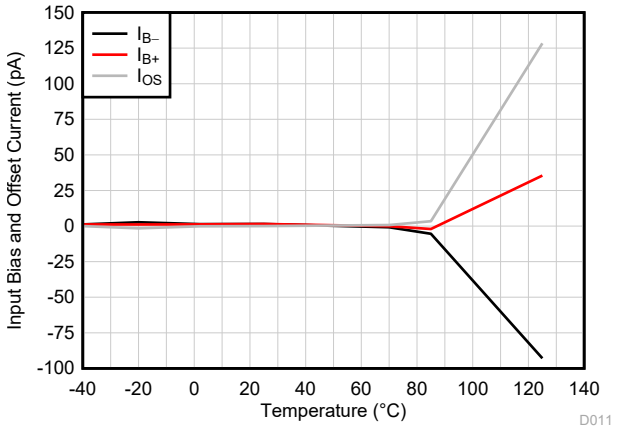


Figure 5-13. Input Bias Current vs Temperature

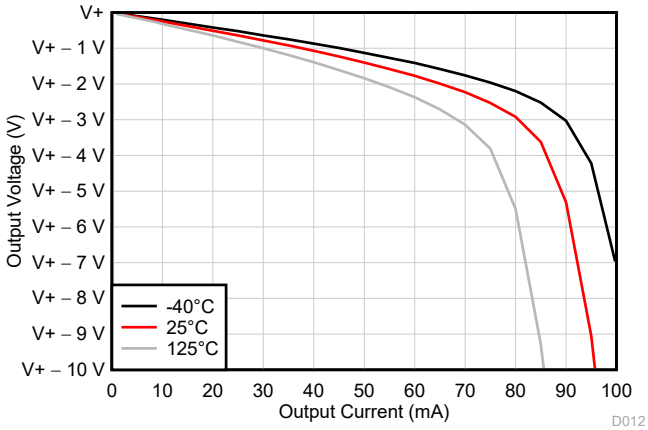


Figure 5-14. Output Voltage Swing vs Output Current (Sourcing)

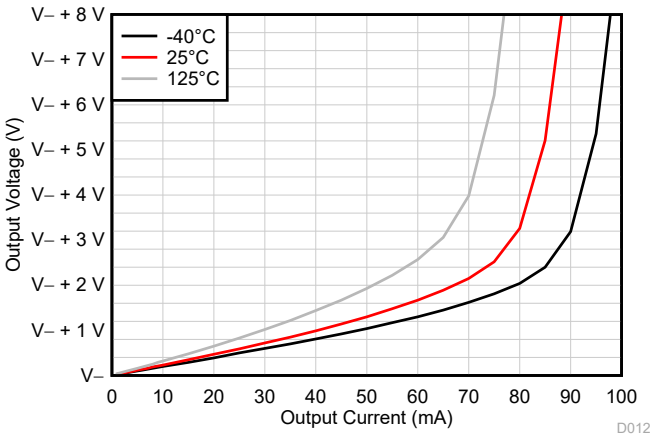


Figure 5-15. Output Voltage Swing vs Output Current (Sinking)

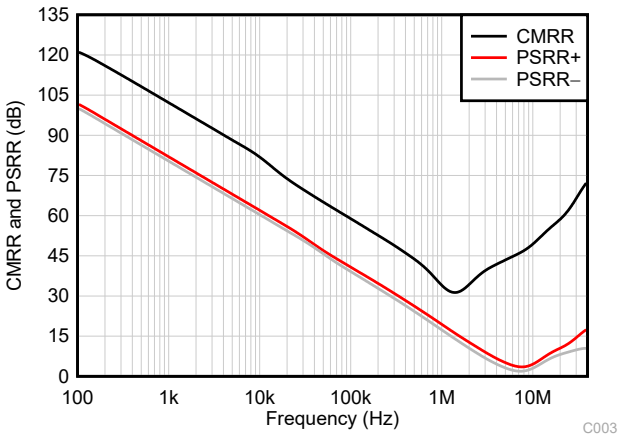
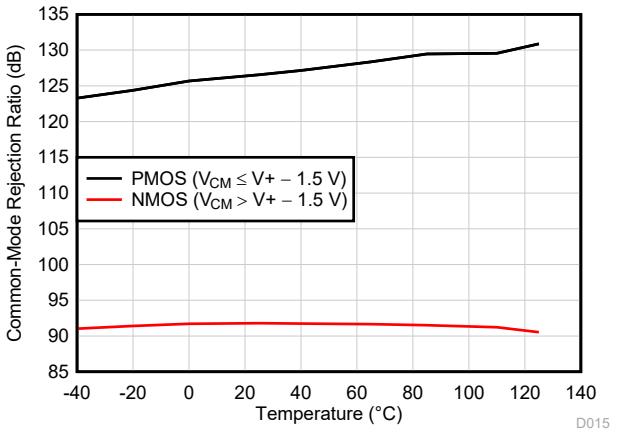
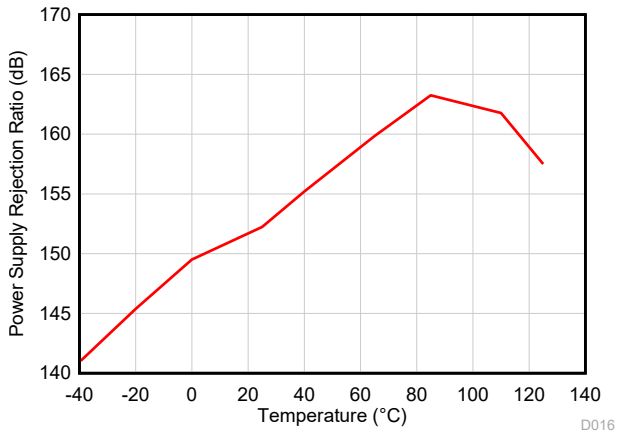


Figure 5-16. CMRR and PSRR vs Frequency



f = 0 Hz

Figure 5-17. CMRR vs Temperature (dB)



f = 0 Hz

Figure 5-18. PSRR vs Temperature (dB)

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5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)

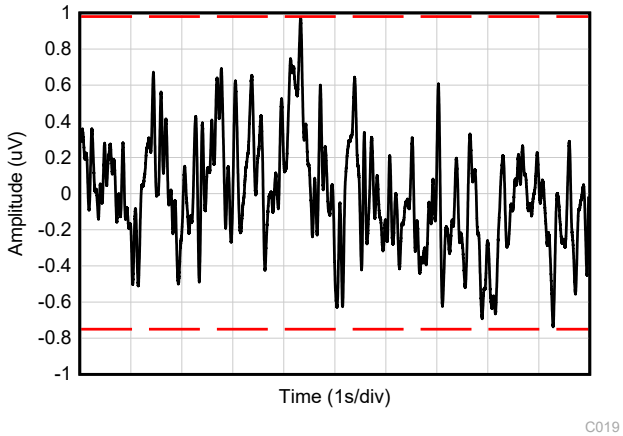


Figure 5-19. 0.1-Hz to 10-Hz Noise

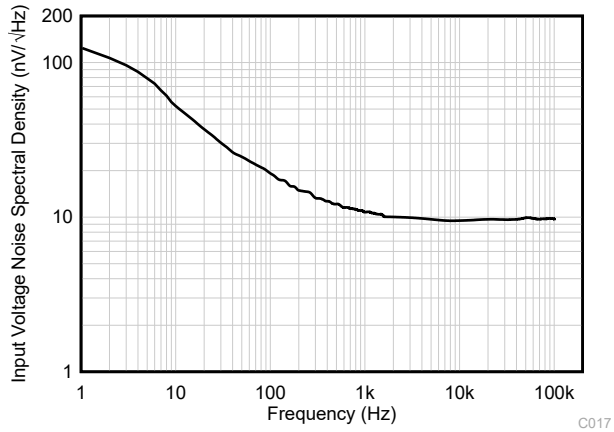
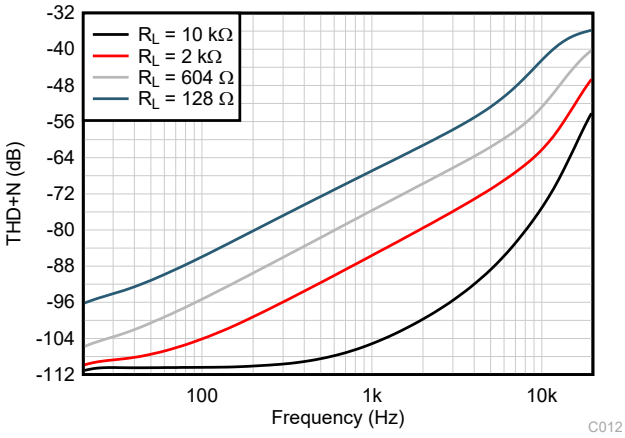
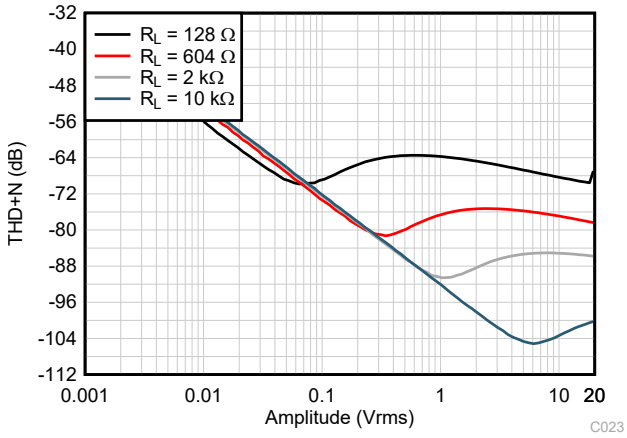


Figure 5-20. Input Voltage Noise Spectral Density vs Frequency



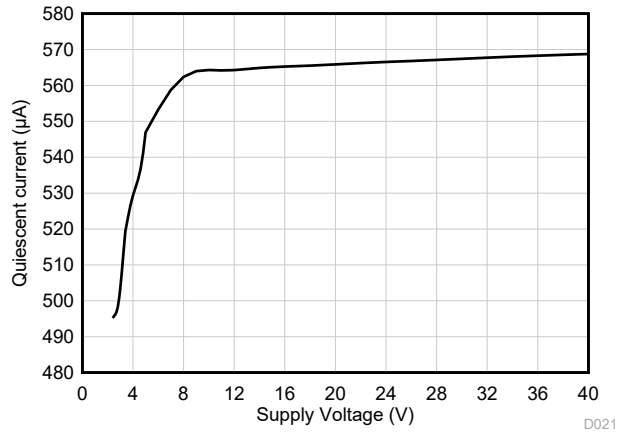
BW = 80 kHz, V_{OUT} = 1 V_{RMS}

Figure 5-21. THD+N Ratio vs Frequency



BW = 80 kHz, f = 1 kHz

Figure 5-22. THD+N vs Output Amplitude



V_{CM} = V–

Figure 5-23. Quiescent Current vs Supply Voltage

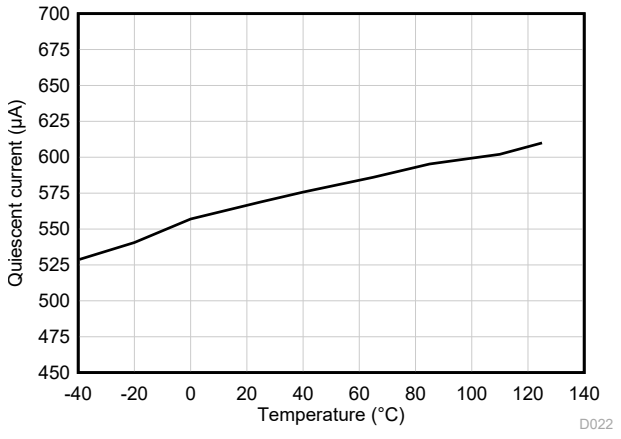


Figure 5-24. Quiescent Current vs Temperature

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5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)

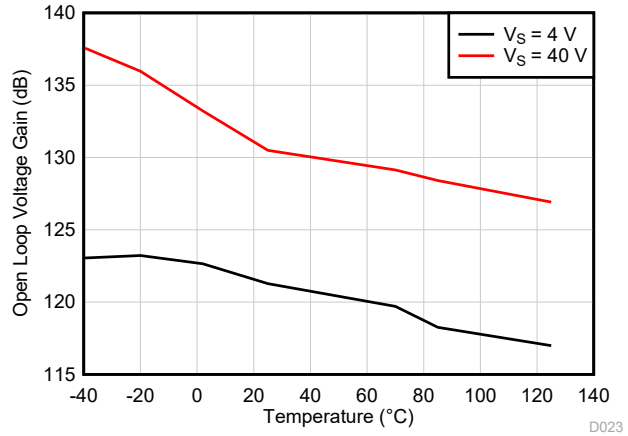


Figure 5-25. Open-Loop Voltage Gain vs Temperature (dB)

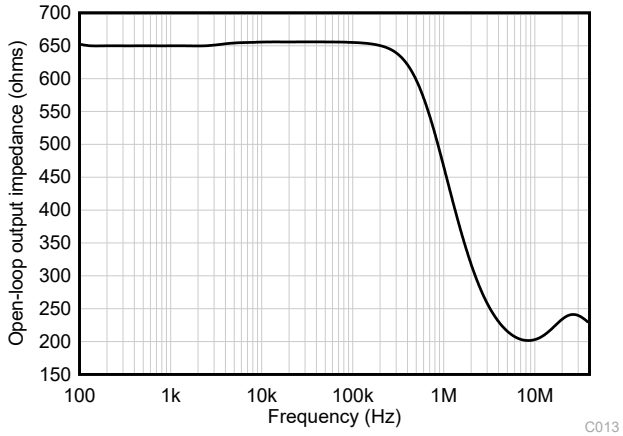
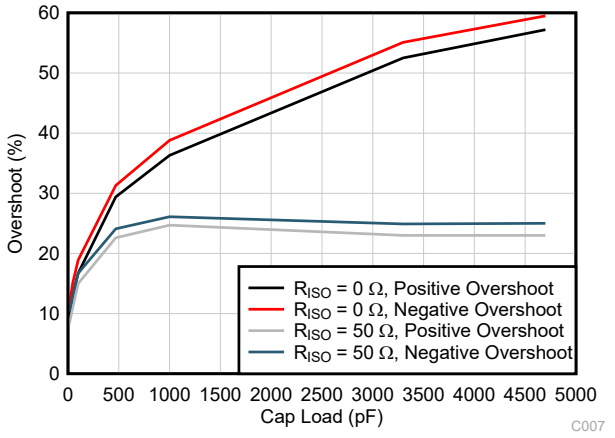
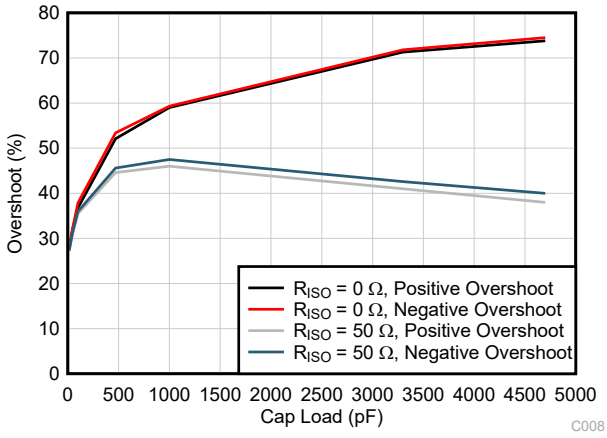


Figure 5-26. Open-Loop Output Impedance vs Frequency



G = –1, 10-mV output step

Figure 5-27. Small-Signal Overshoot vs Capacitive Load



G = 1, 10-mV output step

Figure 5-28. Small-Signal Overshoot vs Capacitive Load

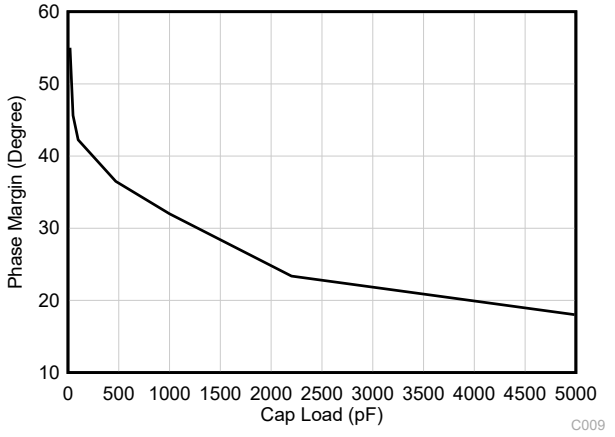
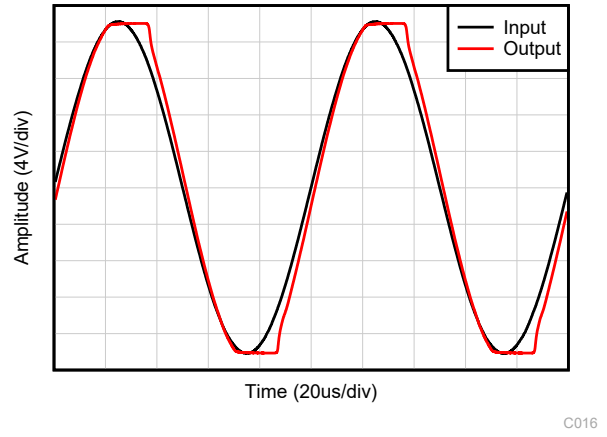


Figure 5-29. Phase Margin vs Capacitive Load



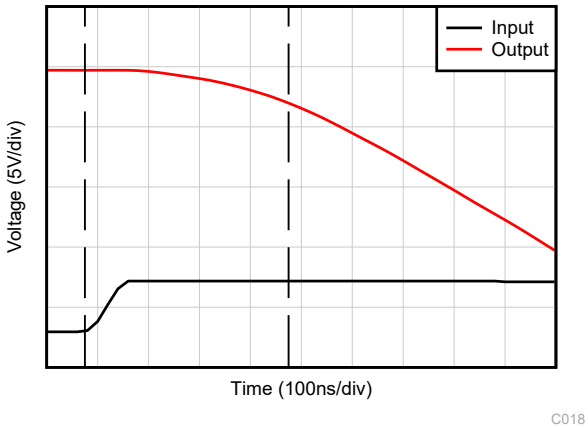
V_{IN} = ±20 V; V_S = V_{OUT} = ±17 V

Figure 5-30. No Phase Reversal

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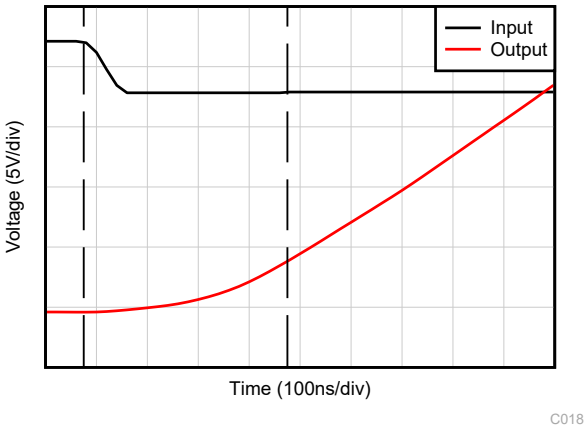
5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)



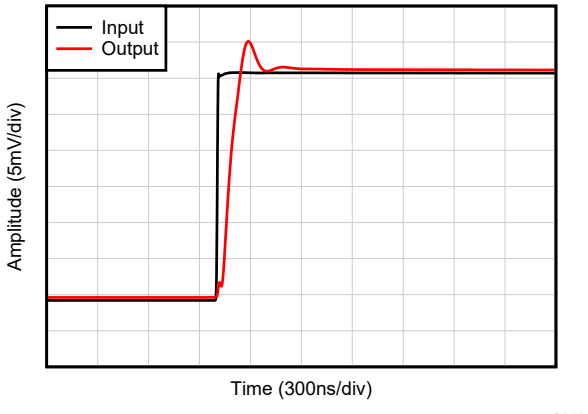
G = –10

Figure 5-31. Positive Overload Recovery



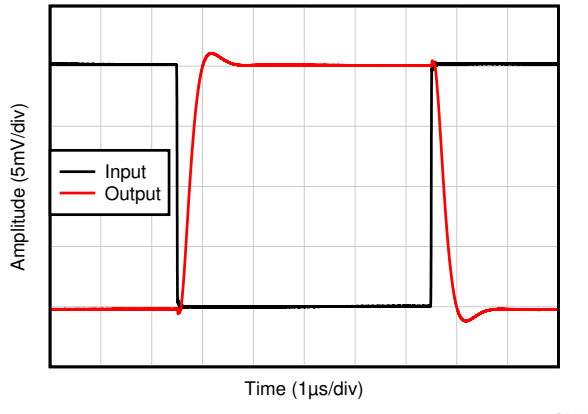
G = –10

Figure 5-32. Negative Overload Recovery



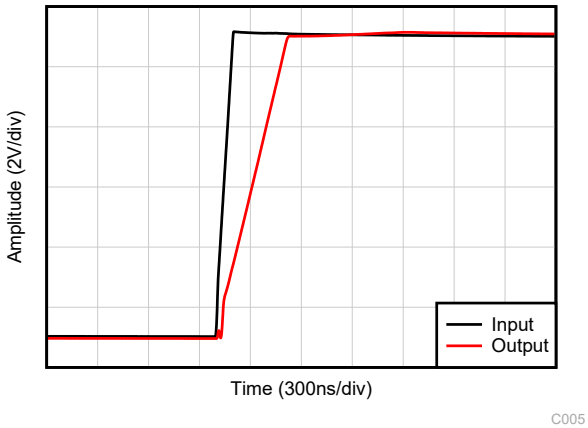
C_L = 20 pF, G = 1, 20-mV step response

Figure 5-33. Small-Signal Step Response, Rising



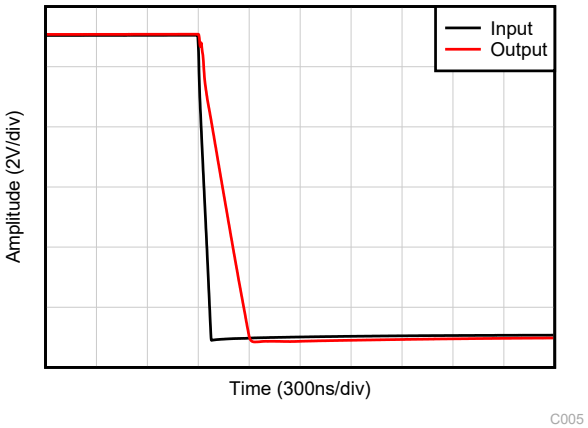
C_L = 20 pF, G = –1, 20-mV step response

Figure 5-34. Small-Signal Step Response



C_L = 20 pF, G = 1

Figure 5-35. Large-Signal Step Response (Rising)



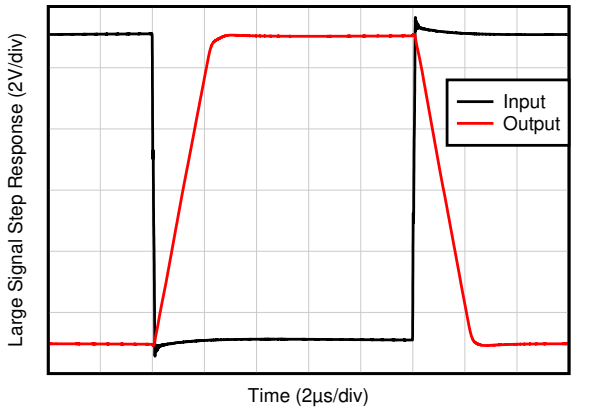
C_L = 20 pF, G = 1

Figure 5-36. Large-Signal Step Response (Falling)

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5.8 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±20 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 10 pF (unless otherwise noted)



C_L = 20 pF, G = –1

Figure 5-37. Large-Signal Step Response

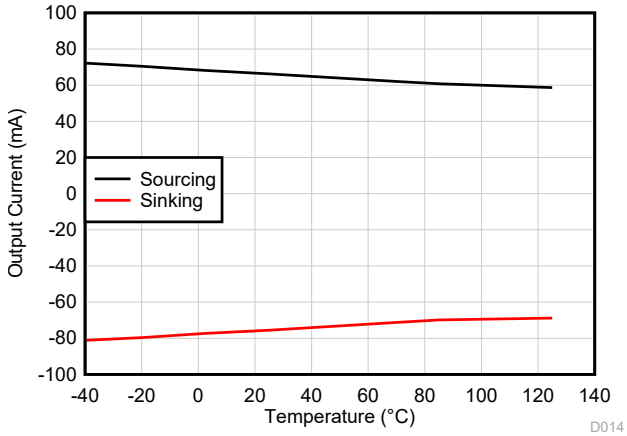


Figure 5-38. Short-Circuit Current vs Temperature

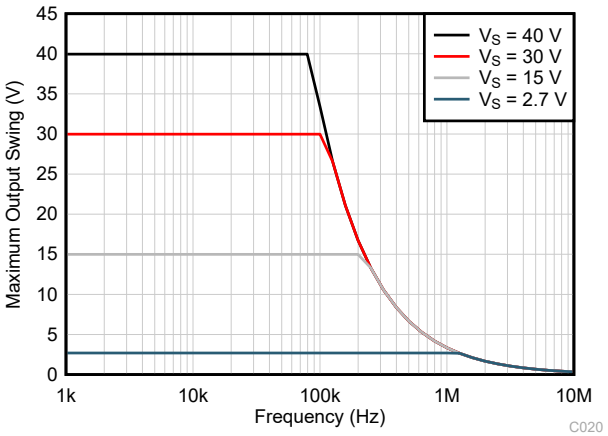


Figure 5-39. Maximum Output Voltage vs Frequency

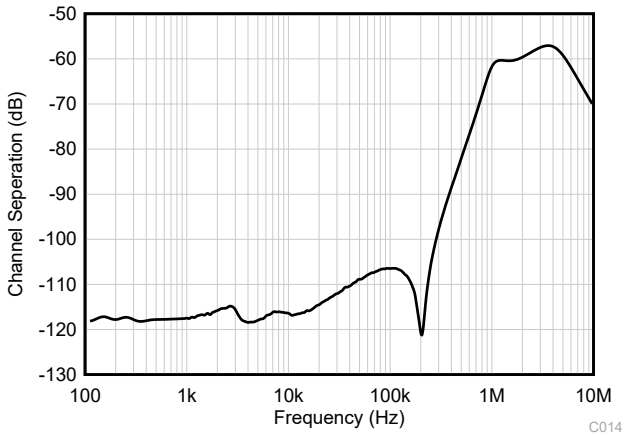


Figure 5-40. Channel Separation vs Frequency

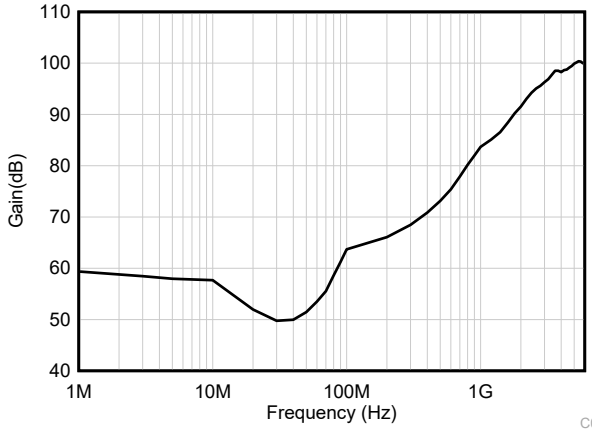


Figure 5-41. EMIRR (Electromagnetic Interference Rejection Ratio) at Inputs vs Frequency

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6 Detailed Description

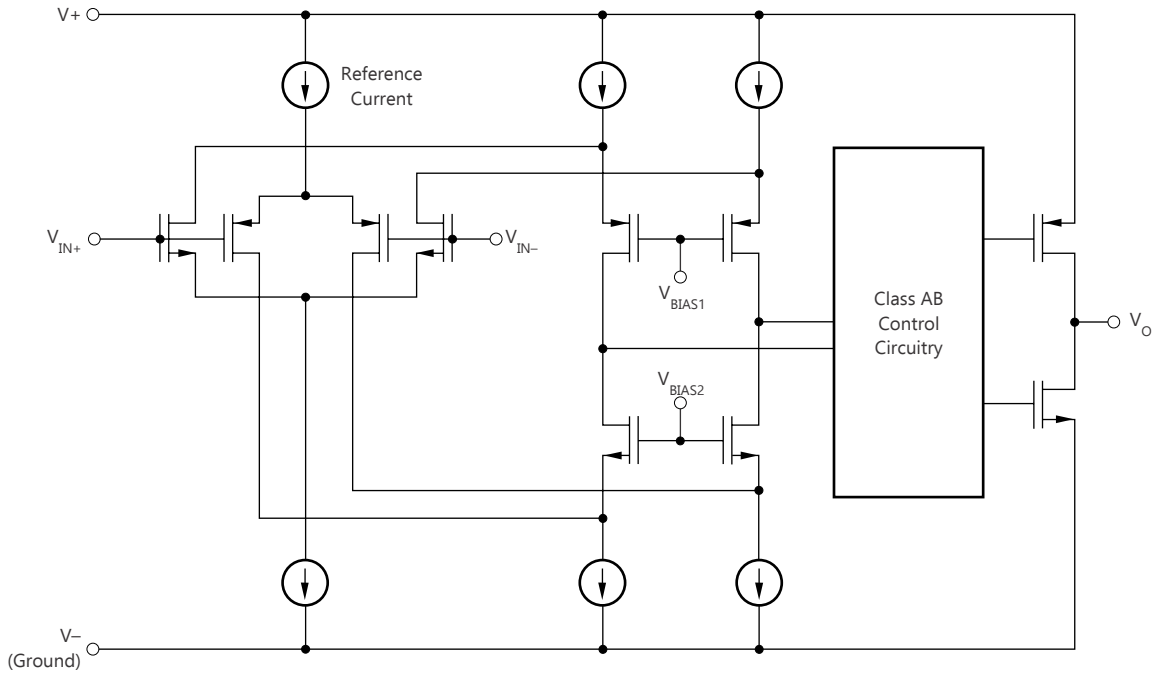
6.1 Overview

The TLV935x-Q1 family (TLV9351-Q1, TLV9352-Q1, and TLV9354-Q1) is a family of 40-V, cost-optimized automotive operational amplifiers. These devices offer strong general-purpose DC and AC specifications, including rail-to-rail output, low offset (±350 µV, typ), low offset drift (±1.5 µV/°C, typ), and 3.5-MHz bandwidth.

Convenient features such as wide differential input-voltage range, high output current (±60 mA), and high slew rate (20 V/µs) make the TLV935x-Q1 a robust operational amplifier for high-voltage, cost-sensitive applications.

The TLV935x-Q1 family of op amps is available in standard packages and is specified from –40°C to 125°C.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Input Protection Circuitry

The TLV935x-Q1 uses a patented input architecture to eliminate the requirement for input protection diodes but still provides robust input protection under transient conditions. Figure 6-1 shows conventional input diode protection schemes that are activated by fast transient step responses and introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 6-2. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current and resulting in extended settling time.

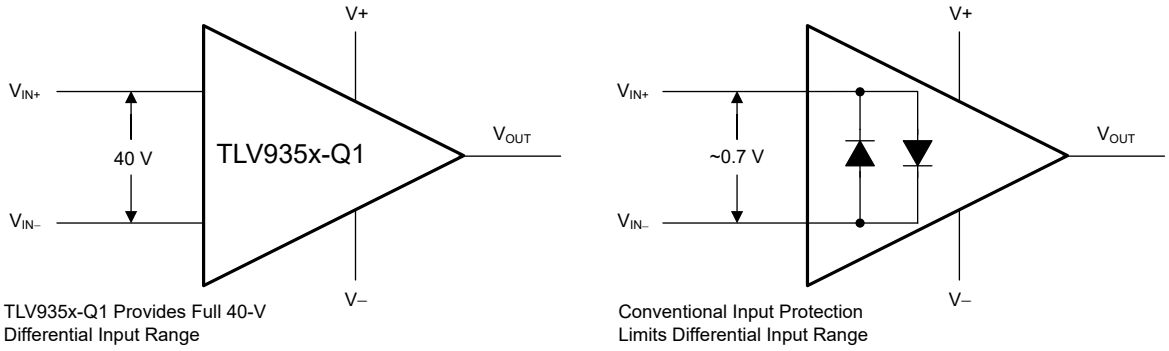


Figure 6-1. TLV935x-Q1 Input Protection Does Not Limit Differential Input Capability

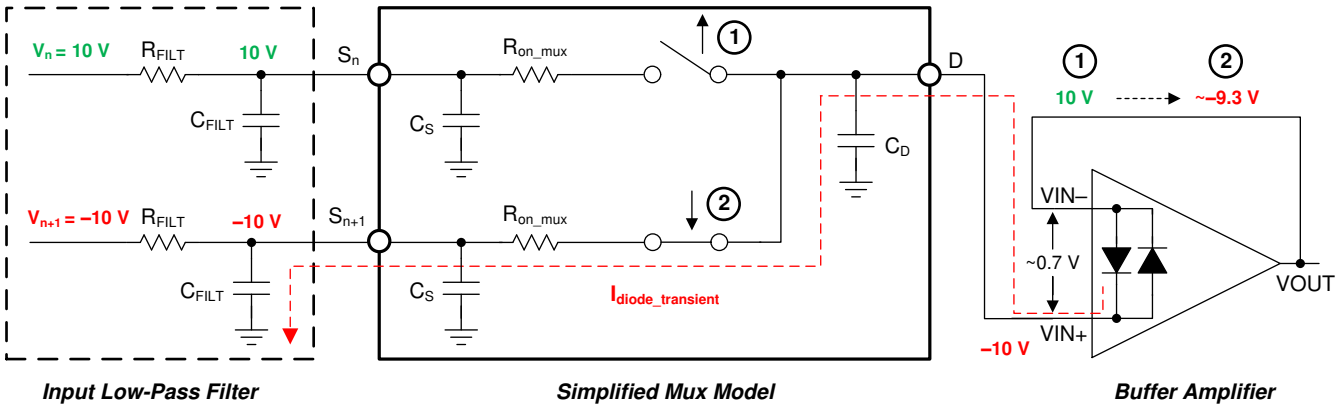


Figure 6-2. Back-to-Back Diodes Create Settling Issues

The TLV935x-Q1 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications. This patented input protection architecture does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The TLV935x-Q1 tolerates a maximum differential swing (voltage between inverting and noninverting pins of the op amp) of up to 40 V, making the device suitable for use as a comparator or in applications with fast-ramping input signals.

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6.3.2 EMI Rejection

The TLV935x-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV935x-Q1 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 6-3 shows the results of this testing on the TLV935x-Q1. Table 6-1 provides the EMIRR IN+ values for the TLV935x-Q1 at particular frequencies commonly encountered in real-world applications. Table 6-1 lists applications that may be centered on or operated near the particular frequency shown. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

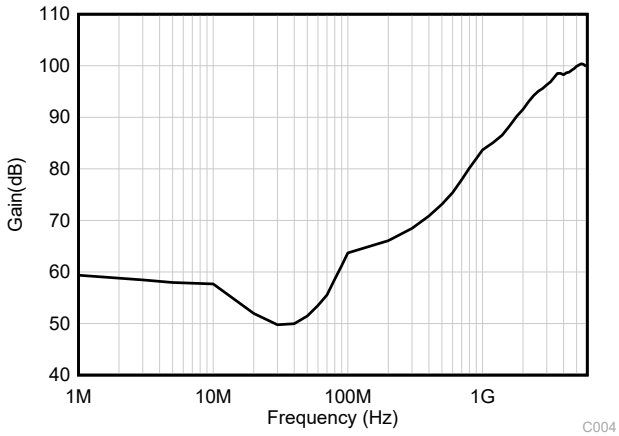


Figure 6-3. EMIRR Testing

Table 6-1. TLV935x-Q1 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	71 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	80 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	87 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	90 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	92 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	94 dB

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6.3.3 Phase Reversal Protection

The TLV935x-Q1 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The TLV935x-Q1 is a rail-to-rail input op amp; therefore, the common-mode range can extend up to the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail.

6.3.4 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the TLV935x-Q1 is 150°C. Exceeding this temperature causes damage to the device. The TLV935x-Q1 has a thermal protection feature that prevents damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 140°C. Figure 6-4 shows an application example for the TLV9351-Q1 that has significant self heating (159°C) because of its power dissipation (0.81 W). Thermal calculations indicate that for an ambient temperature of 65°C the device junction temperature will reach 187°C. The actual device, however, turns off the output drive to maintain a safe junction temperature. Figure 6-4 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3 V. When self heating causes the device junction temperature to increase above 140°C, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor RL.

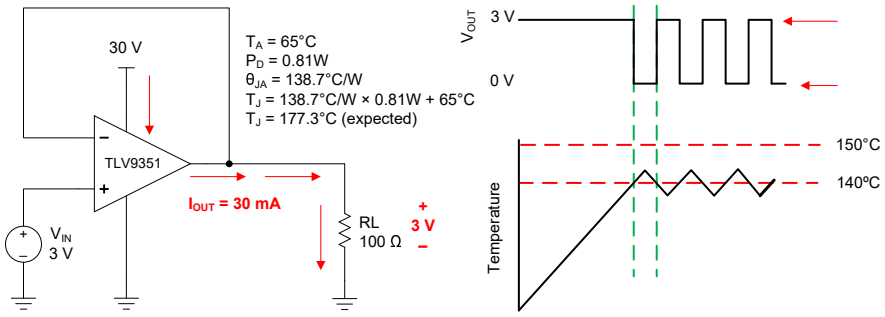


Figure 6-4. Thermal Protection

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6.3.5 Capacitive Load and Stability

The TLV935x-Q1 features a resistive output stage capable of driving smaller capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive large capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see Figure 6-5 and Figure 6-6. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation.

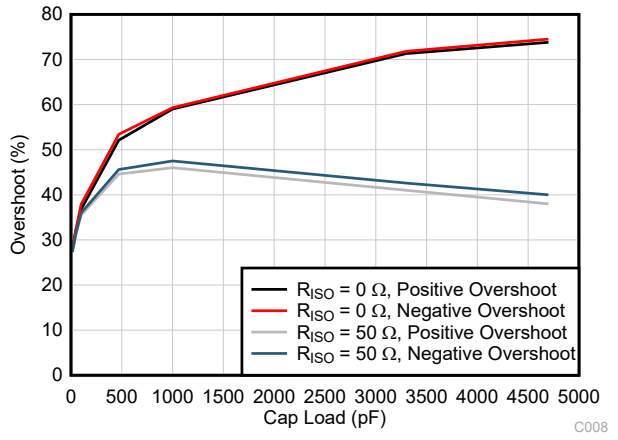


Figure 6-5. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step, G = 1)

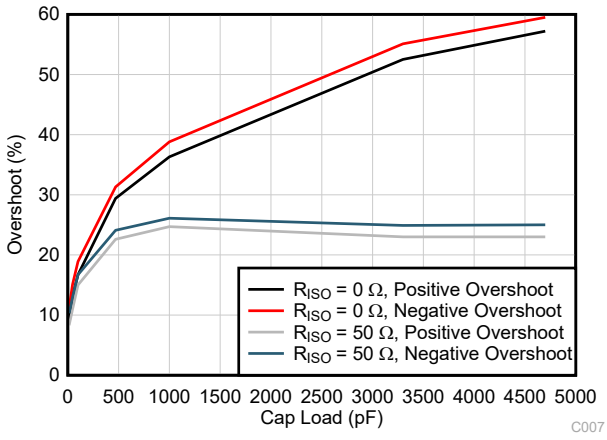


Figure 6-6. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step, G = –1)

For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small (10 Ω to 20 Ω) resistor, R_{ISO}, in series with the output, as shown in Figure 6-7. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio R_{ISO} / R_L, and is generally negligible at low output levels. A high capacitive load drive makes the TLV935x-Q1 well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in Figure 6-7 uses an isolation resistor, R_{ISO}, to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system for increased phase margin. For additional information on techniques to optimize and design using this circuit, TI Precision Design TIDU032 details complete design goals, simulation, and test results.

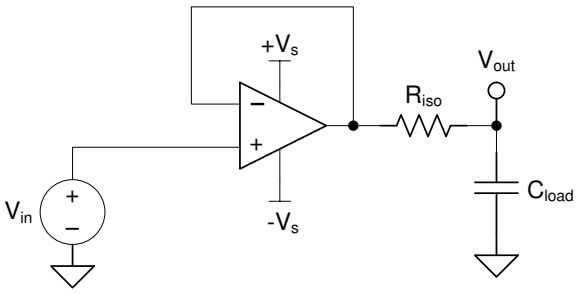


Figure 6-7. Extending Capacitive Load Drive With the TLV9351-Q1

6.3.6 Common-Mode Voltage Range

The TLV935x-Q1 is a 40-V, rail-to-rail output operational amplifier with an input common-mode range that extends 100 mV beyond V– and within 2 V of V+ for normal operation. The device accomplishes this performance through a complementary input stage, using a P-channel differential pair. Additionally, a complementary N-channel differential pair has been included in parallel with the P-channel pair to eliminate common undesirable op amp behaviors, such as phase reversal.

The TLV935x-Q1 can operate with common mode ranges beyond 100 mV of the top rail, but with reduced performance above (V+) – 2 V. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1 V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 2 V. There is a small transition region, typically (V+) –2 V to (V+) – 1 V in which both input pairs are on. This transition region can vary modestly with process variation, and within the transition region and N-channel region, many specifications of the op amp, including PSRR, CMRR, offset voltage, offset drift, noise and THD performance may be degraded compared to operation within the P-channel region.

Table 6-2. Typical Performance for Common-Mode Voltages Within 2 V of the Positive Supply

PARAMETER	MIN	TYP	MAX	UNIT
Input common-mode voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		1.5		mV
Offset voltage drift		2		µV/°C
Common-mode rejection		75		dB
Open-loop gain		75		dB
Gain-bandwidth product		1.5		MHz

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6.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 6-8 shows an illustration of the ESD circuits contained in the TLV935x-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

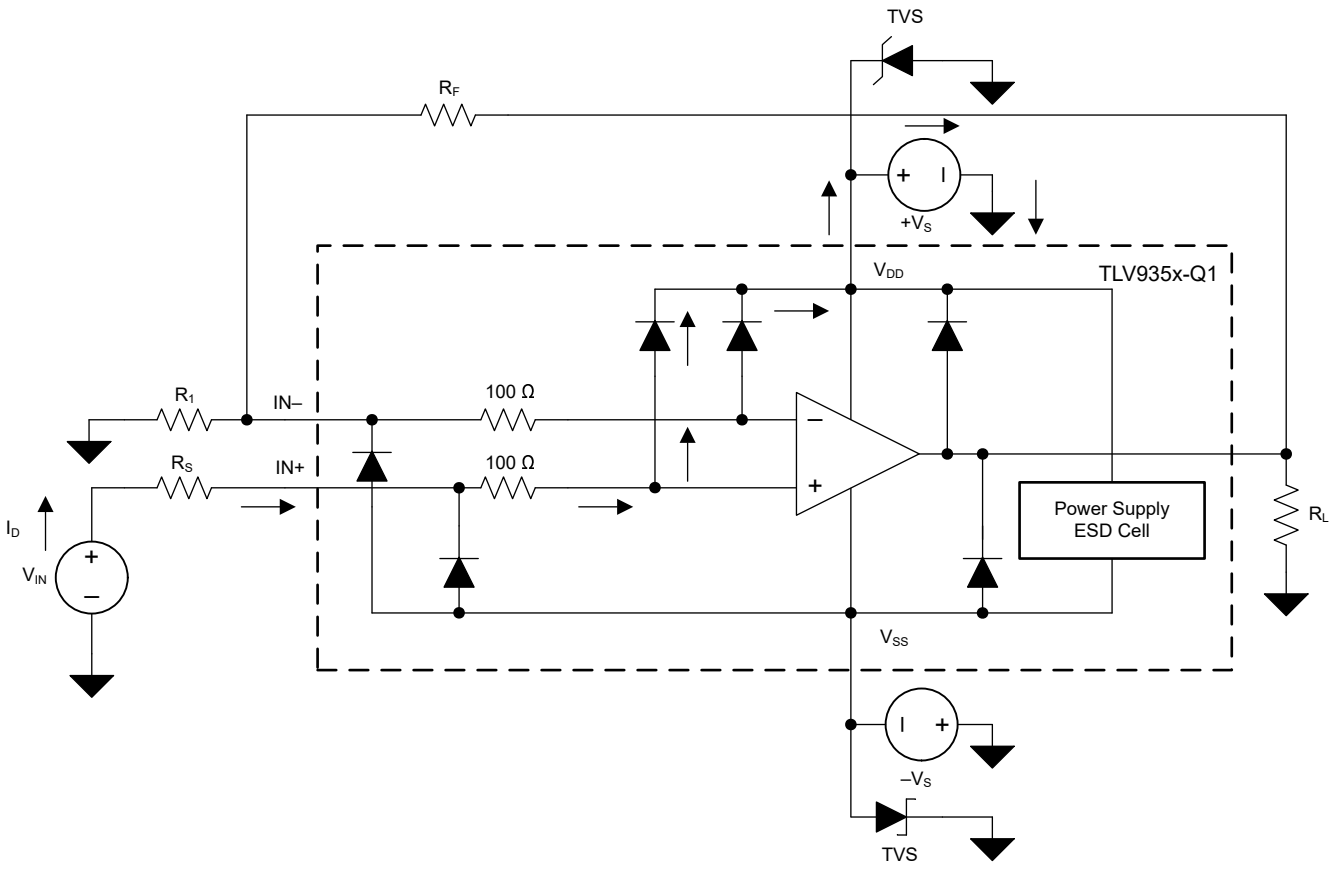


Figure 6-8. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event is very short in duration and very high voltage (for example, 1 kV, 100 ns), whereas an EOS event is long duration and lower voltage (for example, 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

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6.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV935x-Q1 is approximately 600 ns.

6.3.9 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier will exhibit some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian* (*bell curve*), or *normal* distributions, and circuit designers can leverage this information to guardband their system, even when there is not a minimum or maximum specification in Section 5.7.

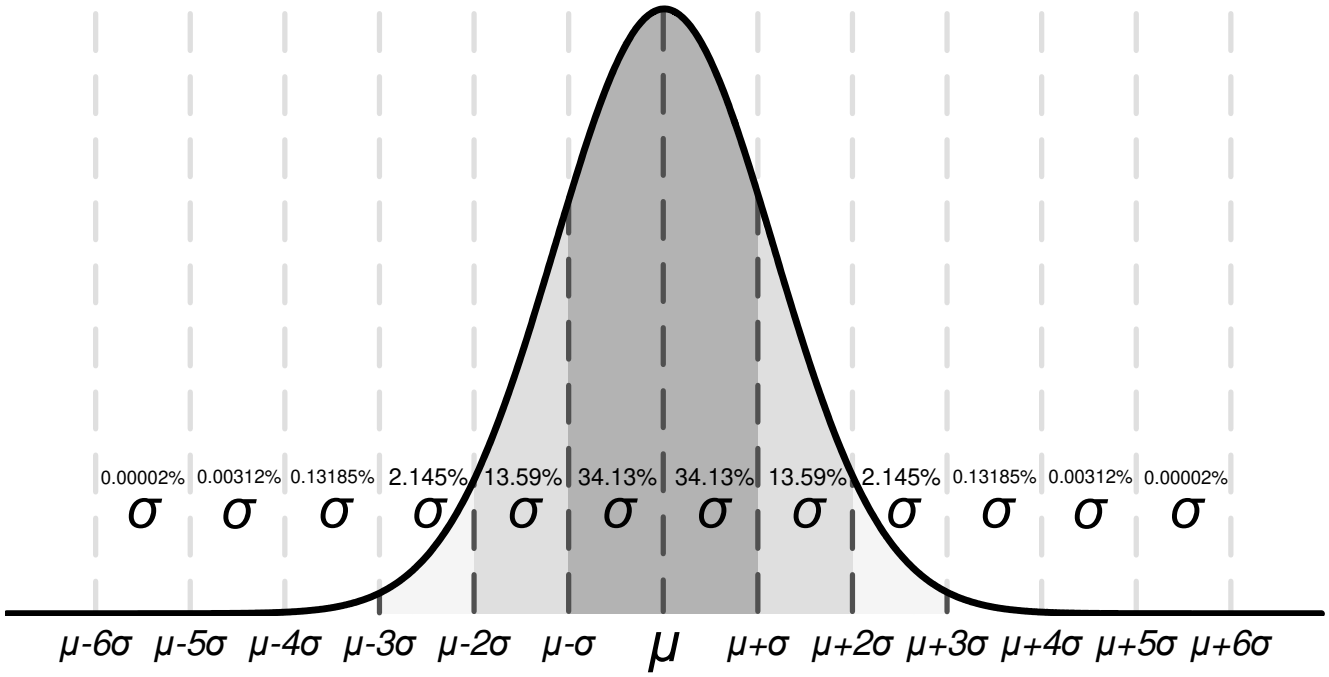


Figure 6-9. Ideal Gaussian Distribution

Figure 6-9 shows an example distribution, where μ, or *mu*, is the mean of the distribution, and where σ, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu - \sigma$ to $\mu + \sigma$).

Depending on the specification, values listed in the *typical* column of Section 5.7 are represented in different ways. As a general rule, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation (μ + σ) to most accurately represent the typical value.

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This chart can be used to calculate approximate probability of a specification in a unit; for example, for TLV935x-Q1, the typical input voltage offset is 350 µV, so 68.2% of all TLV935x-Q1 devices are expected to have an offset from –350 µV to 350 µV. At 4 σ (±1400 µV), 99.9937% of the distribution has an offset voltage less than ±1400 µV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are assured by TI, and units outside these limits will be removed from production material. For example, the TLV935x-Q1 family has a maximum offset voltage of 1.8 mV at 125°C, and even though this corresponds to about 5 σ (≈1 in 1.7 million units), which is extremely unlikely, TI assures that any unit with larger offset than 1.8 mV will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guardband for the application, and design worst-case conditions using this value. For example, the 6-σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and could be an option as a wide guardband to design a system around. In this case, the TLV935x-Q1 family does not have a maximum or minimum for offset voltage drift, but based on the typical value of 1.5 µV/°C in Section 5.7, it can be calculated that the 6-σ value for offset voltage drift is about 9 µV/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should be used only to estimate the performance of a device.

6.4 Device Functional Modes

The TLV935x-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the TLV935x-Q1 is 40 V (±20 V).

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7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TLV935x-Q1 family offers excellent DC precision and DC performance. These devices operate up to 40-V supply rails and offer true rail-to-rail output, low offset voltage and offset voltage drift, as well as 3.5-MHz bandwidth and high output drive. These features make the TLV935x-Q1 a robust, high-performance operational amplifier for high-voltage cost-sensitive applications.

7.2 Typical Applications

7.2.1 High Voltage Precision Comparator

Many different systems require controlled voltages across numerous system nodes for robust operation. A comparator can be used to monitor and control voltages by comparing a reference threshold voltage with an input voltage and providing an output when the input crosses this threshold.

The TLV935x-Q1 family of op amps make excellent high voltage comparators due to their MUX-friendly input stage (for more information, see Section 6.3.1). Previous generation high-voltage op amps often use back-to-back diodes across the inputs to prevent damage to the op amp which greatly limits these op amps to be used as comparators, but the TLV935x-Q1's patented input stage allows the device to have a wide differential voltage between the inputs.

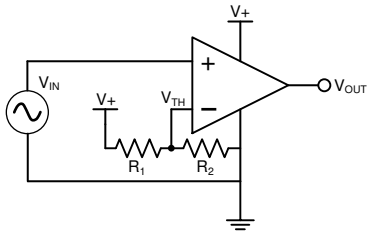


Figure 7-1. Typical Comparator Application

7.2.1.1 Design Requirements

The primary objective is to design a 40-V precision comparator.

- System supply voltage (V+): 40 V
- Resistor 1 value: 100 kΩ
- Resistor 2 value: 100 kΩ
- Reference threshold voltage (V_{TH}): 20 V
- Input voltage range (V_{IN}): 0 V – 40 V
- Output voltage range (V_{OUT}): 0 V – 40 V

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7.2.1.2 Detailed Design Procedure

This noninverting comparator circuit applies the input voltage (V_{IN}) to the noninverting terminal of the op amp. Two resistors (R_1 and R_2) divide the supply voltage (V+) to create a mid-supply threshold voltage (V_{TH}) as calculated in Equation 1. The circuit is shown in Figure 7-1. When V_{IN} is less then V_{TH}, the output voltage transitions to the negative supply and equals the low-level output voltage. When V_{IN} is greater than V_{TH}, the output voltage transitions to the positive supply and equals the high-level output voltage.

In this example, resistor 1 and 2 have been selected to be 100 kΩ, which sets the reference threshold at 20 V. However, resistor 1 and 2 can be adjusted to modify the threshold using Equation 1. Resistor 1 and 2's values have also been selected to reduce power consumption, but these values can be further increased to reduce power consumption, or reduced to improve noise performance.

$$V_{TH} = \frac{R_2}{R_1 + R_2} \times V_+ \quad (1)$$

7.2.1.3 Application Curve

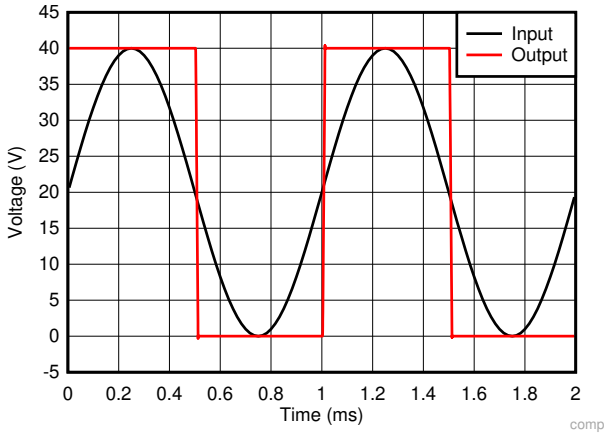


Figure 7-2. Comparator Output Response to Input Voltage

7.3 Power Supply Recommendations

The TLV935x-Q1 is specified for operation from 4.5 V to 40 V (±2.25 V to ±20 V); many specifications apply from –40°C to 125°C.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see Section 5.1.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to Section 7.4.

7.4 Layout

7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.

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  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 7-4, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

7.4.2 Layout Example

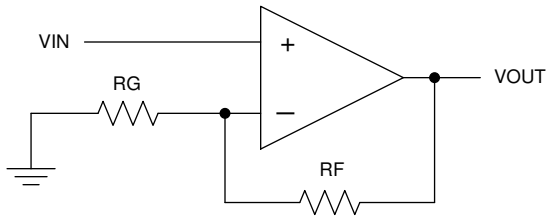


Figure 7-3. Schematic Representation

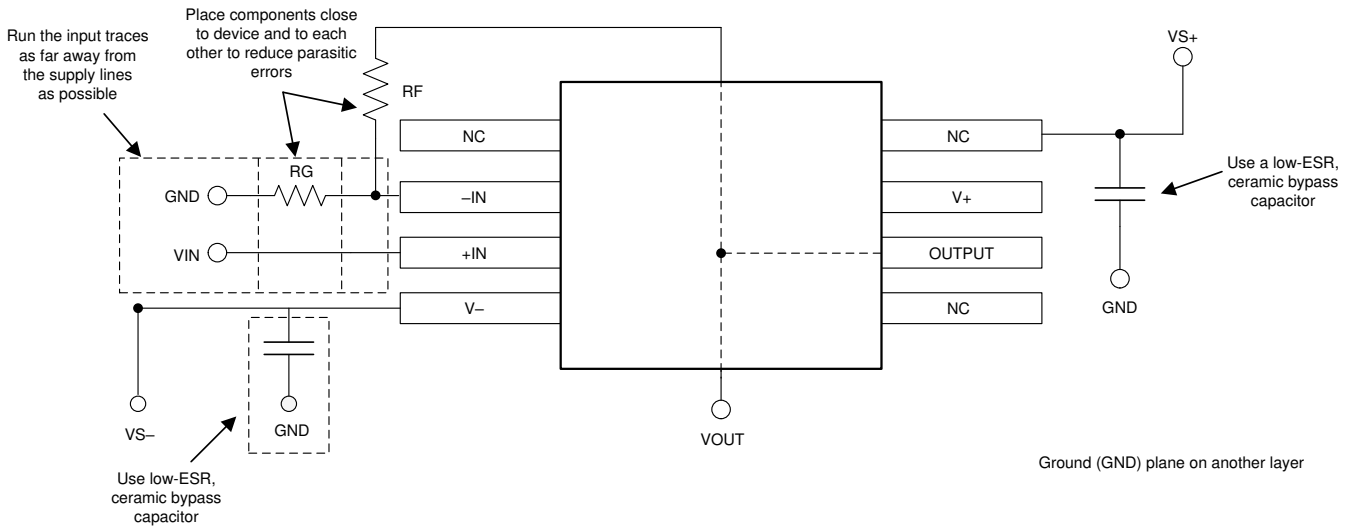


Figure 7-4. Operational Amplifier Board Layout for Noninverting Configuration

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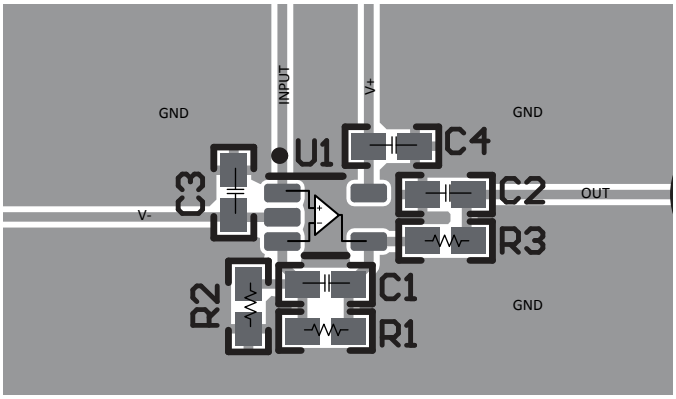


Figure 7-5. Example Layout for SC70 (DCK) Package

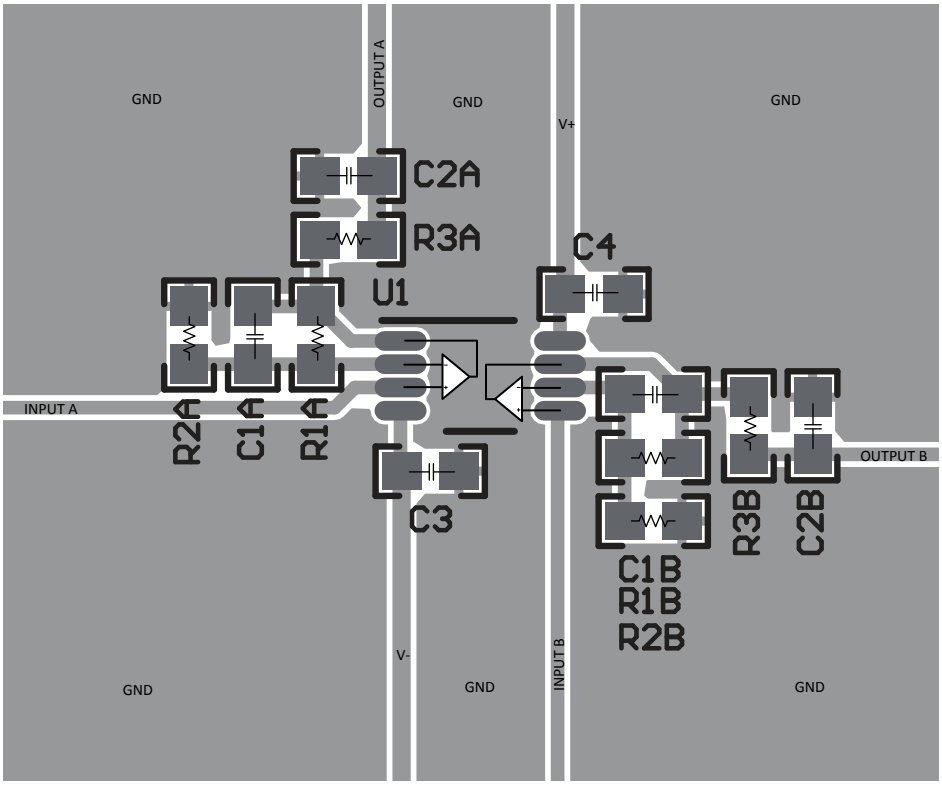


Figure 7-6. Example Layout for VSSOP-8 (DGK) Package

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

8.1.1.2 TI Precision Designs

The TLV935x-Q1 is featured in several TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application note
- Texas Instruments, *Capacitive Load Drive Solution using an Isolation Resistor* reference guide
- Texas Instruments, *Analog Engineer's Circuit Cookbook: Amplifiers* e-book
- Texas Instruments, *AN31 amplifier circuit collection* application note

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (June 2023) to Revision E (March 2024)	Page
• Added the 5-pin SC70 (DCK) package throughout data sheet	1
• Added pinout configuration for 5-pin SC70 (DCK) package to *Pin Configuration and Functions* section	3

Changes from Revision C (September 2021) to Revision D (June 2023)	Page
• Add the 8-pin TSSOP (PW) package throughout data sheet	1

Changes from Revision B (May 2021) to Revision C (September 2021)	Page
• Deleted preview note from SOIC (14) package throughout data sheet.	1
• Deleted preview note from SOT-23 (14) package throughout data sheet.	1
• Deleted preview note from SOIC (8) package throughout data sheet.	1
• Deleted preview note from SOT-23 (5) package throughout data sheet.	1

Changes from Revision A (March 2021) to Revision B (May 2021)	Page
• Deleted preview note from TSSOP (14) package throughout data sheet.	1
• Deleted preview note from PW package in Thermal Information for Quad Channel table	7

Changes from Revision * (January 2021) to Revision A (March 2021)	Page
• Changed device status from *Advance Information* to *Production Data*	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV9351QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2JMF
TLV9351QDBVRQ1.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2JMF
TLV9351QDCKRQ1	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MU
TLV9351QDCKRQ1.A	Active	Production	SC70 (DCK) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MU
TLV9352QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27ST
TLV9352QDGKRQ1.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27ST
TLV9352QDRQ1	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9352Q
TLV9352QDRQ1.A	Active	Production	SOIC (D) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9352Q
TLV9352QPWRQ1	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	TL9352
TLV9352QPWRQ1.A	Active	Production	TSSOP (PW) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9352
TLV9354QDRQ1	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9354QD
TLV9354QDRQ1.A	Active	Production	SOIC (D) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL9354QD
TLV9354QDYYRQ1	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9354Q
TLV9354QDYYRQ1.A	Active	Production	SOT-23-THIN (DYY) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV9354Q
TLV9354QPWRQ1	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	T9354Q
TLV9354QPWRQ1.A	Active	Production	TSSOP (PW) | 14	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9354Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV9351-Q1, TLV9352-Q1, TLV9354-Q1 :

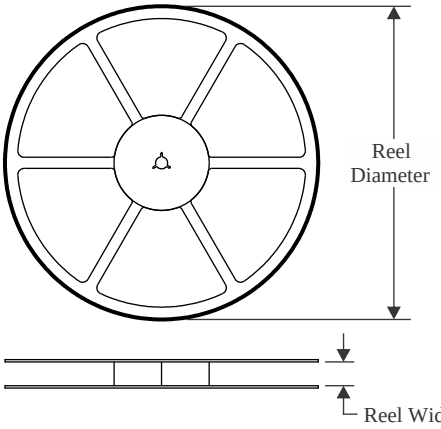
- Catalog : TLV9351, TLV9352, TLV9354

NOTE: Qualified Version Definitions:

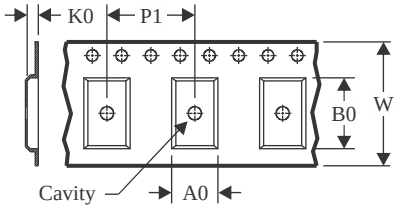
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

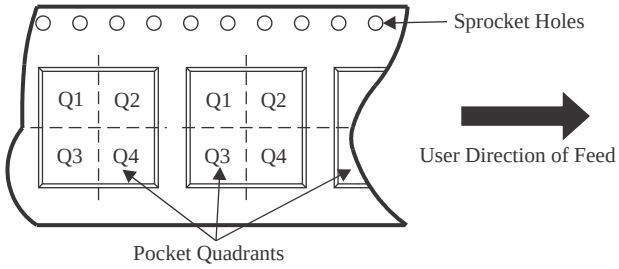


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

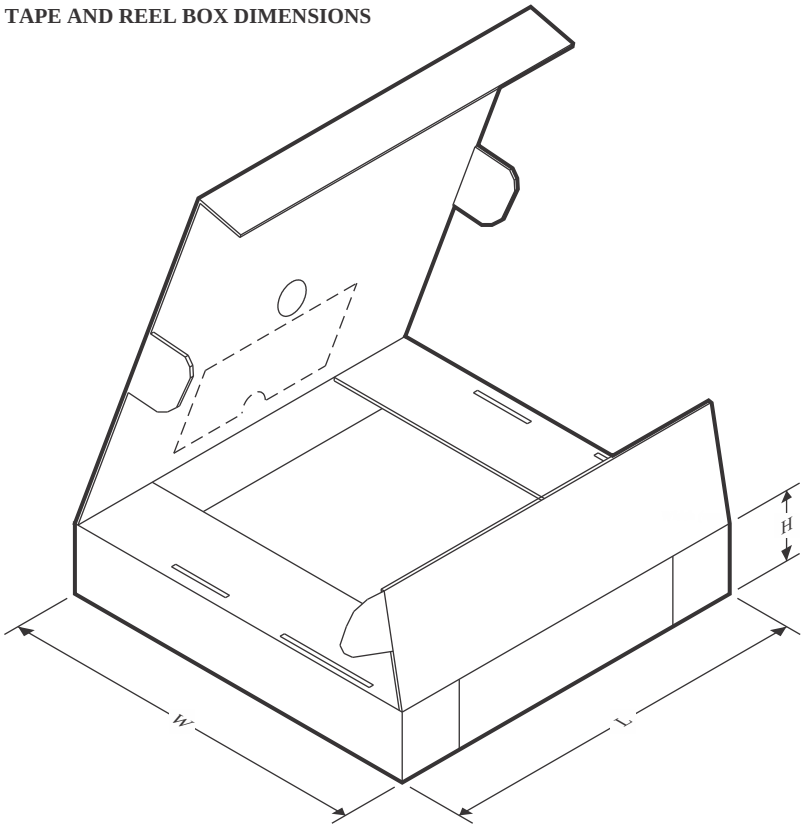
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

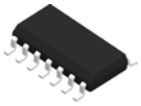
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9351QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9351QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9351QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV9352QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9352QDRQ1	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9352QPWRQ1	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9354QDRQ1	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV9354QDYYRQ1	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TLV9354QPWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV9354QPWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9351QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9351QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9351QDCKRQ1	SC70	DCK	5	3000	180.0	180.0	18.0
TLV9352QDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
TLV9352QDRQ1	SOIC	D	8	3000	353.0	353.0	32.0
TLV9352QPWRQ1	TSSOP	PW	8	3000	353.0	353.0	32.0
TLV9354QDRQ1	SOIC	D	14	3000	353.0	353.0	32.0
TLV9354QDYYRQ1	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TLV9354QPWRQ1	TSSOP	PW	14	3000	356.0	356.0	35.0
TLV9354QPWRQ1	TSSOP	PW	14	3000	353.0	353.0	32.0

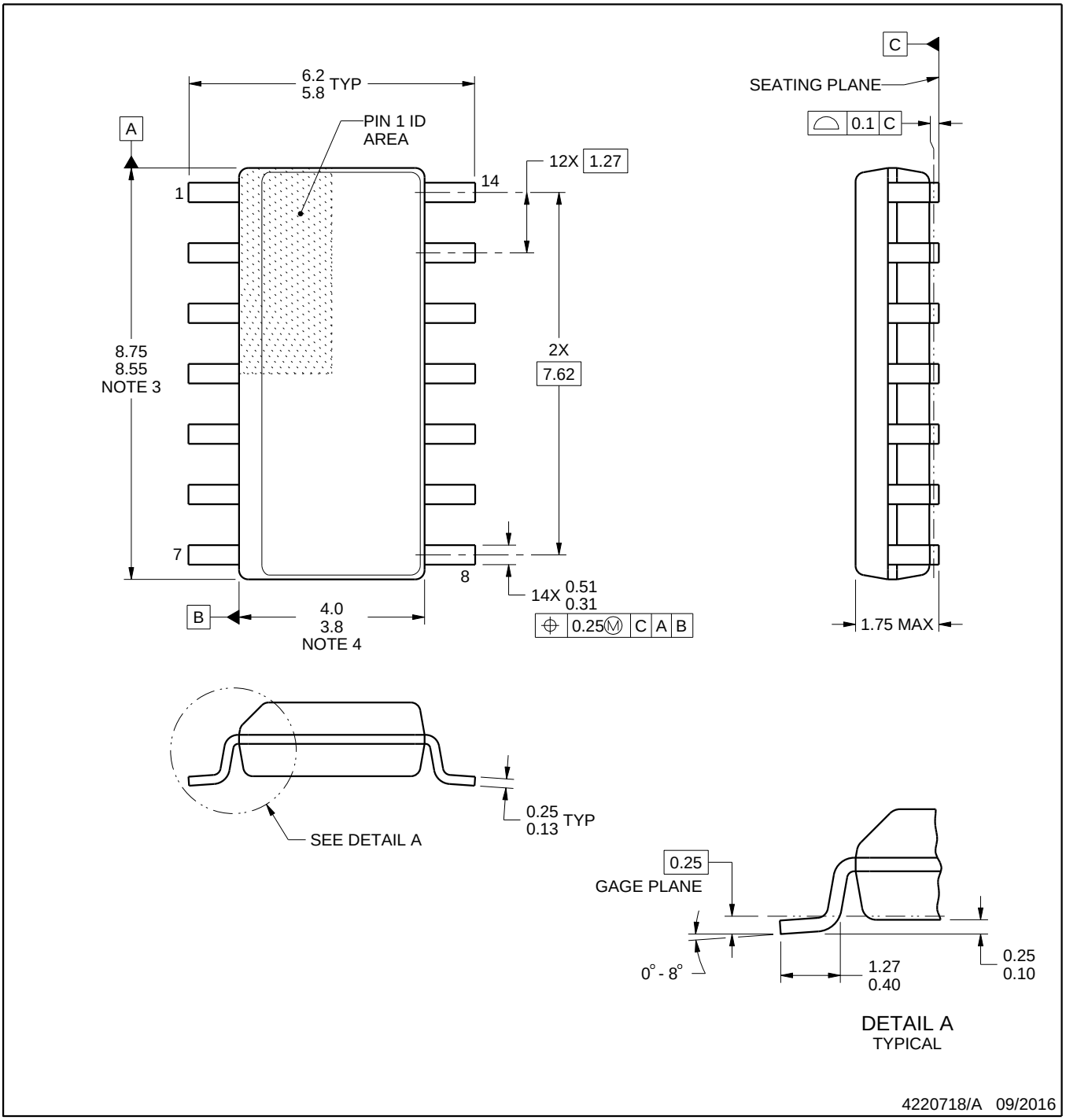


PACKAGE OUTLINE

D0014A

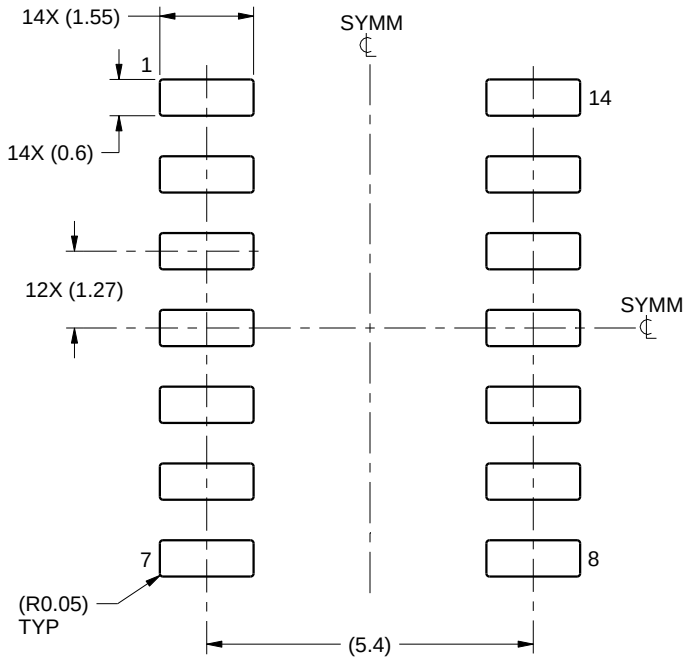
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

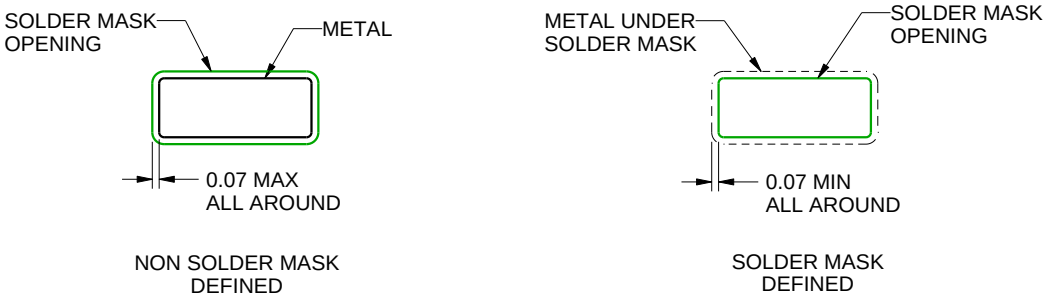


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

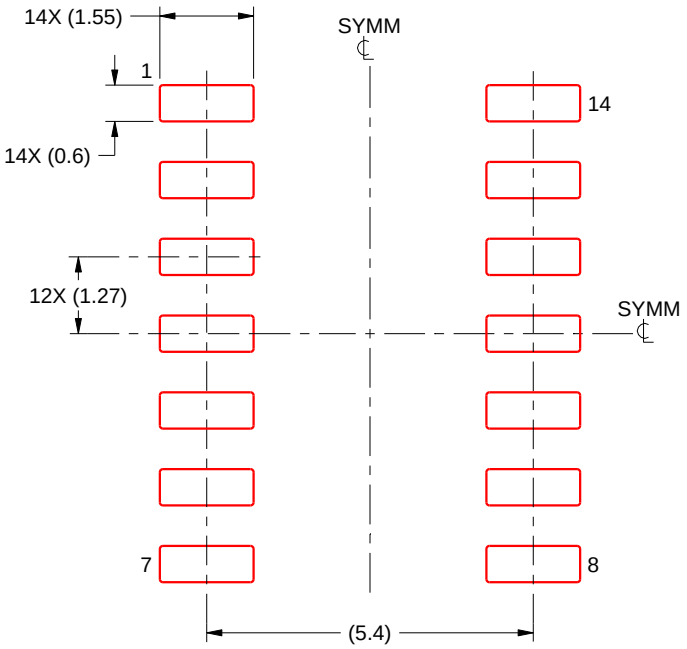
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

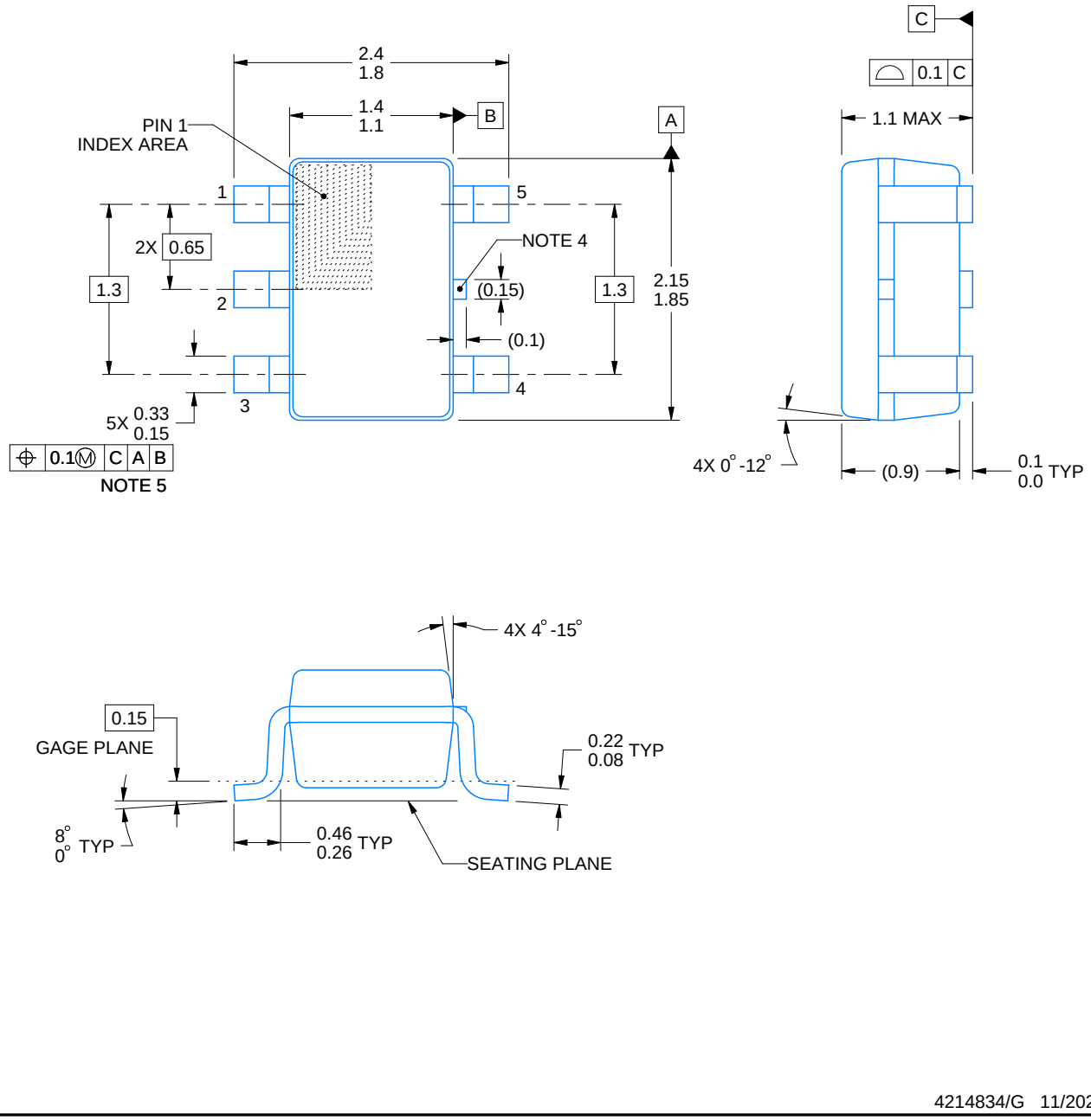
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

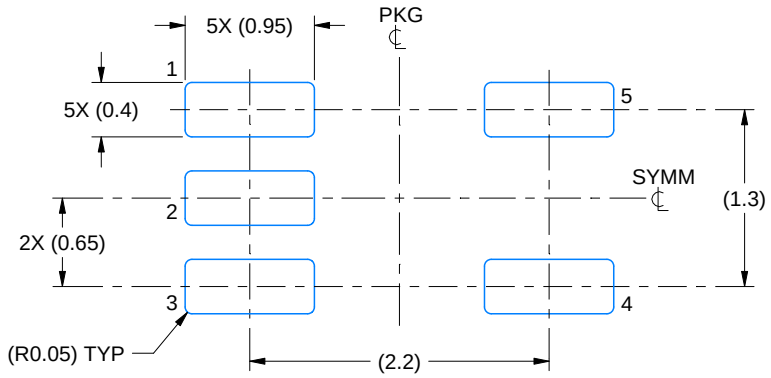
SMALL OUTLINE TRANSISTOR



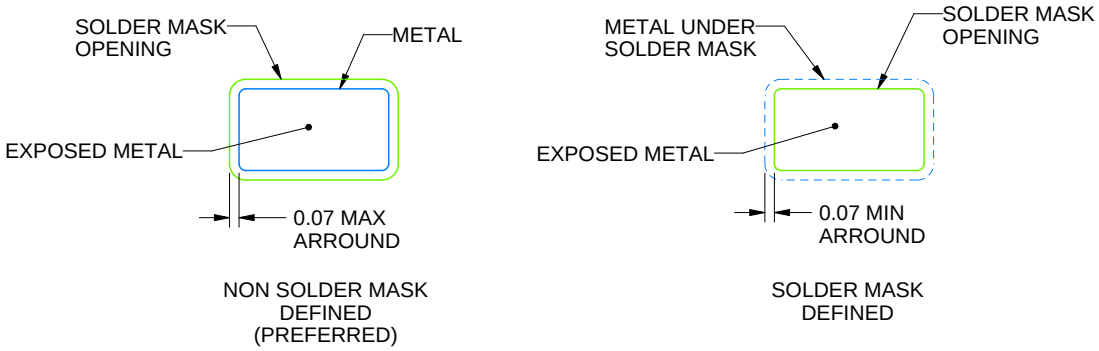
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

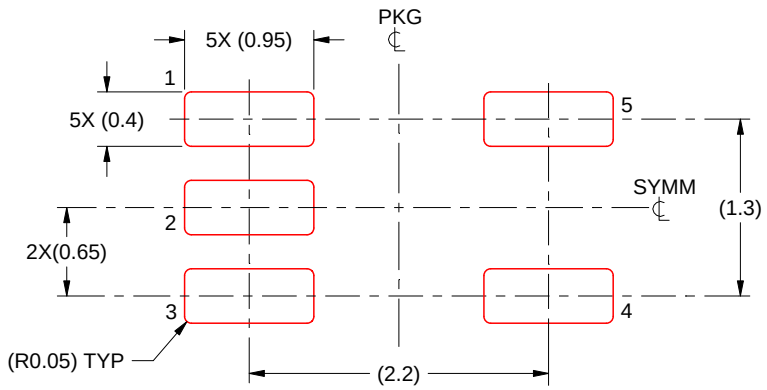


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

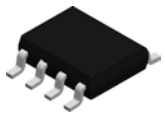


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

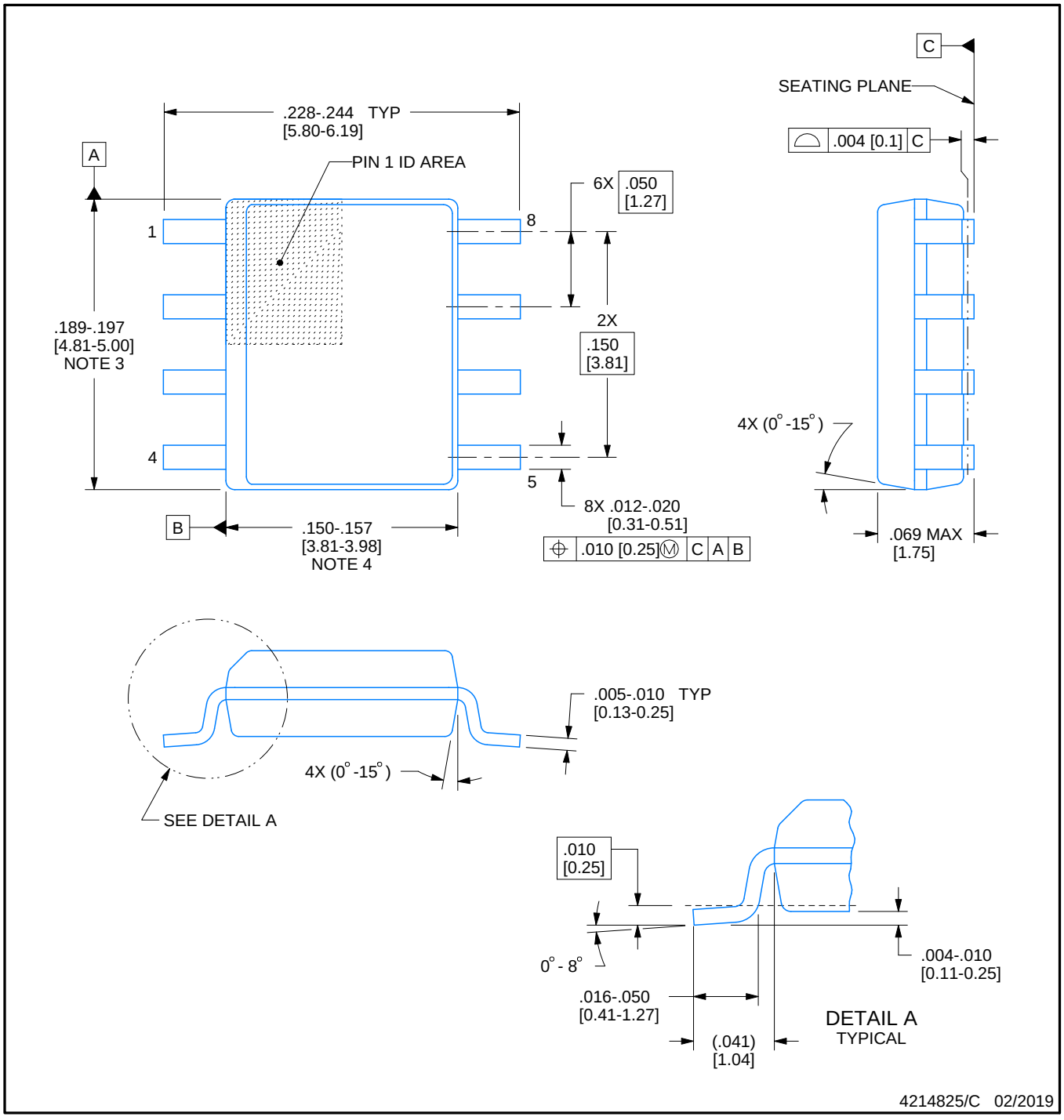


PACKAGE OUTLINE

D0008A

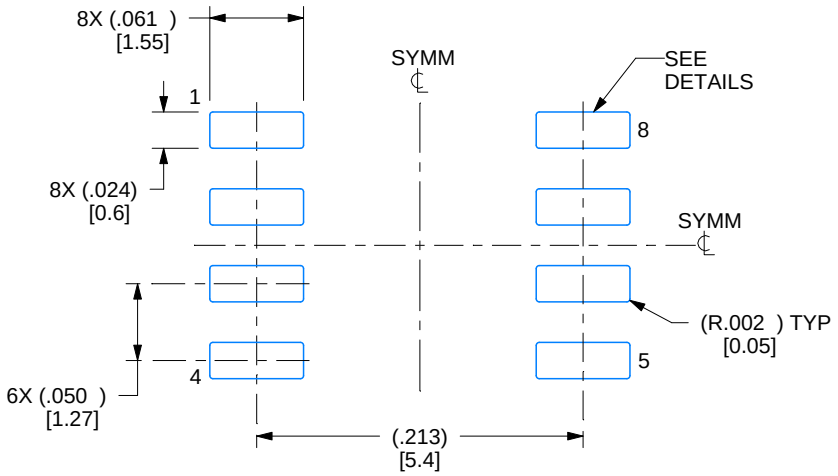
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

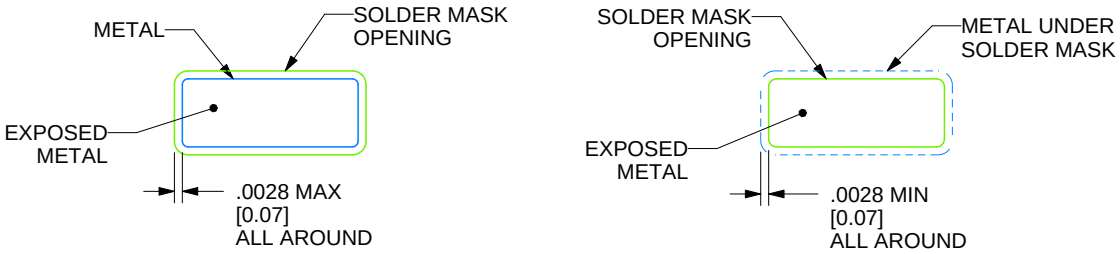


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

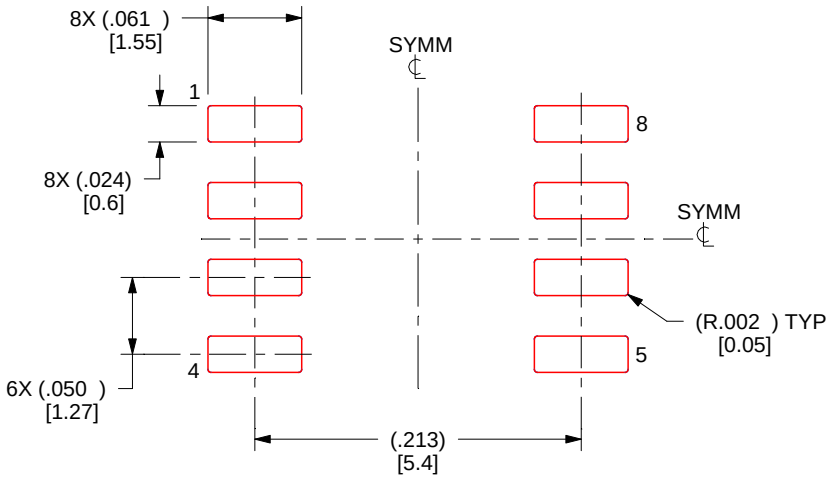
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

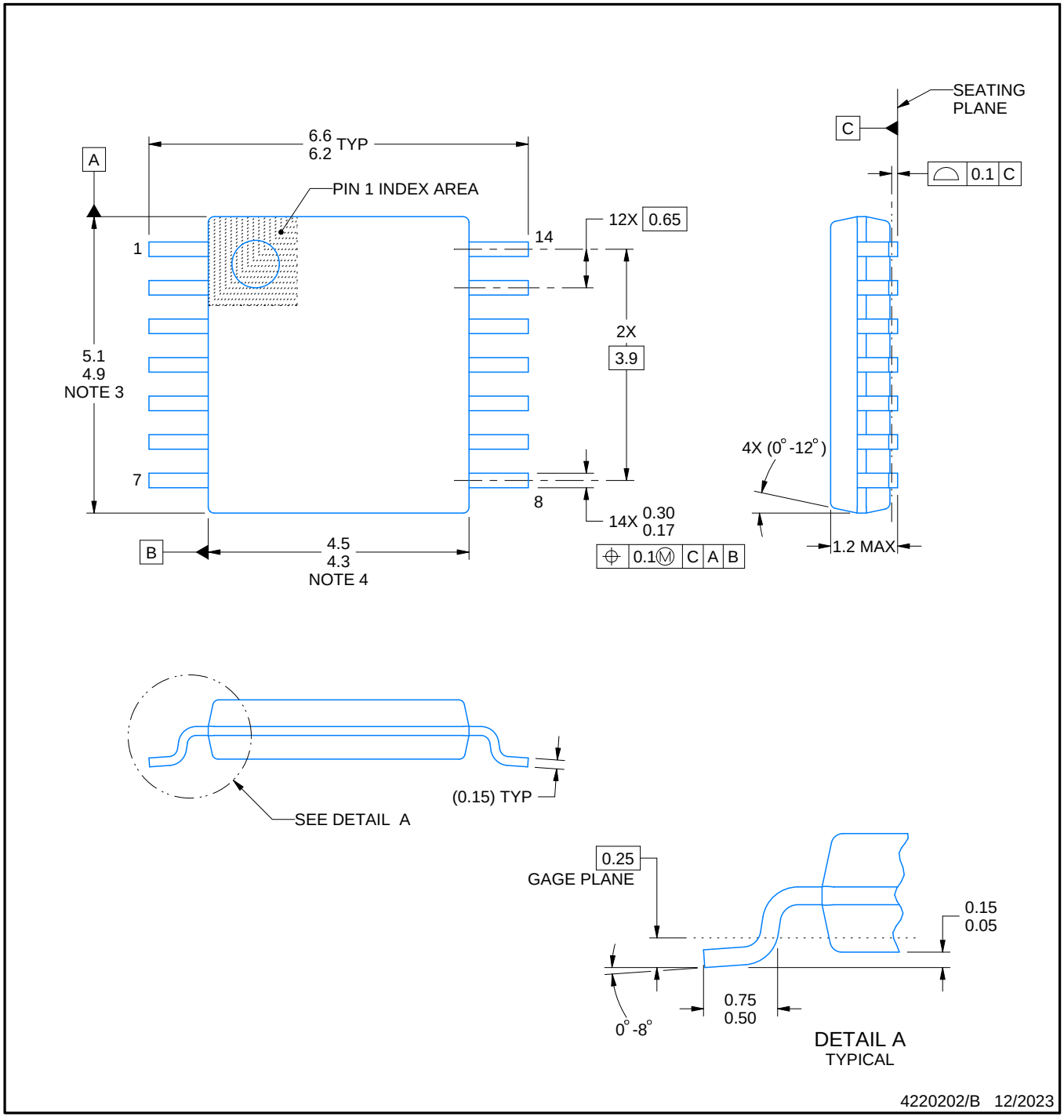
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

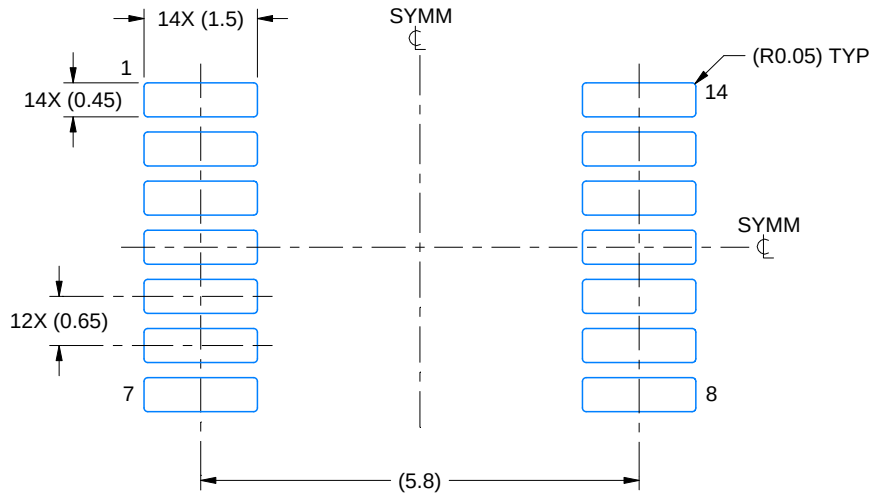
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

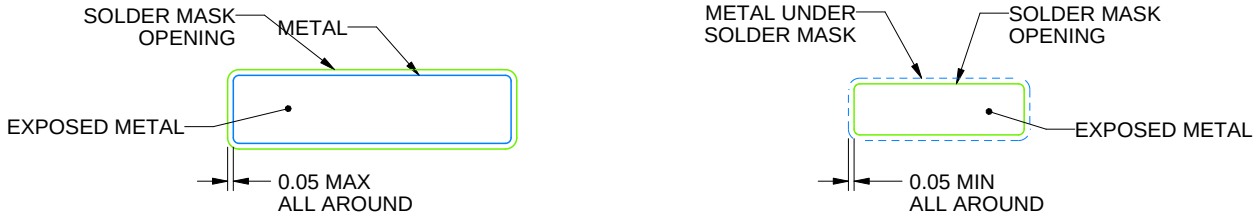


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

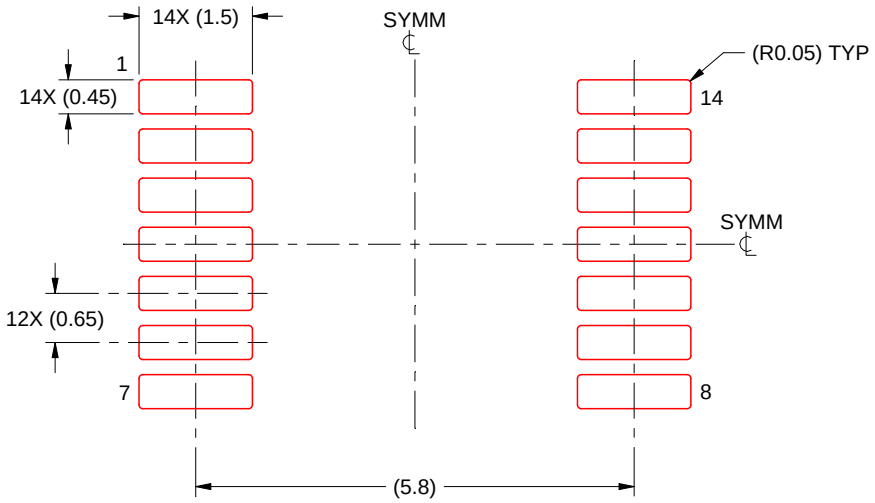


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

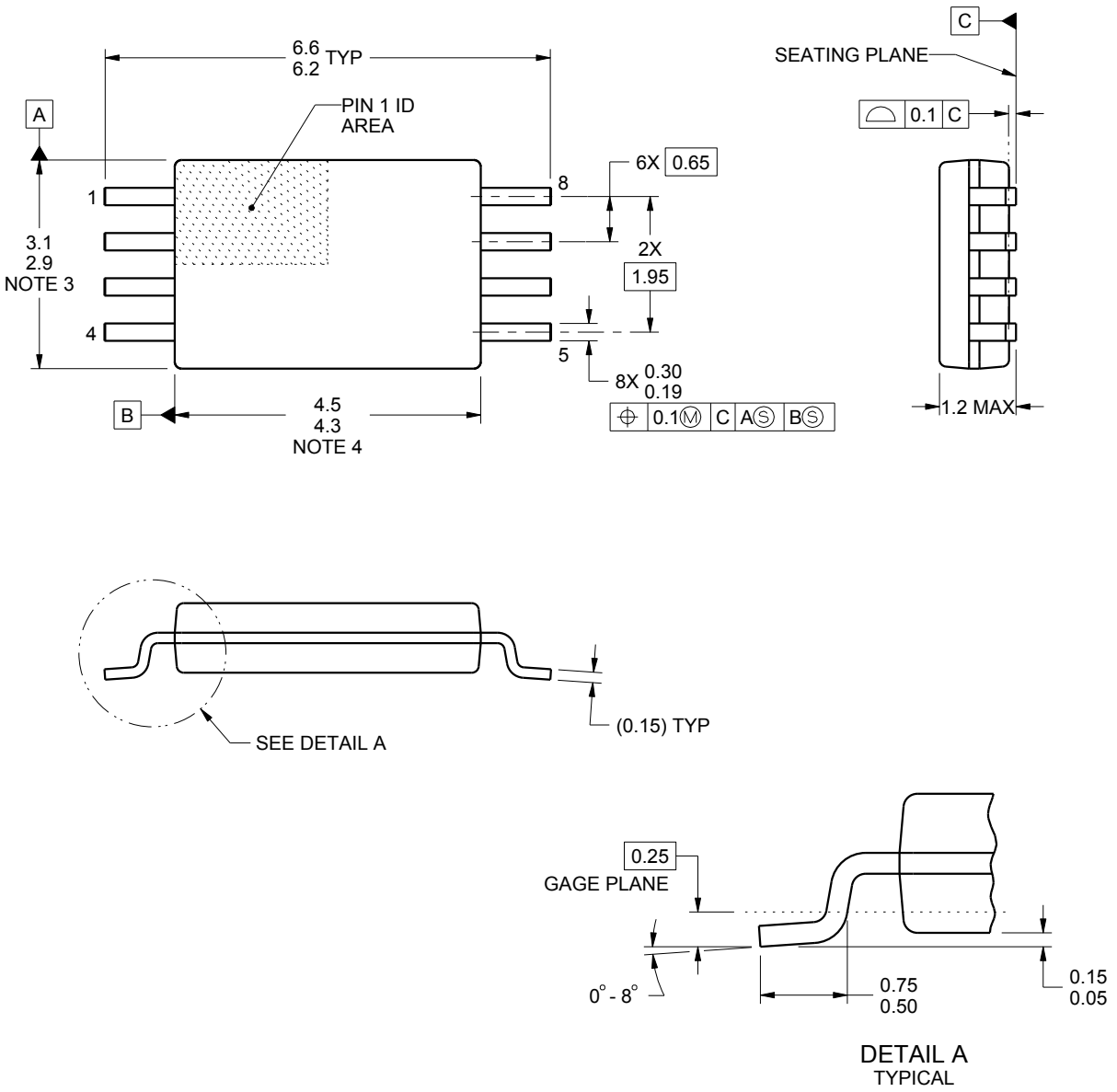
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

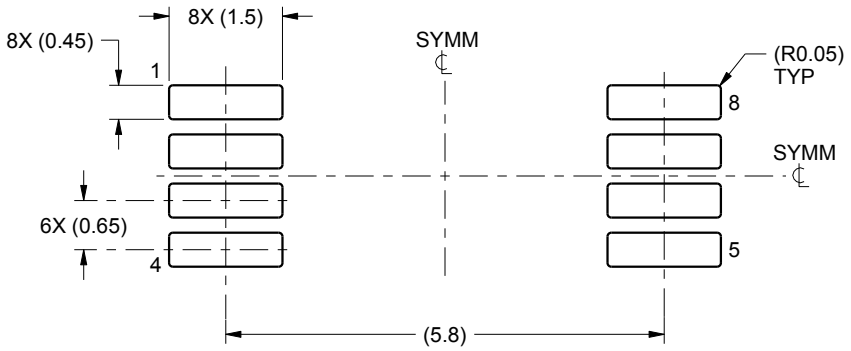
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

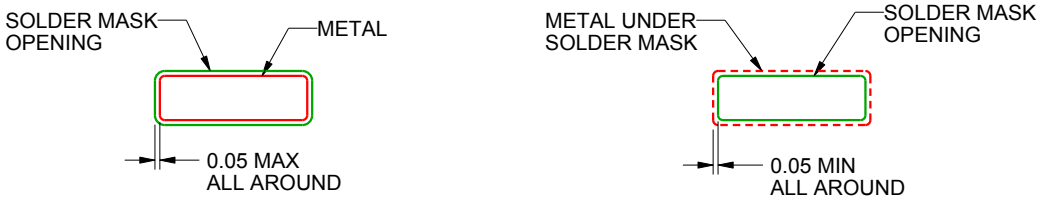


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

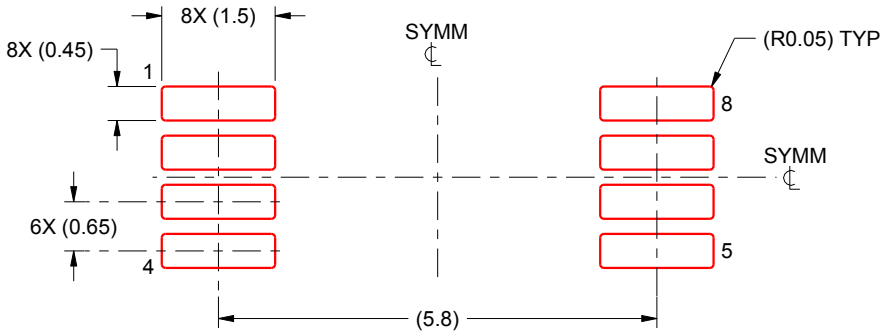


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

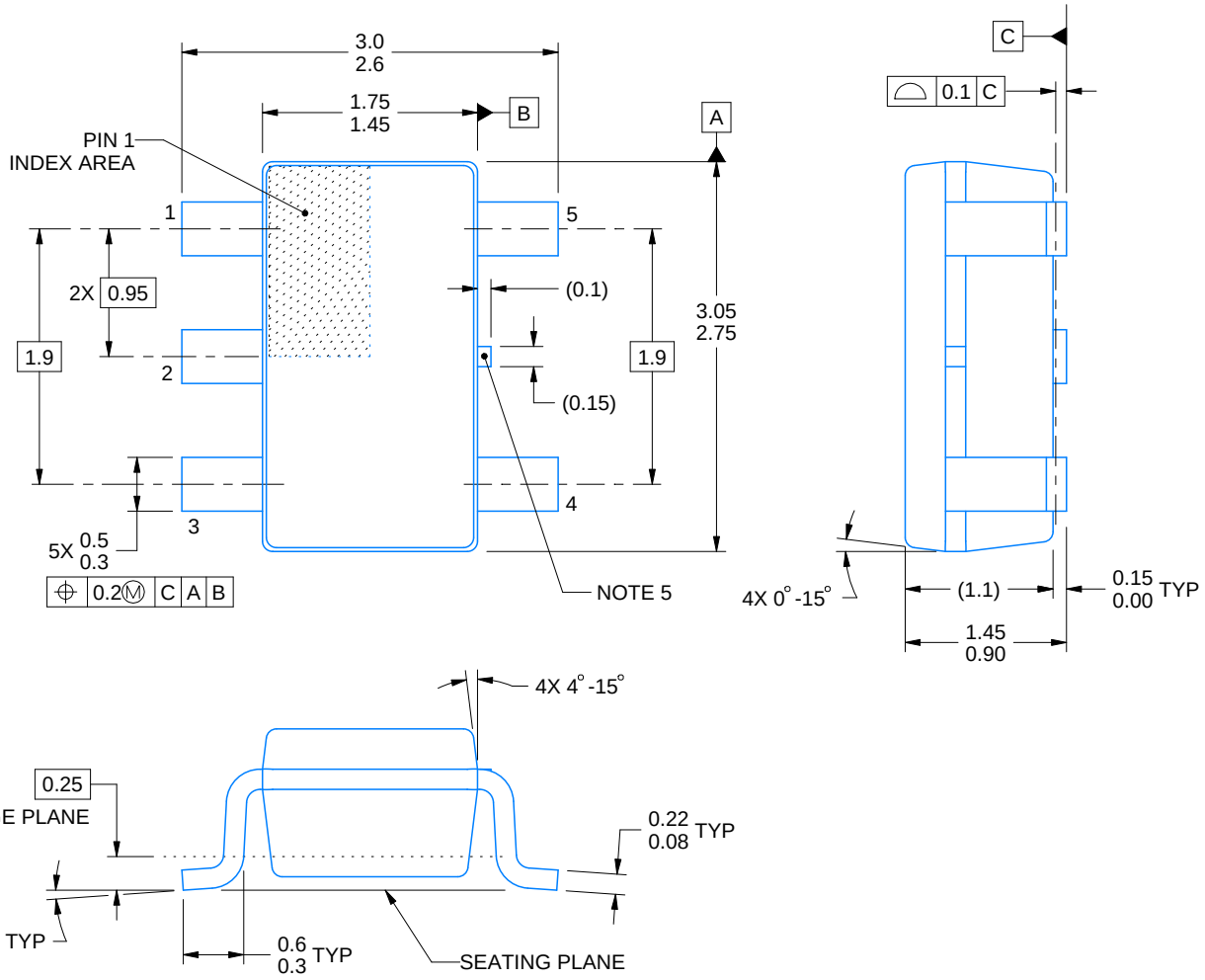
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

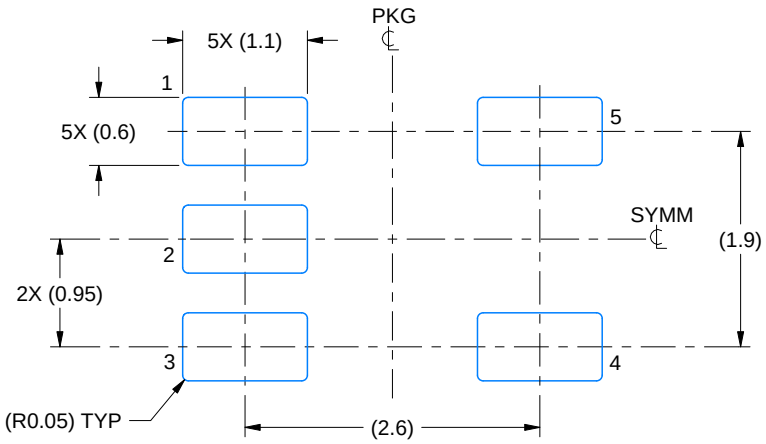
SMALL OUTLINE TRANSISTOR



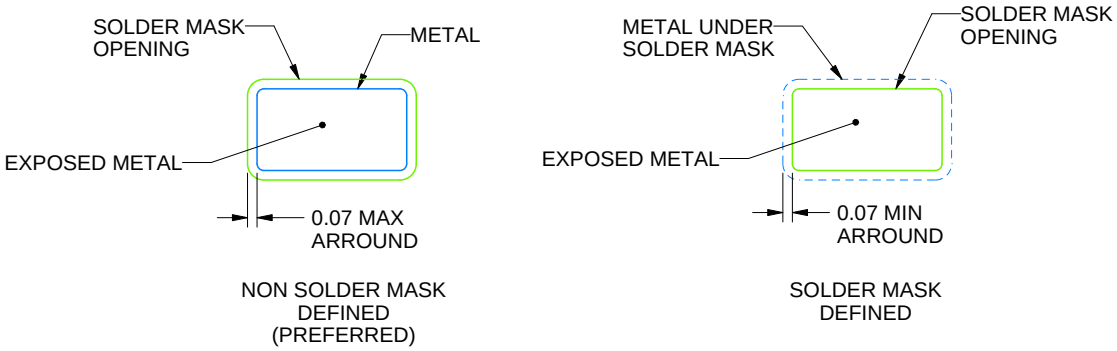
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

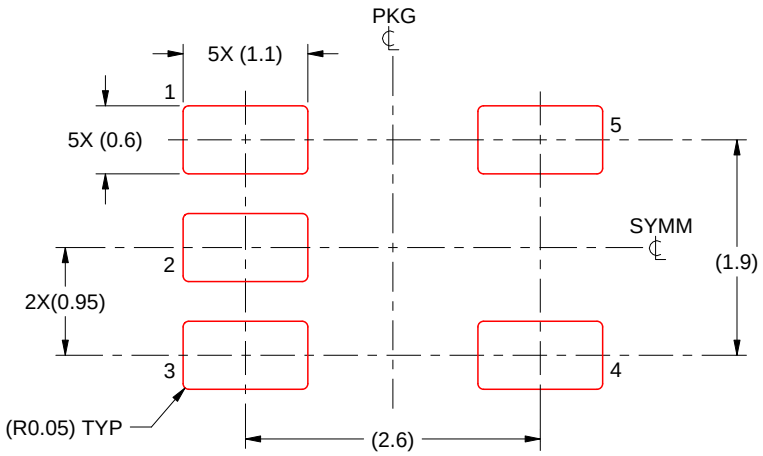


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

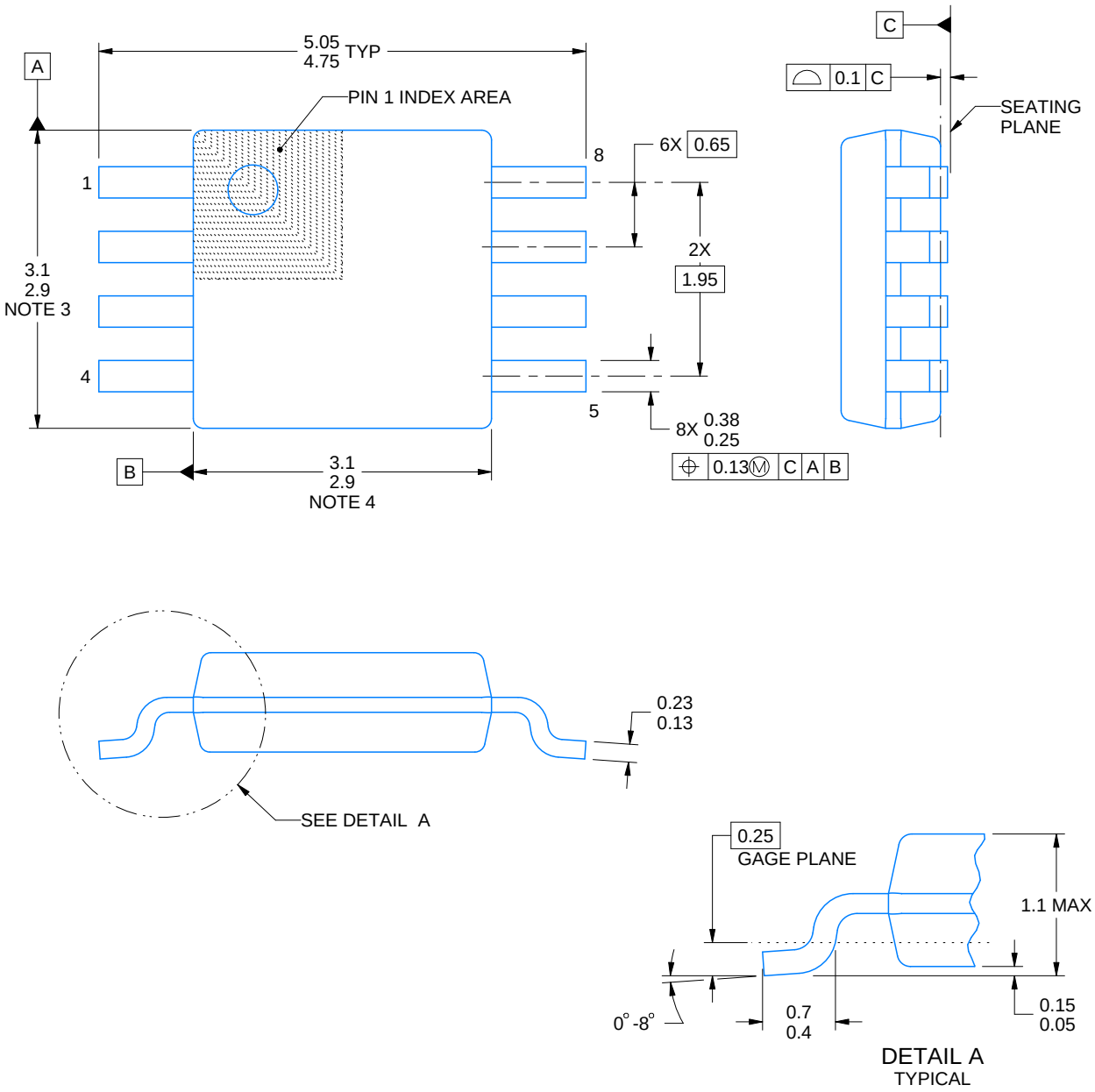
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

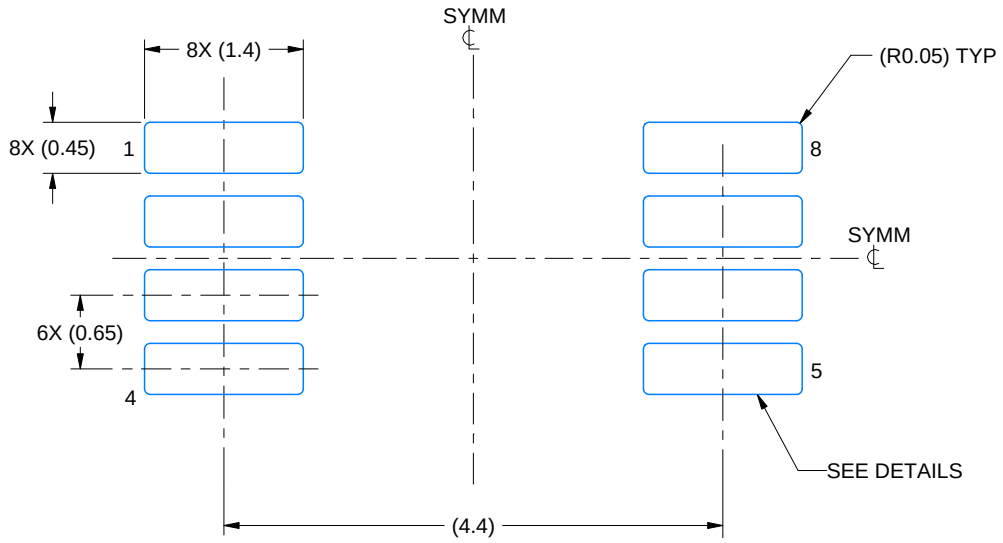
SMALL OUTLINE PACKAGE



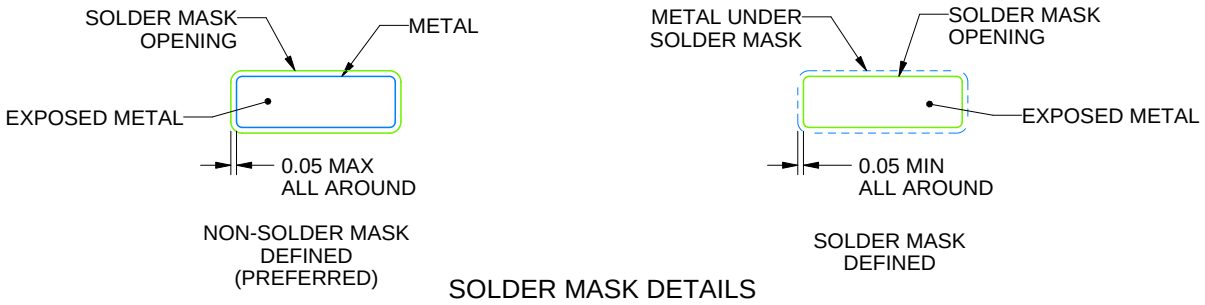
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

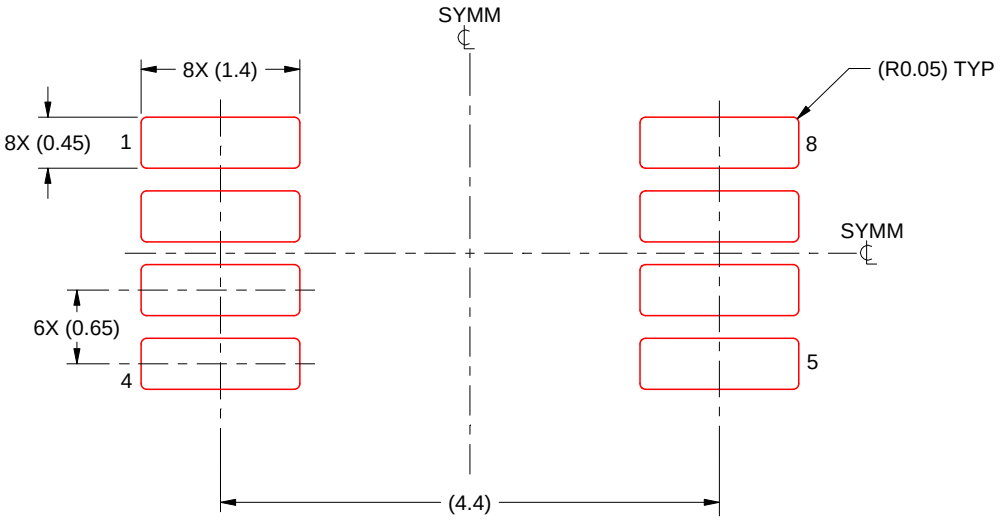


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

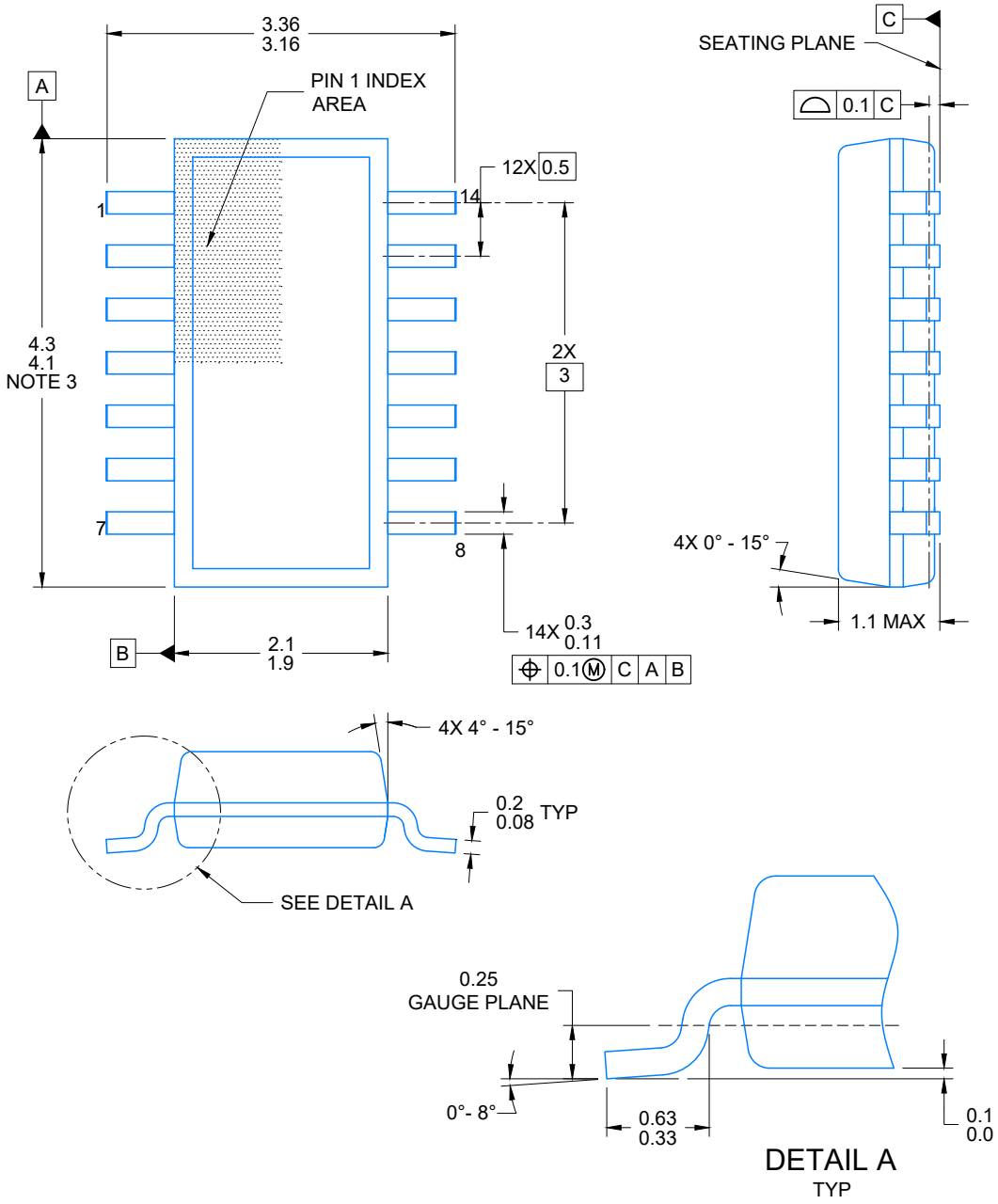
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DYY0014A

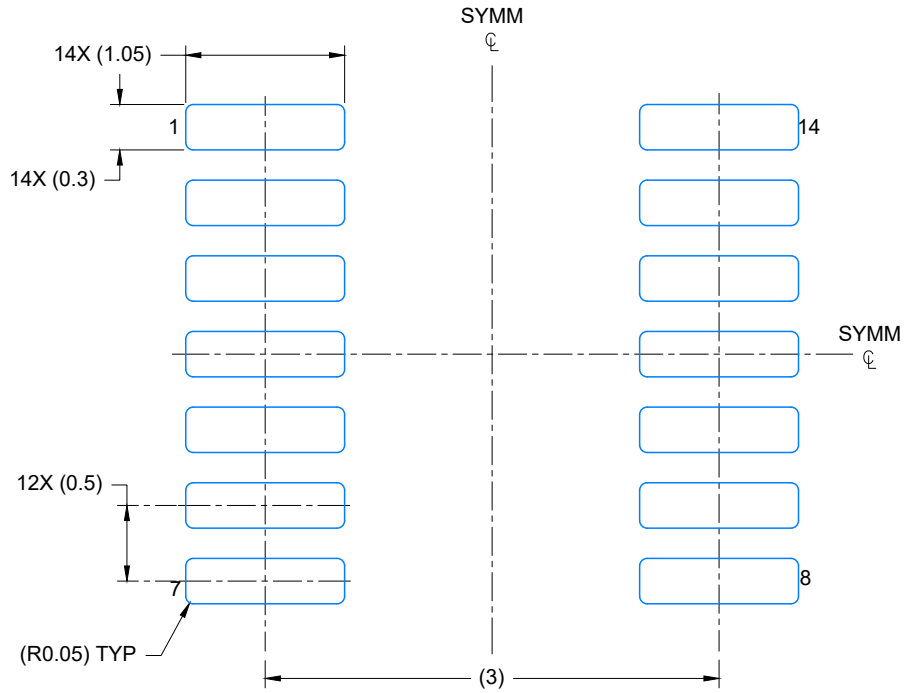
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

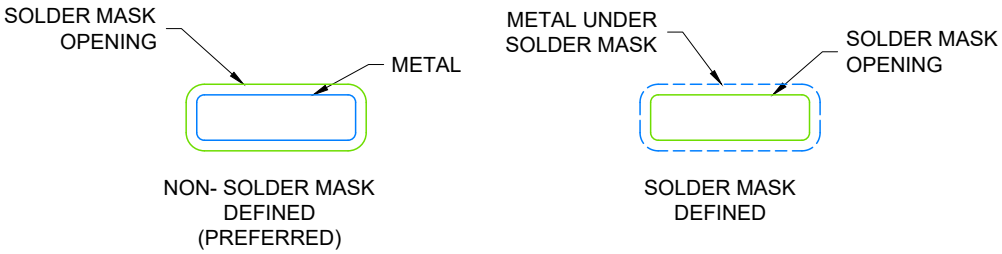


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

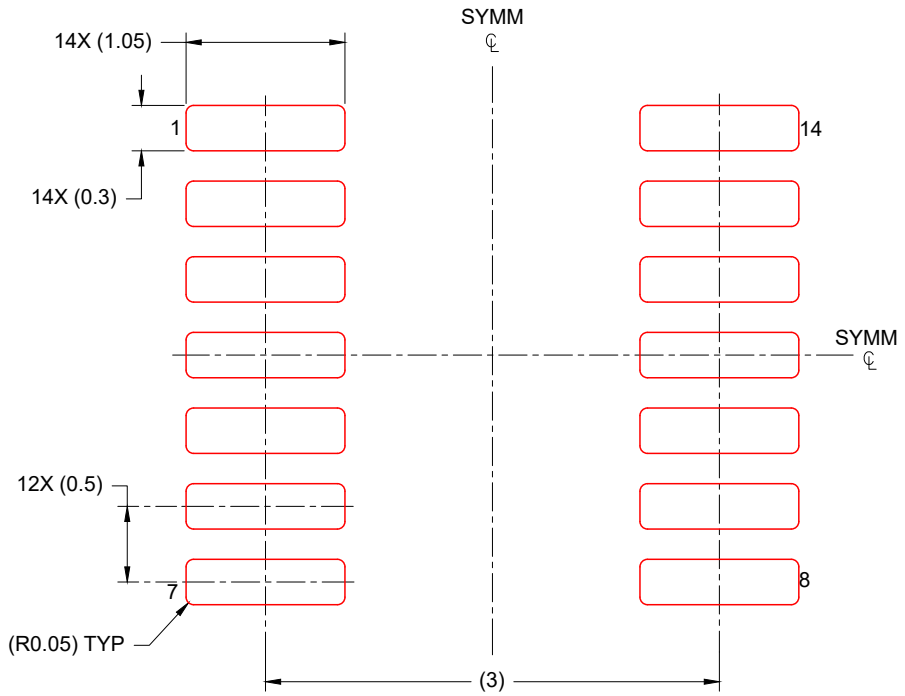


SOLDER MASK DETAILS

4224643/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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