TMF0008 8K bits Serial FRAM With SDQ Interface

1 Features

- 7680 Bits of FRAM for storage of user-programmable configuration data partitioned into multiple pages
- Single-wire interface to reduce circuit board routing
- Communicates at 15.4Kbps (standard Speed) and 90Kbps (overdrive Speed)
- Switch-point hysteresis and filtering embedded in the device to improve performance in the presence of noise
- IEC 61000-4-2 level 4 ESD protection (±8kV contact, ±15kV air, typical)
- Factory-programmed unique 64-bit identification number
- Operating temperature range: -10°C to 85°C
- Operating voltage range: 5V ±5% (standard and overdrive speed)
- Operating voltage range: 3.3V ±5% (standard speed only)
- Available in TO-92 (LP), WSON (DRS) and SO (PS) packages

2 Applications

- Medical cable identification
- Asset trackers
- Connected peripherals & printers
- Counterfeit hardware prevention

3 Description

The TMF0008 is an 8K bits serial Non-Volatile Memory (NVM) device containing a unique factory-programmed 48-bit identification number and 8-bit family code. The memory is FRAM-based and has higher endurance (10^6 R/W cycles) compared to other NVM technologies.

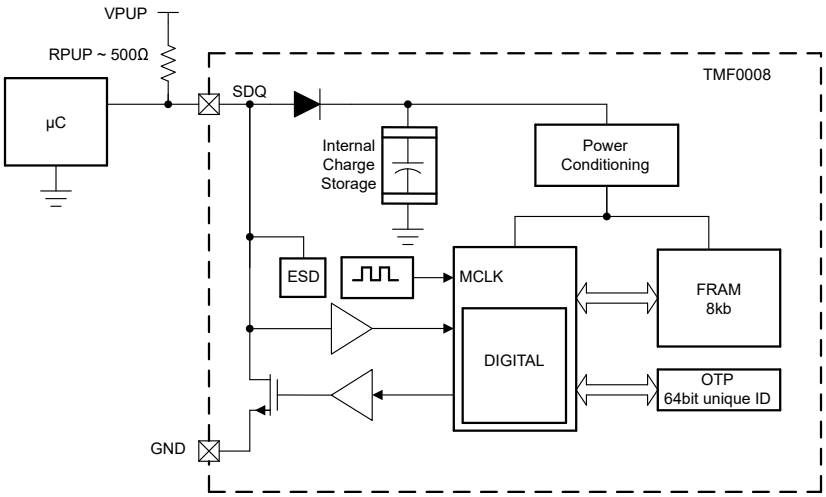
The device communicates over a SDQ™ single-wire interface and supports both 15.4Kbps and 90Kbps speeds. The SDQ pin acts as communication and power for the device. The memory is organized as thirty memory pages of 256 bits each. Data is written to a 32-byte scratchpad for verification before being copied to FRAM memory.

The device operates at two supply voltage ranges: 3.3V ±5% and 5V ±5% and is specified from -10°C to 85°C range. This operating range covers most applications and at the same time enables optimized design for low-cost development.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)
TMF0008LP	TO-92 (LP)	5.20mm × 3.68mm	4.83mm × 4.83mm
TMF0008DRS	WSON (DRS)	3.00mm × 3.00mm	3.00mm × 3.00mm
TMF0008PS	SO (PS)	6.20mm × 7.80mm	6.20mm × 5.30mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Block Diagram

Table of Contents

4 Pin Configuration and Functions

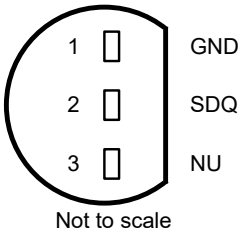


Figure 4-1. TMF0008 LP Package, 3-Pin TO-92 (Bottom View)

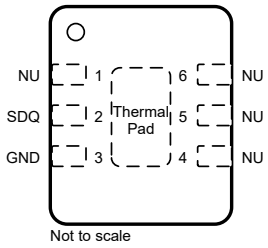


Figure 4-2. TMF0008 DRS Package, 6-Pin WSON (Top View)

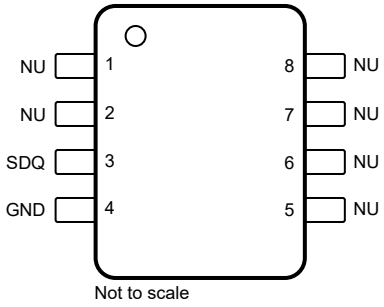


Figure 4-3. TMF0008 PS Package, 8-Pin SOIC (Top View)

Table 4-1. Pin Functions

PIN				Type	DESCRIPTION
NAME	TMF0008				
	TO-92	WSON	SOIC		
EP	—	EP	—	—	Exposed thermal pad. Connect to GND.
GND	1	3	4	GND	Ground
NU	3	1,4,5,6	1,2,5,6,7,8	—	Non-usable terminal. Do not connect.
SDQ	2	2	3	I/O	Data. Open drain, requires external 500Ω pullup resistor.

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{PUP}	DC voltage applied to data	–0.3	5.5	V
I_{OL}	Low-level output current		30	mA
T_{STG}	Storage temperature	–40	125	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and may affect device reliability, functionality, performance, and shorten device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±250	
		ESD IEC 61000-4-2 Air discharge, SDQ and GND	±15000	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. .

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{PUP}	Operational pull-up voltage	3.13		5.25	V
R_{PUP}	Serial Communication interface pull-up resistance		500		Ω
T_A	Operating free-air temperature	-10		85	°C

5.4 Thermal Information

THERMAL METRIC(1)		TMF0008			UNIT
		DRS (WSON)	PS (SO)	TO-92 (LP)	
		6 PINS	8 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70.2	109.9	133.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.5	55.6	99.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.2	61.6	103.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	16.4	28.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.2	60.6	103.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	11.0	-	-	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

Minimum and Maximum specifications apply from T_A of -10°C to 85°C. Typical specifications are at 25°C and V_{PUP} = 3.3 V and 5 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IO Pin: General Data						
V_{PUP}	Pull-up Voltage	±5% variation	3.13	3.3	3.46	V
			4.75	5	5.25	V
R_{PUP}	Pull-up Resistance	Notes (1),(2),(5)		500		Ω
C_{CABLE}	Cable Capacitance	Notes (4),(11)			1.7	nF
C_{IO}	Input Capacitance	Notes (3),(4)		2000		pF
I_L	Input Load Current	Note (6)		7	14	µA
V_{IL}	Input Low Voltage	Note (7)			0.5	V
V_{OL}	Output Low Voltage	Measured with R_{PUP} = 500Ω, V_{PUP} = 3.3V		0.4	0.5	V
		Measured with R_{PUP} = 500Ω, V_{PUP} = 5V		0.4	0.5	V
V_{TL}	High-to-Low Switching threshold (Notes (4),(5),(8))	V_{PUP} = 3.3V	0.84		1.72	V
		V_{PUP} = 5V	2		3	V
V_{TH}	Low-to-High Switching Threshold (Notes (4),(5),(9))	V_{PUP} = 3.3V	1.64		2.75	V
		V_{PUP} = 5V	3.2		4.3	V
V_{HY}	Switching Hysteresis (Notes (4),(5),(10))	V_{PUP} = 3.3V	0.44		1.1	V
		V_{PUP} = 5V	0.9		1.3	V

(1) Maximum allowable pull-up resistance is dependent on the number of devices connected and the recovery time. The specified value is assuming six devices are connected in the system and minimum recovery time.
(2) Resistance tolerance to be within 1% or less.
(3) Maximum Capacitance value represents the internal parasitic capacitance when V_{PUP} is first applied. Once the parasitic charge storage capacitance is charged, normal logic transitions are not affected.
(4) Specified by design, characterization or simulation only. Not production tested.
(5) V_{TL}, V_{TH}, and V_{HY} are a function of the internal supply voltage, which is a function of V_{PUP}, R_{PUP}, single-wire timing, and capacitive loading on SDQ pin. Lower VPUP, higher R_{PUP}, shorter t_{REC}, and heavier capacitive loading all lead to lower values of V_{TL}, V_{TH}, and V_{HY}.
(6) Applicable when SDQ is HIGH (at V_{PUP}) and the device is in idle mode (no digital activity or memory access). The numbers indicates the stand-by current consumption.
(7) The voltage on SDQ needs to be less or equal to V_{ILMAX} at all times the host is driving SDQ to a logic 0 level.
(8) Voltage below which, during a falling edge on SDQ, logic 0 is detected.
(9) Voltage above which, during a rising edge on SDQ, logic 1 is detected.
(10) After V_{TH} is crossed during a rising edge on SDQ pin, the voltage on SDQ must drop by at least V_{HY} to be detected as logic 0.
(11) System requirement.

5.6 Timing Requirements

Minimum and Maximum specifications apply from T_A of -10°C to 85°C. Typical specifications are at 25°C and V_{PUP} = 3.3V and 5V (unless otherwise noted).

			MIN	NOM	MAX	UNIT
IO Pin: General Data						
$t_{STARTUP}$	Start-up time	Minimum time SDQ must be HIGH before device responds with a presence pulse		10		ms
t_{REC}	Recovery Time	Standard speed (1), (2)	5			µs
		Overdrive speed (1), (2)	5			µs
t_{REH}	Rising-Edge Hold-Off Time	Standard speed (1), (2)	0.5		5	µs
t_{SLOT}	Time Slot Duration	Standard speed (3)	65			µs
		Overdrive speed (3)	11			µs
IO Pin: Single-Wire RESET, Presence-detect Cycle						
t_{RSTL}	Reset Low Time	Standard speed	480		550	µs
		Overdrive speed	48		80	µs
t_{PDH}	Presence-Detect High Pulse	Standard speed	15		60	µs
		Overdrive speed	2		6	µs
t_{PDL}	Presence-Detect Low Time	Standard speed	60		240	µs
		Overdrive speed	8		24	µs
t_{PDS}	Presence-Detect Sample Time (4),(5)	Standard speed	60	70	75	µs
		Overdrive speed	6	8.7	10	µs
IO PIN: Single-Wire Write						
t_{W0L}	Write-Zero Low Time	Standard speed (6)	60		120	µs
		Overdrive speed (6)	6		15.5	µs
t_{W1L}	Write-One Low Time	Standard speed (6)	1		15	µs
		Overdrive speed (6)	1		2	µs
IO PIN: Single-Wire Read						
t_{RL}	Read Low Time	Standard speed (2), (7)	5		15 - t_{RC}	µs
		Overdrive speed (2), (7)	1		2 - t_{RC}	µs
t_{RDS}	Read Sample Time (8)	Standard speed (2), (7)	t_{RL} + t_{RC}		15	µs
		Overdrive speed (2), (7)	t_{RL} + t_{RC}		3	µs
FRAM						
NCY	Write/Erase Cycles (Endurance)(2)				1M	Cycles
t_{PROG}	Programming Time(2)	For all 7.5Kb of memory			1	ms
t_{DR}	Data Retention(9)	At 80°C		10		Years
		At 85°C		7		

(1) The voltage on SDQ needs to be less or equal to V_{ILMAX} at all times the host is driving SDQ to a logic 0 level.
(2) Specified by design, characterization or simulation only. Not production tested.
(3) Defines maximum possible bit rate.
(4) Interval after t_{RSTL} during which a bus host can read logic 0 on SDQ if there is a TMF0008 present. The presence detect pulse can be outside this interval, but is complete within 2ms after power-up. This behavior addresses the scenario where the single-wire device has been powered off (bus low) for a long time. Bus power is then applied. The device is allowed to malfunction, and generate a presence pulse that violates the presence timing specification. However, the abnormal condition is resolved typically within 10ms.
(5) System requirement
(6) t_ε in Figure 6-17 and Figure 6-18 represents the time required for the pullup circuitry to raise the voltage on the SDQ pin from V_{IL} to V_{TH}. Hence the actual maximum duration for the host to pull the line low is $t_{W1LMAX} + t_F - t_\varepsilon$ and $t_{W0LMAX} + t_F - t_\varepsilon$, respectively.

(7) t_{RC} in Figure 6-19 represents the time required for the pullup circuitry to raise the voltage on the SDQ pin from V_{IL} to the input-high threshold of the host device. Hence, the actual maximum duration for the host to pull the line low is t_{RLMAX} + t_F.
(8) Refers to the minimum time after which the recognition of negative edge is possible after V_{TH} has been reached on the preceding rising edge.
(9) Data retention time is degraded as T_A increases. Long-term storage at elevated temperatures is not recommended.

5.7 Functional Tests

Over operating free-air temperature range and V_{PUP} = 3.3V and 5V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Multi-target bus	Any TMF0008 must be able to communicate in a network where there are multiple responder devices. An example configuration of 3 responder devices (including the DUT) is shown in *Multiple Responder Configurations*. (1)		0		Multi-responder Bus Fails

(1) See *Test Procedures for Functional Tests*.

5.8 Typical Characteristics

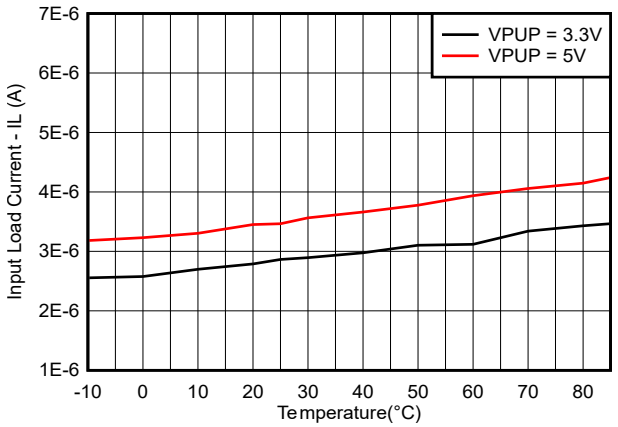


Figure 5-1. Input Load Current (I_L) vs Temperature (Standard Speed)

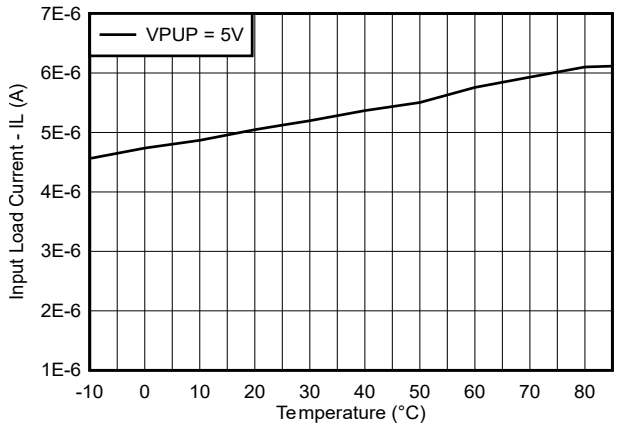


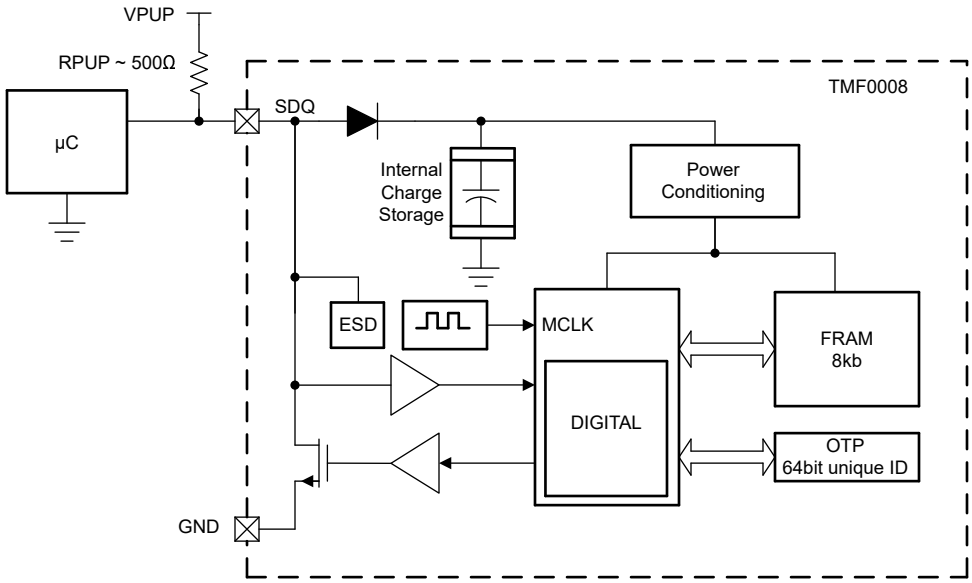
Figure 5-2. Input Load Current (I_L) vs Temperature (Overdrive Speed)

6 Detailed Description

6.1 Overview

The *Functional Block Diagram* section presents the on-chip block level components of the TMF0008 device. The TMF0008 has the following data components: a 64-bit factory-programmed ROM, containing 8-bit family code, 48-bit identification number and 8-bit CRC value, and 7680 bits of FRAM Data Memory. Power for read and write operations is derived from the SDQ pin. An internal capacitor stores energy while the signal line is high and releases energy during the low times of the SDQ pin, until the pin returns high to replenish the charge on the capacitor.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 7680-Bit FRAM

Table 6-1 is a memory map of the 7680-bit FRAM section of the TMF0008, configured as 30 pages of 32-bytes each. Four adjacent pages form one 128-byte block. The 32-byte volatile scratchpad buffer is used when programming the FRAM memory. The process for writing to the FRAM memory includes two steps. Data is first written to the scratchpad buffer. The data is then verified by reading the scratchpad buffer that confirms proper receipt of the data. If the buffer content is correct, a copy scratchpad command is issued to copy the scratchpad buffer to the FRAM memory. This process verifies data integrity when programming the memory. The details for programming and reading the 7680-bit FRAM portion of the TMF0008 are in the *Memory Function Commands* section of this data sheet.

Table 6-1. FRAM Data Memory Map

ADDRESS RANGE	TYPE (1)	DESCRIPTION	PROTECTION CODES (NOTES)
0000h to 007Fh	R/(W)	Data Memory Pages 0 to 3 (Block 0)	(Protection controlled by address 03C0h)
0080h to 00FFh	R/(W)	Data Memory Pages 4 to 7 (Block 1)	(Protection controlled by address 03C1h)
0100h to 017Fh	R/(W)	Data Memory Pages 8 to 11 (Block 2)	(Protection controlled by address 03C2h)
0180h to 01FFh	R/(W)	Data Memory Pages 12 to 15 (Block 3)	(Protection controlled by address 03C3h)
0200h to 027Fh	R/(W)	Data Memory Pages 16 to 19 (Block 4)	(Protection controlled by address 03C4h)
0280h to 02FFh	R/(W)	Data Memory Pages 20 to 23 (Block 5)	(Protection controlled by address 03C5h)
0300h to 037Fh	R/(W)	Data Memory Pages 24 to 27 (Block 6)	(Protection controlled by address 03C6h)
0380h to 03BFh	R/(W)	Data Memory Pages 28 to 29 (Block 7)	(Protection controlled by address 03C7h)

(1) R = Read, W = Write

In FRAM devices, digital information is stored as polarization in a dielectric. This polarization can be lost at a temperature-dependent rate. Increasing temperatures increase the de-polarization rate. Data Retention metrics are listed in the Electrical Characteristics table.

6.3.2 FRAM Status Memory

As shown in Table 6-1, the data memory of the TMF0008 consists of eight contiguous blocks of FRAM memory. Blocks 0 to 6 are 128 bytes each, formed by four adjacent memory pages, whereas block 7 is 64 bytes, formed by two adjacent memory pages (A data memory page is 32 adjacent memory bytes).

In addition to the data memory, the TMF0008 consists of the status memory starting at address 03C0h as shown in *Table 6-2*. The register page in the status memory consists of eight protection control bytes, six bytes of user EEPROM, and one byte each to lock the memory block and the register page.

The eight protection control bytes and the memory block lock byte together control the access to the eight data memory blocks. By default, the memory blocks are set to open access. A protection byte value of 55h sets the corresponding memory block to write protection mode, whereas a protection byte value of AAh sets the corresponding memory block to EPROM mode.

If the memory block lock byte is programmed to either 55h or AAh, copy protection is set for all write-protected data memory blocks (memory blocks in EPROM mode are not affected). Similarly, if the register page lock byte is programmed to either 55h or AAh, copy protection is set for the entire register page.

Setting a memory location into write protection mode allows the copy-scratch pad operation, but prevents data from being changed. This allows memory to be reprogrammed with the same data, refreshing the polarization for data retention longevity.

As compared to write protection, copy protection blocks the copy-scratchpad function. Only use this feature after all write-protected blocks and associated protection control bytes are set to the final values. Note that copy protection does not prevent copying data across devices. When set to 55h or AAh, the protection control registers and the lock bytes write-protect themselves. Any other setting allows unrestricted write access.

Addresses 03D1h and 03D2h are available for programming an optional manufacturer ID. These values can be read by the host, for example, to associate an end-user product with a TMF0008. At address 03D0h, the TMF0008 stores a byte for locking the manufacturer ID, with a default value of 00h. After writing AAh or 55h to this location, the manufacturer ID and lock byte are permanently write protected.

Table 6-2. FRAM Status Memory Map

ADDRESS RANGE	TYPE (1)	DESCRIPTION	PROTECTION CODES (NOTES)
03C0h	R/(W)	Protection Control Byte (Block 0)	55h: Write Protect Block 0; AAh: EPROM Mode Block 0; 55h or AAh: Write Protect 03C0h
03C1h	R/(W)	Protection Control Byte (Block 1)	55h: Write Protect Block 1; AAh: EPROM Mode Block 1; 55h or AAh: Write Protect 03C1h
03C2h	R/(W)	Protection Control Byte (Block 2)	55h: Write Protect Block 2; AAh: EPROM Mode Block 2; 55h or AAh: Write Protect 03C2h
03C3h	R/(W)	Protection Control Byte (Block 3)	55h: Write Protect Block 3; AAh: EPROM Mode Block 3; 55h or AAh: Write Protect 03C3h
03C4h	R/(W)	Protection Control Byte (Block 4)	55h: Write Protect Block 4; AAh: EPROM Mode Block 4; 55h or AAh: Write Protect 03C4h
03C5h	R/(W)	Protection Control Byte (Block 5)	55h: Write Protect Block 5; AAh: EPROM Mode Block 5; 55h or AAh: Write Protect 03C5h
03C6h	R/(W)	Protection Control Byte (Block 6)	55h: Write Protect Block 6; AAh: EPROM Mode Block 6; 55h or AAh: Write Protect 03C6h

Table 6-2. FRAM Status Memory Map (continued)

ADDRESS RANGE	TYPE (1)	DESCRIPTION	PROTECTION CODES (NOTES)
03C7h	R/(W)	Protection Control Byte (Block 7)	55h: Write Protect Block 7; AAh: EPROM Mode Block 7; 55h or AAh: Write Protect 03C7h
03C8h-03CDh	R/(W)	USER EEPROM	
03CEh	R/(W)	Memory Block Lock	55h or AAh: Copy Protect Write-Protected Data Memory Pages 55h or AAh: Write Protect 03CEh
03CFh	R/(W)	Register Page Lock	55h or AAh: Copy Protect 03C0h-03CFh
03D0h	R/(W)	Factory Byte	55h or AAh: Write protect 03D0h-03D2h Other: 03D0h-03D2h are programmable
03D1h	R/(W)	Manufacturer ID	
03D2h	R/(W)	Manufacturer ID	
03D3h	R	RESERVED	

(1) R = Read, W = Write

6.3.3 Address Registers and Transfer Status

The TMF0008 uses three address registers: TA1, TA2, and E/S (Figure 6-1, Figure 6-2, and Figure 6-3).

The registers TA1 and TA2 are loaded with the target address to which the data is to be written or from which data is to be read. Register E/S is a read-only transfer status register used to verify data integrity with write commands. During a Write Scratchpad command, the E/S bits E[4:0] are initially loaded with the incoming T[4:0] and are then incremented on each incoming subsequent data byte. Thus, E[4:0] is the ending offset counter within the 32-byte scratchpad. The PF bit of the E/S register is a Partial byte Flag and is set when the received byte is partial (data bits not an integer multiple of 8) or if the scratchpad data is invalid due to a loss of power.

The PF bit is cleared when there is a successful scratchpad write. The AA (Authorization Accepted) bit of the E/S register is set when there is an authorization match during a Copy Scratchpad command. If AA=1 and PF=0, these values indicate that the data stored in the scratchpad has already been copied to the target memory. The AA flag is cleared whenever data is written into the scratchpad. The AA flag is valid only if the PF flag is 0.

Figure 6-1. Target Address (TA1)

7	6	5	4	3	2	1	0
T7	T6	T5	T4	T3	T2	T2	T0

Figure 6-2. Target Address (TA2)

7	6	5	4	3	2	1	0
T15	T14	T13	T12	T11	T10	T9	T8

Figure 6-3. Ending Address with Data Status (E/S) (Read Only)

7	6	5	4	3	2	1	0
AA	0	PF	E4	E3	E2	E1	E0

6.3.4 Writing Data to the FRAM

The TMF0008 device does not allow writes to the FRAM memory directly by the host. Writing to the FRAM memory directly by the host is achieved by using the scratchpad as an interim repository. To write into the scratchpad, the host first issues the Write Scratchpad command followed by the desired target address and the data to be written into the scratchpad. Depending on the conditions described in the Write Scratchpad Command section, the host can receive an inverted CRC16 of the entire write scratchpad sequence (the write scratchpad command, the address, and the data) at the end of the Write Scratchpad command sequence.

If the host receives the CRC16 value, the host can compare this value to the expected computed value. If there is a match, the write scratchpad communication is successful and the host can decide to proceed to the Copy Scratchpad command.

If the host does not receive the CRC16 value, then the host can use the Read Scratchpad command to verify integrity of the data stored in the scratchpad. After the Read Scratchpad command is received, the TMF0008 initially transmits the contents of the target address registers (TA1, TA2) and the E/S register. If the PF flag is set, or if the AA flag is set but PF flag cleared, the previous Write Scratchpad command is not successful. In this case, the host can terminate the Read Scratchpad sequence and start another attempt to write data to the scratchpad. If the previous Write Scratchpad is successful, both flags are cleared and the E[4:0] that is read indicates the address of the last byte written to the scratchpad. In this case, the host can continue reading from the TMF0008, verifying all the data bytes. If there is a match, the host can send the Copy Scratchpad command followed by the exact data of the registers TA1, TA2, and E/S that the host obtained by reading the scratchpad. At the end of the Copy Scratchpad sequence, if the authorization pattern matches, the TMF0008 starts copying the scratchpad data to the requested location, provided copy protection is not set, the PF flag is cleared, and there are no Read Memory or Extended Read Memory commands issued between Write and Copy Scratchpad commands.

6.3.5 TMF0008 Device ID

The 64-bit ID identifies each TMF0008. The 48-bit serial number is unique and programmed by Texas Instruments. The default Family code is 23h.

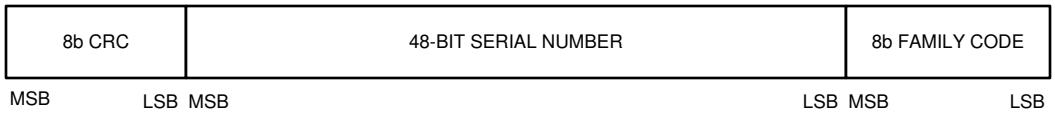


Figure 6-4. 64-Bit Factory Programmed EPROM

6.3.6 Bus Termination

The drive output of the TMF0008 is an open-drain, N-channel MOSFET, for proper operation, a 500-Ω external pullup resistor must be connected on the SDQ bus (see Figure 7-1).

6.4 Device Functional Modes

6.4.1 Test Procedures for Functional Tests

This section outlines the specific test procedures used to obtain the parameters listed in *Functional Tests*.

6.4.1.1 Multiple Responder Configurations

This test verifies the operation of the TMF0008 in a multi-drop use case. The host must be able to communicate with multiple devices on the SDQ bus. The presence of other DUTs must not impact communication to the selected DUT.

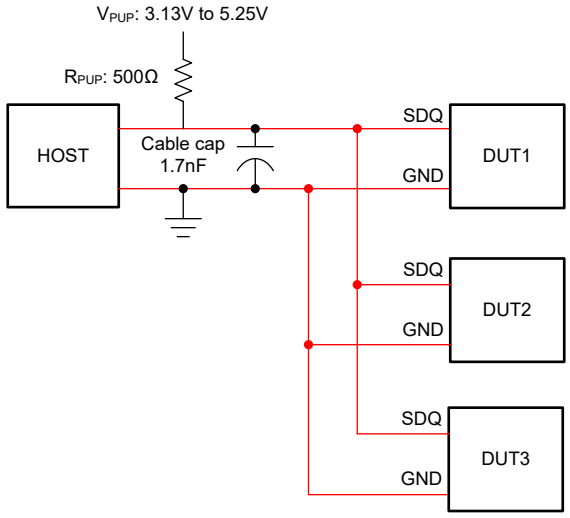


Figure 6-5. Multiple Target Configuration

Successful communication implies the following sequence of instructions must be executed without failure:

1. Issue RESET in standard speed and check for presence pulse
2. Issue SEARCH ROM command to identify the IDs of responder devices on the SDQ bus.
3. Issue RESET in standard speed and check for presence pulse.
4. Select one of the targets by issuing MATCH ROM command with the specific ID of the responder device identified from the SEARCH ROM command.
5. Issue MEMORY Commands to program or read from the memory.
6. Repeat steps 3, 4, and 5 for other responder devices on the SDQ bus.

6.5 Programming

6.5.1 Serial Communication

The host reads, programs, or checks the status of the TMF0008 through the command structure of the SDQ interface as shown in Figure 6-6. The command structure includes ROM and MEMORY commands.

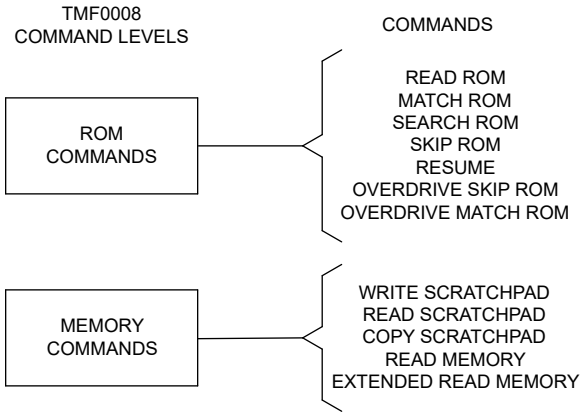


Figure 6-6. Command Structure for the TMF0008

6.5.2 Initialization

The host always begins the transaction with the TMF0008 (responder) devices through an initialization process. The Initialization process consists of the RESET and PRESENCE pulses. The host generates the RESET pulse, while the responder devices acknowledges the RESET pulse with the PRESENCE pulse. The host resets the

responder devices by driving the SDQ bus low for at least 480 µs. The PRESENCE pulse lets the host know that there are one or more responder devices on the SDQ bus.

6.5.3 ROM Commands

After the host detects the presence of one or more responder devices on the SDQ bus, the host can send an 8-bit ROM function commands shown in Figure 6-6. This section describes the scenarios where each of the ROM command can be issued. See Figure 6-6 for list of these commands.

6.5.3.1 READ ROM Command [33h]

The READ ROM command sequence (shown in Figure 6-7) starts with the host generating the RESET pulse of at least 480 µs. The device responds with a PRESENCE pulse. Next, the host continues by issuing the READ ROM command, 33h, and then reads back the 56-bit Family code and serial number followed by the 8-bit CRC using the READ signaling (see the READ and WRITE signals section) during the data frame. The READ ROM command can be issued by the host only if there is a single responder device on the SDQ bus. If the host issues the command when there are more than 1 responder device on the SDQ bus, then data collision occurs because all the responder devices try to respond to the host. The host can identify the data collision by comparing the CRC from the READ ROM sequence with the computed CRC, which results in a mismatch.

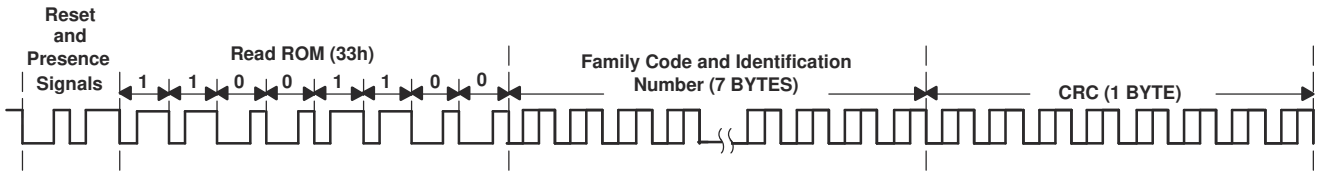


Figure 6-7. READ ROM Sequence

6.5.3.2 Match ROM Command [55h]

When there are multiple responder devices on the bus, the Match ROM command, 55h, is used by the host to select a specific responder device when the family code and identification number is known. The host issues the Match ROM command followed by the family code, serial number, and the CRC byte. The responder device that matches the 64-bit serial ID is selected and available to perform subsequent memory function commands. The MATCH ROM command can also be used with a single responder device on the bus.

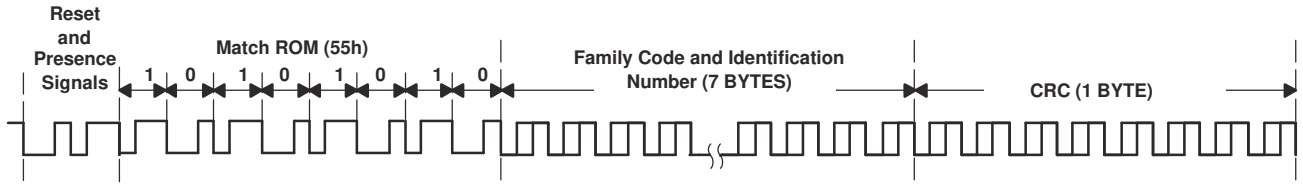


Figure 6-8. Match ROM Sequence

6.5.3.3 SKIP ROM Command [CCh]

The SKIP ROM command sequence (shown in Figure 6-9) is the fastest sequence that allows the host to begin transacting with the responder device. The Skip ROM command, CCh, allows the host to access the memory functions without issuing the 64-bit serial ID. The Skip ROM command is directly followed by a memory function command. The SKIP ROM command is only issued with one device present on the SDQ bus. If the SKIP ROM command is issued when there are multiple responder devices on the SDQ bus, all the responder devices begin responding to the subsequent memory command resulting in a data collision on the bus.

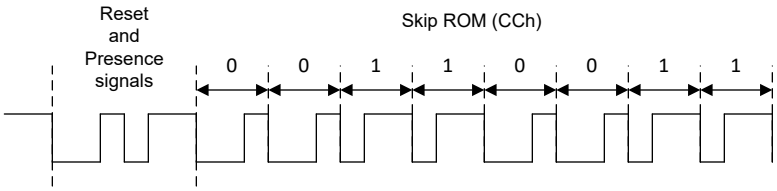


Figure 6-9. SKIP ROM Sequence

6.5.3.4 SEARCH ROM Command [F0h]

The SEARCH ROM command helps to identify the number of devices and the 64-bit unique ID of each of the devices during the initial system bring-up when the host is not aware of the number of devices on the SDQ bus. The SEARCH ROM command sequence begins with the host generating the RESET pulse of at least 480 µs. All the responder devices on the SDQ bus responds with a PRESENCE pulse. Next, the host continues by issuing the SEARCH ROM command, F0h. Following the SEARCH ROM command, the host issues three time slots for each bit of the 64-bit serial ID as shown in Figure 6-10. In the first time slot, the responder devices begin transmitting the bit of the 64 serial ID starting with the least significant bit. In the second time slot, the responder devices transmit the complement of the bit. In the third time slot, the host writes the bit to be selected. The process continues until the end of the 64-bit serial ID. All the responder devices that do not match the bit written by the host in the third time slot exits from the search process. If the host read zeros in the first two time slots, then a collision condition has occurred. The host knows there is more than one device on the SDQ bus. By choosing the bit value to write, the host is branching out to eliminate one or more contending responder devices. At the end of the first run sequence, the host knows the serial ID of a single device. The sequence is then repeated to identify the serial IDs of the remaining devices on the SDQ bus.

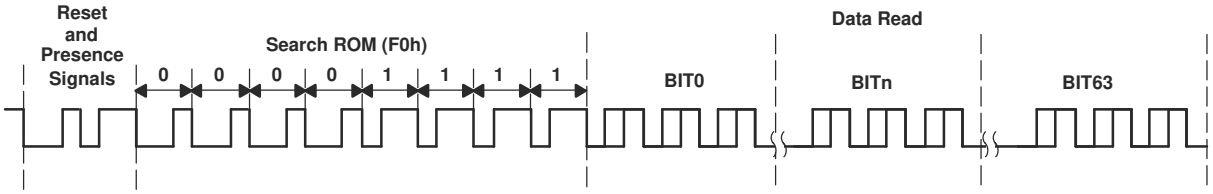


Figure 6-10. SEARCH ROM Sequence

6.5.3.5 RESUME Command [A5h]

When there are multiple responder devices on the SDQ bus, the RESUME command, A5h, can be used to maximize the data throughput by reducing the number of bit transactions needed to select the responder device. Before issuing the RESUME command, the host must first select the responder device by issuing the MATCH ROM or OVERDRIVE MATCH ROM command sequence. This selects the responder device. All other responder devices do not respond to subsequent memory function commands and RESUME command function.

6.5.3.6 OVERDRIVE SKIP ROM Command [3Ch]

The TMF0008 supports a high speed mode called the Overdrive mode. The OVERDRIVE SKIP ROM command sequence starts with the host generating the RESET pulse of at least 480 µs. The device responds with a PRESENCE pulse. Next, the host continues by issuing the OVERDRIVE SKIP ROM command, 3Ch, in standard speed. The device now enters Overdrive mode. Make sure all subsequent communication with the target device are at overdrive speed. The host can bring all the responder devices back to standard speed by issuing a reset pulse of at least 480 µs.

If the OVERDRIVE SKIP ROM command is issued when there are multiple responder devices on the SDQ bus. All the responder devices enter Overdrive mode. All subsequent communication addresses a specific device. This procedure is initiated by issuing a reset pulse at overdrive speed followed by a OVERDRIVE Match ROM or Search ROM command sequence. This sequence speeds up the time for the search process. If the OVERDRIVE SKIP ROM command is issued when there are multiple responder devices on the SDQ bus, all the responder devices begin responding to the subsequent memory command resulting in a bus data collision.

6.5.3.7 OVERDRIVE MATCH ROM Command [69h]

The OVERDRIVE MATCH ROM command is used to select a specific responder device when there are multiple responder devices on the SDQ bus, and sets the device into Overdrive mode at the same time. The OVERDRIVE MATCH ROM command can also be used with a single responder device on the bus. The responder device that matches the 64-bit serial ID is selected and available to perform subsequent memory function commands in overdrive speed. Other responder devices that are already in Overdrive mode continue to be in Overdrive mode until the host can bring all the responder devices back to standard speed by issuing a reset pulse of at least 480 µs.

6.5.4 Memory Function Commands

6.5.4.1 Write Scratchpad Command [0Fh]

The Write Scratchpad command, 0Fh, is used to write to the scratchpad. After selecting the target TMF0008 using the ROM command, the host provides the 2-byte address followed by the data. The TMF0008 sets the 5 LSB bits of the 2-byte address as the scratchpad offset address. Additionally, the 5 LSB bits of the E/S register (E[4:0]) are also loaded with the scratchpad offset address. For each subsequent data byte, both the scratchpad offset address and the E/S bits (E[4:0]) are incremented. If the data byte is partial, that data byte is ignored and a error flag called the partial byte flag (PF) is set. This flag is also set if full 2-byte address is not received. This flag is cleared once the device receives a complete 2-byte address.

During the execution of the Write Scratchpad command, the internal CRC generator computes the 16-bit CRC based on the data stream which includes the write scratchpad command (0Fh), the 2-byte address and the data bytes. This CRC is generated using the CRC16 polynomial ($X^{16} + X^{15} + X^2 + 1$) by first clearing the CRC generator. The Write Scratchpad command sequence can be terminated by the host at any time by issuing a RESET command. The host can read the 16-bit CRC generated by the TMF0008 when the scratchpad offset address reaches 11111b.

The TMF0008 memory address range is 0000h to 03D3h, therefore if the host attempts to write beyond the address range, the internal circuitry of the device sets the six most significant address bits to zero as the 2-byte address is shifted into the internal address register. This modified address can be read back from the Read Scratchpad command. If the host issues a Copy Scratchpad command without reading the scratchpad and verifying the address and the data bytes, the memory contents in the scratchpad is not copied to the destination FRAM memory. If the host attempts to write to a memory location that is write-protected, the device copies the data byte from the 2-byte address from the FRAM memory into the scratchpad instead of the data byte written by the host. In a similar manner, if the host attempts to write to a memory location that is EEPROM-protected, the device copies the bit-wise logical AND of the data byte written by the host and the data byte from the 2-byte address from the FRAM memory into the scratchpad.

6.5.4.2 Read Scratchpad Command [AAh]

To read the scratchpad, the host issues the Read Scratchpad command (AAh) and then reads the 2-byte address, the Ending Offset/Data Status byte (E/S) and finally the scratchpad data starting at the scratchpad offset address. The host verifies the address, E/S byte, and the scratchpad data match with the information transmitted during the Write Scratchpad command. The validity of the 2-byte address and the scratchpad data can be verified with the Read Scratchpad command. The host can read the inverted CRC16 once the end of the scratchpad is reached. If the host continues to read after reading the 2 CRC bytes, the host only receives 1s.

6.5.4.3 Copy Scratchpad [55h]

To copy the data from the scratchpad to the FRAM memory, the host can issue the Copy Scratchpad command (55h), followed by the 2-byte address and the E/S byte (referred to as Authorization code) obtained from the Read Scratchpad command. The device copies the scratchpad to the FRAM memory beginning with the target address and ending with the target address plus the scratchpad offset address listed in the E/S byte only if the authorization code matches with the E/S byte, the PF flag is not set and the target address is within in the addressable range. If the host continues to read, the device transmits alternating 0s and 1s. The host can terminate the Copy Scratchpad command sequence by issuing a reset pulse but only after t_{PROG} duration has elapsed. The TMF0008 does not allow the memory copy by resetting the AA flag if the memory pages are

copy-protected pages or if the PF flag is set. This operation can be verified by reading the AA flag bit in the E/S byte through the Read Scratchpad command.

6.5.4.4 Read Memory [F0h]

The host can read the FRAM memory by issuing the Read Memory command (F0h), followed by the 2-byte address. If the host issues an address greater than 03D3h, the device sets the six most significant address bits to zero. The host can then read the data from either the address within the address range or the modified address until address 03D3h is reached. If the host continues to read further, the TMF0008 transmits 1s. The host can terminate the Read Memory command sequence by issuing a reset pulse.

6.5.4.5 Extended Read Memory [A5h]

The Extended Read Memory command works similar to the Read Memory command except for the 2-byte CRC that is transmitted at the end of each memory page. The host can read the FRAM memory by issuing the Extended Read Memory command (A5h), followed by the 2-byte address. If the host issues an address greater than 03D3h, the device sets the six most significant address bits to zero. The host can then read the data from either the address within the address range or the modified address until the end of a 32-byte page. At the end of the memory page, the host reads the 2-byte inverted CRC. If the host continues to read, the host receives the data corresponding to the beginning of next page and so on until the end address 03D3h is reached. If the host continues to read further, the TMF0008 transmits 1s. The host can terminate the Read Memory command sequence by issuing a reset pulse.

6.5.4.6 Memory Command Flow Charts

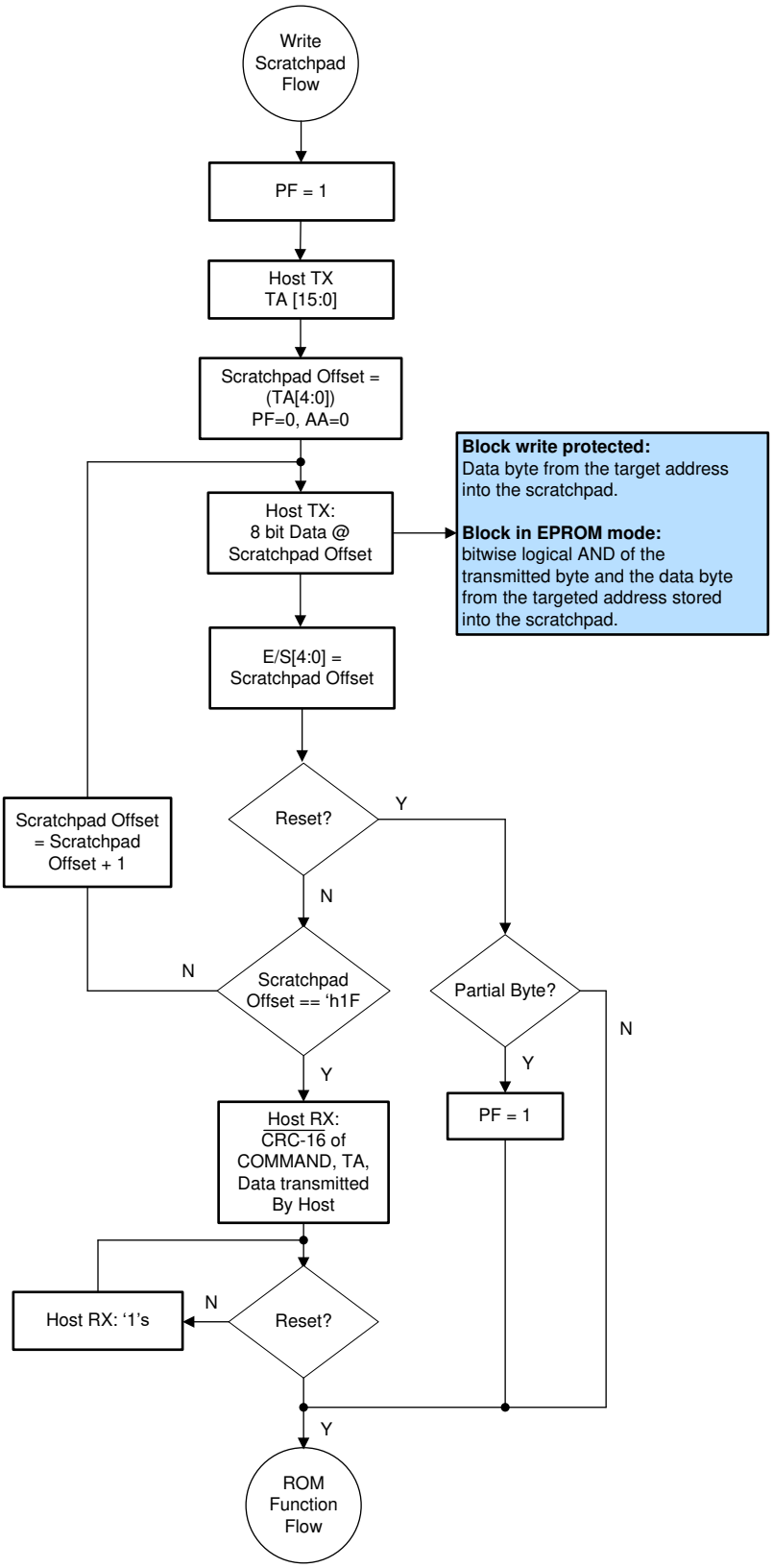


Figure 6-11. Write Scratch Pad Flowchart

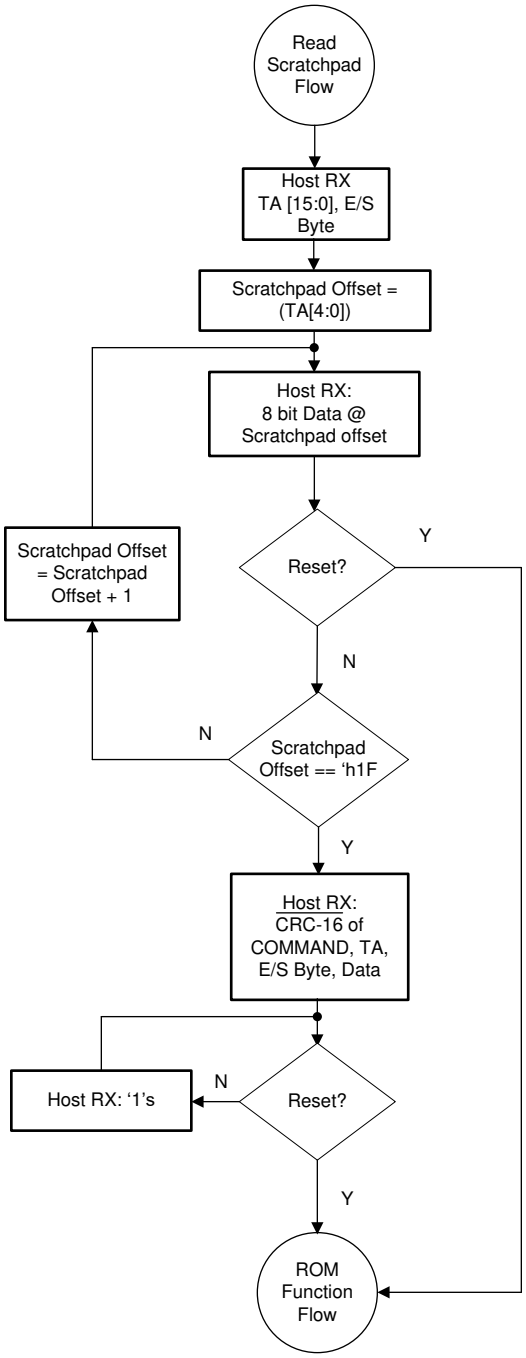


Figure 6-12. Read Scratch Pad Flowchart

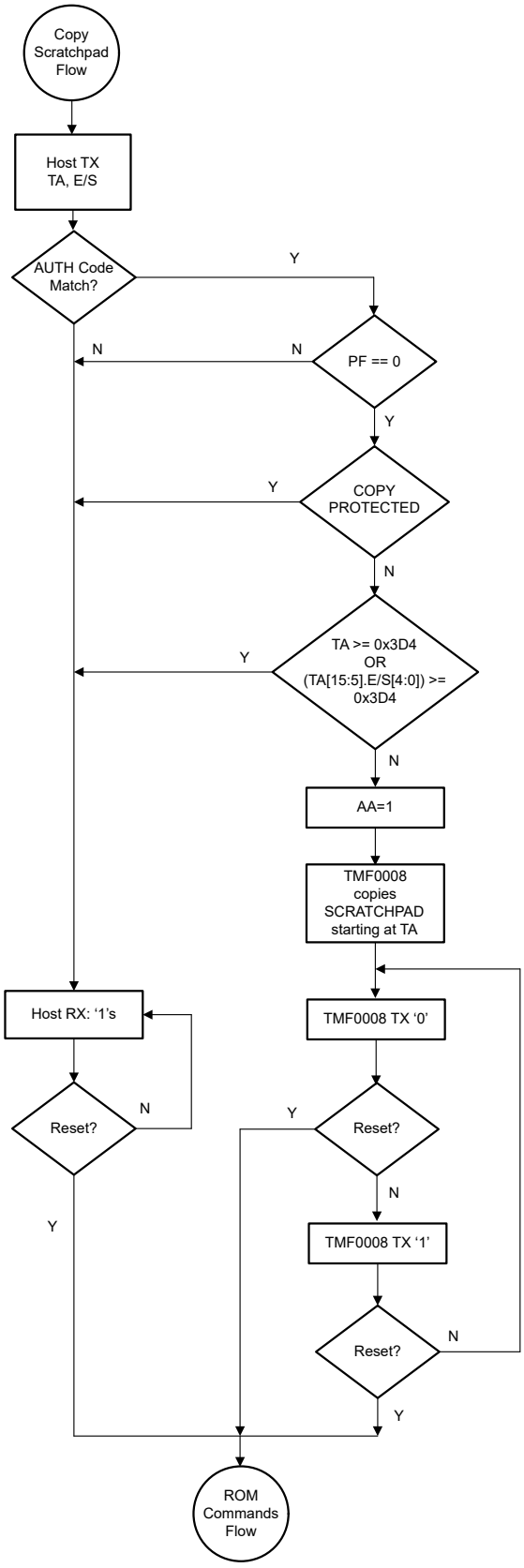


Figure 6-13. Copy Scratch Pad Flowchart

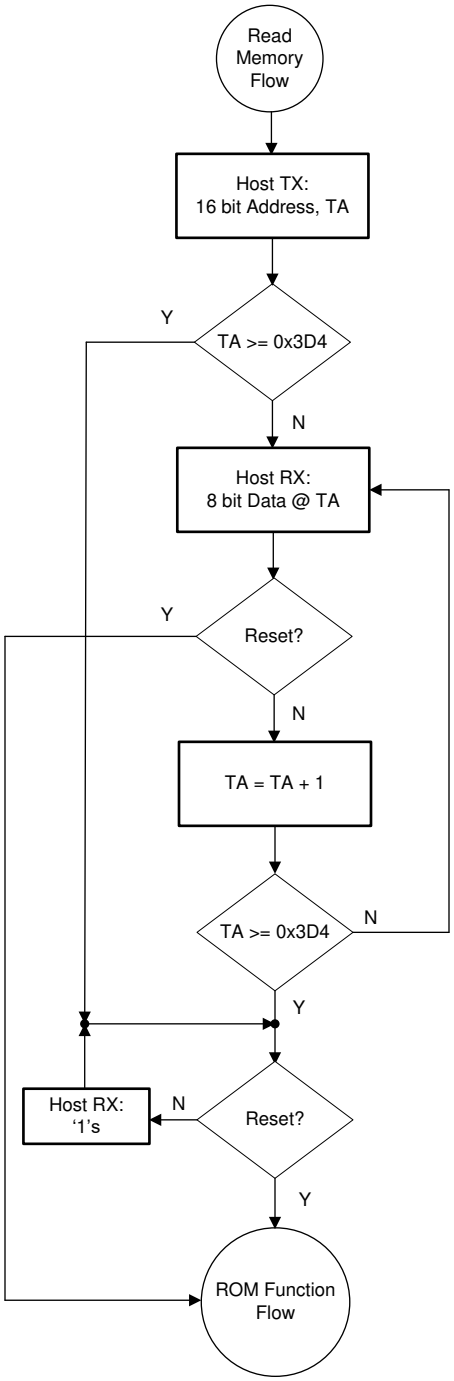


Figure 6-14. Memory Read Flowchart

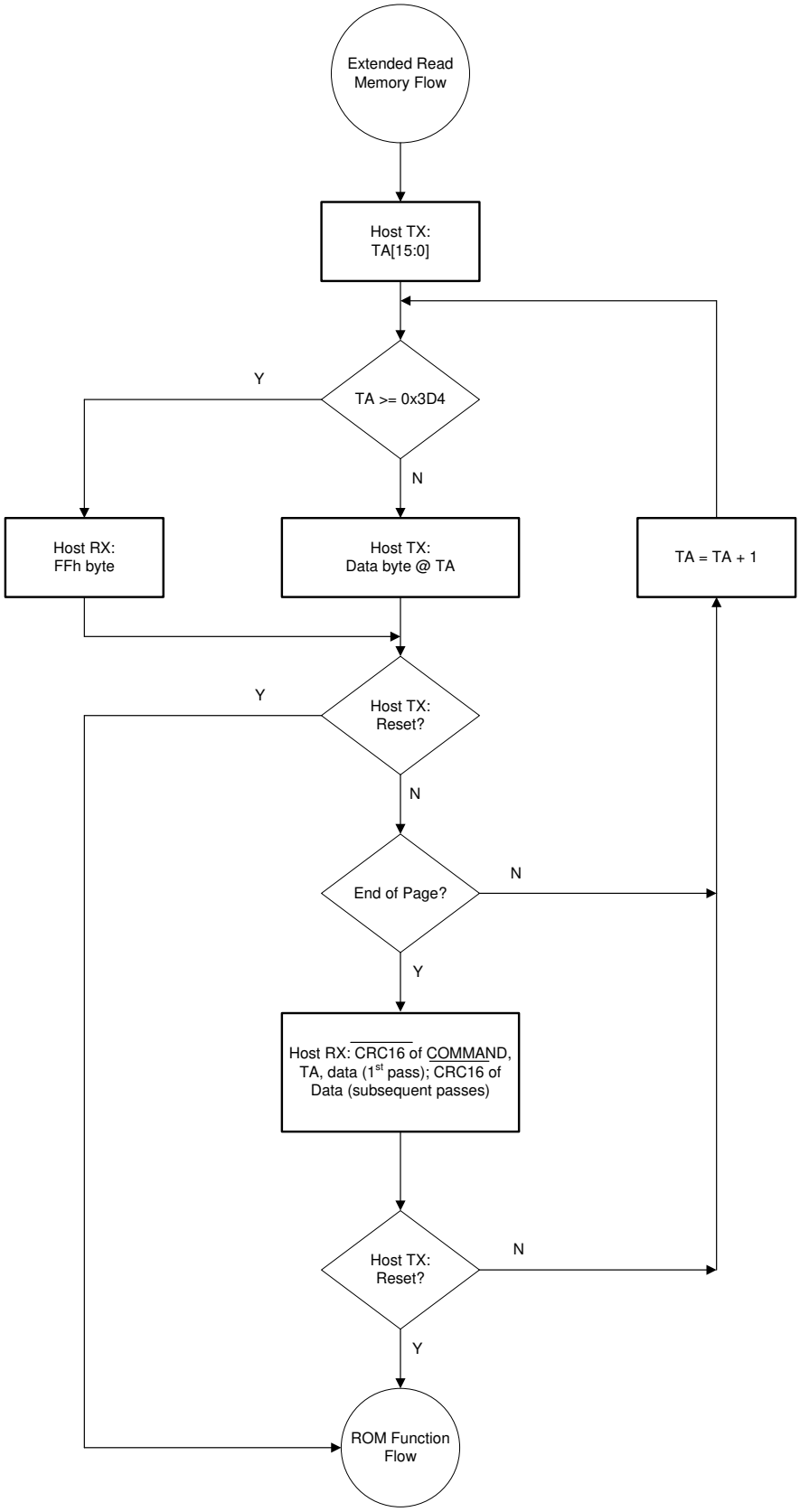


Figure 6-15. Extended Memory Read Flowchart

6.5.5 SDQ Signaling

The single wire communication does not have a reference clock and is critical to adhere to stringent timing protocols to maintain the data integrity. The timing protocol consists of four types of signaling:

1. Reset sequence with reset pulse and presence pulse
2. Write-zero timing sequence
3. Write-one timing sequence
4. Read-data timing sequence

The host initiates the communication by pulling the SDQ line low, except for the presence pulse which is initiated by the responder devices on the SDQ bus. The responder devices can communicate at two different speeds: standard speed and overdrive speed. The responder device by default only communicates at standard speed unless the device is set into the Overdrive mode, in which case the responder device responds to commands issued in the Overdrive timing (fast timing). All the timing waveforms shown below are applicable to both Standard timing and Overdrive timing.

All SDQ signaling begins with initializing the device, followed by the host driving the bus low to write a 1 or 0, or to begin the start frame for a bit read. Figure 6-16 shows the initialization timing, whereas Figure 6-17, Figure 6-18, and Figure 6-19 show that the host initiates each bit by driving the SDQ bus low for the start period, t_{W1L} / t_{W0L} / t_{RL}. After the bit is initiated, either the host continues controlling the bus during a WRITE, or the responder device controls the bus to transfer a 0 bit during a READ.

6.5.5.1 RESET and PRESENCE PULSE

During the reset sequence, if the SDQ bus is driven low for more than 120 µs, the responder devices can be reset. If the SDQ bus is driven low for more than 480 µs, then the responder devices reset and indicate that the devices are ready for communication by responding with a presence pulse. If the TMF0008 is in Overdrive mode and a t_{RSTL} duration of 480 µs or longer is issued by the host, the device exits the Overdrive mode returning to standard speed. If the device is in Overdrive mode and t_{RSTL} is no longer than 80 µs, the device remains in Overdrive mode. If the device is in Overdrive mode and t_{RSTL} is between 80 µs and 480 µs, the device resets, but the communication speed is undetermined.

Figure 6-16 shows the reset pulse initiated by host and Response Presence Pulse initiated by TMF0008 (target).

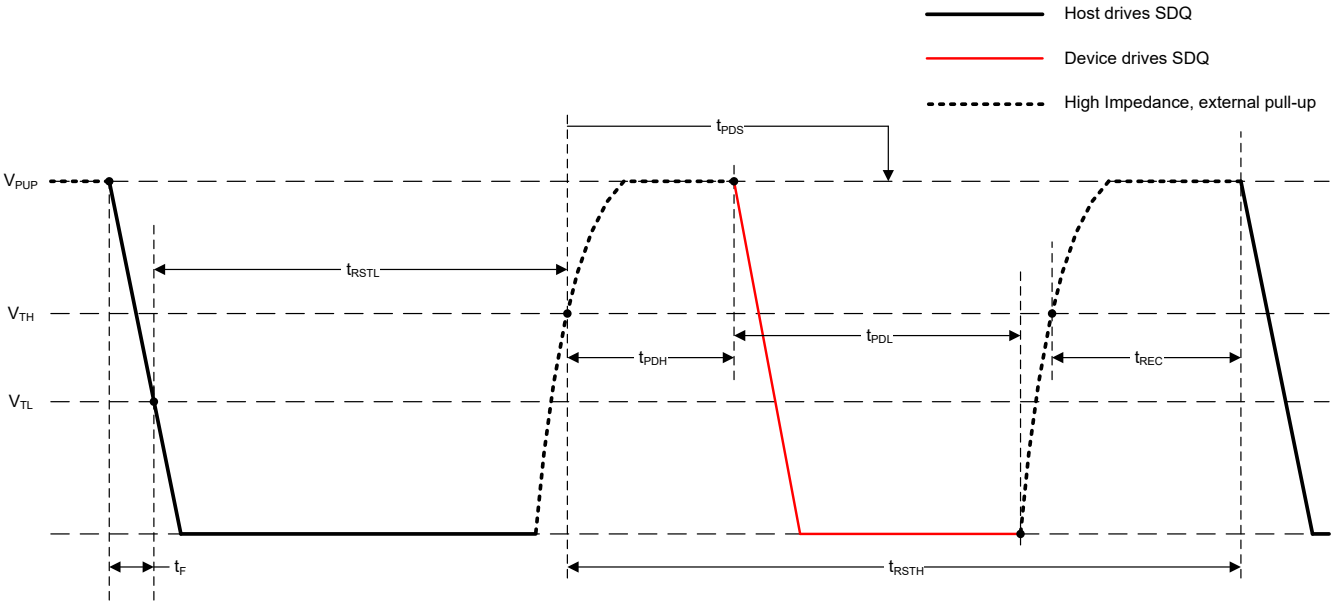


Figure 6-16. Reset Sequence Timing Diagram

6.5.5.2 Write-Read-Time Slots

The single wire interface communication does not have a reference clock. Hence, all communication is performed asynchronously with fixed time slot (t_{SLOT}) and variable pulse width to indicate logic 0 and 1. In idle state, the external pullup resistor holds the line high. Whether all bit communication is a write or a read, both are initiated by the host by driving the data line low and the bit value is decoded as the time for which the data line is held low.

Even though the communication is one bit at a time, the data exchanged between the host and device is performed at byte boundary. Every byte is sent least significant bit first. The device behavior is not verified when incomplete bytes are sent.

The Write-One timing diagram in Figure 6-17 shows that the host initiates the write-one transmission by pulling the SDQ bus low for the $t_F + t_{W1L} - t_\varepsilon$ duration and then releasing the SDQ bus. Similarly, the Write-Zero timing diagram in Figure 6-18 shows that the host initiates the write-zero transmission by the pulling the SDQ bus low for the $t_F + t_{W0L} - t_\varepsilon$ duration and then releasing the SDQ bus. As the voltage on the SDQ bus falls below the threshold V_{TL}, the device starts the internal timing generator that determines when the SDQ line is sampled during a write-time slot to determine whether the bit is 1 or 0. The device samples the SDQ line some time between the max t_{W1L} duration and the min t_{W0L} duration.

The read-data timing diagram in Figure 6-19 shows that the host initiates the transmission of the bit by pulling the SDQ bus low for the $t_F + t_{RL}$ duration. The device then responds by either driving the SDQ bus low to transmit a READ 0 or releasing the SDQ bus to transmit a READ 1. The host must factor the rise time due to the pullup resistor and bus capacitance, to determine the sampling window to sample the bit level sent by the device or driving the next read bit time slot.

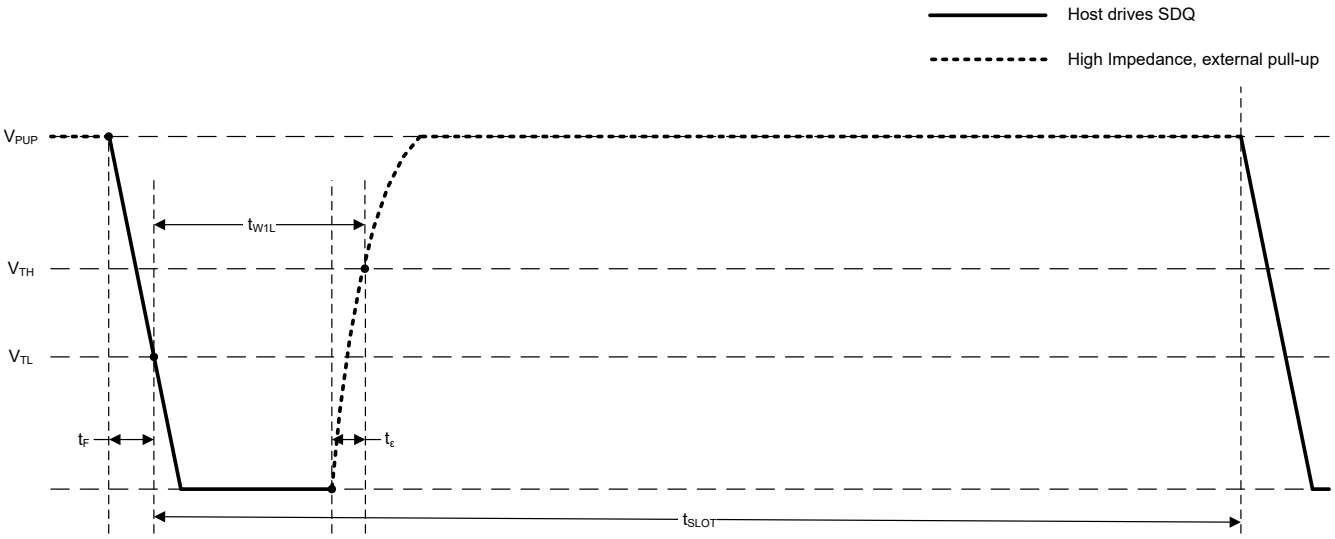


Figure 6-17. Write-One Timing Diagram

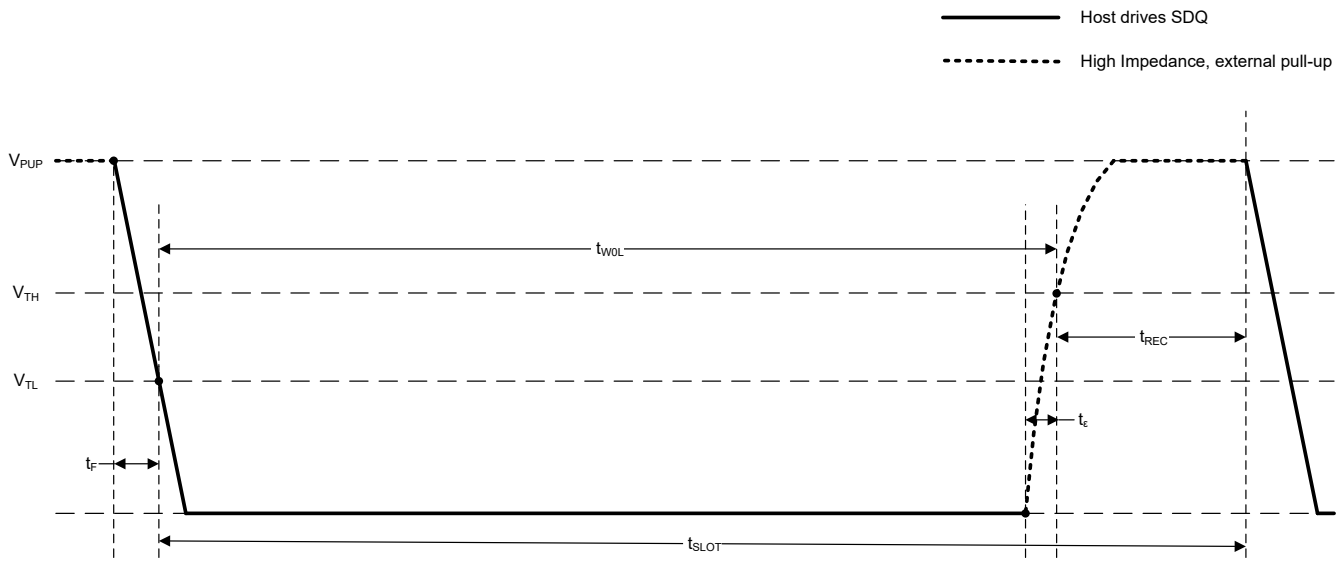


Figure 6-18. Write-Zero Timing Diagram

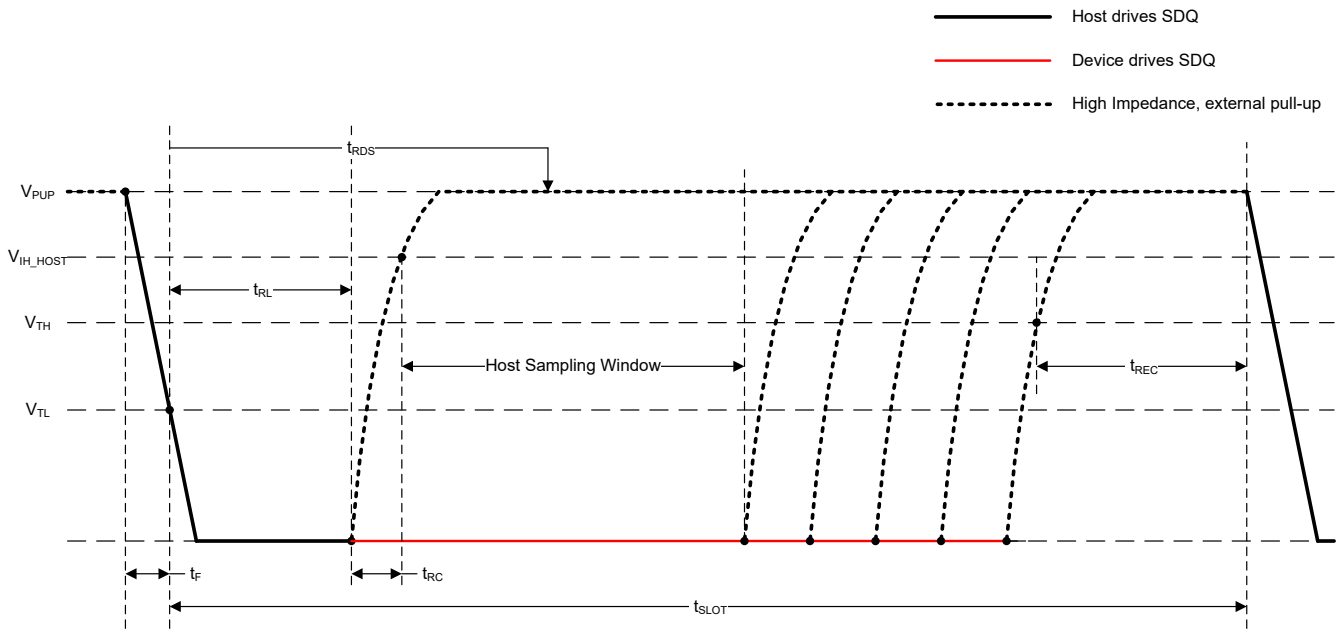


Figure 6-19. Read-Data Timing Diagram

6.5.6 IDLE

If the SDQ bus is high, the bus is in the IDLE state. Bus transactions can be suspended by leaving the SDQ bus in IDLE. Bus transactions can resume at any time from the IDLE state.

6.5.7 CRC Generation

The TMF0008 has an 8-bit CRC stored in the most significant byte of the 64-bit ROM. The bus host can compute a CRC value from the first 56 bits of the 64-bit ROM and compare these bits to the value stored within the TMF0008 to determine if the ROM data has been received error-free by the bus host. The equivalent polynomial function of this CRC is: $X^8 + X^5 + X^4 + 1$.

The comparison of CRC values and decision to continue with an operation are determined entirely by the bus host. No circuitry on the TMF0008 prevents a command sequence from proceeding if the CRC stored in or

calculated by the TMF0008 does not match the value generated by the bus host. Proper use of the CRC can result in a communication channel with a high level of integrity.

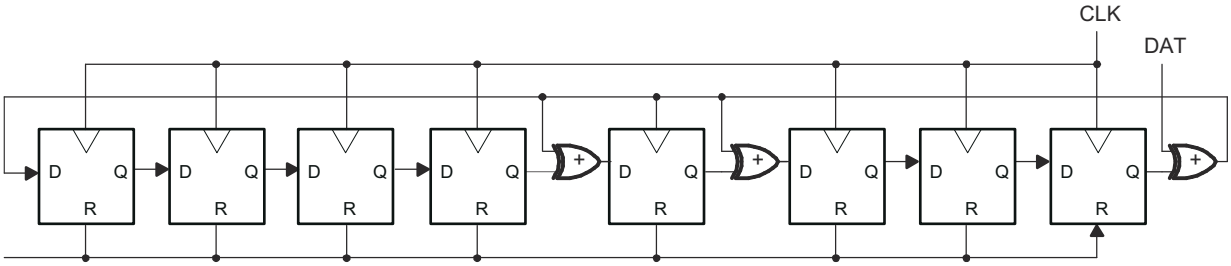


Figure 6-20. 8-Bit CRC Generator Circuit ($X^8 + X^5 + X^4 + 1$)

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

A typical application consists of a microcontroller configured as the SDQ communication host device and the TMF0008 being the SDQ responder device. The host and responder have open drain functionality for which an external pull-up resistor (typically 500Ω) is required and connected to a pullup voltage in the range of 3.13V to 5.25V.

7.2 Typical Application

Avoid additional capacitances on the SDQ bus. Any capacitance greater than C_{CABLE} can result in communication failure. Do not add decoupling or bypass capacitors to the SDQ line.

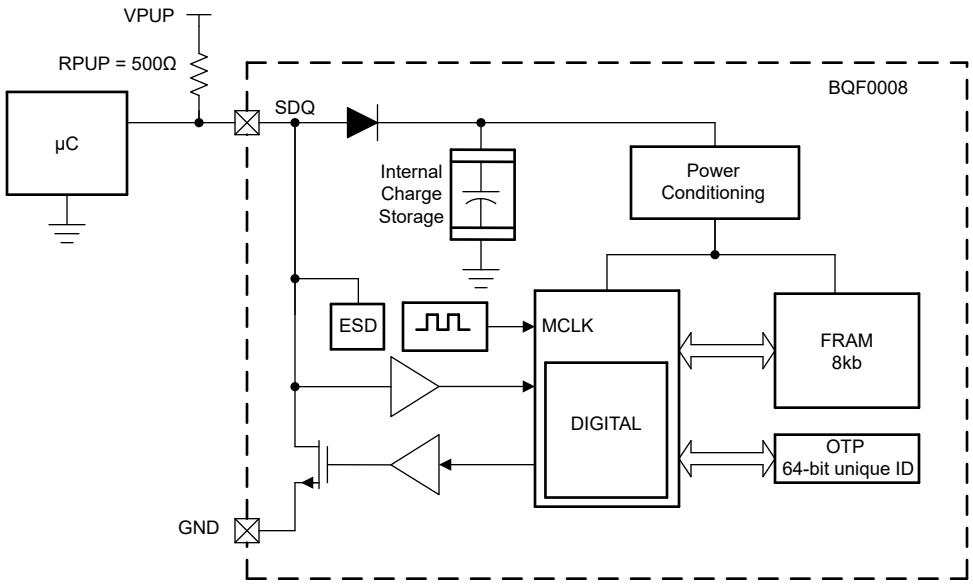


Figure 7-1. Typical Application Circuit

7.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Pullup voltage	3.13V to 5.25V
Operating free-air temperature	–10℃ to 85℃
Pullup resistor	500Ω

7.2.2 Detailed Design Procedure

Implementing the SDQ host via bit-banging over GPIO is possible. In this case, consider additional error checking for the reset routine of the TMF0008 to verify that the responder is operating as expected on the bus.

Whenever the host sends a reset, the responder devices acknowledge the reset with a presence pulse. The host must confirm, before the presence pulse, that the bus has been released and returned to a high level, indicating that nothing is holding the bus unexpectedly low. As the minimum t_{PDH} is 15µs, having the host look for a logic high on the bus 10µs after releasing the bus at the end of the reset is sufficient to confirm the bus is released for the responder devices to acknowledge.

7.2.3 Application Curves

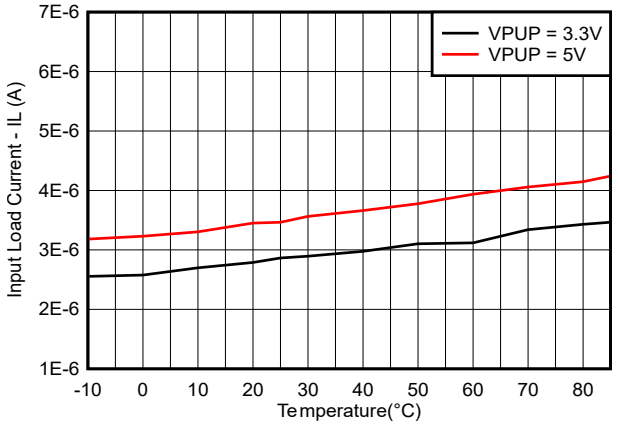


Figure 7-2. Input Load Current (I_L) vs Temperature (Standard Speed)

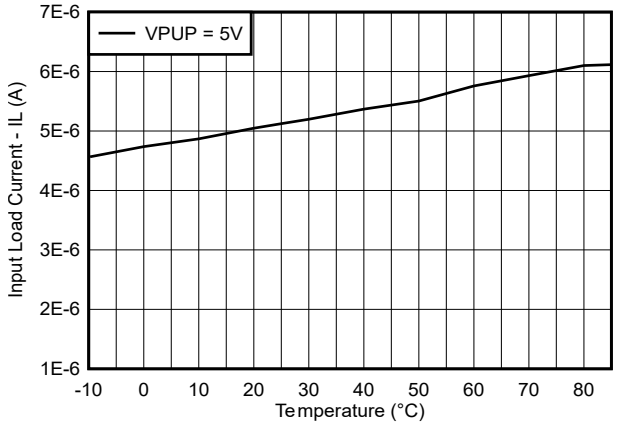


Figure 7-3. Input Load Current (I_L) vs Temperature (Overdrive Speed)

7.3 Power Supply Recommendations

The TMF0008 is a low-power device that only needs to be turned on when communicating. The device power comes from the voltage supply that is used for digital I/O in the system. A dedicated VCC pin does not exist in the device. The device obtains power from the SDQ communication input which can be sustained during normal communication activity. Do not install any capacitors on the SDQ line.

The ramp time of the SDQ voltage when power is initially applied can be slow due to current limiting from the source. Ramp times greater than 200µs can cause undesired bouncing of the POR circuit and result in the device not generating a presence pulse. To account for this undesired effect on the device, a best practice for the communication host is to issue a “hard” reset to the device by pulling down the SDQ line for >5ms and then releasing the SDQ bus before issuing the reset pulse that is approximately 480µs long.

Figure 7-4 illustrates the best practice for dealing with initial power-on ramps.

1. Initial power-on ramps can be long in duration.
2. The host issues a “hard” reset of > 5ms, which resets the device
3. TMF0008 responds to the hard reset by issuing a presence pulse.
4. A "soft" reset of approximately 480µs can be applied after the previous presence pulse.
5. TMF0008 responds to the soft reset by issuing a presence pulse.

Figure 7-4. Power-Up Best Practice

7.4 Layout

7.4.1 Layout Guidelines

The TMF0008 only has one signal (SDQ). Routing the signal trace directly from the SDQ pin of TMF0008 to the external connector of the application system or to host SDQ host device is advised. Shield the signal trace properly with a parallel ground plane as shown in Figure 7-5. If a ground plane is not available to the TMF0008, connect GND with a large trace surrounding most of the device and have the SDQ trace parallel with GND back to the host.

7.4.2 Layout Example

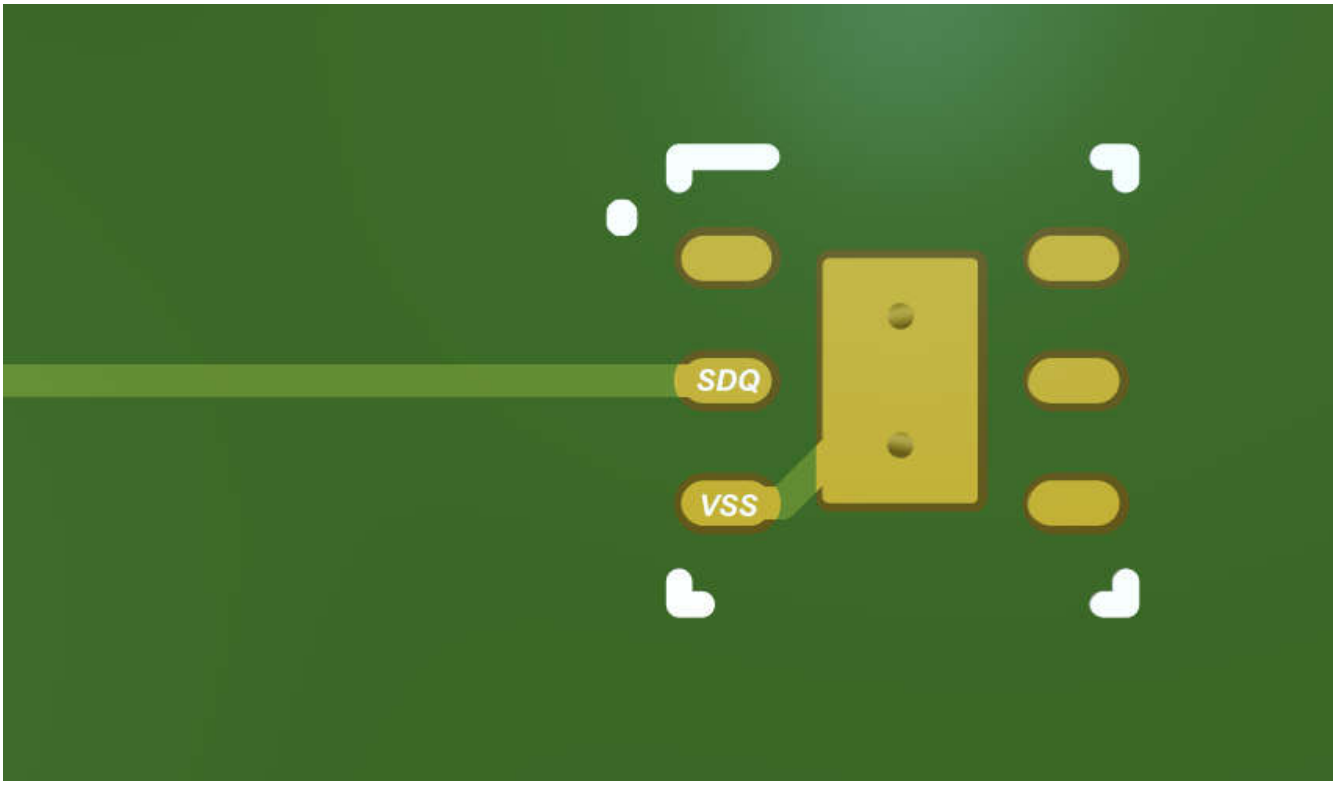


Figure 7-5. Example Board Layout

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

SDQ™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMF0008LP	Active	Production	TO-92 (LP) | 3	1000 | LARGE T&R	Yes	SN	N/A for Pkg Type	-10 to 85	TMF0008
TMF0008PSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-10 to 85	TMF0008

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

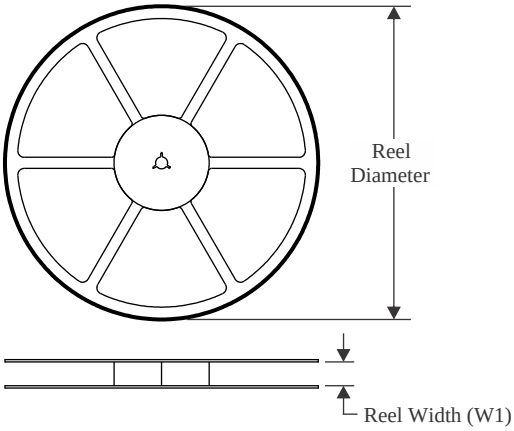
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

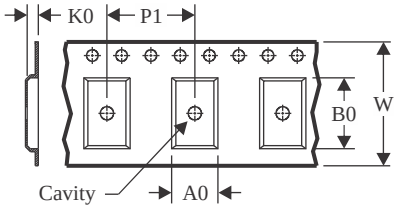
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

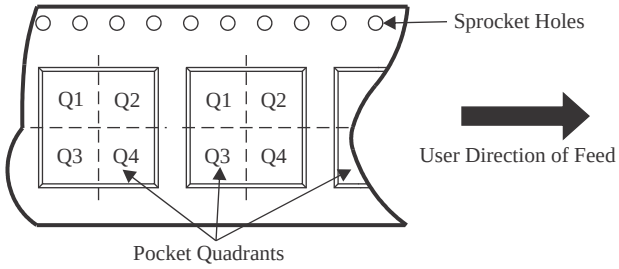


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

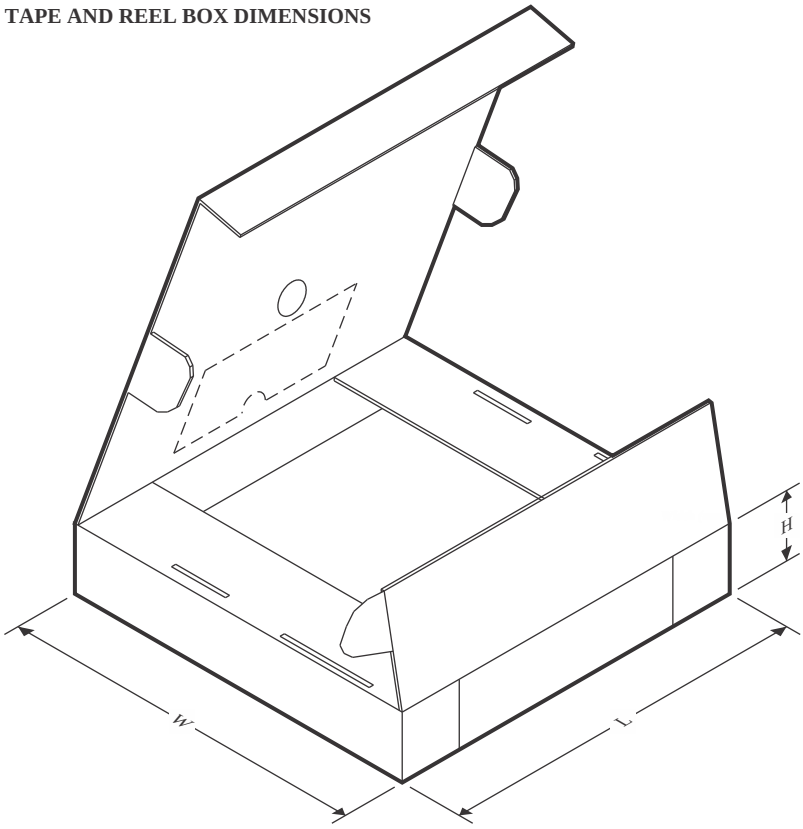
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMF0008PSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

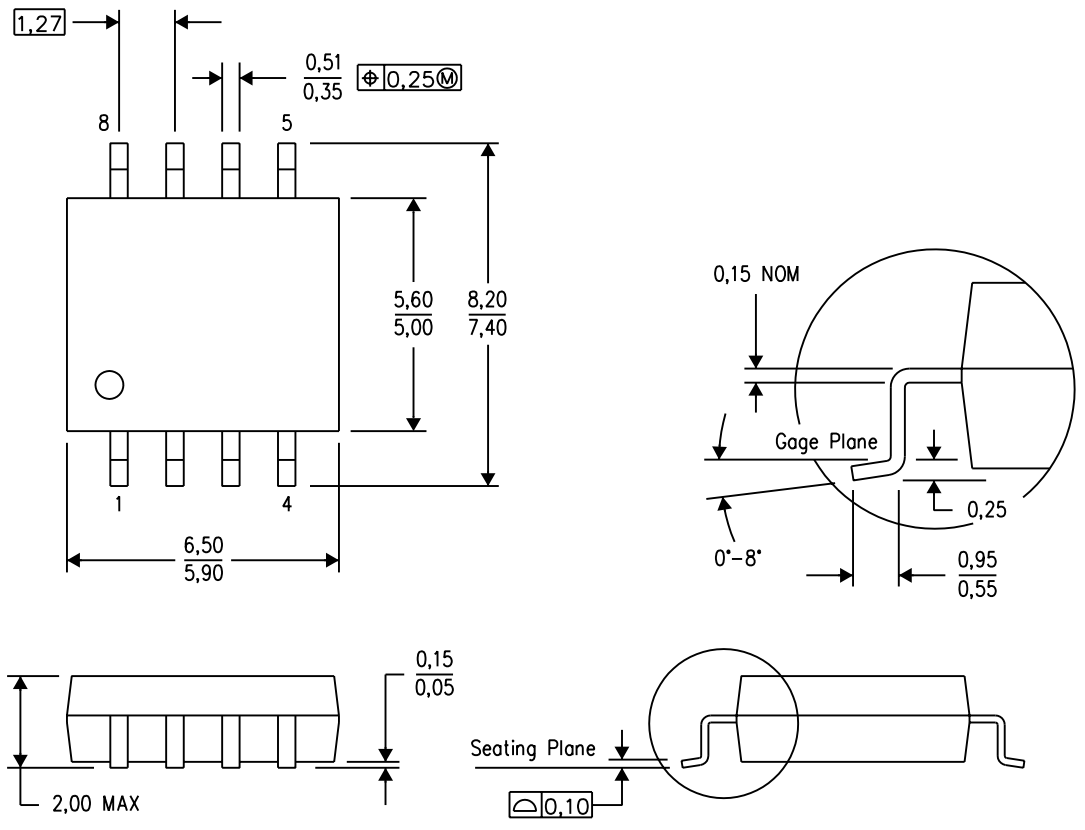


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMF0008PSR	SO	PS	8	2000	353.0	353.0	32.0

MECHANICAL DATA

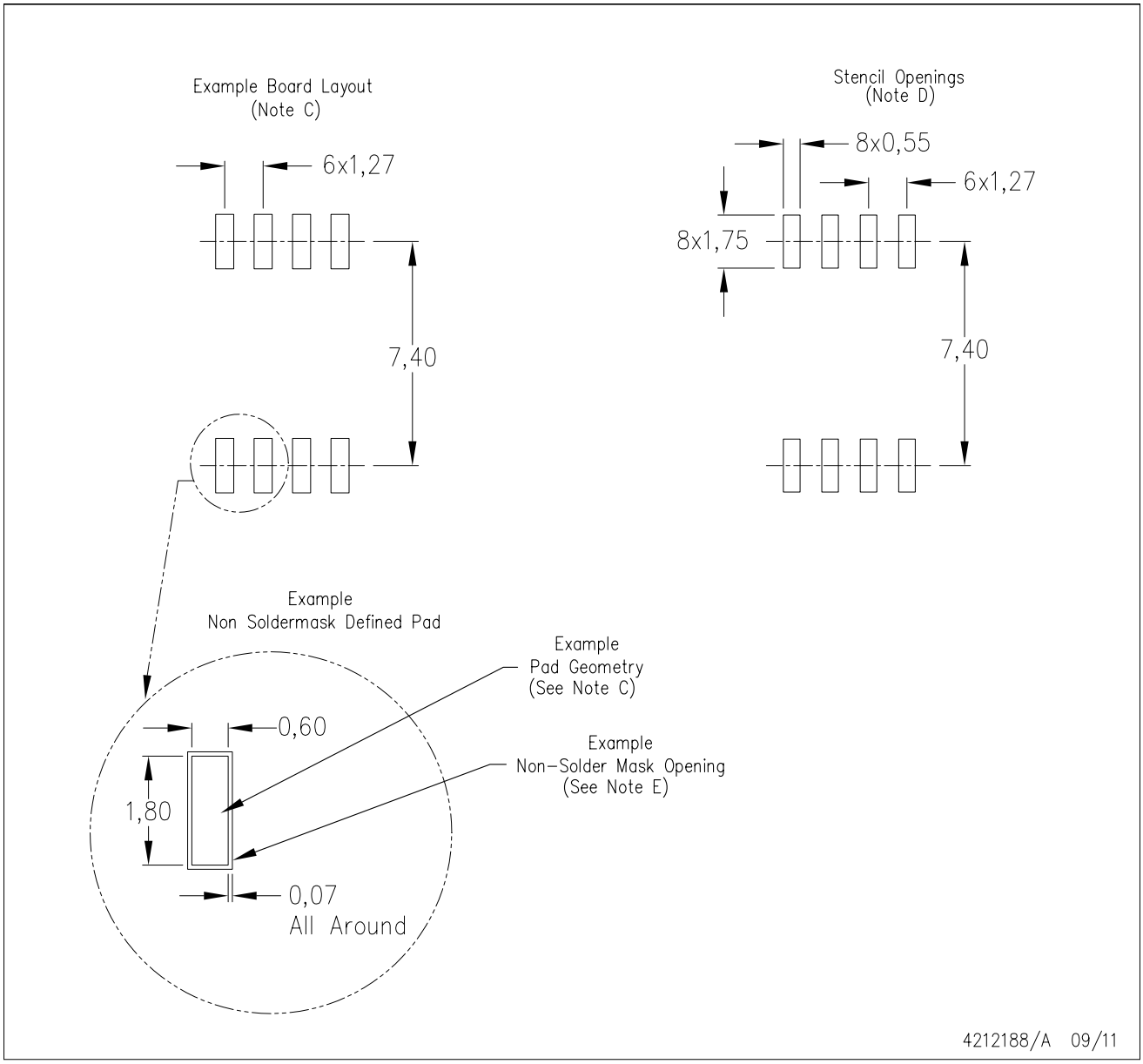
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



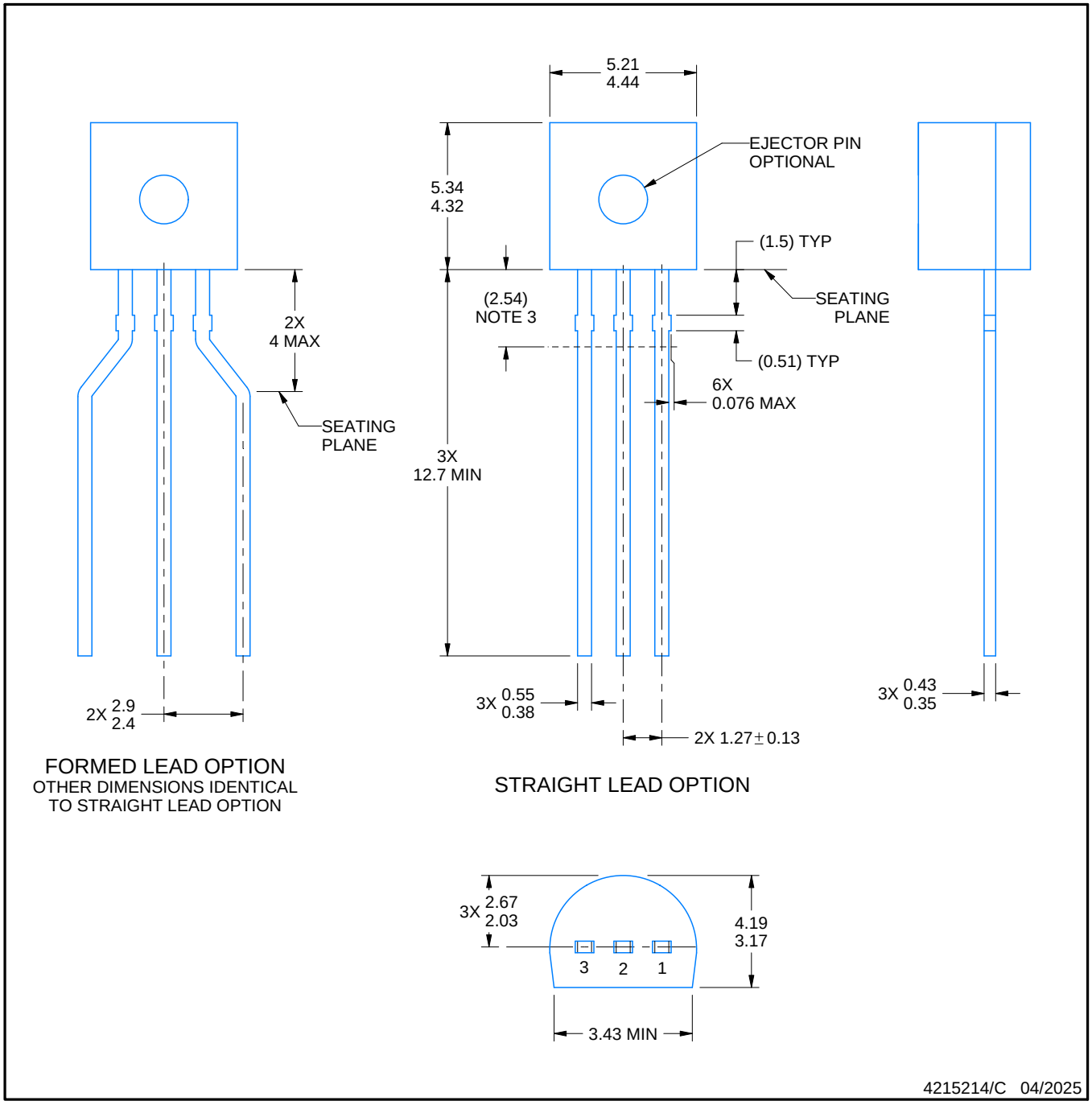
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

LP0003A

PACKAGE OUTLINE

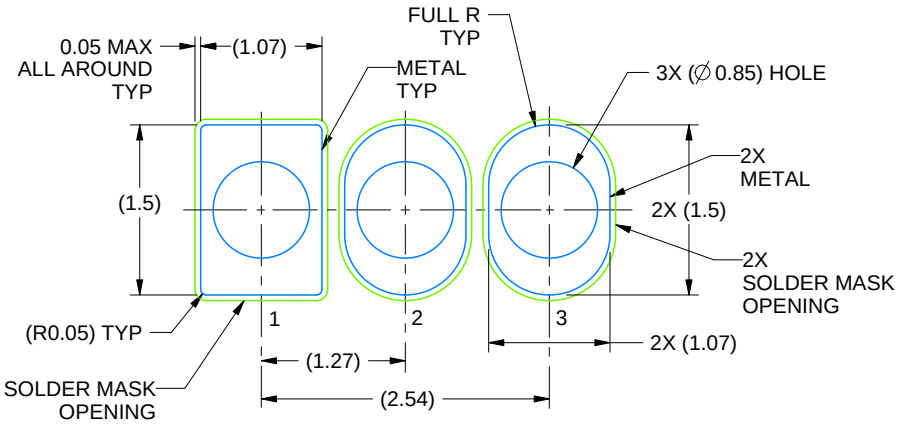
TO-92 - 5.34 mm max height

TO-92

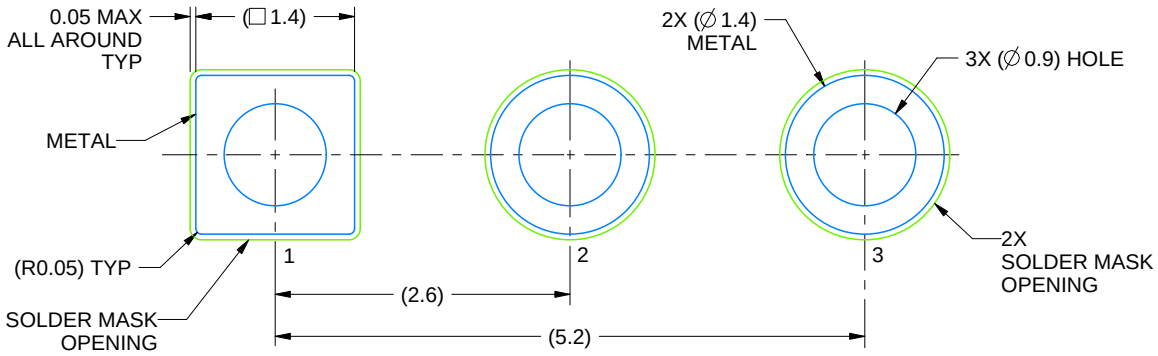


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



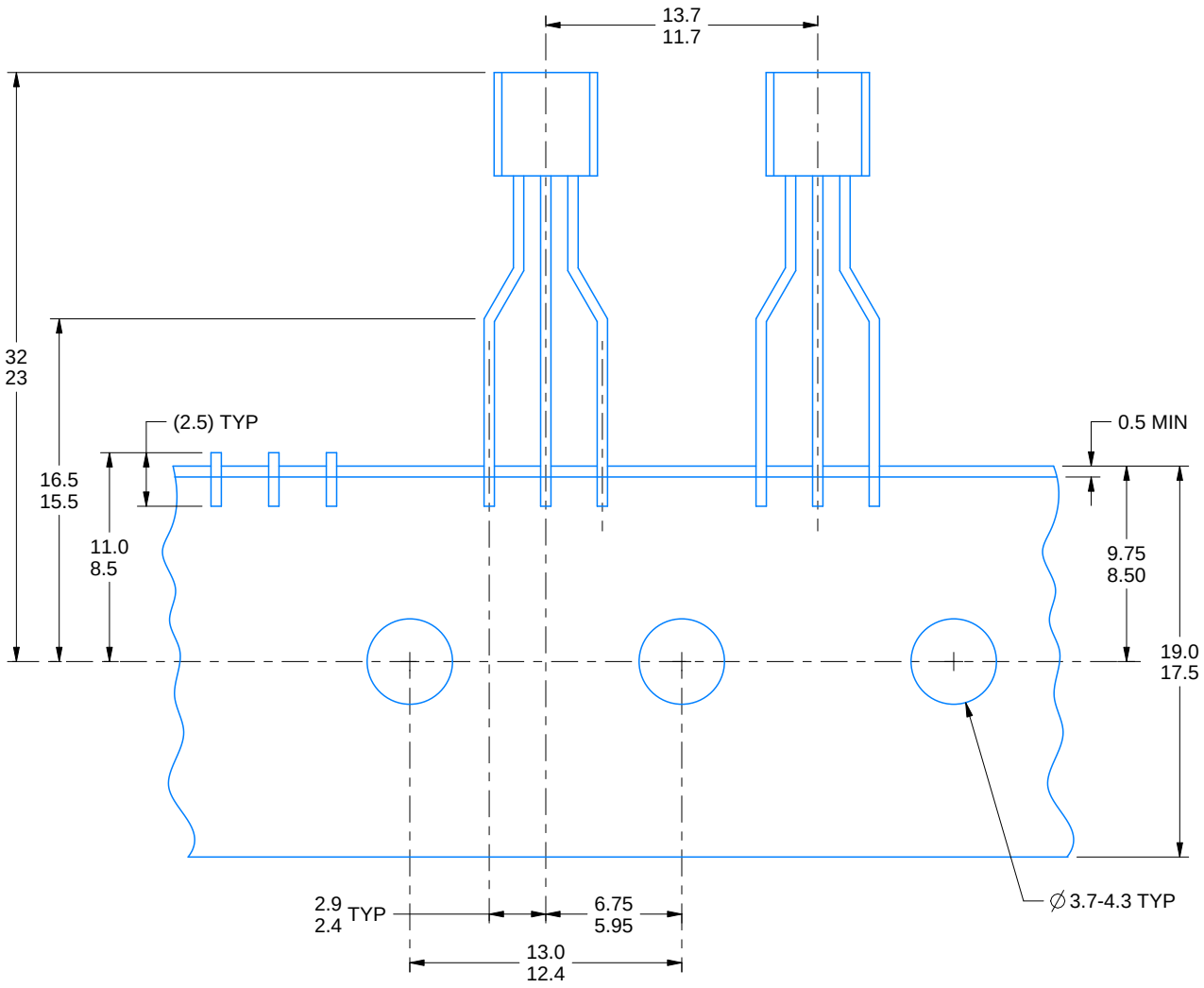
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/C 04/2025

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

4215214/C 04/2025

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025