TMUX48xx ±15V Beyond the Supply, 1:1 2-Channel, 2:1 1-Channel, Power-Off Protection Switch, with 0.16Ω Ron, 1.2V and 1.8V Compatible Logic

1 Features

- Supply range: 1.8V to 5.5V
- Beyond the supply signal range: -15V to 15V
- High current support: 1.1A (maximum)
- Ultra-low on-resistance: 0.16Ω
- Low on-resistance flatness: 0.1mΩ typ
- Low THD+N: 0.001% (-100dB)
- –40°C to +125°C operating temperature
- Power-Off Protection
- 1.8V logic compatible at 5V V_{DD}
- 1.2V logic compatible at 1.8V V_{DD}
- Integrated Pull-Down Resistor on Logic Pins
- Fail-safe logic
- Break-before-make switching

2 Applications

- Land mobile radios
- Defense radios
- Audio input or output switching
- Ultrasonic gas flow transmitters
- Analog input modules
- Industrial module detection

3 Description

The TMUX48xx is a complementary metal-oxide semiconductor (CMOS) multiplexer with 2 configurations available: 1:1, single-pole, single-throw (SPST) 2-channel (TMUX4821) and 2:1, single-pole, double-throw (SPDT) 1-channel (TMUX4819). This device works with a single supply (1.8V to 5.5V), but can pass bidirectional analog and digital signals beyond the supply from -15V to 15V.

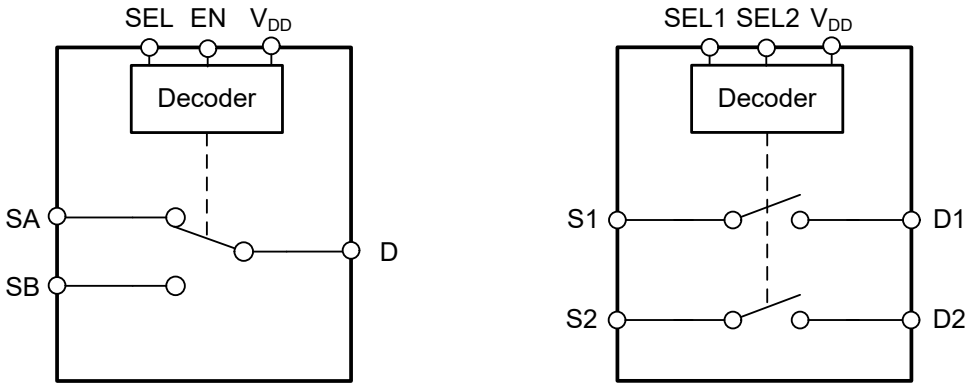
The TMUX48xx also features bidirectional powered off protection up to ±15V, which isolates the switch even when there is no supply voltage present (V_{DD} = 0V). Without this protection feature, any voltage on the switch can back-power the supply rail through an internal ESD diode and cause potential damage to the rest of the system.

With 0.001% THD+N and 1mΩ R_{ON}-flatness, the TMUX48xx is an excellent choice for passing precision analog and audio signals without adding distortion.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMUX4819 TMUX4821	DSG (SON, 8)	2mm × 2mm

(1) For more information, see Section 19.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TMUX4819 and TMUX4821 Block Diagram

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4 Pin Configuration and Functions

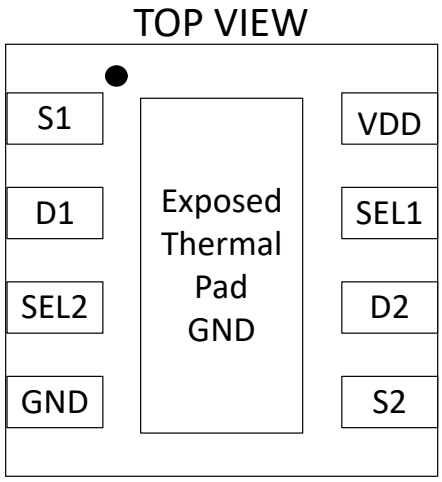


Figure 4-1. DSG Package TMUX4821 (1:1 2ch)

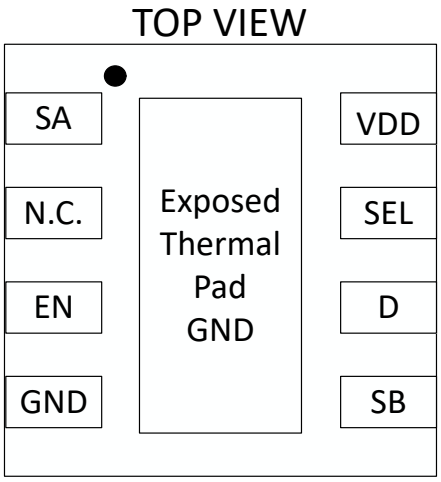


Figure 4-2. DSG Package TMUX4819 (2:1 1ch)

Pin Functions

PIN			TYPE[1]	DESCRIPTION
NO.	TMUX4821	TMUX4819		
1	S1	SA	I/O	Source pin 1 OR A. Can be an input or output.
2	D1	N.C	I/O	Drain pin 1. Can be an input or output. For N.C. connect pin to GND to keep pin in a known state (Not internally connected).
3	SEL2	EN	I	Logic control input. Controls the switch connection
4	GND	GND	GND	Ground (0V) reference
5	S2	SB	I/O	Source pin 2 OR B. Can be an input or output.
6	D2	D	I/O	Drain pin 2 OR Drain. Can be an input or output.
7	SEL1	SEL	I	Logic control input. Controls the switch connection.
8	VDD	VDD	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between VDD and GND. Controls the switch connection as provided in Table 15-1
Thermal Pad	GND	GND	GND	Ground (0V) reference

(1) I = input, I/O = input or output, GND = ground, P = power.

5 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1] [2]

		MIN	MAX	UNIT
V_{DD} to GND	Supply voltage	-0.5	6	V
V_{SEL} to GND	Logic control input pin voltage	-0.5	6	V
V_S or V_D to GND	Source or drain voltage (Sx, Dx) to ground	-17	17	V
V_S to V_D or V_S	Source to drain or source (same channel)[4]	-18	18	V
	Source to drain or source (seperate channel)[3]	-24	24	V
I_{SEL}	Logic control input pin current	-30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, Dx)		I_{DC} + 10 %[5]	mA
T_A	Ambient temperature	-55	150	°C
T_{stg}	Storage temperature	-65	150	°C

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
T_J	Junction temperature		150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(4) Maximum voltage between source and drain pins within the same channel. For example: S1A to D1 or S1A to S1B
(5) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

6 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7 Thermal Information

THERMAL METRIC[1]		TMUX48xx DSG 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	69.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	84.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	35.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	14.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Positive power supply voltage	1.8		5.5	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	-15		15	V
V_{SEL}	Address/Select pin voltage	0		5.5	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)			I_{DC} (1)	A
T_A	Ambient temperature	-40		125	°C

(1) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

9 Source or Drain Continuous Current

V_{DD} = 3.3V, GND = 0V (unless otherwise noted)

CONTINUOUS CURRENT PER CHANNEL (I_{DC})				
PACKAGE	25°C	85°C	125°C	UNIT
DSG	1.1	0.87	0.27	A

10 Source or Drain RMS Current

V_{DD} = 3.3V, GND = 0V (unless otherwise noted)

RMS CURRENT PER CHANNEL (I_{RMS})				
PACKAGE	25°C	85°C	125°C	UNIT
DSG	1.1	1.1	0.54	A

11 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)
Typical at V_{DD} = 3.3 V T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_{DD} = 2.5 V to 5.5 V V_S = –15 V to +15 V I_D = –100 mA	25°C		0.16	0.20	Ω
			–40°C to +85°C			0.225	Ω
			–40°C to +125°C			0.3	Ω
R_{ON}	On-resistance	V_{DD} = 1.8 V to 2.5 V V_S = –15 V to +15 V I_D = –100 mA	25°C		0.16	0.25	Ω
			–40°C to +85°C			0.26	Ω
			–40°C to +125°C			0.3	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_{DD} = 2.5 V to 5.5 V V_S = –15 V to +15 V I_D = –100 mA	25°C		0.0008	0.03	Ω
			–40°C to +85°C			0.03	Ω
			–40°C to +125°C			0.05	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_{DD} = 1.8 V to 2.5 V V_S = –15 V to +15 V I_D = –100 mA	25°C		0.008	0.035	Ω
			–40°C to +85°C			0.04	Ω
			–40°C to +125°C			0.06	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_{DD} = 2.5 V to 5.5 V V_S = –15 V to +15 V I_D = –100 mA	25°C		0.0001	0.01	Ω
			–40°C to +85°C			0.05	Ω
			–40°C to +125°C			0.07	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_{DD} = 1.8 V to 2.5 V V_S = –15 V to +15 V I_D = –100 mA	25°C		0.0004	0.015	Ω
			–40°C to +85°C			0.07	Ω
			–40°C to +125°C			0.09	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –100 mA	–40°C to +125°C		0.00065		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	Switch state is off V_S = ±15 V / 0 V V_D = 0 V / ±15 V	25°C		0.001		uA
			–40°C to +85°C	-0.1		0.1	uA
			–40°C to +125°C	-1		1	uA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	Switch state is on V_S = V_D = ±15 V	25°C		0.001		uA
			–40°C to +85°C	-0.1		0.1	uA
			–40°C to +125°C	-1		1	uA
$I_{S(POFF)}$	Source powered-off leakage current[1]	V_{DD} = 0 V V_S = ±15 V / 0 V V_D = 0 V / ± 15 V	25°C		0.02		uA
			–40°C to +85°C	-0.1		0.1	uA
			–40°C to +125°C	-2		2	uA
$I_{D(POFF)}$	Drain powered-off leakage current[1]	V_{DD} = 0 V V_S = ±15 V / 0 V V_D = 0 V / ± 15 V	25°C		0.02		uA
			–40°C to +85°C	-0.1		0.1	uA
			–40°C to +125°C	-2		2	uA

Over operating free-air temperature range (unless otherwise noted)
Typical at V_{DD} = 3.3 V T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high	V_{DD} = 5.5 V	–40°C to +125°C	1.2		5.5	V
		V_{DD} = 3.3 V		1.1		5.5	
		V_{DD} = 1.8 V		0.8		5.5	
V_{IL}	Logic voltage low	V_{DD} = 5.5 V		0		0.6	
		V_{DD} = 3.3 V		0		0.6	
		V_{DD} = 1.8 V		0		0.42	
I_{IH}	Input leakage current		–40°C to +125°C		1	1.5	µA
I_{IL}	Input leakage current		–40°C to +125°C	-10	-1		nA
C_{IN}	Logic input capacitance		–40°C to +125°C		5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V, 5 V, or V_{DD}	25°C		55	125	µA
			–40°C to +85°C			130	µA
			–40°C to +125°C			140	µA

(1) When V_S is at a voltage potential, V_D is 0 V, or when V_S is 0 V, V_D is at a voltage potential.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

12 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)
Typical at V_{DD} = 3.3 V T_A = 25°C (unless otherwise noted)

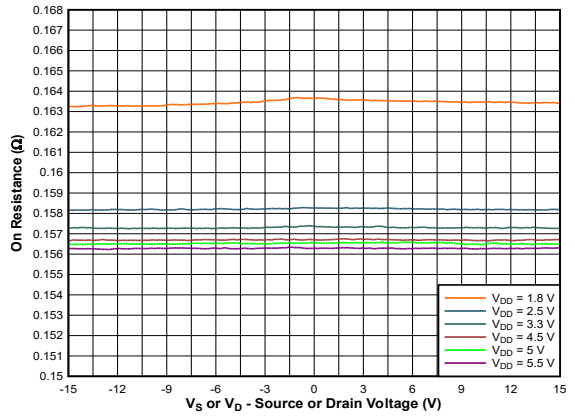
PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_{DD} = 2.5 V to 5.5 V V_S = 3.3 V R_L = 50 Ω, C_L = 35 pF	25°C		80	185	us
			–40°C to +85°C			220	
			–40°C to +125°C			220	
		V_{DD} = 1.8 V to 2.5 V V_S = 3.3 V R_L = 50 Ω, C_L = 35 pF	25°C		10	340	
			–40°C to +85°C			490	
			–40°C to +125°C			490	
t_{BBM}	Break-before-make time delay	V_{DD} = 2.5 V to 5.5 V V_S = 3.3 V R_L = 50 Ω, C_L = 35 pF	25°C	40		300	us
			–40°C to +85°C	40		300	
			–40°C to +125°C	40		300	
		V_{DD} = 1.8 V to 2.5 V V_S = 3.3 V R_L = 50 Ω, C_L = 35 pF	25°C	40		420	
			–40°C to +85°C	40		490	
			–40°C to +125°C	40		490	
t_{ON}	Turn-on time from control input	V_S = 3.3 V R_L = 50 Ω, C_L = 35 pF	25°C		155	300	us
			–40°C to +85°C			400	us
			–40°C to +125°C			450	us
t_{OFF}	Turn-off time from control input	V_S = 3.3 V R_L = 50 Ω, C_L = 35 pF	25°C		14		us
			–40°C to +85°C		14		us
			–40°C to +125°C		14		us
$t_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 50 Ω, C_L = 35 pF	25°C		175		us
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 100 pF	25°C		5		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 100 kHz	25°C		-50		dB
X_{TALK}	Crosstalk - 4821	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 100 kHz	25°C		-100		dB
	Crosstalk - 4819	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 100 kHz	25°C		-55		
BW	–3dB Bandwidth (Small signal)	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V,	25°C		100		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		-0.01		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} R_L = 32 Ω , C_L = 5 pF, f = 20 kHz	25°C		-100		dB
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		70		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0 V, f = 1 MHz	25°C		40		pF

Over operating free-air temperature range (unless otherwise noted)
Typical at V_{DD} = 3.3 V T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 0.5 V, V_{BIAS} = 0 V R_L = 600 Ω f = 20 Hz to 20 kHz	25°C		-107		dB
			–40°C to +85°C		-105		
			–40°C to +125°C		-105		
		V_{PP} = 0.5 V, V_{BIAS} = 0 V R_L = 32 Ω f = 20 Hz to 20 kHz	25°C		-102		
			–40°C to +85°C		-102		
			–40°C to +125°C		-102		

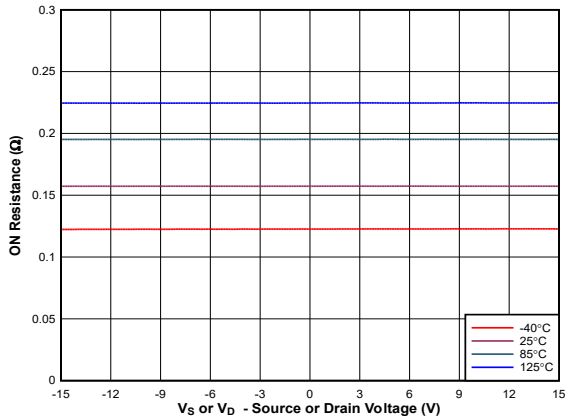
13 Typical Characteristics

at T_A = 25°C (unless otherwise noted)



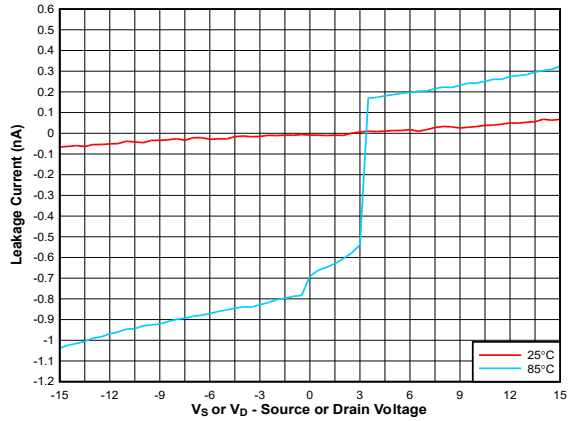
T_A = 25°C

Figure 13-1. On-Resistance vs Source or Drain Voltage



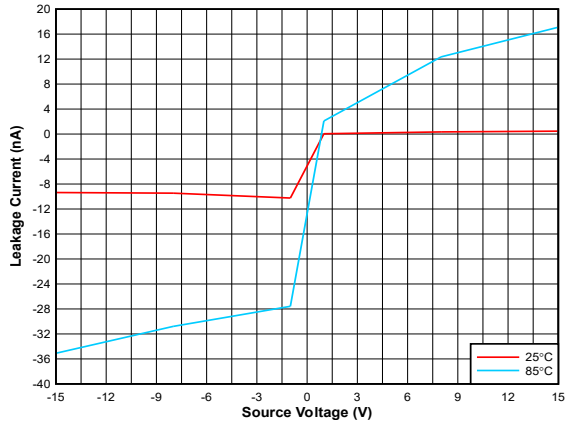
V_{DD} = 3.3V

Figure 13-2. On-Resistance vs Source or Drain Voltage Across Temperature



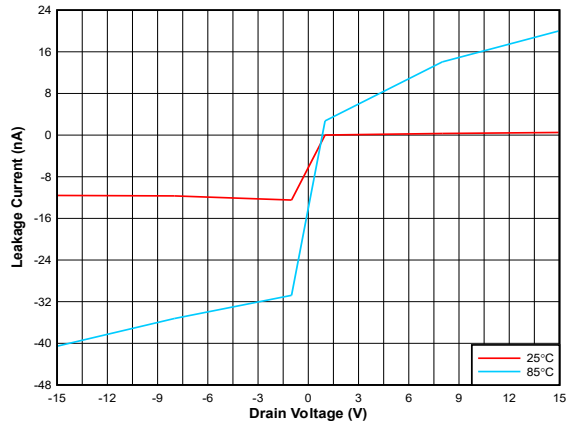
V_{DD} = 3.3V

Figure 13-3. On Leakage Current vs Source or Drain Voltage



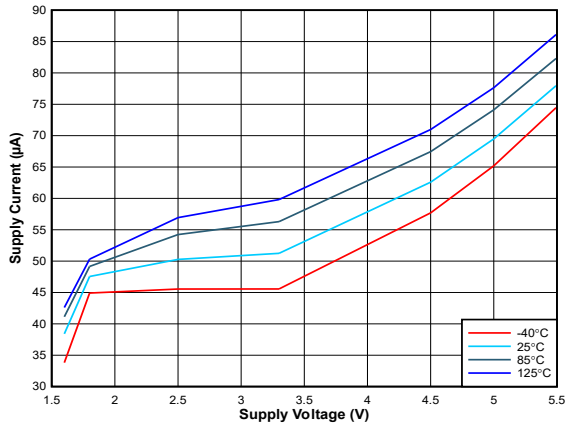
V_{DD} = 3.3V

Figure 13-4. ISOFF Leakage vs Source Voltage



V_{DD} = 3.3V

Figure 13-5. IDOFF Leakage vs Drain Voltage

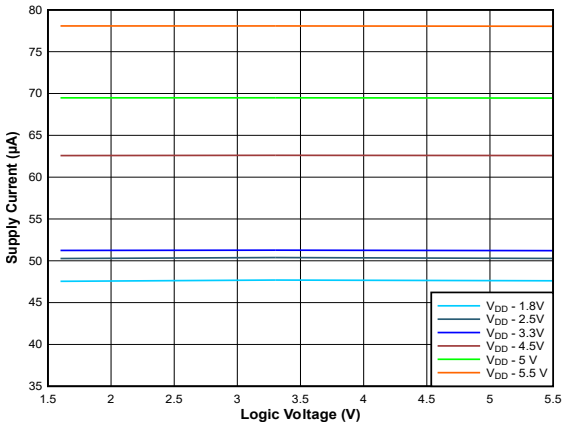


T_A = 25°C

Figure 13-6. Supply Current vs Supply Voltage

13 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



T_A = 25°C, V_S = 15V

Figure 13-7. Supply Current vs Logic Voltage

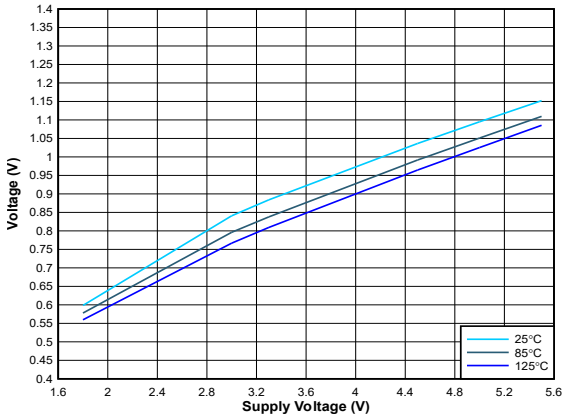


Figure 13-8. V_{IH} Logic Threshold vs Supply Voltage

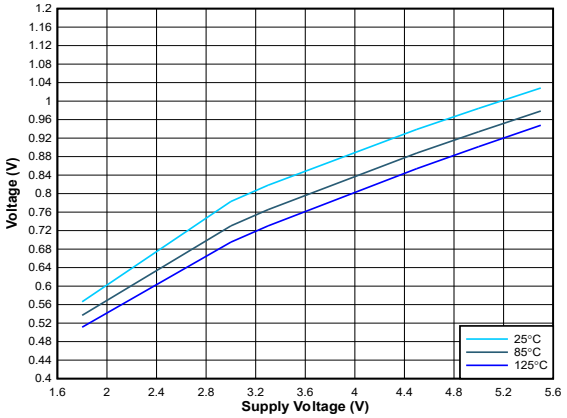
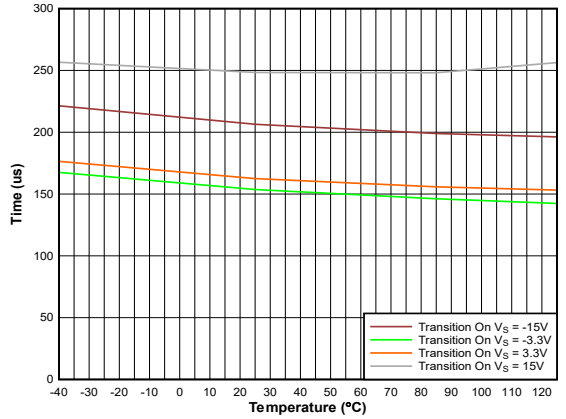
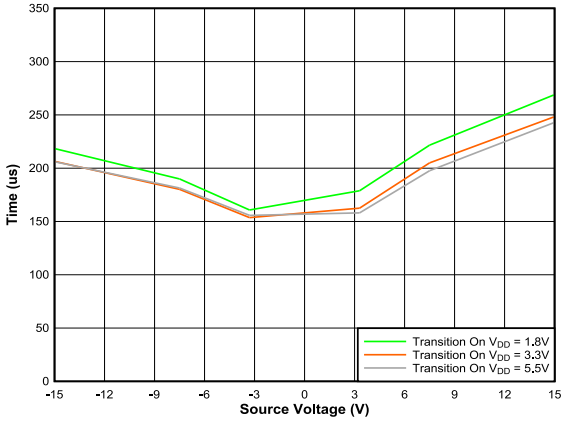


Figure 13-9. V_{IL} Logic Threshold vs Supply Voltage



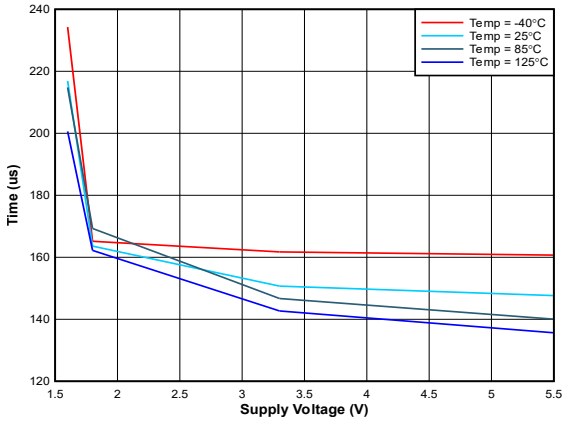
V_{DD} = 3.3V

Figure 13-10. Transition Time vs Temperature



T_A = 25°C

Figure 13-11. Transition Time vs Supply Voltage

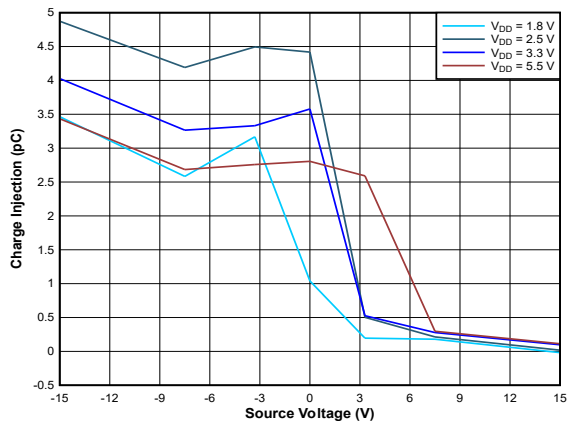


T_S = 3.3V

Figure 13-12. tBBM vs Supply Voltage

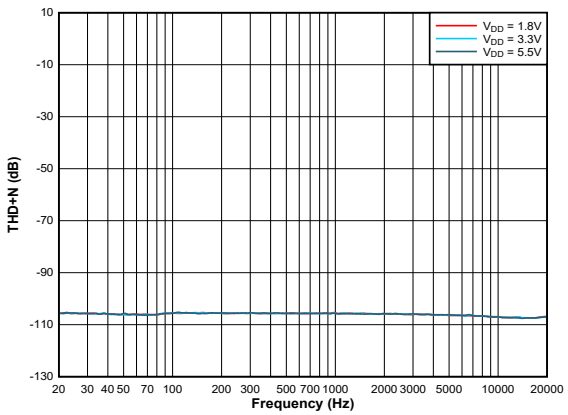
13 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



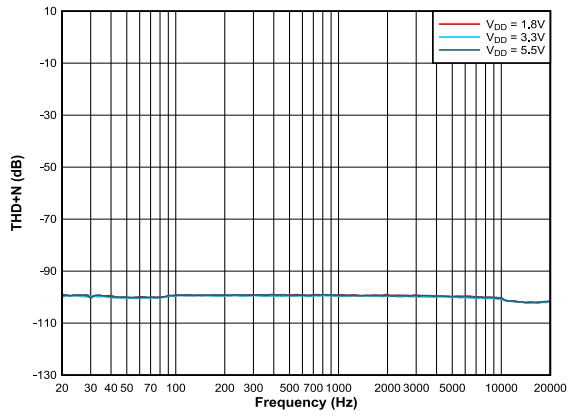
T_A = 25°C

Figure 13-13. Charge Injection vs Source Voltage



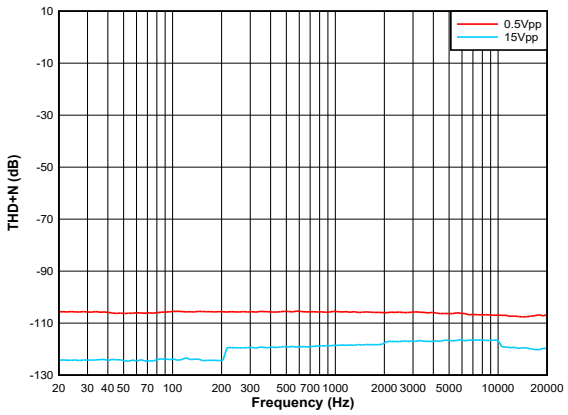
R_{LOAD} = 600Ω, T_A = 25°C

Figure 13-14. THD+N vs Frequency



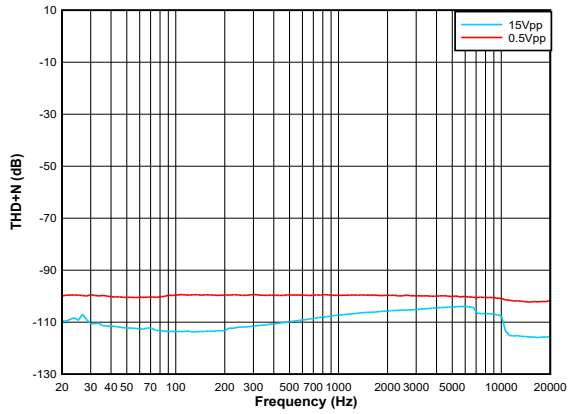
R_{LOAD} = 32Ω, T_A = 25°C

Figure 13-15. THD+N vs Frequency



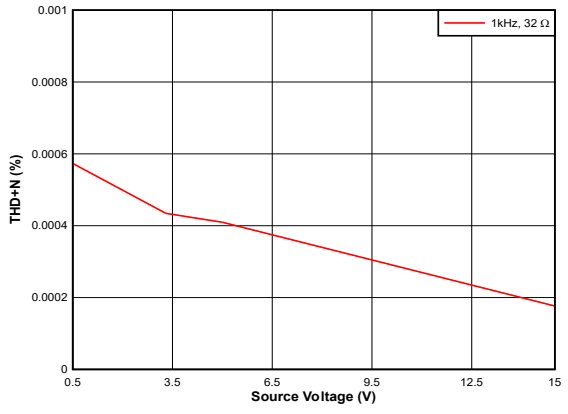
V_{DD} = 3.3V, R_{LOAD} = 600Ω, T_A = 25°C

Figure 13-16. THD+N vs Frequency



V_{DD} = 3.3V, R_{LOAD} = 32Ω, T_A = 25°C

Figure 13-17. THD+N vs Frequency

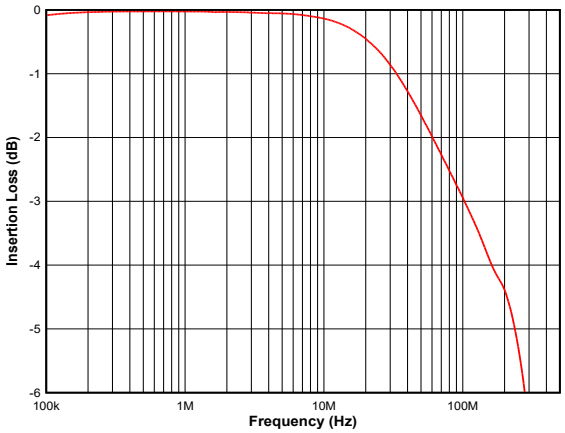


V_{DD} = 3.3V, T_A = 25°C

Figure 13-18. THD+N vs Peak-to-Peak Voltage

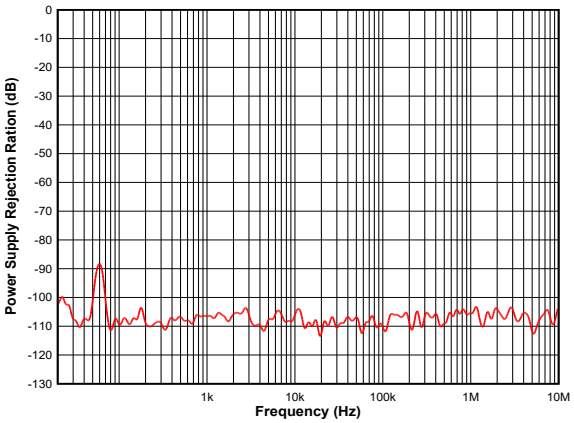
13 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



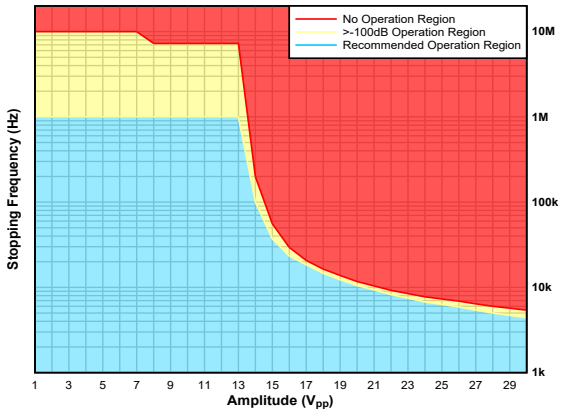
V_{DD} = 3.3V, T_A = 25°C

Figure 13-19. Insertion Loss vs Frequency



V_{DD} = 3.3V, T_A = 25°C

Figure 13-20. ACPSRR vs Frequency



V_{DD} = 5V

Figure 13-21. Maximum Sinusoidal Signal Swing

14 Parameter Measurement Information

14.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. Figure 14-1 shows the measurement setup used to measure R_{ON}. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$.

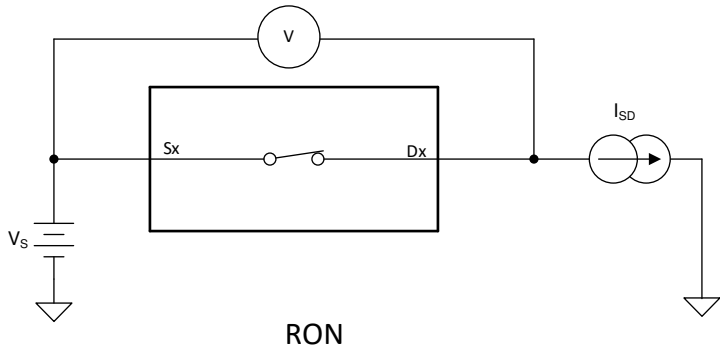


Figure 14-1. On-Resistance Measurement Setup

14.2 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$. Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$. Either the source pin or drain pin is left floating during the measurement. Figure 14-2 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

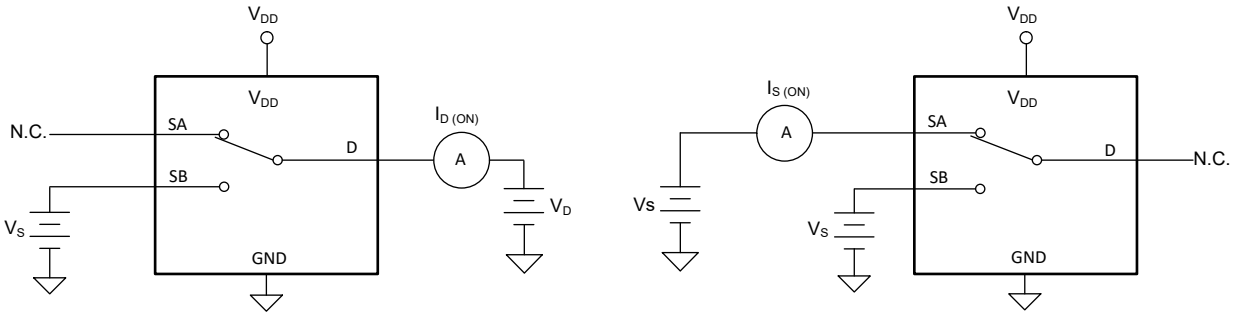


Figure 14-2. On-Leakage Measurement Setup

14.3 Off-Leakage Current

Source and drain off-leakage current is defined as the leakage current flowing into or out of the source or drain pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$ and $I_{D(OFF)}$. Figure 14-3 shows the setup used to measure off-leakage current.

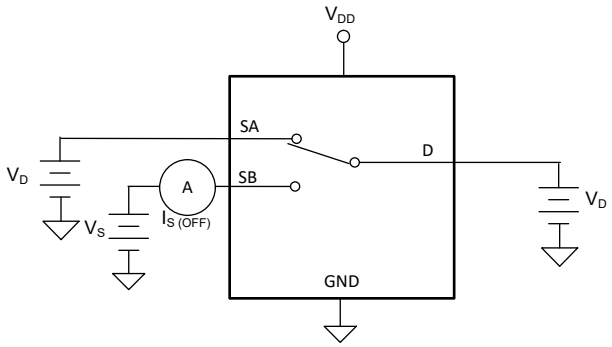


Figure 14-3. Off-Leakage Measurement Setup

14.4 Power-Off Leakage Current

Powered-off source and drain leakage current is defined as the leakage current flowing into or out of the source or drain pin when the device is powered off. This current is denoted by the symbol $I_{PS(OFF)}$ and $I_{PD(OFF)}$. Figure 14-4 shows the setup used to measure off-leakage current.

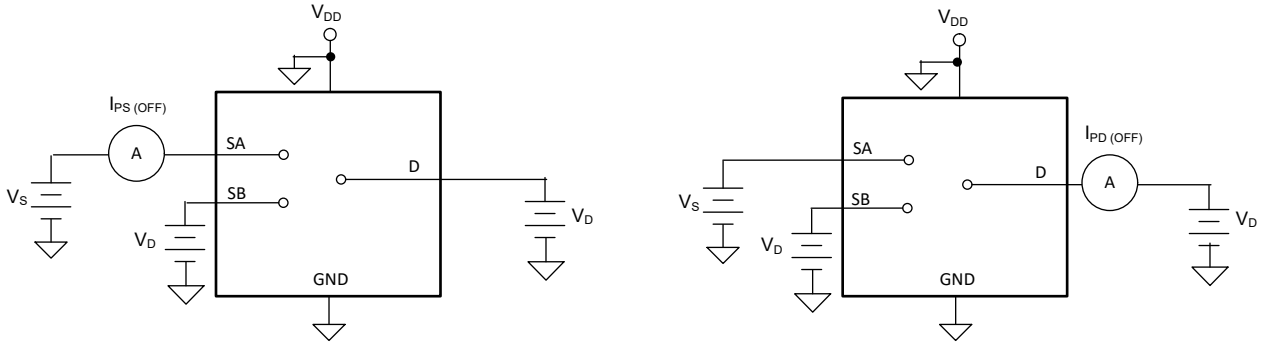


Figure 14-4. Power-Off Leakage Measurement Setup

14.5 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 14-5 shows the setup used to measure propagation delay, denoted by the symbol t_{PD}.

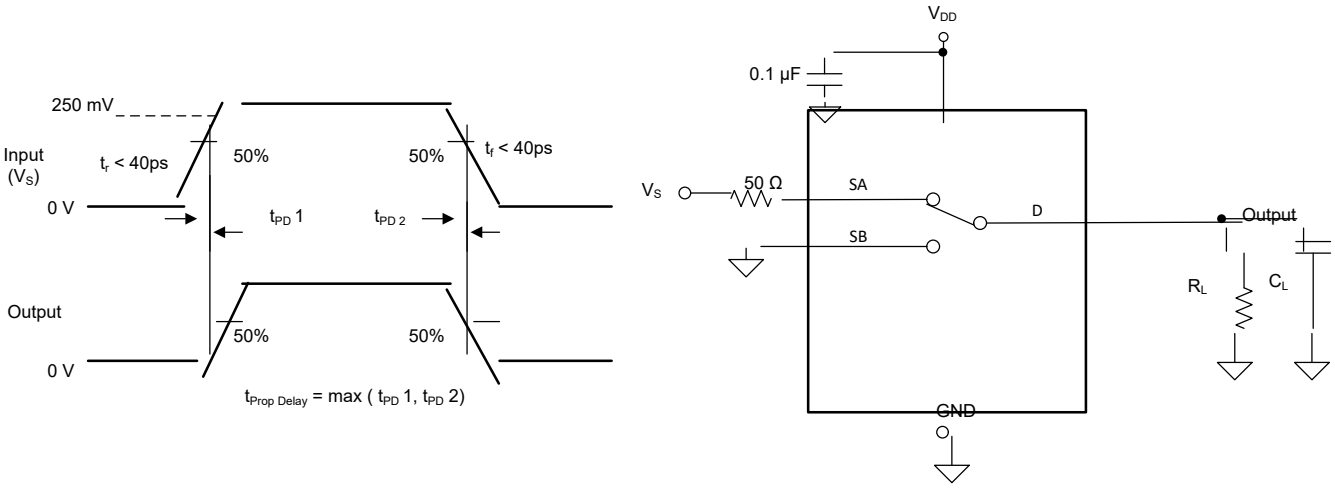


Figure 14-5. Propagation Delay Measurement Setup

14.6 $t_{ON\ (VDD)}$ and $t_{OFF\ (VDD)}$ Time

The $t_{ON\ (VDD)}$ time is defined as the time taken by the output of the device to rise 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. Figure 14-6 shows the setup used to measure turn on time, denoted by the symbol $t_{ON\ (VDD)}$

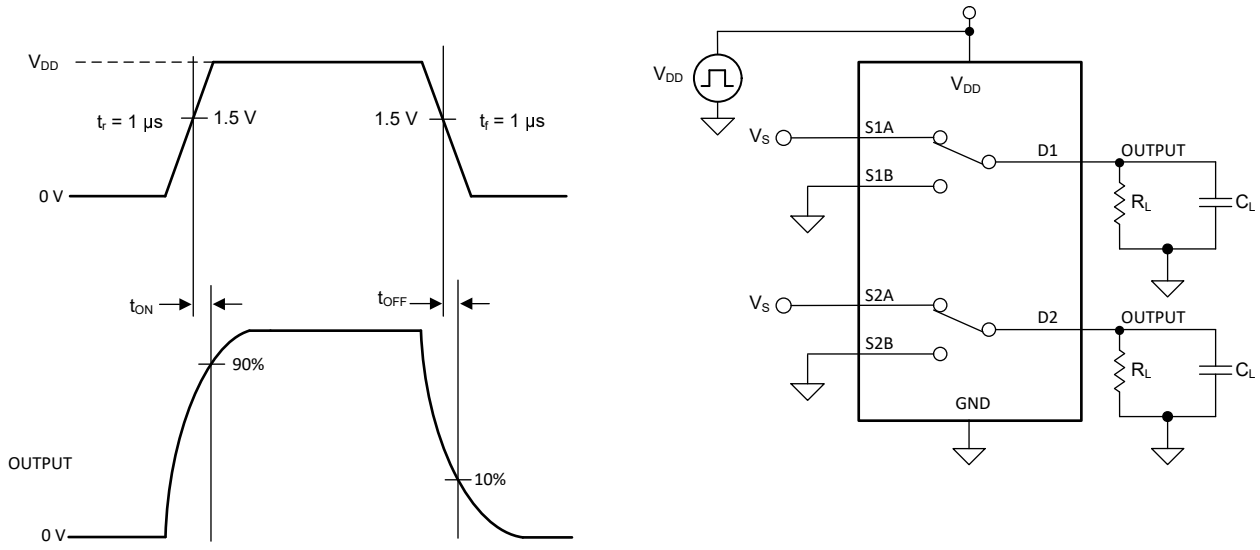


Figure 14-6. $t_{ON\ (VDD)}$ and $t_{OFF\ (VDD)}$ Time Measurement Setup

14.7 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the control signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 14-7 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

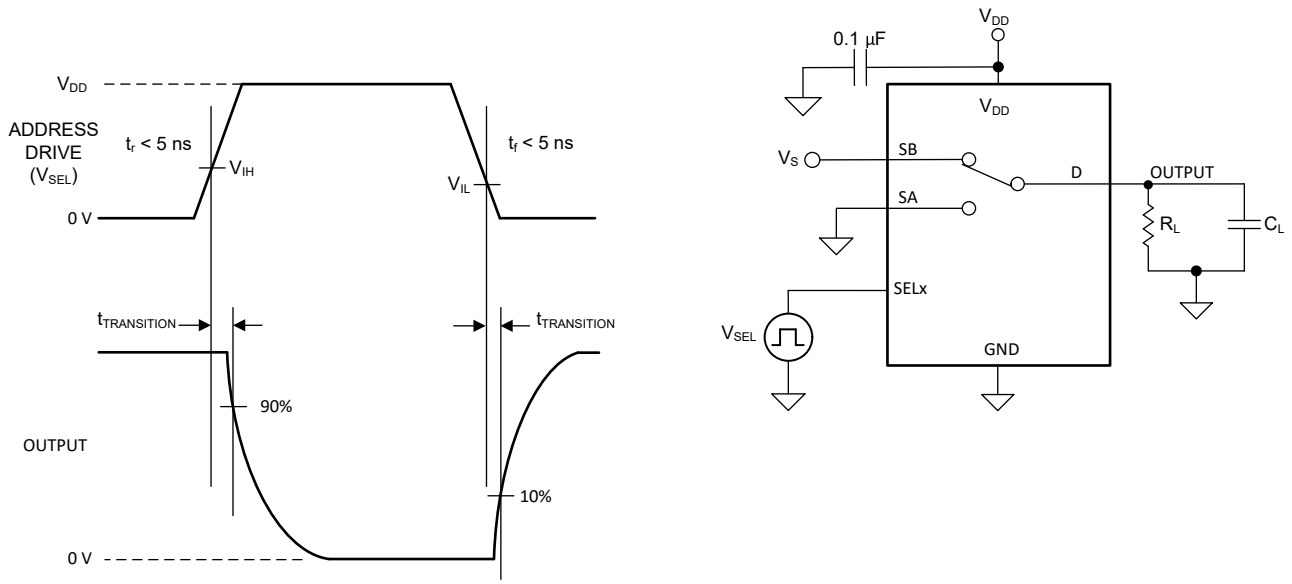


Figure 14-7. Transition-Time Measurement Setup

14.8 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 14-8 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

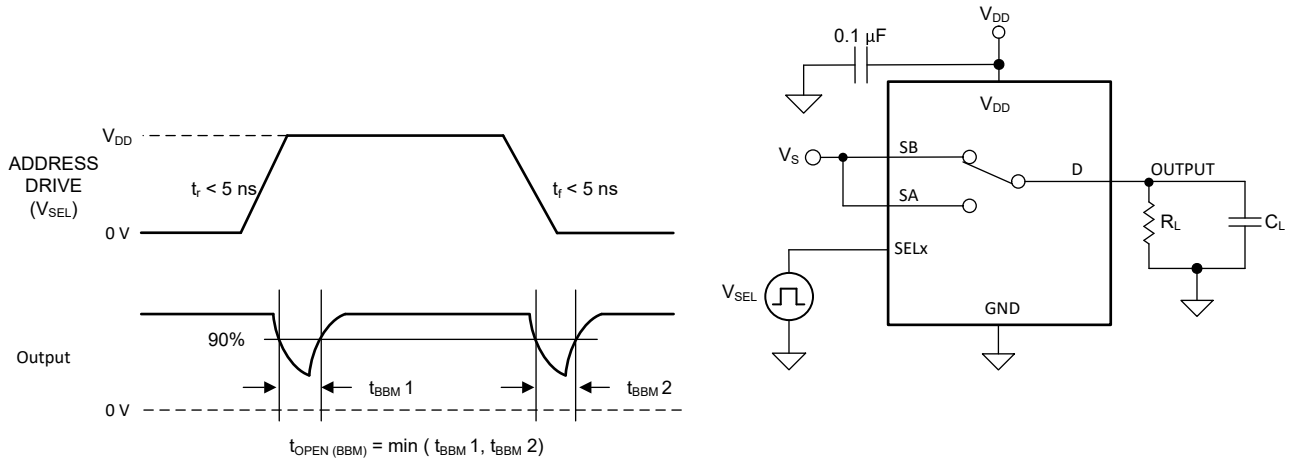


Figure 14-8. Break-Before-Make Delay Measurement Setup

14.9 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD + N.

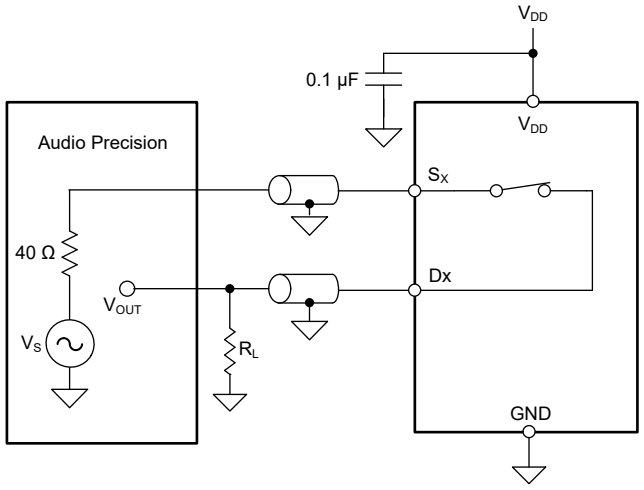


Figure 14-9. THD + N Measurement Setup

14.10 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 100mV$_{PP}$. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR.

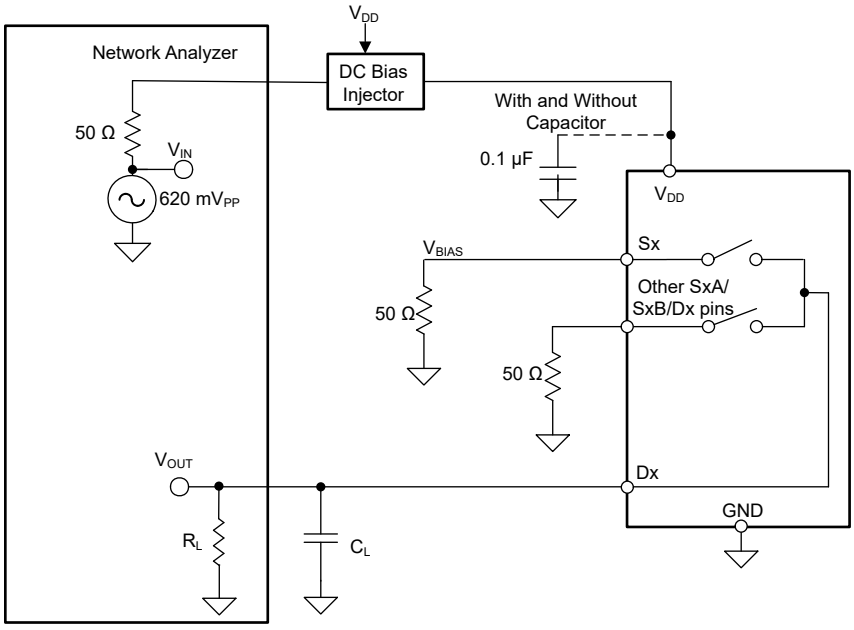


Figure 14-10. AC PSRR Measurement Setup

14.11 Charge Injection

Any mismatch in capacitance results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. Figure 14-11 shows the setup used to measure charge injection from Drain (D) to Source (Sx).

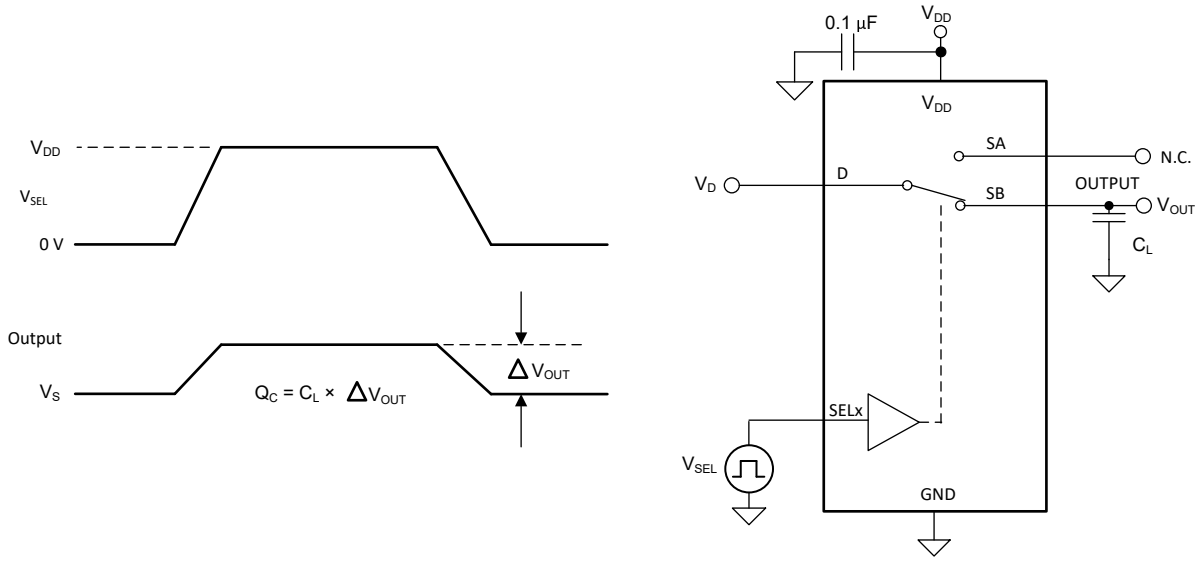


Figure 14-11. Charge Injection Measurement Setup

14.12 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the device. Figure 14-12 shows the setup used to measure bandwidth.

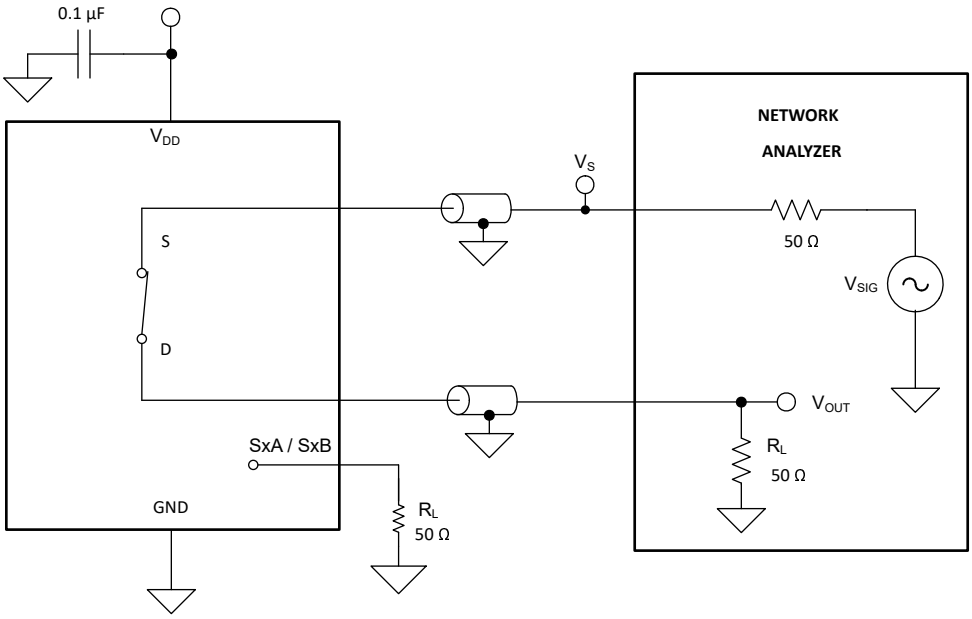


Figure 14-12. Bandwidth Measurement Setup

14.13 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. Figure 14-13 shows the setup used to measure, and the equation used to calculate off isolation.

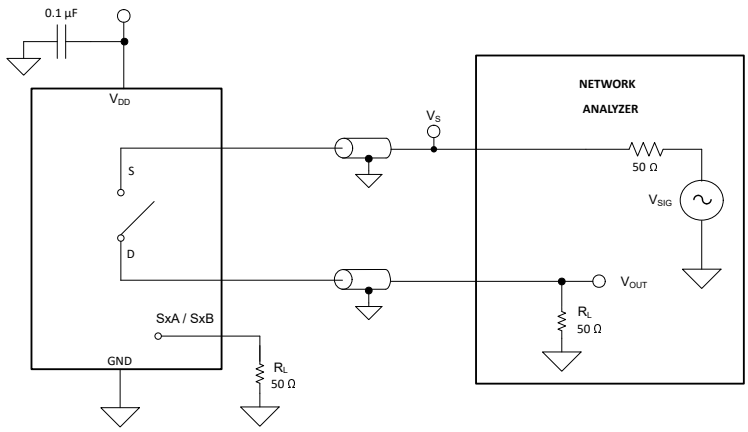


Figure 14-13. Off Isolation Measurement Setup

$$Off\ Isolation\ =\ 20\ \times\ Log\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

14.14 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. Figure 14-14 shows the setup used to measure, and the equation used to calculate crosstalk.

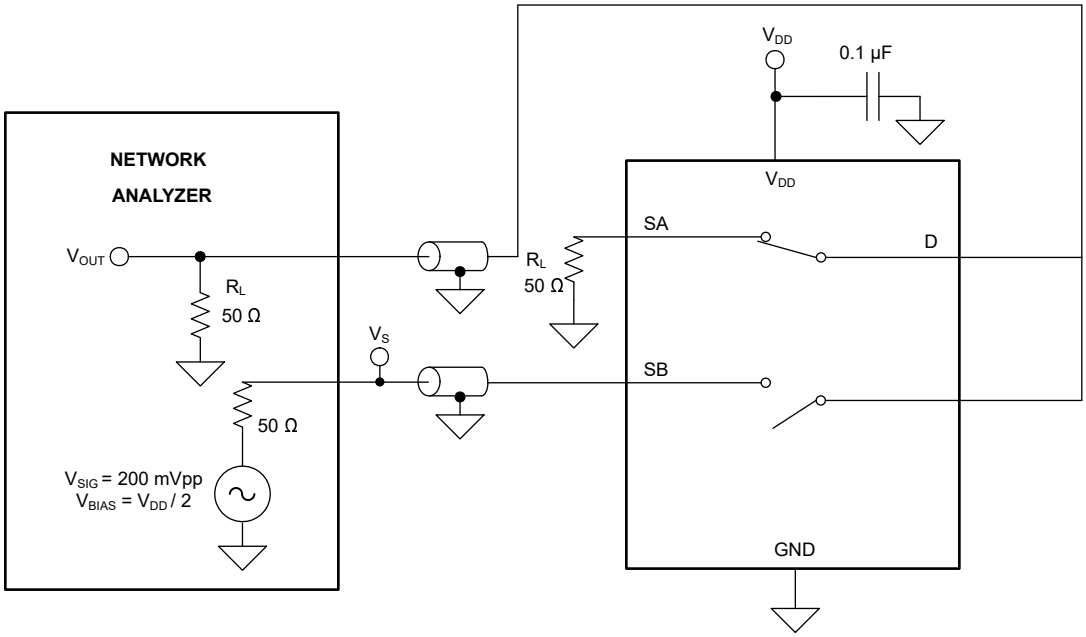


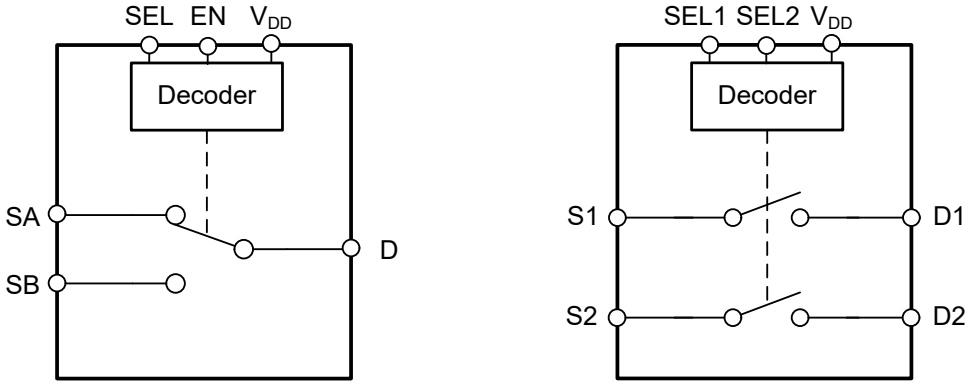
Figure 14-14. Crosstalk Measurement Setup

$$Channel-to-Channel\ Crosstalk\ =\ 20\ \times\ Log\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

15 Detailed Description

15.1 Functional Block Diagram

The TMUX4821 is a 1:1, 2-channel and the TMUX4819 is a 2:1 1-channel multiplexer or demultiplexer. Each input is turned on or turned off based on the state of the select lines and V_{DD} pin.



15.2 Device Functional Modes

Table 15-1 provides the truth table for the TMUX48xx.

Table 15-1. TMUX4821 Truth Table

VDD	SELx	Channel x
0	X(1)	All channels are off (Hi-Z). Device is in power-off protection.
1	0	Channel x OFF
1	1	Channel x ON

Table 15-2. TMUX4819 Truth Table

VDD	SEL	EN	Selected Input Connected To Drain (D) Pin
0	X(1)	X	All channels are off (Hi-Z). Device is in power-off protection.
1	X	0	All channels are off (Hi-Z). Device is in power-off protection.
1	0	1	SxA
1	1	1	SxB

(1) X denotes *do not care*.

15.3 Feature Description

15.3.1 Beyond the Supply

The TMUX48xx supports signal voltages beyond the supply on the source (Sx) and drain (Dx) pins up to ±15V. This feature allows both AC and DC bidirectional signals above V_{DD} and below ground to pass through the switch without distortion, using a unidirectional supply. The device remains within the performance mentioned in the *Electrical Characteristics*.

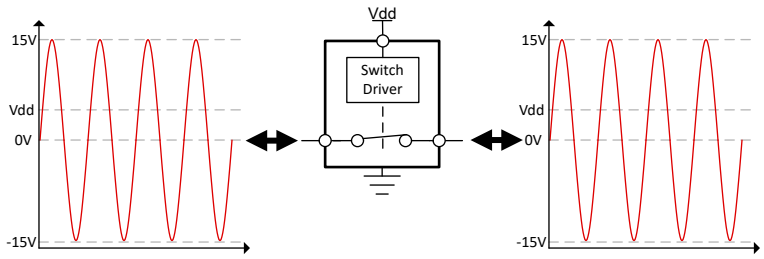


Figure 15-1. Beyond the Supply Signal Support

15.3.2 Bidirectional Operation

The TMUX48xx conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

15.3.3 Power-Off Protection

The TMUX48xx has powered-off protection up to ±15V on the switch path. This keeps the switch in a high impedance mode and isolates the source (Sx) and drain (Dx) pins when the supply is removed (Vdd = 0V). Powered-off protection minimizes system complexity by removing the need for power supply sequencing on the signal path. The device performance remains within the leakage performance mentioned in the Electrical Specifications. For more information on powered-off protection, refer to *Eliminate Power Sequencing with Powered-off Protection Signal Switches*.

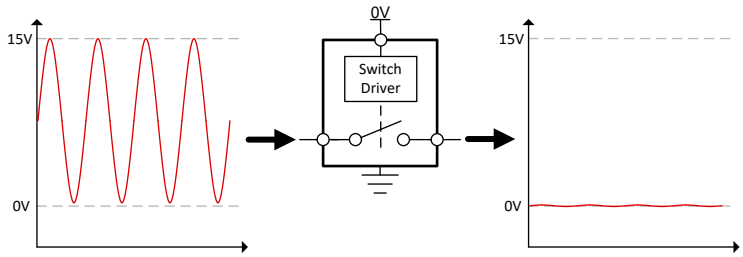


Figure 15-2. Beyond the Supply Power-Off Protection

15.3.4 1.2V and 1.8V Logic Compatible Inputs

The TMUX48xx has 1.2V logic compatibility with a supply of 1.8V and a 1.8V logic compatibility with a 5V supply (V_{DD}). Having lower logic level inputs allows the device to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and bill of material (BOM) cost. For more information on 1.8V logic implementations, refer to Simplifying Design with 1.8V logic Muxes and Switches

15.3.5 Integrated Pull-Down Resistor on Logic Pins

The TMUX48xx has internal weak pull-down resistors to GND so the logic pins are not left floating. This feature integrates up to two external components and reduces system size and cost.

The value of this pull-down resistor is approximately 6MΩ.

15.3.6 Fail-Safe Logic

The TMUX48xx supports Fail-Safe Logic on the control input pin (SEL) allowing for operation up to 5.5V, regardless of the state of the supply pin. This feature allows voltages on the control pin to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the logic input pin of the TMUX48xx to be ramped to 5.5V while V_{DD} = 0V. The logic control input is protected against positive faults of up to 5.5V in powered-off condition, but does not offer protection against negative overvoltage conditions.

16 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

16.1 Application Information

TMUX4821 and TMUX4819 are part of the *beyond the supply switches and multiplexers* family of devices. This means that this device can switch signals from -15V to 15V with a low voltage supply from 1.8V to 5.5V. Additionally, TMUX48xx features powered-off protection, which by design keeps the switches open even when there is no supply. This unique feature combination enables the TMUX48xx to be extremely versatile for a wide variety of applications such as boosted outputs and high common mode offsets.

16.2 Typical Applications

16.2.1 Audio Amplifier Switching

Often, there are multiple audio sources in a system giving the user options on which source will connect to the speaker. To enable switching between these sources, a TMUX48xx can be used. The line-in can be biased to a negative voltage, and class-D amplifier output can be higher than the typically used 3V and 5V supplies. So any circuitry connected needs to handle this bipolar voltage. This same scheme can be used in systems where there are multiple speaker outputs and one source as well. Here the switch is used to switch from an internal speaker to an external one. Figure 16-1 shows the block diagram for these applications. Here a TLV320AIC3x is used as an audio codec driving a TPA313x class D audio amplifier. Additionally, if IEC protection is needed on the external connectors (audio jack input or external speaker), then a 2 channel TPD2E007 can be used.

The TMUX48xx can be used to switch up to ±15V with a supply voltage from 1.8V to 5.5V. The supply can also be driven directly with a GPIO, allowing the user to put the device into ultra-low power mode. In this mode, the TMUX48xx operates with powered-off protection, so any high voltage present on the inputs will not propagate to the outputs. This feature allows for the correct power up cycling and increases system robustness. Additionally, the TMUX48xx features excellent THD+N performance, so there is minimal impact to the audio signal quality through the switch. This allows the system designer to save a significant portion of board area without impacting signal integrity.

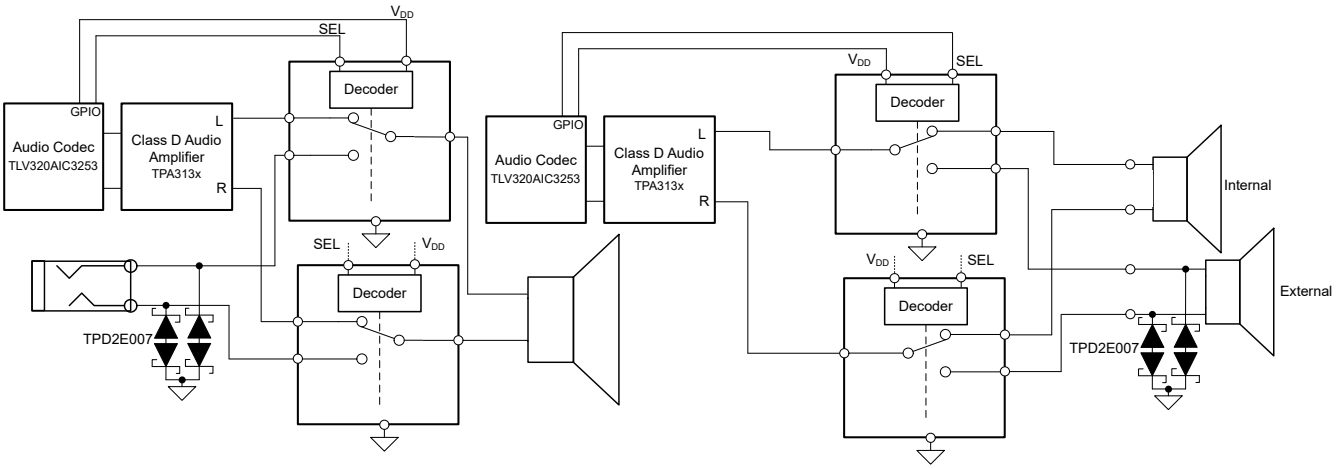


Figure 16-1. Audio Amplifier Switching

16.2.1.1 Design Requirements

Table 16-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	1.8V to 5.5V
MUX I/O signal range (V_S, V_D)	-15V to 15V
Control logic thresholds (V_{SEL})	1.8V to 5.5V

16.2.1.2 Detailed Design Procedure

The TMUX48xx can support bidirectional signals beyond the supply without any external components except for the supply decoupling capacitors. Figure 15-1 shows how the signal range is above and below the device supply range. Additionally with a very low on-resistance and an ultra flat response, the TMUX48xx has a very low THD+N as well as a reduced impact to DC losses and thermal self-heating. These features make the TMUX48xx designed for audio application.

16.2.1.3 Application Curves

The low on-resistance and ultra flat response enable the TMUX48xx to have an extremely low THD+N. This results in little to no impact in audio fidelity, even in high performance systems. This allows the system design to save a significant portion of board area without impacting signal integrity.

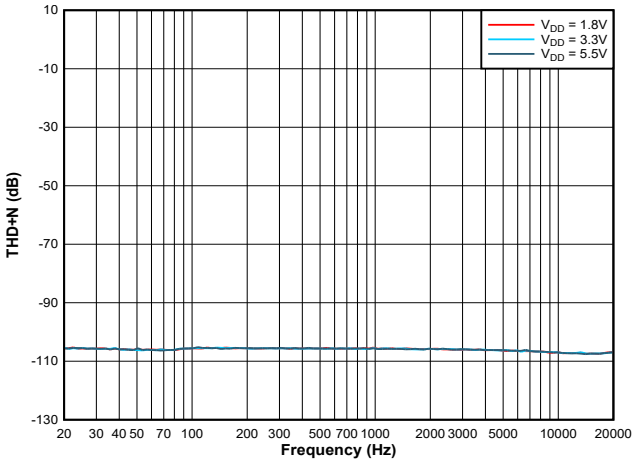


Figure 16-2. THD+N with R_L = 600Ω

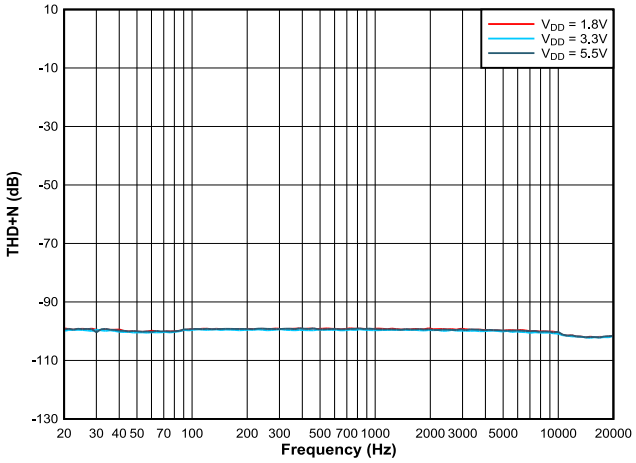


Figure 16-3. THD+N with R_L = 32Ω

Because this device has such a low on-resistance, it can be used in applications with very low output speaker impedance such as 8Ω or 4Ω systems. In these applications, the current through the switch can increase drastically, causing self heating.

16.2.2 Smart Drug Delivery Flow Meters

For smart drug delivery applications, a precise measurement of the dosage must be monitored. One very accurate architecture that is used is differential time of flight (TOF) using transducers. Many liquid flow sensor systems are higher attenuation compared to gas applications. In these high attenuation scenarios, a higher excitation voltage is used to significantly increase the signal to noise ratio (SNR). A bidirectional 2:1 multiplexer is used to switch the transmission and reception signals from the MCU to the transceivers without distortion.

Because the TMUX48xx can support signals beyond the supply, it is an excellent choice for handling this higher excitation voltage. The TMUX48xx can be used to switch up to -15V to 15V with a supply voltage from 1.8V to 5.5V, with an ultra-low on-resistance to minimize the impact on the signal quality. The supply can also be driven directly with a GPIO, allowing the user to put the device into ultra-low power mode. In this mode the TMUX48xx operates with powered-off protection, so any high voltage present on the inputs will not propagate to the outputs. This allows correct power up cycling and increases system robustness. Additionally, the TMUX48xx features excellent THD+N performance, so there is minimal impact to the signal quality through the switch.

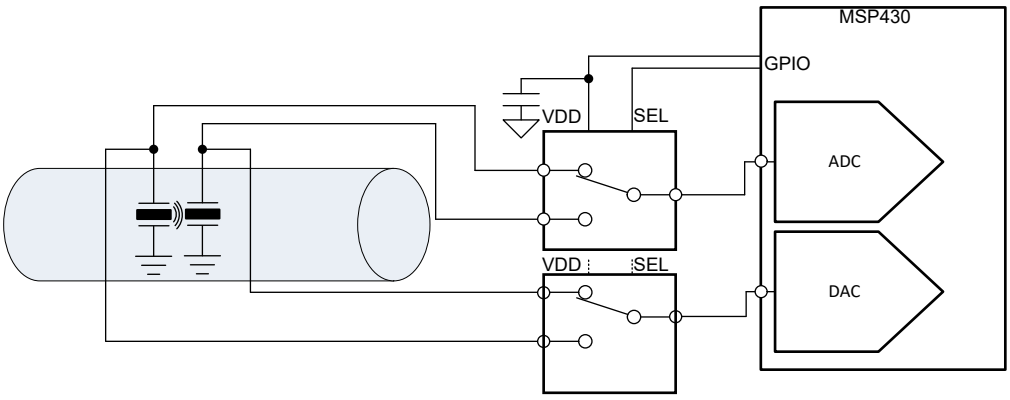


Figure 16-4. Smart Drug Delivery Flow Meters

16.2.2.1 Design Requirements

Table 16-2. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	1.8V to 5.5V
MUX I/O signal range (V_S, V_D)	-15V to 15V (Beyond the Supply)
Control logic thresholds (V_{SEL})	1.8V to 5.5V

16.2.2.2 Detailed Design Procedure

The TMUX48xx can support bidirectional signals beyond the supply without any external components except for the supply decoupling capacitors. Section 15.3.1 shows how the signal range is above and below the device supply range. Additionally with a very low on-resistance and an ultra flat response, the TMUX48xx has a very low THD+N as well as a reduced impact to DC losses and thermal self-heating. These features make the TMUX48xx ideal for high attenuation transducer application. For a more detailed analysis of the flow meter system refer to Section 16.2.2.3 .

16.2.2.3 Application Curve

The linear response of the TMUX48xx reduces any impact to signal distortion and loss, making it an excellent choice for high precision industrial systems. The TMUX48xx utilizes a specialized architecture to keep the on-resistance extremely flat, while supporting signals beyond the supply from -15V to 15V. Additionally, the TMUX48xx supports a wide frequency range to drive output capacitive transducers. This with the low on-resistance results in an extremely low insertion loss as well.

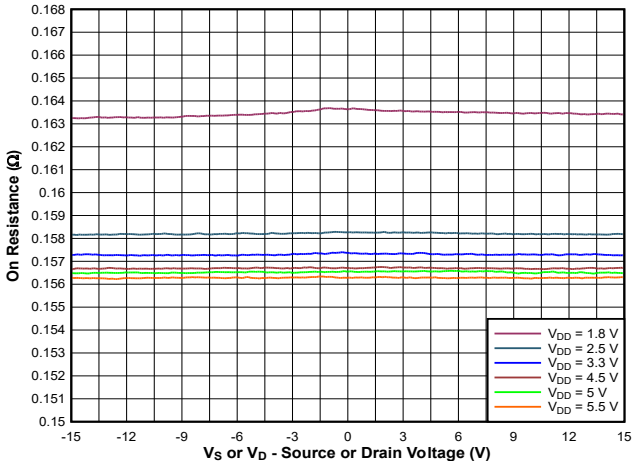


Figure 16-5. Insertion Loss Across Frequency

16.3 Power Supply Recommendations

The operates across a wide supply range from 1.8V to 5.5V, while supporting input or output signals from -15V to 15V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF at V_{DD} to ground. Place the bypass capacitors as close to the power supply pin of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes.

For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always confirm that the ground (GND) connection is established before supplies are ramped.

16.4 Layout

16.4.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 16-6 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

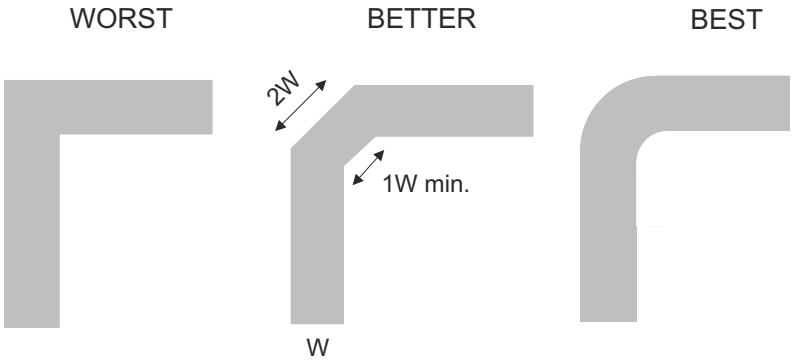


Figure 16-6. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Some key considerations are as follows:

- For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10µF between VDD and GND. TI recommends a 0.1µF and 1µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

16.4.2 Layout Example

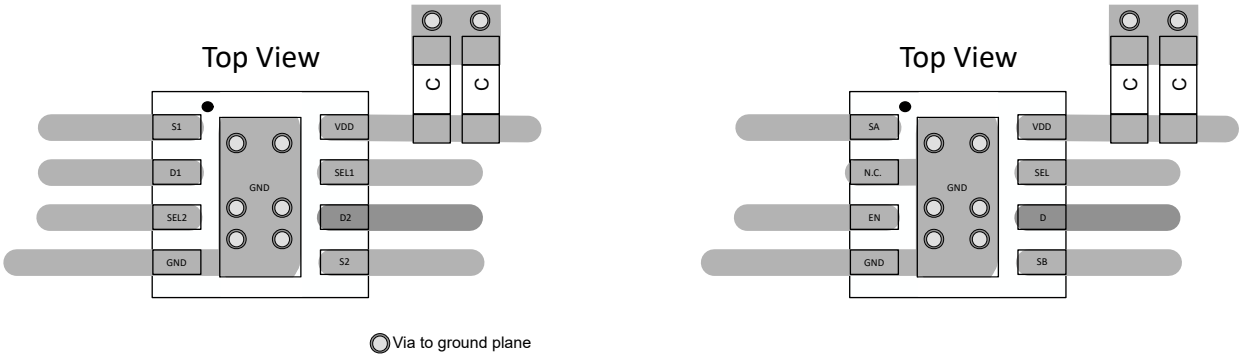


Figure 16-7. TMUX48xx Layout Example

17 Device and Documentation Support

17.1 Documentation Support

17.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Eliminate Power Sequencing with Powered-off Protection Signal Switches* application brief
- Texas Instruments, *Simplifying Design with 1.8V logic Muxes and Switches* application brief

17.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

17.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

17.4 Trademarks

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17.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

17.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

18 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2025) to Revision A (December 2025)	Page
• Updated data sheet status from *Advanced Information* to *Production Data*	1
• Updated Section 13	10
• Updated Section 16.1	23

DATE	REVISION	NOTES
October 2025	*	Initial Release

19 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX4819DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T481
TMUX4821DSGR	Active	Production	WSON (DSG) | 8	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T482

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

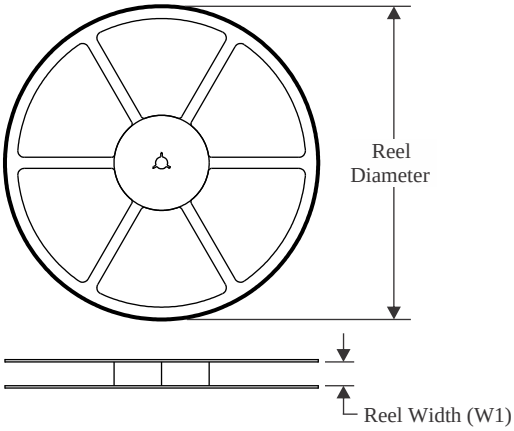
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

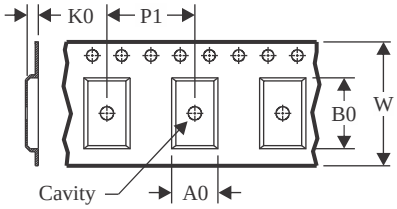
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

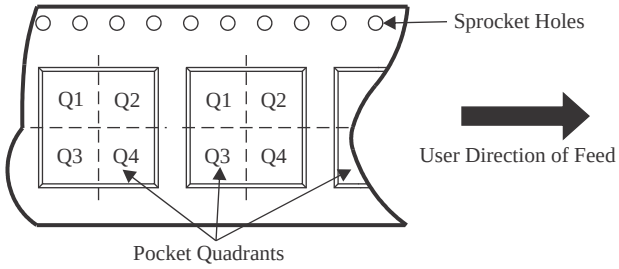


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

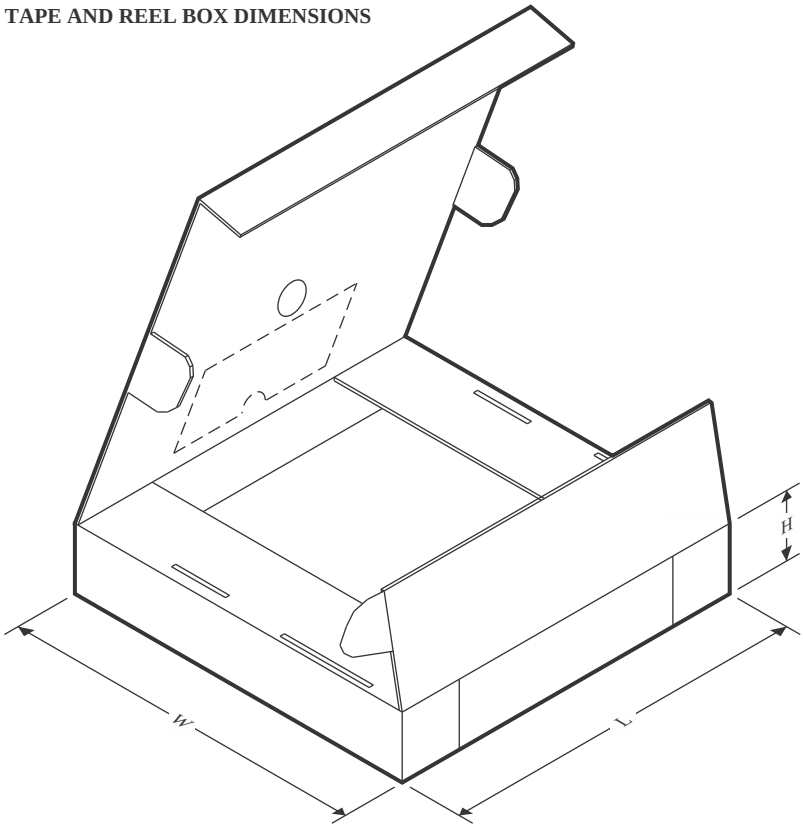
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX4819DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TMUX4821DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX4819DSGR	WSON	DSG	8	3000	182.0	182.0	20.0
TMUX4821DSGR	WSON	DSG	8	3000	182.0	182.0	20.0

GENERIC PACKAGE VIEW

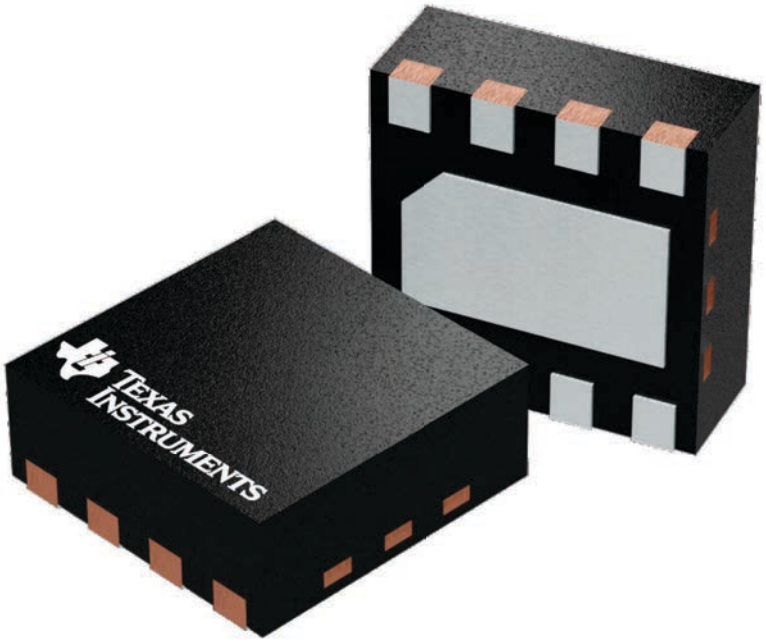
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



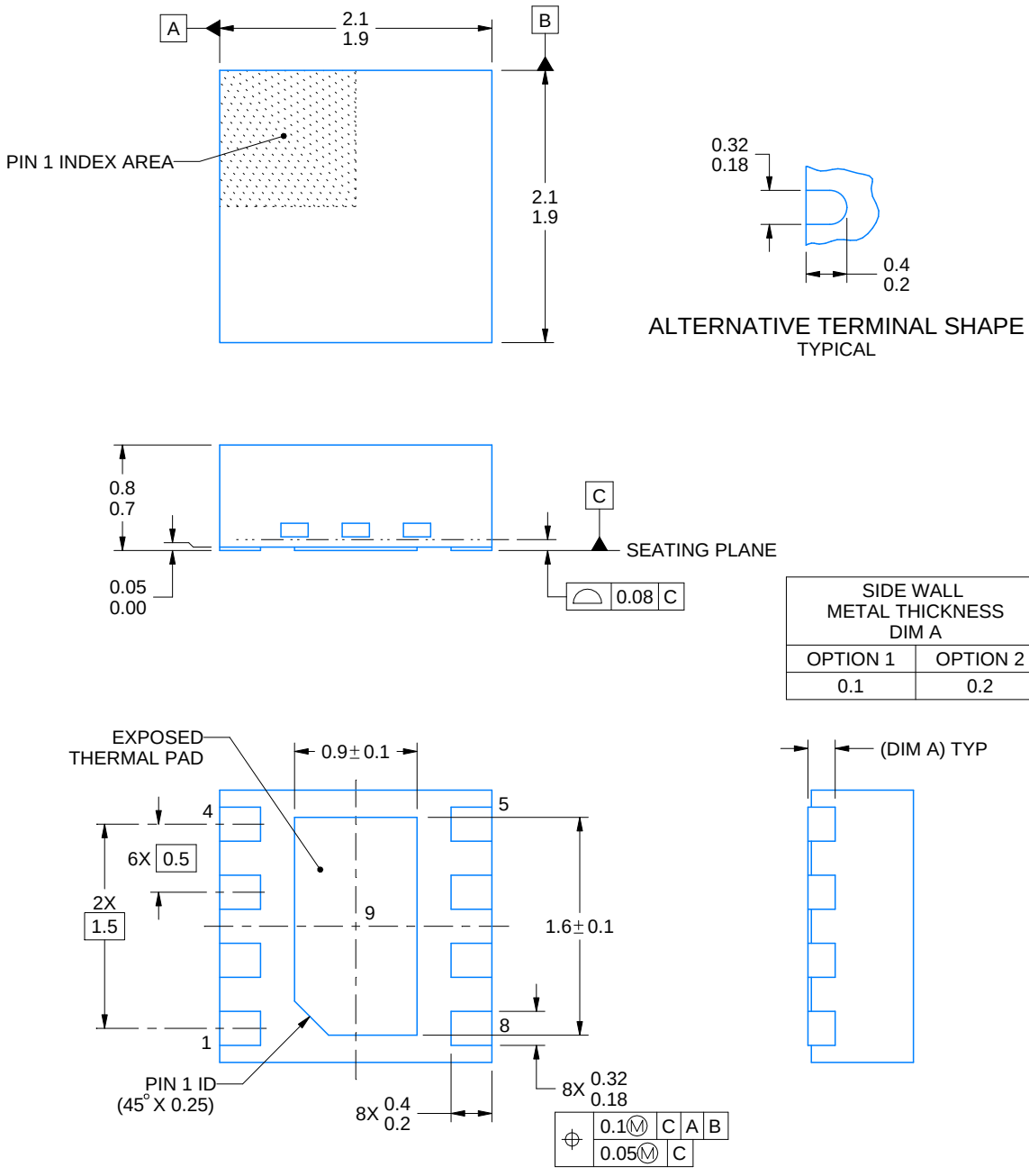
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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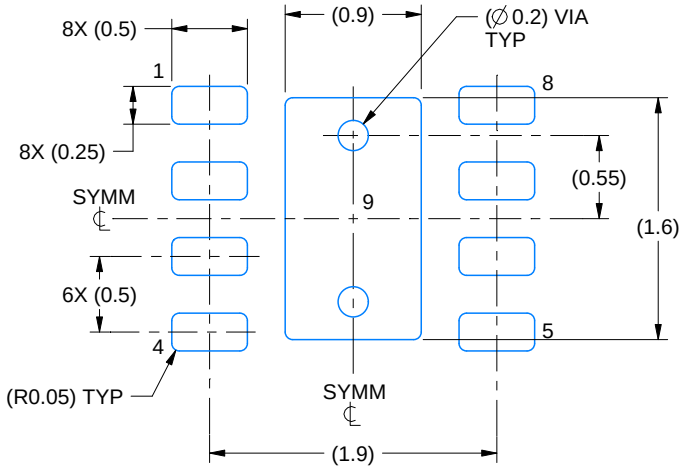
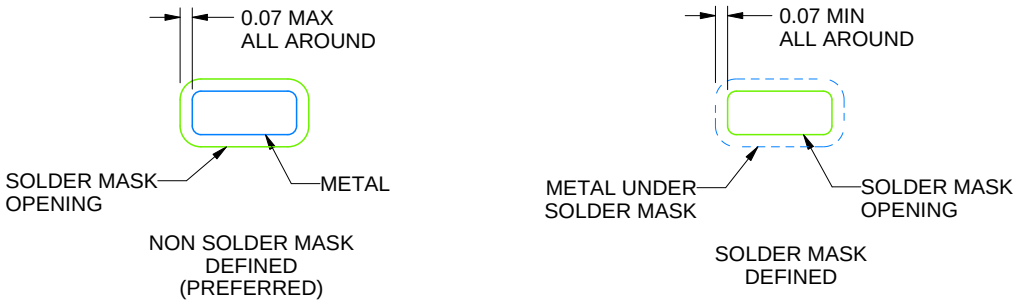
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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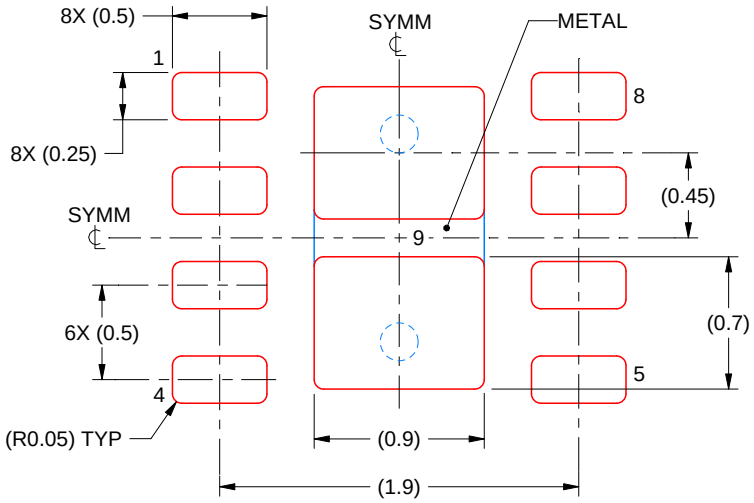
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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