TMUX541x 50V, 21Ω, 1:1 (SPST) 4-Channel Switches with 1.8V Logic

1 Features

- Dual supply range: ±4.5V to ±25V
- Single supply range: 4.5V to 50V
- Asymmetric dual supply support (For example: V_{DD} = 37.5V, V_{SS} = -12.5V)
- 1.8V logic compatible
- Low on-resistance: 21Ω (typical)
- Low on-capacitance: 12pF (typical)
- Ultra-low on-resistance flatness: 0.005Ω (typical)
- Low on-leakage current: 0.002nA (typical), 40nA (maximum)
- Low charge injection: 13pC (typical)
- –40°C to +125°C operating temperature
- Rail-to-rail operation
- Bidirectional operation
- Break-before-make switching (TMUX5413)

2 Applications

- Sample-and-hold circuits
- Feedback gain switching
- Signal isolation
- Semiconductor test equipment
- Programmable logic controllers (PLC)
- Factory automation and control
- Professional Audio Equipment
- Instrumentation: lab, analytical, and portable
- Data acquisition systems (DAQ)
- Optical test equipment

3 Description

The TMUX541x is a general purpose complementary metal-oxide semiconductor (CMOS) switch device with four independently selectable 1:1, single-pole, single-throw (SPST) switch channels. The device works with a single supply (4.5V to 50V), dual supplies (±4.5V to ±25V), or asymmetric supplies (such as V_{DD} = 37.5V, V_{SS} = –12.5V). The TMUX541x supports bidirectional analog and digital signals on the source (Sx) and drain (Dx) pins ranging from V_{SS} to V_{DD}.

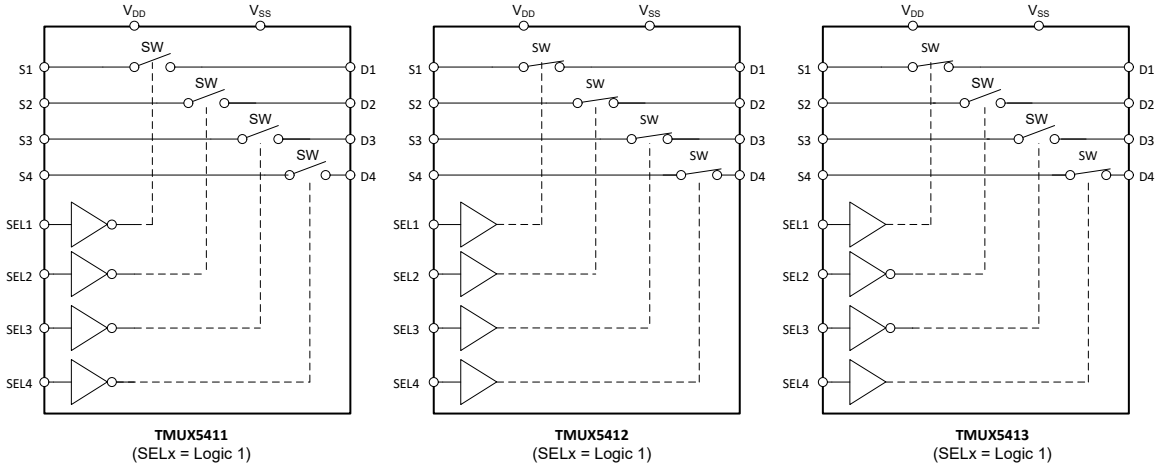
The switches of the TMUX541x are controlled with appropriate logic control inputs on the SELx pins. The TMUX541x exhibits break-before-make switching, allowing the device to be used in cross-point and multiplexing applications.

The TMUX541x is a part of the general purpose switches and multiplexers family of devices emphasizing uses in broad range of applications while reducing BOM cost.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMUX5411 TMUX5412 TMUX5413	PW (TSSOP, 16)	5mm × 6.4mm
	DYY (SOT-23-THIN, 16)	3.26mm x 4.2mm

(1) For all available packages, see the package option addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TMUX541x Block Diagram

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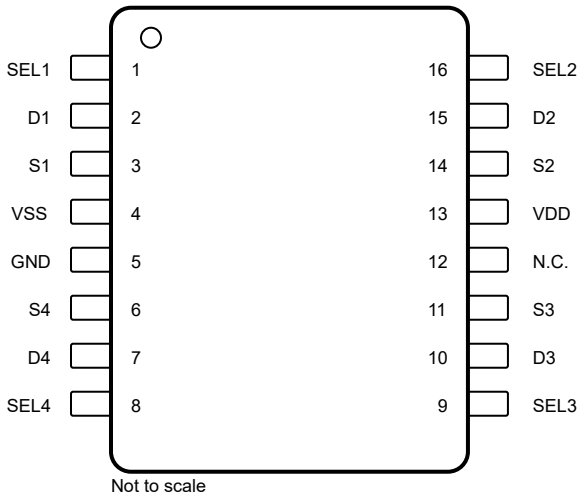
4 Pin Configuration and Functions



Not to scale

Figure 4-1. 16-Pin PW (TSSOP) & DYY (SOT-23-THN) Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	TSSOP & SOT-23-THN		
D1	2	I/O	Drain pin 1. Can be an input or output.
D2	15	I/O	Drain pin 2. Can be an input or output.
D3	10	I/O	Drain pin 3. Can be an input or output.
D4	7	I/O	Drain pin 4. Can be an input or output.
GND	5	P	Ground (0 V) reference.
N.C.	12	—	No internal connection. Can be shorted to GND or left floating
S1	3	I/O	Source pin 1. Can be an input or output.
S2	14	I/O	Source pin 2. Can be an input or output.
S3	11	I/O	Source pin 3. Can be an input or output.
S4	6	I/O	Source pin 4. Can be an input or output.
SEL1	1	I	Logic control input 1, has internal pull-down resistor. Controls channel 1 state as provided in Table 7-2.
SEL2	16	I	Logic control input 2, has internal pull-down resistor. Controls channel 2 state as provided in Table 7-2.
SEL3	9	I	Logic control input 3, has internal pull-down resistor. Controls channel 3 state as provided in Table 7-2.
SEL4	8	I	Logic control input 4, has internal pull-down resistor. Controls channel 4 state as provided in Table 7-2.
VDD	13	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD and GND
VSS	4	P	Negative power supply. This pin is the most negative power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1µF to 10 µF between VSS and GND. In single-supply applications, this pin should be connected to ground.

(1) I = input, O = output, I/O = input and output, P = power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
$V_{DD} – V_{SS}$	Supply voltage		55	V
V_{DD}		–0.5	55	V
V_{SS}		–55	0.5	V
V_{SEL} or V_{EN}	Logic control input pin voltage (SELx)	–0.5	55	V
I_{SEL} or I_{EN}	Logic control input pin current (SELx)	-30	30	mA
V_S or V_D	Source or drain voltage (Sx, Dx)	V_{SS}–0.5	V_{DD}+0.5	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, Dx)	-30	30	mA
I_{peak}	Source or drain pulse current (Sx, Dx: pulsed at 1ms, 10% duty cycle max)	-100	100	mA
T_A	Ambient temperature	–55	125	°C
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information

THERMAL METRIC[1]		TMUX541x		UNIT
		PW (TSSOP)	DYY (SOT-23)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.7	120.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.8	57.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.2	53.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2,6	2.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	66.5	53.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$ [1]	Power supply voltage differential		4.5		50	V
V_{DD}	Positive power supply voltage		4.5		50	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)		V_{SS}		V_{DD}	V
V_{SEL} - V_{SS}	Address or enable pin voltage		0		48	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)		-30		30	mA
T_A	Ambient temperature		–40		125	°C
V_{IH}	Logic Input High [2]	Logic Inputs (SEL / EN pins)	1.3		48	V
V_{IL}	Logic Input Low	Logic Inputs (SEL / EN pins)	0		0.8	V

(1) V_{DD} and V_{SS} can be any value as long as 4.5V ≤ (V_{DD} – V_{SS}) ≤ 50V, and the minimum V_{DD} is met.
(2) Please note the VIH is limited by the following constraints: V_{SEL} - V_{SS} ≤ 48V

5.5 ±15V Dual Supply: Electrical Characteristics

V_{DD} = +15V ± 10%, V_{SS} = –15V ±10%, GND = 0V (unless otherwise noted). Typical at V_{DD} = +15V, V_{SS} = –15V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10V to +10V I_D = –10mA Refer to On-Resistance	25°C		21	26	Ω
			–40°C to +85°C			32	Ω
			–40°C to +125°C			37	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10V to +10V I_D = –10mA Refer to On-Resistance	25°C		0.15	0.75	Ω
			–40°C to +85°C			1.2	Ω
			–40°C to +125°C			1.5	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –10V to +10V I_S = –10mA Refer to On-Resistance	25°C		0.02	0.45	Ω
			–40°C to +85°C			0.6	Ω
			–40°C to +125°C			0.7	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0V, I_S = –10mA Refer to On-Resistance	–40°C to +125°C		0.085		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 16.5V, V_{SS} = –16.5V Switch state is off V_S = +10V / –10V V_D = –10V / + 10V Refer to Off-Leakage Current	25°C		0.003		nA
			–40°C to +85°C	-5		5	nA
			–40°C to +125°C	-10		10	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 16.5V, V_{SS} = –16.5V Switch state is off V_S = +10V / –10V V_D = –10V / + 10V Refer to Off-Leakage Current	25°C		0.003		nA
			–40°C to +85°C	-5		5	nA
			–40°C to +125°C	-10		10	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 16.5V, V_{SS} = –16.5V Switch state is on V_S = V_D = ±10V Refer to On-Leakage Current	25°C		0.002		nA
			–40°C to +85°C	-20		20	nA
			–40°C to +125°C	-40		40	nA
LOGIC INPUTS (SEL / EN pins)							
I_{IH}	Input leakage current	Logic Inputs = 50V	–40°C to +125°C			1.4	µA
I_{IH}	Input leakage current	Logic Inputs = 1.8V - 5V	–40°C to +125°C			0.6	µA
I_{IL}	Input leakage current		–40°C to +125°C	-0.1	0.00004	0.1	µA
C_{IN}	Logic input capacitance		–40°C to +125°C		4		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 16.5V, V_{SS} = –16.5V Logic inputs = 0V, 5V, or V_{DD}	25°C		105	140	µA
			–40°C to +85°C			155	µA
			–40°C to +125°C			170	µA
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 16.5V, V_{SS} = –16.5V All Switches OFF	–40°C to +125°C			65	µA
$I_{DD\ (1.8V)}$	V_{DD} supply current	V_{DD} = 16.5V, V_{SS} = –16.5V Logic inputs = 1.8V	–40°C to +125°C			175	µA
I_{SS}	V_{SS} supply current	V_{DD} = 16.5V, V_{SS} = –16.5V Logic inputs = 0V, 5V, or V_{DD}	25°C		90	110	µA
			–40°C to +85°C			120	µA
			–40°C to +125°C			130	µA
I_{SSQ}	V_{SS} quiescent supply current	V_{DD} = 16.5V, V_{SS} = –16.5V All Switches OFF	–40°C to +125°C			25	µA
$I_{SS\ (1.8V)}$	V_{SS} supply current	V_{DD} = 16.5V, V_{SS} = –16.5V Logic inputs = 1.8V	–40°C to +125°C			130	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.

(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

5.6 ±15V Dual Supply: Switching Characteristics

V_{DD} = +15V ± 10%, V_{SS} = –15V ± 10%, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +15V, V_{SS} = –15V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 10V R_L = 1kΩ, C_L = 35pF	25°C		240	300	ns
			–40°C to +85°C			315	ns
			–40°C to +125°C			320	ns
t_{OFF}	Turn-off time from control input	V_S = 10V R_L = 1kΩ, C_L = 35pF	25°C		80	100	ns
			–40°C to +85°C			105	ns
			–40°C to +125°C			110	ns
t_{BBM}	Break-before-make time delay (TMUX5413Only)	V_S = 10V, R_L = 1kΩ, C_L = 35pF	25°C		180		ns
			–40°C to +85°C			205	ns
			–40°C to +125°C			210	ns
$t_{ON (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1µs R_L = 1kΩ, C_L = 35pF	25°C		0.04		ms
			–40°C to +85°C		0.05		ms
			–40°C to +125°C		0.06		ms
t_{PD}	Propagation delay	R_L = 50Ω , C_L = 5pF	25°C		400		ps
Q_{INJ}	Charge injection	V_S = 0V, C_L = 100pF	25°C		13		pC
O_{ISO}	Off-isolation	R_L = 50Ω , C_L = 5pF V_S = 0V, f = 100kHz	25°C		-100		dB
O_{ISO}	Off-isolation	R_L = 50Ω , C_L = 5pF V_S = 0V, f = 1MHz	25°C		-82		dB
X_{TALK}	Crosstalk	R_L = 50Ω , C_L = 5pF V_S = 0V, f = 100kHz	25°C		-110		dB
X_{TALK}	Crosstalk	R_L = 50Ω , C_L = 5pF V_S = 0V, f = 1MHz	25°C		-100		dB
BW	–3dB Bandwidth	R_L = 50Ω , C_L = 5pF V_S = 0V	25°C		430		MHz
I_L	Insertion loss	R_L = 50Ω , C_L = 5pF V_S = 0V, f = 1MHz	25°C		-1.6		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62V on V_{DD} and V_{SS} R_L = 50Ω , C_L = 5pF, f = 1MHz	25°C		-59		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 15V, V_{BIAS} = 0V R_L = 10kΩ , C_L = 5pF, f = 20Hz to 20kHz	25°C		0.0004		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0V, f = 1MHz	25°C		5		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0V, f = 1MHz	25°C		5		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0V, f = 1MHz	25°C		12		pF

5.7 48V Single Supply: Electrical Characteristics

V_{DD} = +48V, V_{SS} = 0V, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +48V, V_{SS} = 0V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 5V to 43V I_D = –10mA Refer to On-Resistance	25°C		21	26	Ω
			–40°C to +85°C			32	Ω
			–40°C to +125°C			40	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 5V to 43V I_D = –10mA Refer to On-Resistance	25°C		0.14	1	Ω
			–40°C to +85°C			1.6	Ω
			–40°C to +125°C			1.7	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 5V to 43V I_D = –10mA Refer to On-Resistance	25°C		0.04	0.6	Ω
			–40°C to +85°C			0.7	Ω
			–40°C to +125°C			0.8	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 24V, I_S = –10mA Refer to On-Resistance	–40°C to +125°C		0.085		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 48V, V_{SS} = 0V Switch state is off V_S = 43V / 1V V_D = 1V / 43V Refer to Off-Leakage Current	25°C		0.004		nA
			–40°C to +85°C	–25		25	nA
			–40°C to +125°C	–35		35	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 48V, V_{SS} = 0V Switch state is off V_S = 43V / 1V V_D = 1V / 43V Refer to Off-Leakage Current	25°C		0.004		nA
			–40°C to +85°C	–25		25	nA
			–40°C to +125°C	–35		35	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 44V, V_{SS} = 0V Switch state is on V_S = V_D = 40V or 1V Refer to Section 6.3	25°C		0.004		nA
			–40°C to +85°C	–25		25	nA
			–40°C to +125°C	-35		35	nA
LOGIC INPUTS (SEL / EN pins)							
I_{IL}	Input leakage current		–40°C to +125°C	-0.1	–0.001	0.1	µA
C_{IN}	Logic input capacitance		–40°C to +125°C		5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 48V, V_{SS} = 0V Logic inputs = 0V, 5V, or V_{DD}	25°C		125	155	µA
			–40°C to +85°C			170	µA
			–40°C to +125°C			180	µA
$I_{DD\ (1.8V)}$	V_{DD} supply current	V_{DD} = 48V, V_{SS} = 0V Logic inputs = 1.8V	–40°C to +125°C			190	µA
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 48V, V_{SS} = 0V All Switches OFF	–40°C to +125°C			65	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

5.8 48V Single Supply: Switching Characteristics

V_{DD} = +48V, V_{SS} = 0V, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +48V, V_{SS} = 0V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 18V R_L = 1kΩ, C_L = 35pF	25°C		225	275	ns
			–40°C to +85°C			285	ns
			–40°C to +125°C			295	ns
t_{OFF}	Turn-off time from control input	V_S = 18V R_L = 1kΩ, C_L = 35pF	25°C		90	115	ns
			–40°C to +85°C			120	ns
			–40°C to +125°C			125	ns
$t_{ON (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1µs R_L = 1kΩ, C_L = 35pF	–40°C to +125°C		0.01		ms
t_{PD}	Propagation delay	R_L = 50Ω , C_L = 5pF	25°C		475		ps
Q_{INJ}	Charge injection	V_S = 24V, C_L = 100pF	25°C		13		pC
O_{ISO}	Off-isolation	R_L = 50Ω , C_L = 5pF V_S = 6V, f = 100kHz	25°C		-100		dB
O_{ISO}	Off-isolation	R_L = 50Ω , C_L = 5pF V_S = 6V, f = 1MHz	25°C		-82		dB
X_{TALK}	Crosstalk	R_L = 50Ω , C_L = 5pF V_S = 6V, f = 100kHz	25°C		-110		dB
X_{TALK}	Crosstalk	R_L = 50Ω , C_L = 5pF V_S = 6V, f = 1MHz	25°C		-100		dB
BW	–3dB Bandwidth	R_L = 50Ω , C_L = 5pF V_S = 6V	25°C		400		MHz
I_L	Insertion loss	R_L = 50Ω , C_L = 5pF V_S = 6V, f = 1MHz	25°C		-1.6		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62V on V_{DD} and V_{SS} R_L = 50Ω , C_L = 5pF, f = 1MHz	25°C		-62		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 24V, V_{BIAS} = 24V R_L = 10kΩ , C_L = 5pF, f = 20Hz to 20kHz	25°C		0.0003		%
$C_{S(OFF)}$	Source off capacitance	V_S = 24V, f = 1MHz	25°C		5		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 24V, f = 1MHz	25°C		5		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 24V, f = 1MHz	25°C		12		pF

5.9 12 V Single Supply: Electrical Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 10 V I_D = –10 mA Refer to On-Resistance	25°C		42	50	Ω
			–40°C to +85°C			70	Ω
			–40°C to +125°C			75	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 10 V I_D = –10 mA Refer to On-Resistance	25°C		0.4	1.3	Ω
			–40°C to +85°C			1.5	Ω
			–40°C to +125°C			1.6	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 10 V I_S = –10 mA Refer to On-Resistance	25°C		21	25	Ω
			–40°C to +85°C			35	Ω
			–40°C to +125°C			40	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 6 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.085		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V Refer to Off-Leakage Current	25°C		0.01		nA
			–40°C to +85°C	-25		25	nA
			–40°C to +125°C	-35		35	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V Refer to Off-Leakage Current	25°C		0.01		nA
			–40°C to +85°C	-25		25	nA
			–40°C to +125°C	-35		35	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is on V_S = V_D = 10 V or 1 V Refer to On-Leakage Current	25°C		0.01		nA
			–40°C to +85°C	–25		25	nA
			–40°C to +125°C	–35		35	nA
LOGIC INPUTS (SEL / EN pins)							
C_{IN}	Logic input capacitance		–40°C to +125°C		5.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		115	135	µA
			–40°C to +85°C			150	µA
			–40°C to +125°C			165	µA
$I_{DD\ (1.8V)}$	V_{DD} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V Logic inputs = 1.8 V	–40°C to +125°C			170	µA
I_{DDQ}	V_{DD} quiescent supply current	V_{DD} = 13.2 V, V_{SS} = 0 V All Switches OFF	–40°C to +125°C			50	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

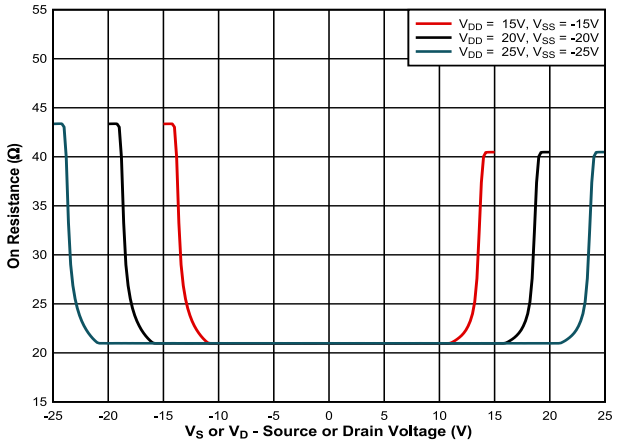
5.10 12V Single Supply: Switching Characteristics

V_{DD} = +12V ± 10%, V_{SS} = 0V, GND = 0V (unless otherwise noted)
Typical at V_{DD} = +12V, V_{SS} = 0V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from control input	V_S = 8V R_L = 1kΩ, C_L = 35pF	25°C		250	300	ns
			–40°C to +85°C			310	ns
			–40°C to +125°C			320	ns
t_{OFF}	Turn-off time from control input	V_S = 8V R_L = 1kΩ, C_L = 35pF	25°C		85	120	ns
			–40°C to +85°C			125	ns
			–40°C to +125°C			130	ns
$t_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1µs R_L = 1kΩ, C_L = 35pF	25°C		0.06		ms
t_{PD}	Propagation delay	R_L = 50Ω , C_L = 5pF	25°C		500		ps
Q_{INJ}	Charge injection	V_S = 6V, C_L = 100pF	25°C		7		pC
O_{ISO}	Off-isolation	R_L = 50Ω , C_L = 5pF V_S = 6V, f = 100kHz	25°C		-100		dB
O_{ISO}	Off-isolation	R_L = 50Ω , C_L = 5pF V_S = 6V, f = 1MHz	25°C		--82		dB
X_{TALK}	Crosstalk	R_L = 50Ω , C_L = 5pF V_S = 6V, f = 100kHz	25°C		--110		dB
X_{TALK}	Crosstalk	R_L = 50Ω , C_L = 5pF V_S = 6V, f = 1MHz	25°C		-100		dB
BW	–3dB Bandwidth	R_L = 50Ω , C_L = 5pF V_S = 6V	25°C		375		MHz
I_L	Insertion loss	R_L = 50Ω , C_L = 5pF V_S = 6V, f = 1MHz	25°C		-1.6		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62V on V_{DD} and V_{SS} R_L = 50Ω , C_L = 5pF, f = 1MHz	25°C		-56		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 6V, V_{BIAS} = 6V R_L = 10kΩ , C_L = 5pF, f = 20Hz to 20kHz	25°C		0.004		%
$C_{S(OFF)}$	Source off capacitance	V_S = 6V, f = 1MHz	25°C		6		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 6V, f = 1MHz	25°C		6		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 6V, f = 1MHz	25°C		14.5		pF

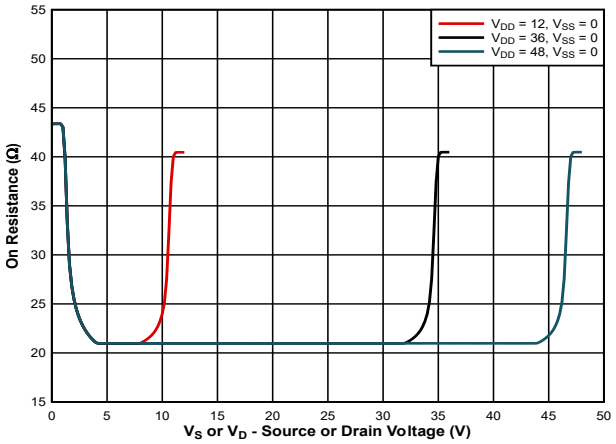
5.11 Typical Characteristics

at T_A = 25°C (unless otherwise noted)



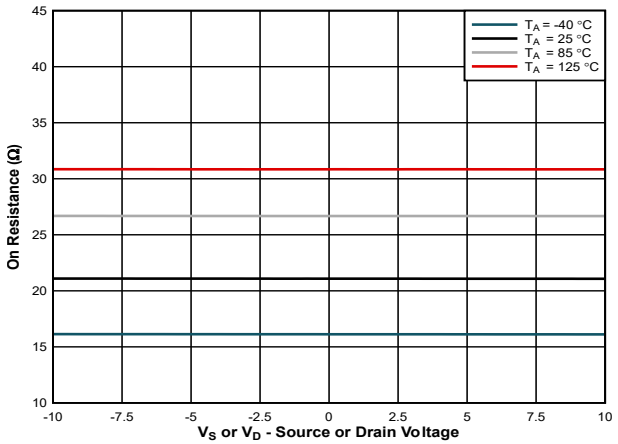
T_A = 25°

Figure 5-1. On-Resistance vs Source or Drain Voltage for Dual Supply



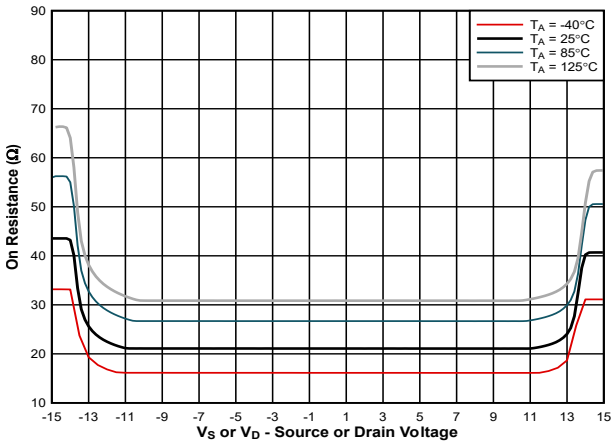
T_A = 25°

Figure 5-2. On-Resistance vs Source or Drain Voltage for Single Supply



V_{DD}=15V, V_{SS}=-15V

Figure 5-3. On-Resistance vs Source or Drain Operational Voltage (Flat Region)

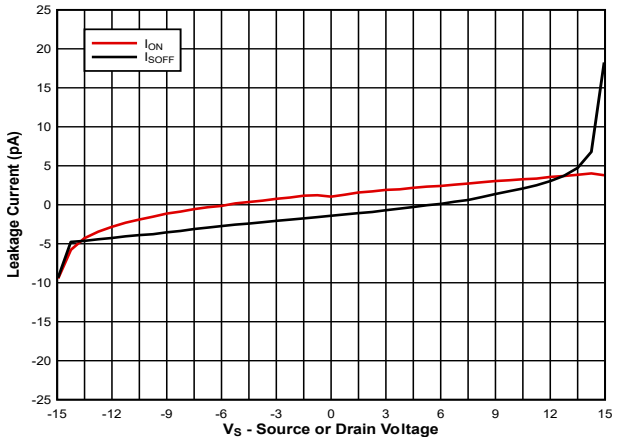


V_{DD} = 15V, V_{SS} = -15V

Figure 5-4. On-Resistance vs Source or Drain Voltage

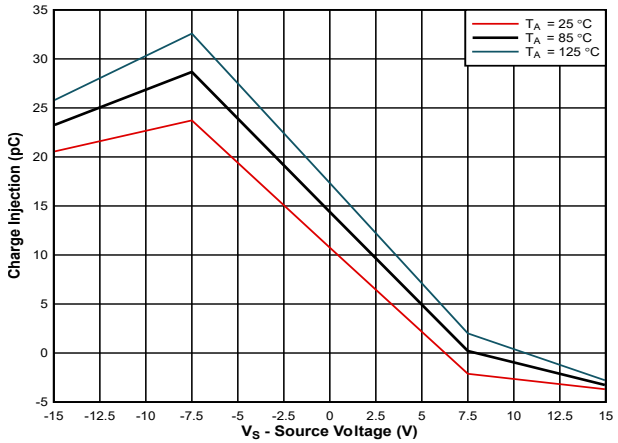
5.11 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



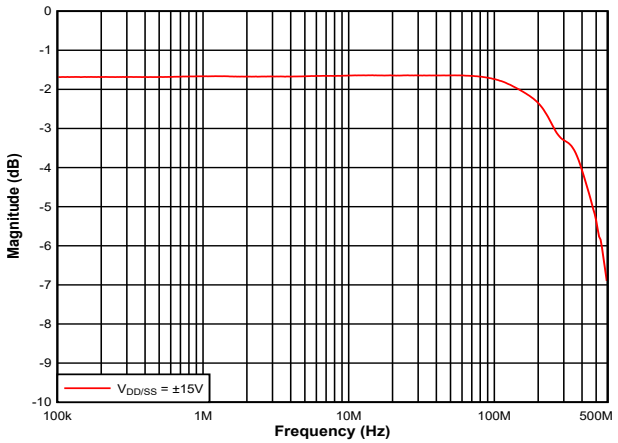
V_{DD} = 15V, V_{SS} = -15V; T_A = 25°

Figure 5-5. Leakage Current vs Bias Voltage



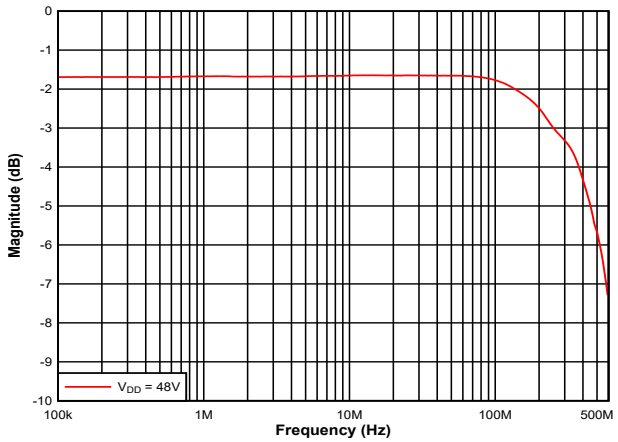
V_{DD} = 15V, V_{SS} = -15V

Figure 5-6. Charge Injection vs Source Voltage



V_{DD} = 15V, V_{SS} = -15V

Figure 5-7. ±15V Bandwidth vs. Frequency



V_{DD} = 48V, V_{SS} = GND

Figure 5-8. 48V Bandwidth vs. Frequency

6 Parameter Measurement Information

6.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. Figure 6-1 shows the measurement setup used to measure R_{ON}. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:

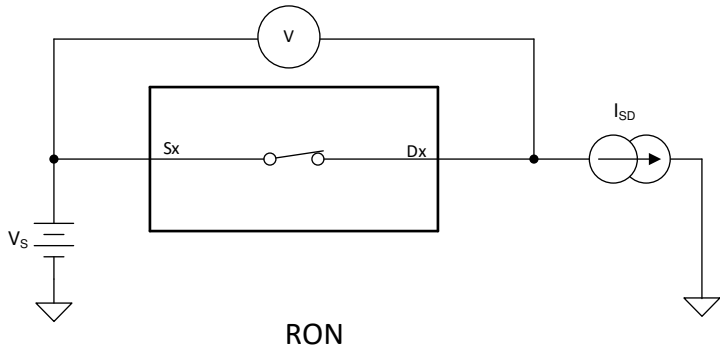


Figure 6-1. On-Resistance Measurement Setup

6.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current.
2. Drain off-leakage current.

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

Figure 6-2 shows the setup used to measure both off-leakage currents.

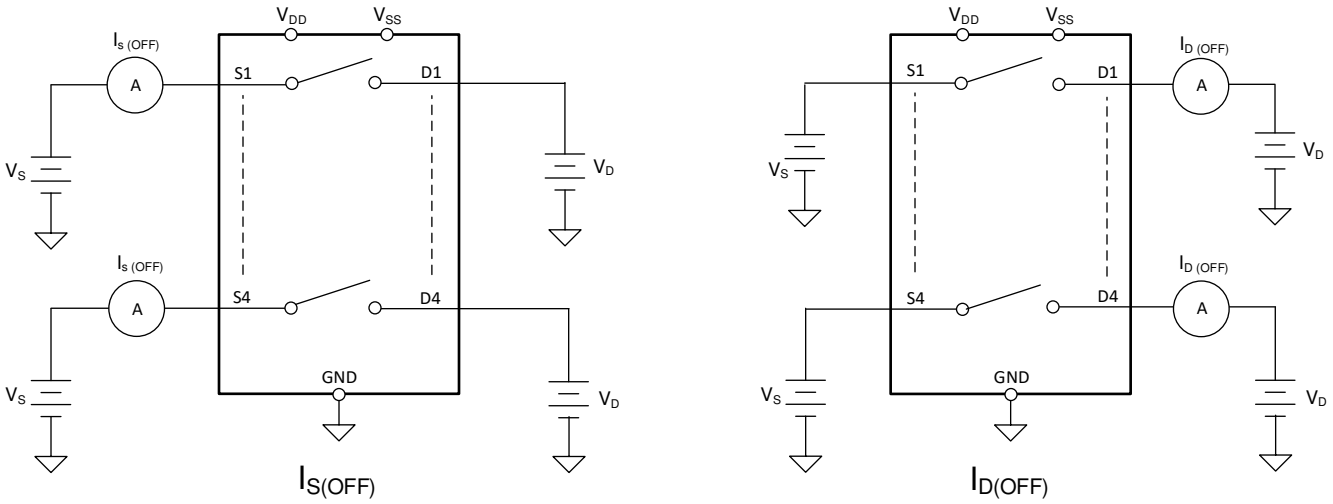


Figure 6-2. Off-Leakage Measurement Setup

6.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 6-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

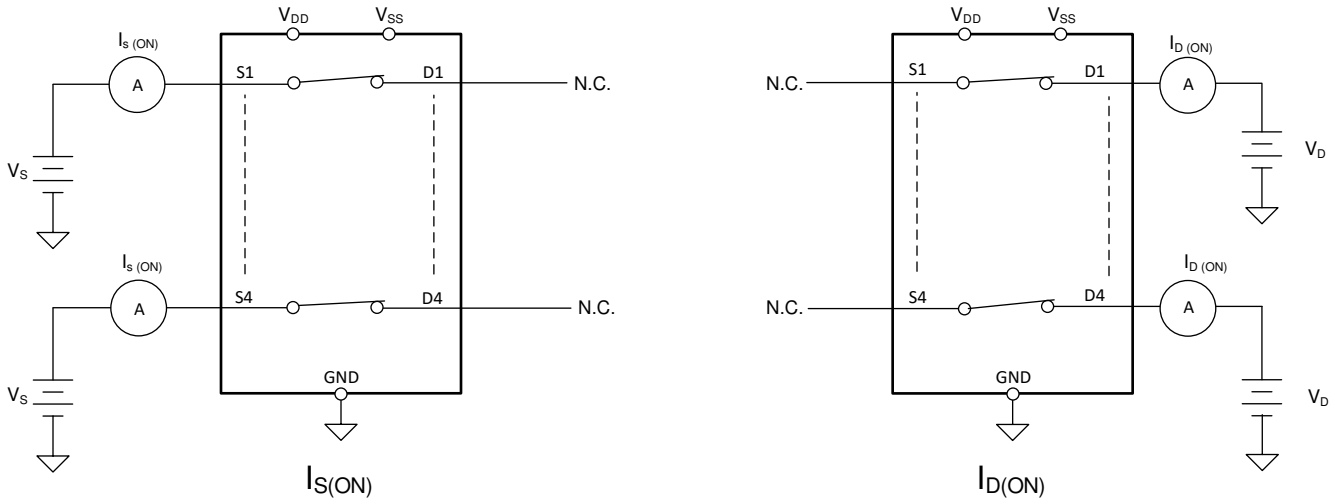


Figure 6-3. On-Leakage Measurement Setup

6.4 t_{ON} and t_{OFF} Time

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-4 shows the setup used to measure turn-on time, denoted by the symbol t_{ON}.

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-4 shows the setup used to measure turn-off time, denoted by the symbol t_{OFF}.

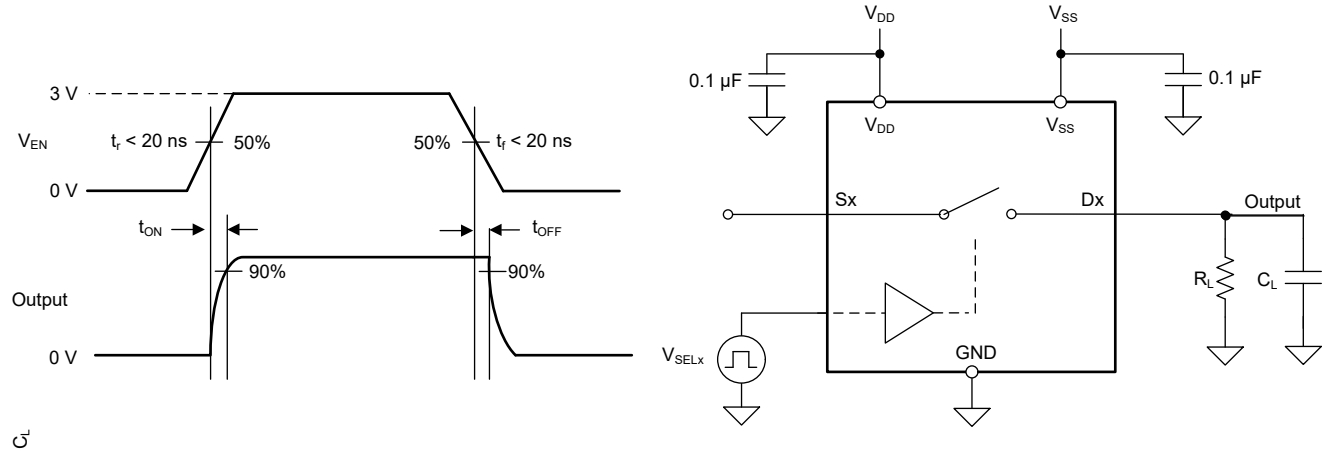


Figure 6-4. Turn-On and Turn-Off Time Measurement Setup

6.5 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 6-5 shows the setup used to measure propagation delay, denoted by the symbol t_{PD}.

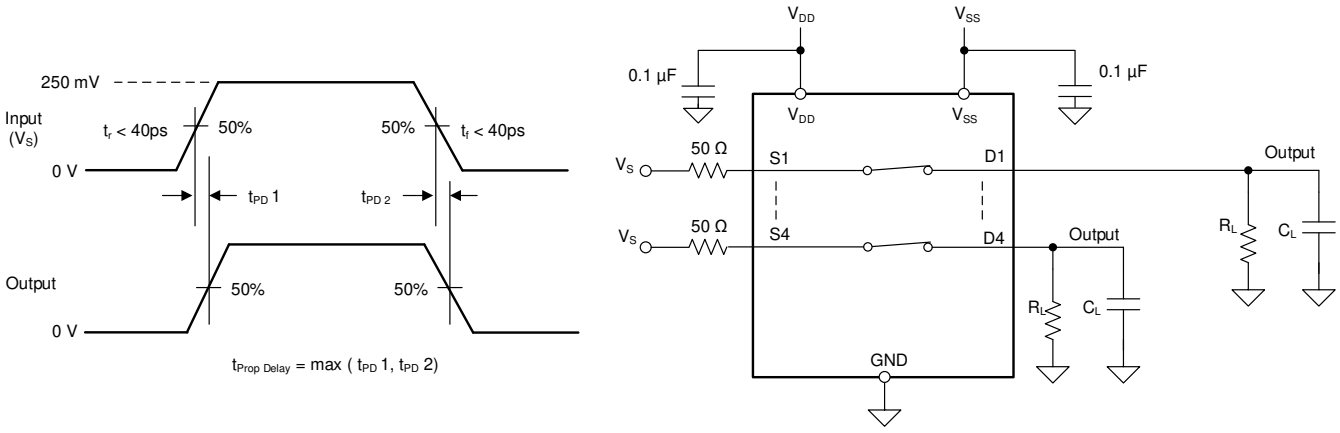


Figure 6-5. Propagation Delay Measurement Setup

6.6 Charge Injection

This device has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. Figure 6-6 shows the setup used to measure charge injection from source (Sx) to drain (Dx).

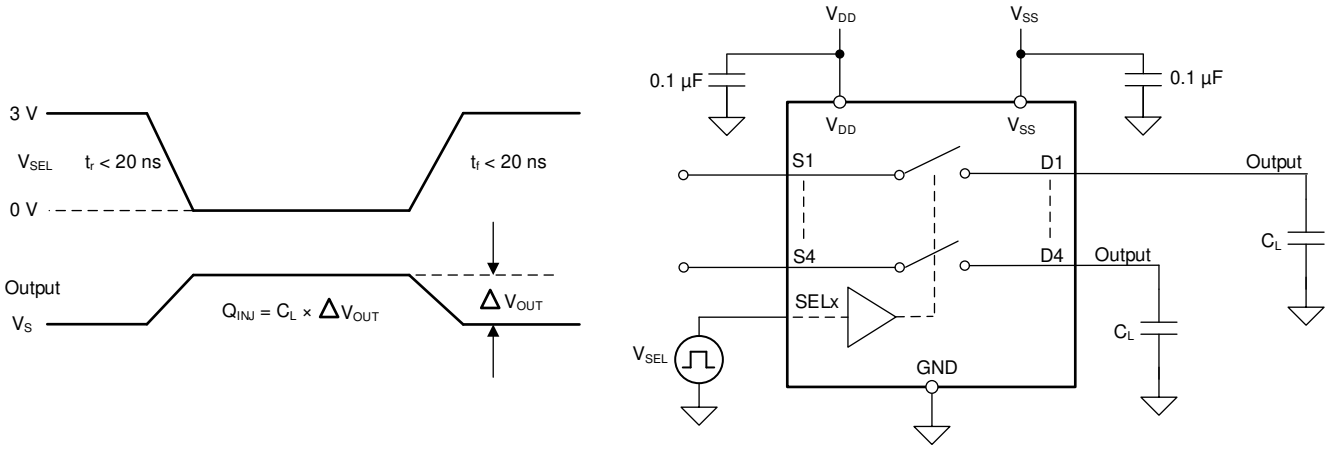
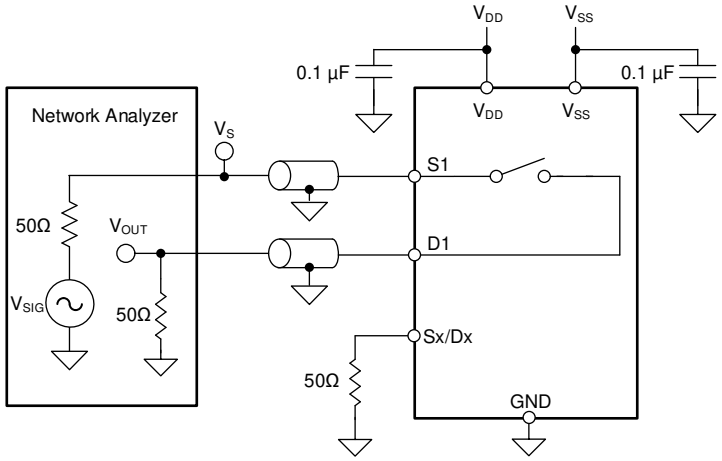


Figure 6-6. Charge-Injection Measurement Setup

6.7 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance, Z_0, for the measurement is 50Ω. Figure 6-7 shows the setup used to measure off isolation. Use off isolation equation to compute off isolation.

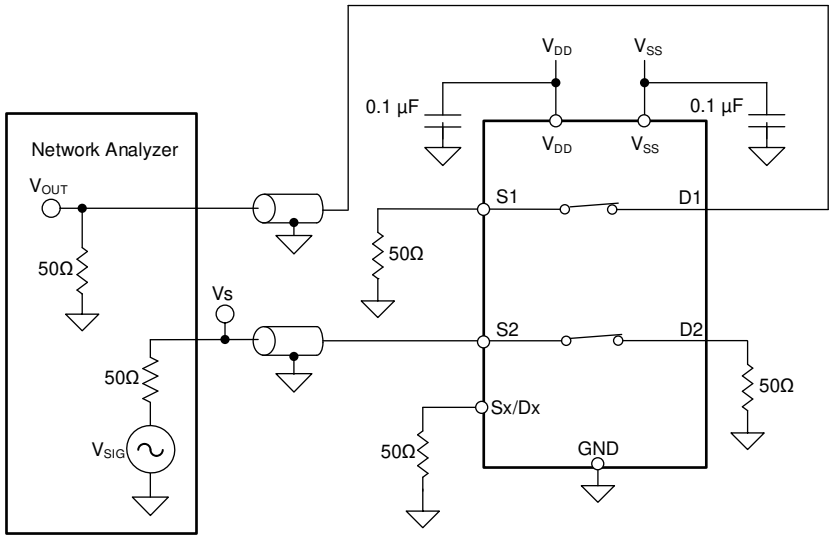


$$Off\ Isolation = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 6-7. Off Isolation Measurement Setup

6.8 Channel-to-Channel Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (Dx) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. The characteristic impedance, Z_0, for the measurement is 50Ω. Figure 6-8 shows the setup used to measure, and the equation used to compute crosstalk.

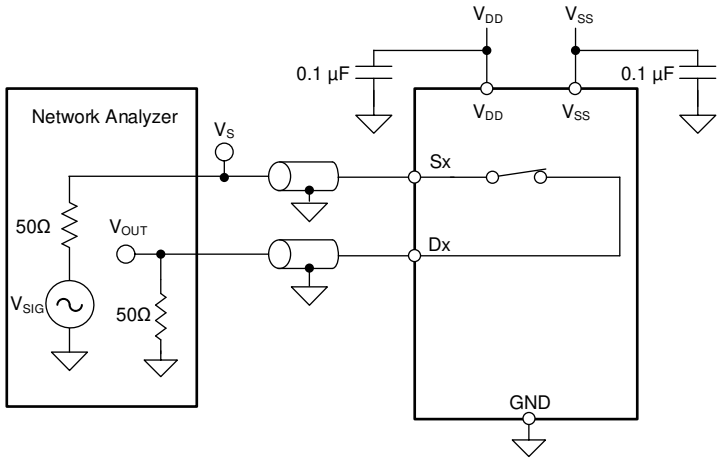


$$Crosstalk = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 6-8. Channel-to-Channel Crosstalk Measurement Setup

6.9 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the device. The characteristic impedance, Z_0, for the measurement is 50Ω. Figure 6-9 shows the setup used to measure bandwidth.



$$Bandwidth = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 6-9. Bandwidth Measurement Setup

6.10 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD + N.

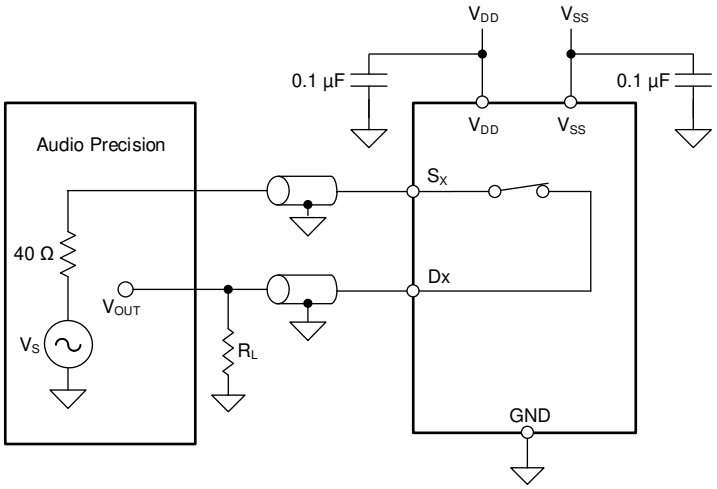
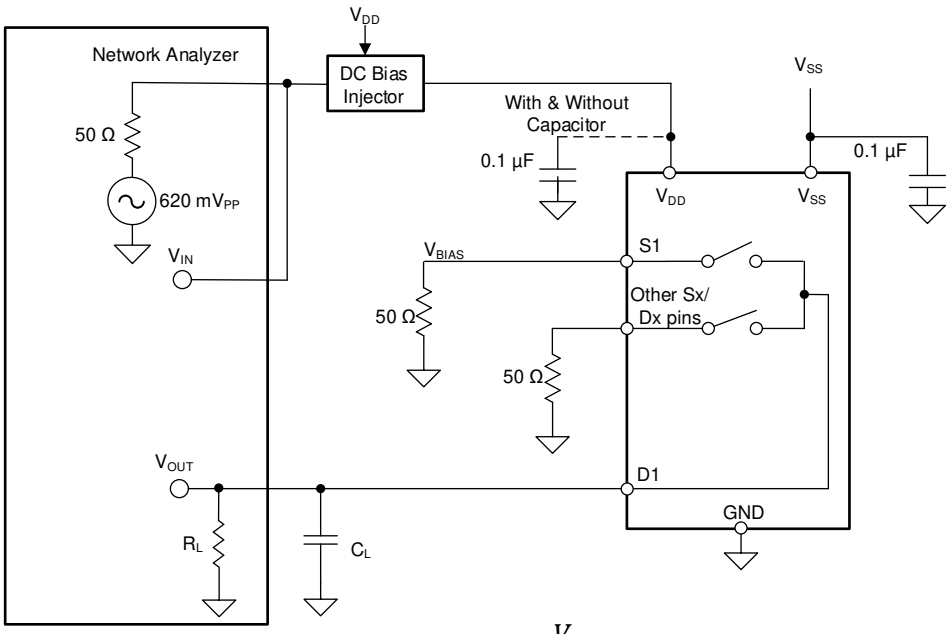


Figure 6-10. THD + N Measurement Setup

6.11 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 100mV$_{PP}$. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the AC PSRR.



$$PSRR = 20 \times Log \frac{V_{OUT}}{V_{IN}}$$

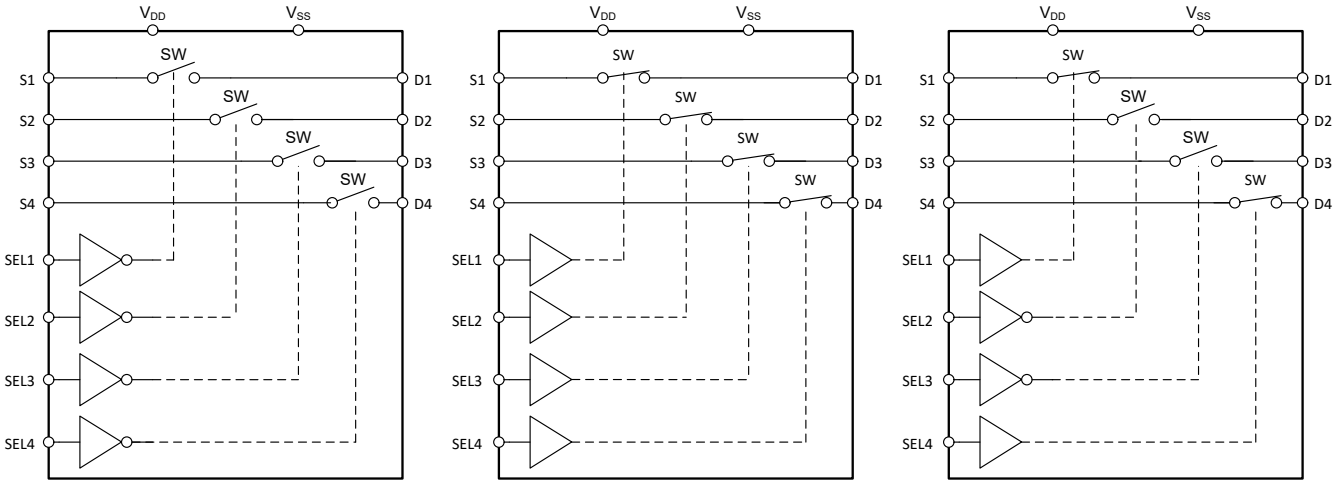
Figure 6-11. AC PSRR Measurement Setup

7 Detailed Description

7.1 Overview

TMUX541x is a 1:1 (SPST), 4-channel switch. This device has four independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the state of the corresponding select pin. This device works well with dual supplies, a single supply, or asymmetric supplies such as V_{DD} = 37.5V, V_{SS} = –12.5V.

7.2 Functional Block Diagram



TMUX5411
(SELx = Logic 1)

TMUX5412
(SELx = Logic 1)

TMUX5413
(SELx = Logic 1)

7.3 Feature Description

7.3.1 Bidirectional Operation

The TMUX541x conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has similar characteristics in both directions and supports both analog and digital signals.

7.3.2 Rail-to-Rail Operation

The valid signal path input and output voltage for TMUX541x ranges from V_{SS} to V_{DD}.

7.3.3 1.8 V Logic Compatible Inputs

The TMUX541x has 1.8V logic compatible control for all logic control inputs. 1.8V logic level inputs allows the TMUX541x to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8V logic implementations, refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

7.3.4 Flat On-Resistance

The TMUX541x is designed with a special switch architecture to produce ultra-flat on-resistance (RON) across most of the switch input operating region. The flat RON response allows the device to be used in a wide variety of applications since the RON is controlled regardless of the signals sampled. The architecture is implemented without a charge pump so unwanted noise is not produced from the device to affect sampling accuracy.

This architecture also keeps RON the same regardless of the supply voltage. The flattest on-resistance region extends roughly from 5V above VSS to 5V below VDD. As long as this headroom is maintained, the TMUX541x exhibits an extremely linear response.

7.3.5 Power-Up Sequence Free

The TMUX541x supports any power up sequencing. With the supply rails (VDD and VSS), any rail can be powered on first. Similarly, when powering down the supply rails can be powered down in any order.

7.4 Device Functional Modes

The TMUX541x has four independently selectable single-pole, single-throw switches that are turned-on or turned-off based on the state of the corresponding select pin. The control pins operate down to 1.8V logic and can be as high as 48V.

The TMUX541x devices can be operated without any external components except for the supply decoupling capacitors. The SELx pins have internal pull-down resistors.

7.4.1 Truth Tables

TMUX5412 Truth Table provides the truth table for TMUX541x.

Table 7-1. TMUX5411 Truth Table

SEL x (1)	CHANNEL x
0	Channel x ON
1	Channel x OFF

Table 7-2. TMUX5412 Truth Table

SEL x (1)	CHANNEL x
0	Channel x OFF
1	Channel x ON

Table 7-3. TMUX5413 Truth Table

SEL1	SEL2	SEL3	SEL4	ON / OFF CHANNELS(1)
0	X	X	X	CHANNEL 1 OFF
1	X	X	X	CHANNEL 1 ON
X	0	X	X	CHANNEL 2 ON
X	1	X	X	CHANNEL 2 OFF
X	X	0	X	CHANNEL 3 ON
X	X	1	X	CHANNEL 3 OFF
X	X	X	0	CHANNEL 4 OFF
X	X	X	1	CHANNEL 4 ON

(1) x denotes 1, 2, 3, or 4 for the corresponding channel.

8 Application and Implementation

Note

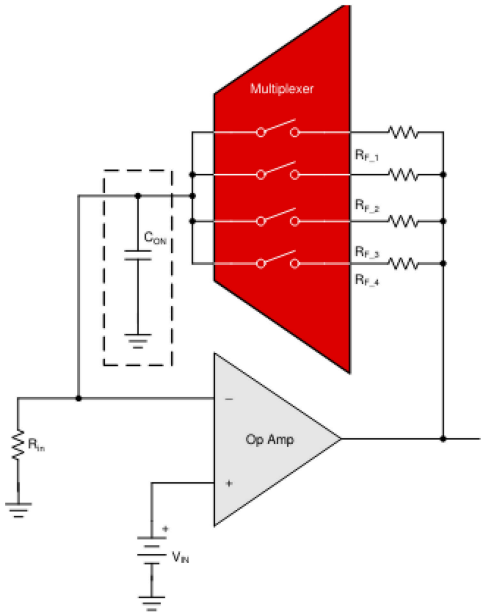
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TMUX541x is a part of the general purpose switches and multiplexers family of devices. The device operates with dual supplies (±4.5V to ±25V), a single supply (4.5V to 50V), or asymmetric supplies (such as V_{DD} = 37.5V, V_{SS} = –12.5V), and offers a true rail-to-rail input and output signal range. The TMUX541x offers a low R_{ON}, low on and off leakage currents, and high bandwidth. These features make the TMUX541x a great option for broad range of high-voltage industrial applications.

8.1.1 Typical Application - Gain Switching

In some applications, such as audio, changes in signal amplification are needed often. Commonly a multiplexer is used to switch between gain resistors, but when your system is operating at ±15V or higher it's challenging to find an appropriate option. TMUX541x is TI's first line of high-voltage general purpose multiplexers that give a cost-efficient option for high voltage applications such as these.



Gain Switching Example

Figure 8-1. On-Resistance vs Source or Drain Voltage

8.1.1.1 Design Requirements

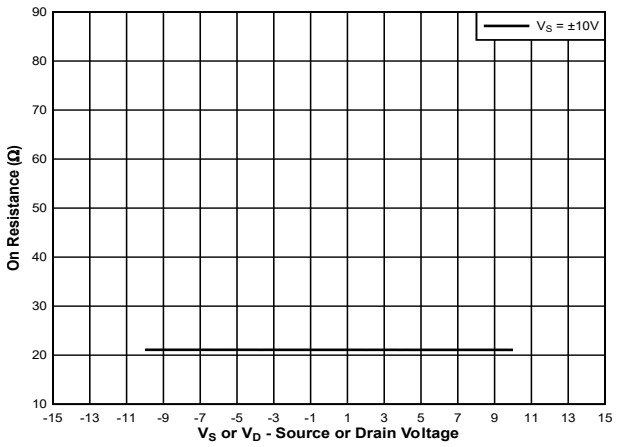
For this design example, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	15V
Supply (V_{SS})	–15V
Input / Output signal range	–15V to 15V (Rail-to-Rail operation)
	–10V to 10V (Best performance with headroom)
Max current through each channel	30mA
Control logic thresholds	1.8V compatible

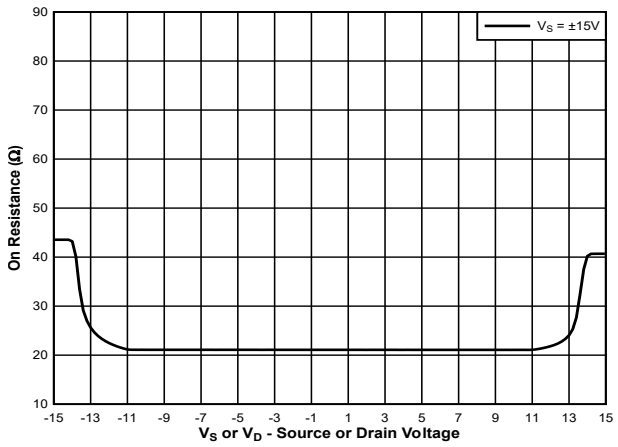
8.1.1.2 Application Curve

TMUX541x has very flat R_{ON}; however, when the signal approaches within 5V of either supply the R_{ON} increases. The plots below show two scenarios: 1. operating with the signal range 5V away from the supply rail and 2. operating with the signal range up to the supply rail.



V_{DD} = 15 V, V_{SS} = -15 V

Figure 8-2. On-Resistance vs Source or Drain Voltage up to ±10V



V_{DD} =15 V, V_{SS} = -15 V

Figure 8-3. On-Resistance vs Source or Drain Voltage up to ±15V

8.2 Power Supply Recommendations

The TMUX541x device operates across a wide supply range of ±4.5V to ±25V (4.5V to 50V in single-supply mode). The device also performs well with asymmetrical supplies such as V_{DD} = 37.5V and V_{SS} = –12.5V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1µF to 10µF at both the V_{DD} and V_{SS} pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always make sure a solid ground (GND) connection is established before supplies are ramped.

8.3 Layout

8.3.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 8-4 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

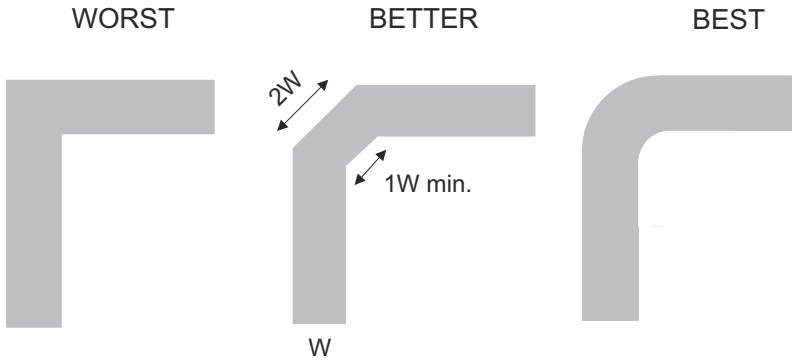


Figure 8-4. Trace Example

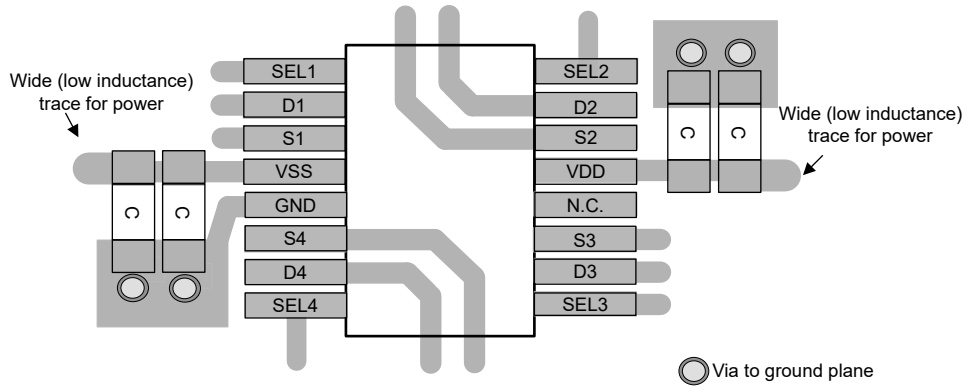
Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Figure 8-5 shows an example of a PCB layout with the TMUX541x.

Some key considerations are:

- For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD/VSS and GND. We recommend a 0.1µF and 1µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

8.3.2 Layout Example



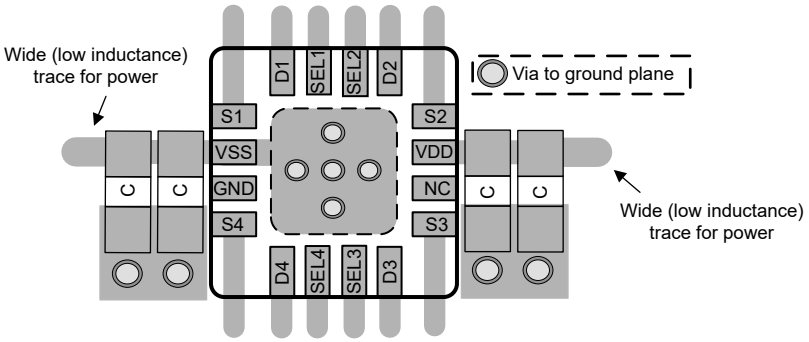


Figure 8-5. TMUX541x Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *When to Replace a Relay with a Multiplexer* application brief
- Texas Instruments, *Improving Signal Measurement Accuracy in Automated Test Equipment* application brief
- Texas Instruments, *Sample & Hold Glitch Reduction for Precision Outputs Reference Design* reference guide
- Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches* application brief
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers* application note
- Texas Instruments, *QFN/SON PCB Attachment* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2025) to Revision A (September 2025)	Page
• Updated data sheet status from *Advanced Information* to *Production Data*	1

DATE	REVISION	NOTES
July 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PTMUX5411DYYR	Active	Preproduction	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTMUX5411PWR	Active	Preproduction	TSSOP (PW) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTMUX5412DYYR	Active	Preproduction	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTMUX5412PWR	Active	Preproduction	TSSOP (PW) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTMUX5413DYYR	Active	Preproduction	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
PTMUX5413PWR	Active	Preproduction	TSSOP (PW) | 16	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TMUX5411DYYR	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM5411
TMUX5411PWR	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM5411
TMUX5412DYYR	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM5412
TMUX5412PWR	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM5412
TMUX5413DYYR	Active	Production	SOT-23-THIN (DYY) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM5413
TMUX5413PWR	Active	Production	TSSOP (PW) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM5413

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

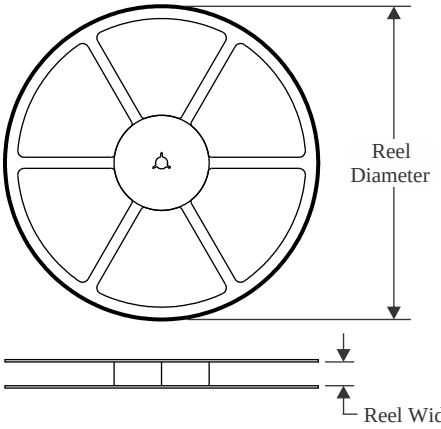
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

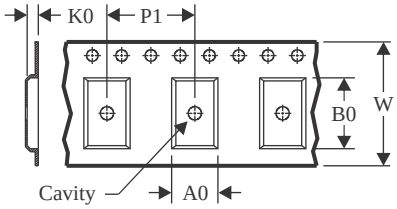
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

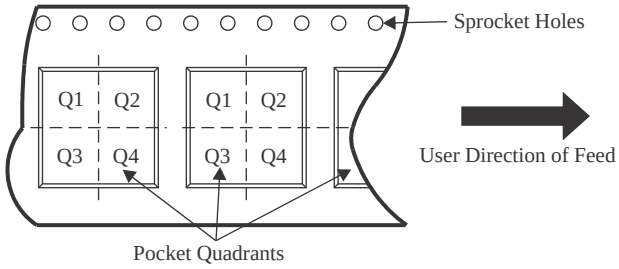


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

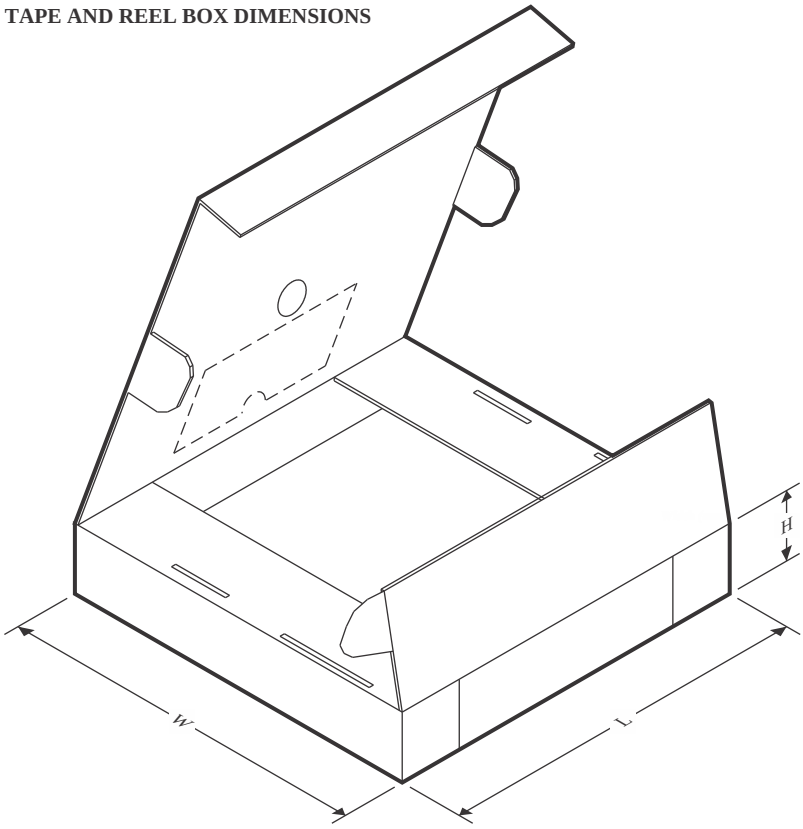
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX5411DYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TMUX5411PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX5412DYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TMUX5412PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX5413DYYR	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TMUX5413PWR	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

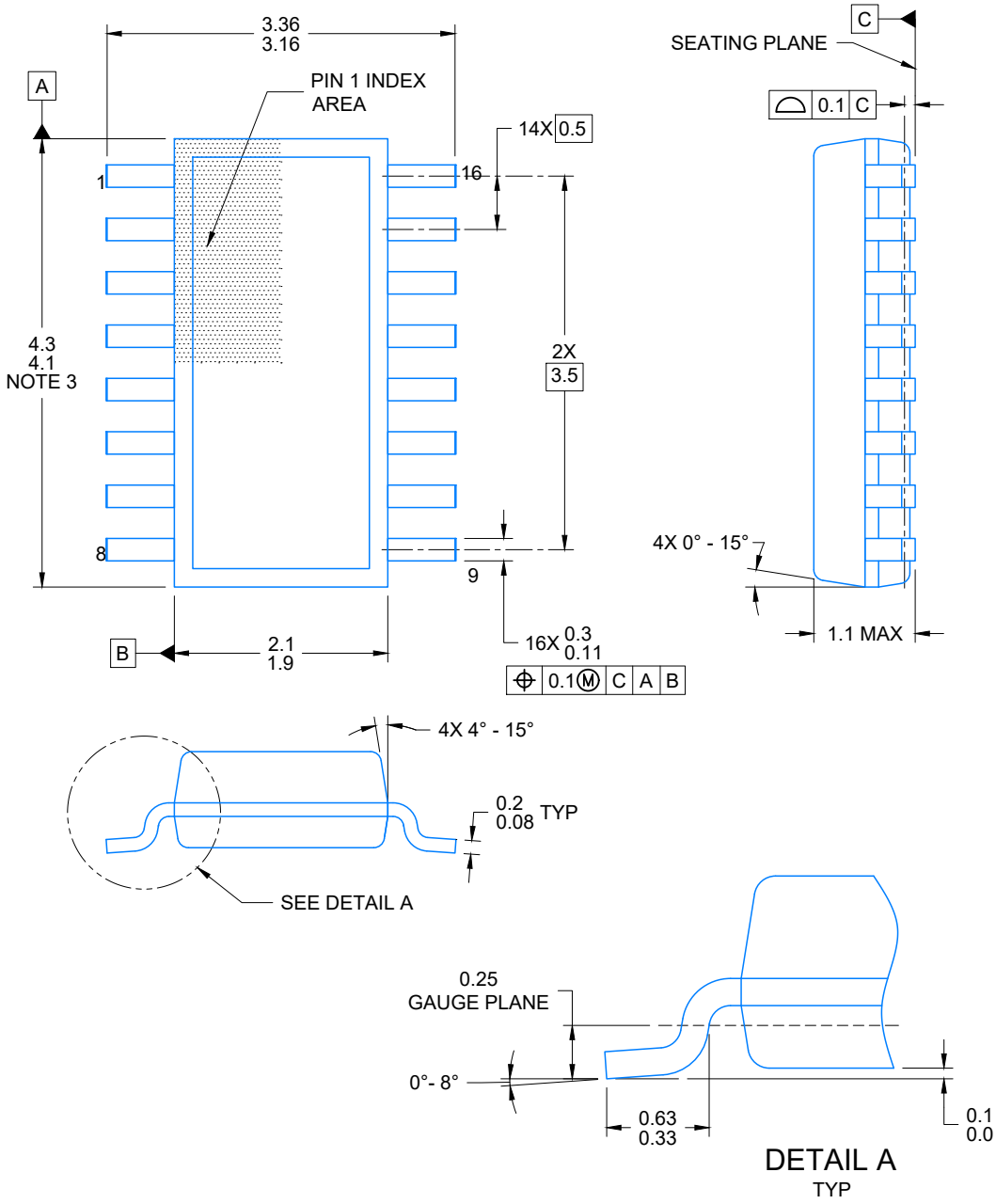
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX5411DYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
TMUX5411PWR	TSSOP	PW	16	3000	353.0	353.0	32.0
TMUX5412DYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
TMUX5412PWR	TSSOP	PW	16	3000	353.0	353.0	32.0
TMUX5413DYYR	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
TMUX5413PWR	TSSOP	PW	16	3000	353.0	353.0	32.0

PACKAGE OUTLINE

DYY0016A

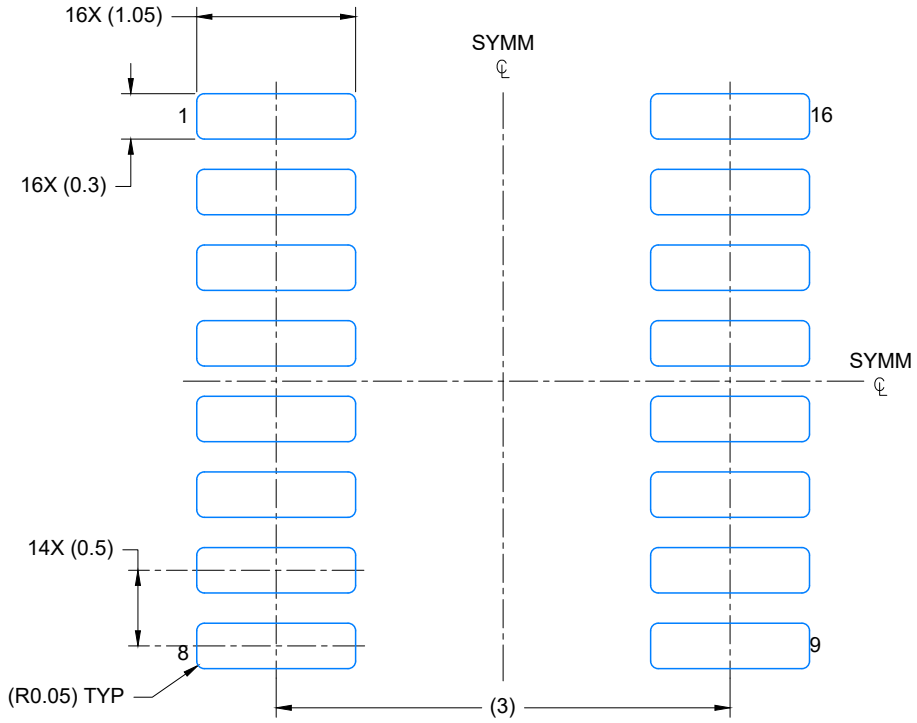
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

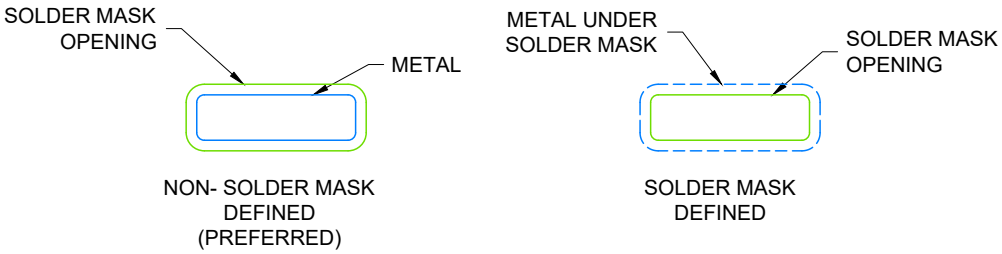


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224642/D 07/2024

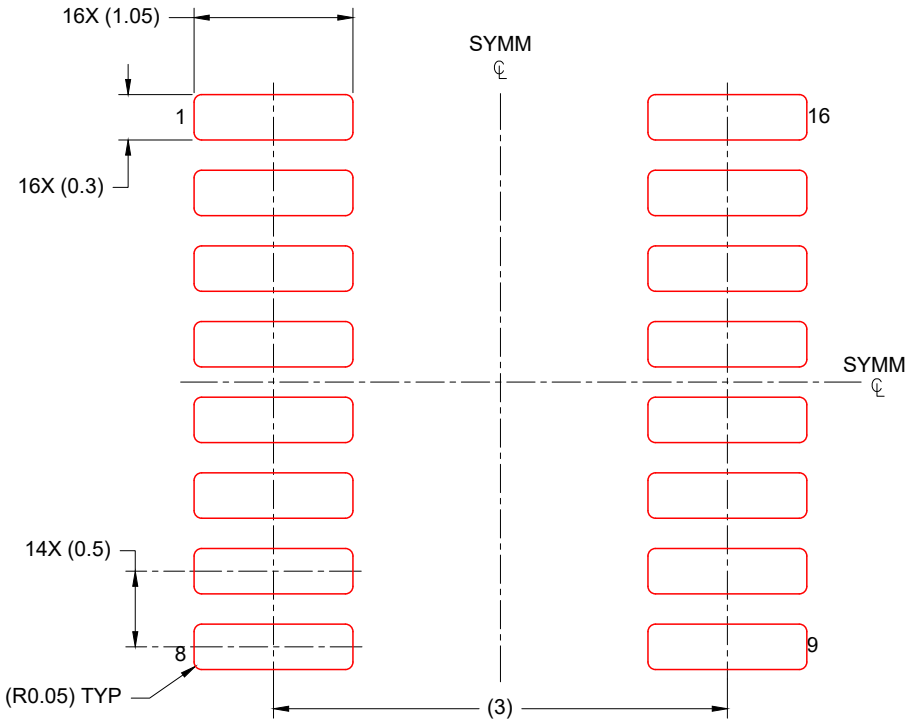
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

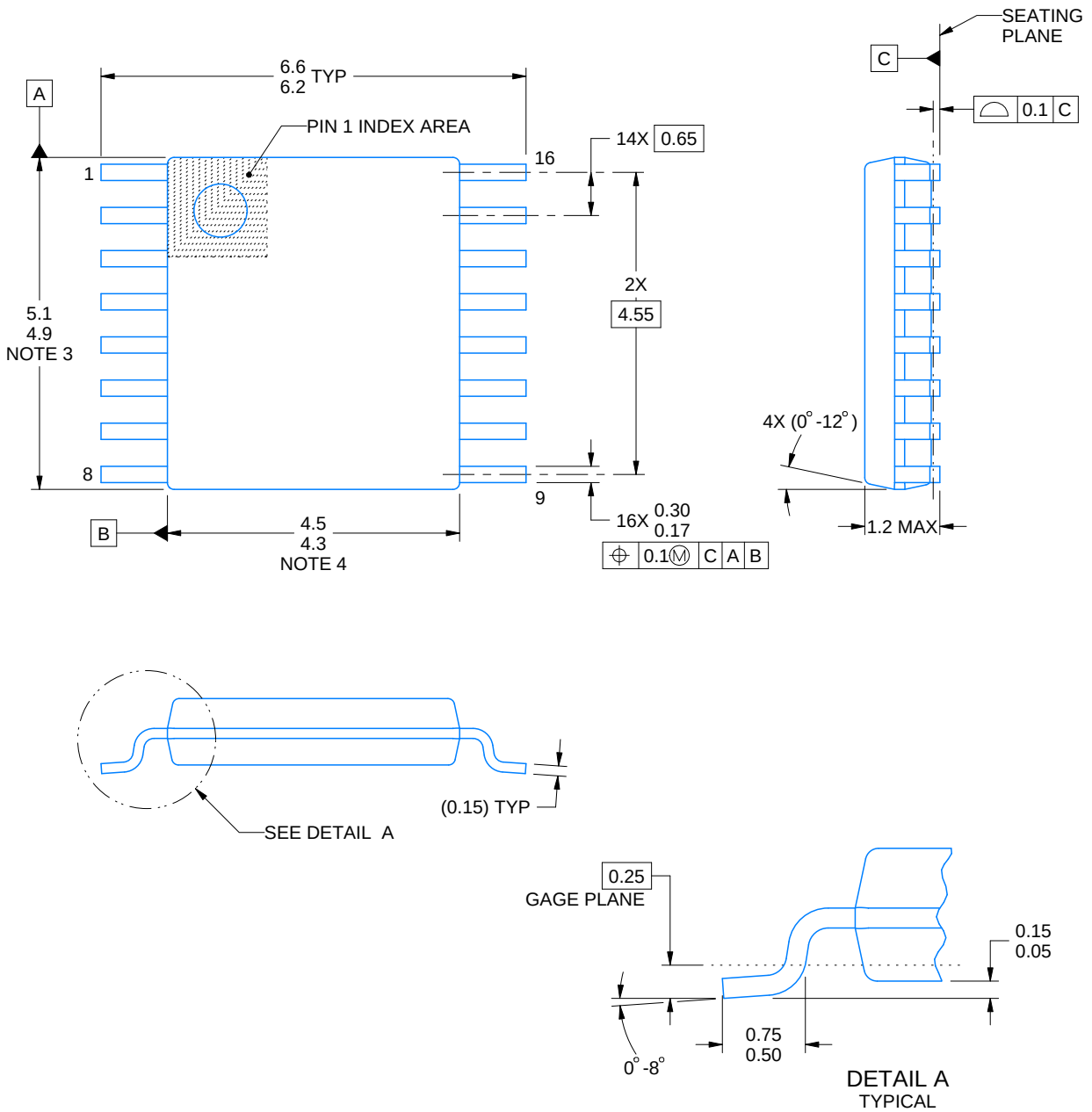
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0016A

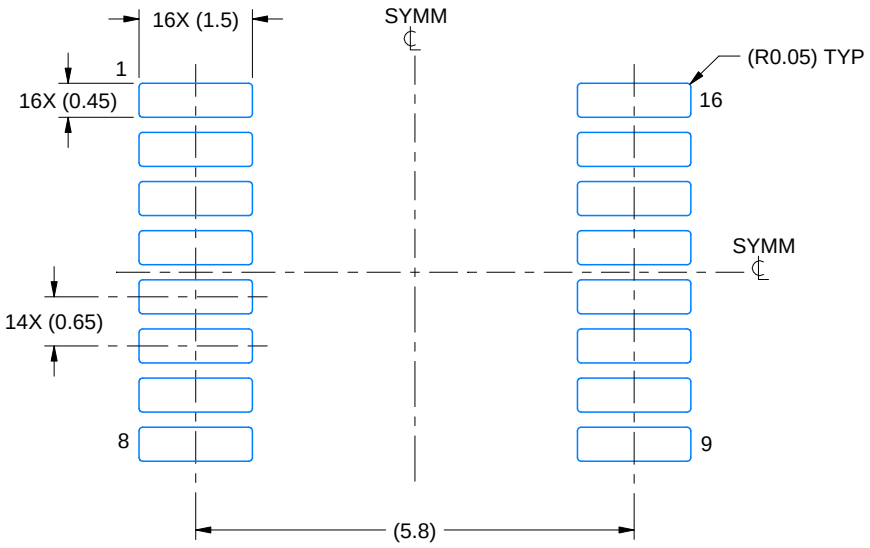
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



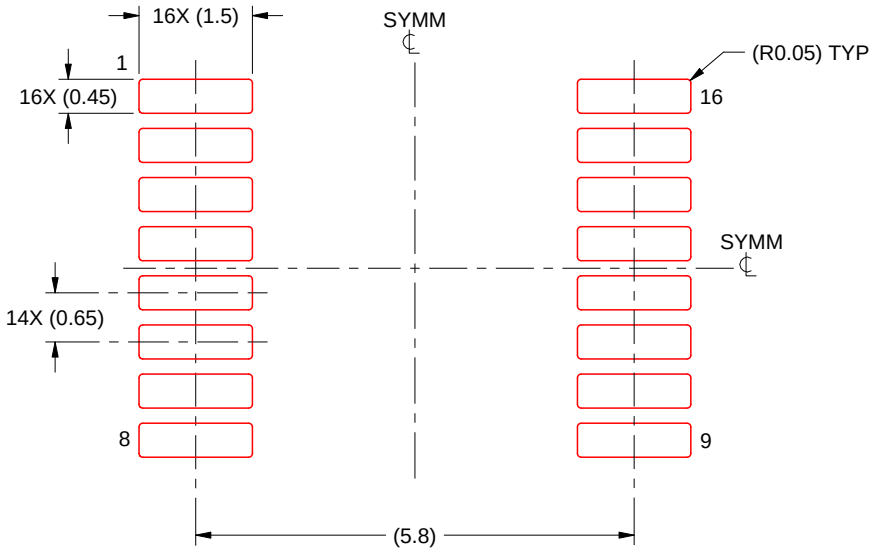
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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Last updated 10/2025