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TEXAS INSTRUMENTS

TMUX582F-SEP
SCDS460 – JUNE 2023

TMUX582F-SEP ±60-V Protected, Latch-up Immune 8:1 Multiplexer with Adjustable Fault Thresholds in Space Enhanced Plastic

1 Features

- Radiation hardened
- Single event latch-up (SEL) immune to 43 MeV-cm2/mg at 125°C
- ELDRS free to 30 krad(Si)
- Total ionizing dose (TID) RLAT for every wafer lot up to 20 krad(Si)
- TID characterized up to 50 krad(Si)
- Space enhanced plastic
- Supply range: 8 V to 22 V or ±5 V to ±16.5 V
- Integrated powered-off and overvoltage protection:
  - Overvoltage tolerance up to 85 V from source to supplies or to drain
  - Overvoltage and power-off protected up to ±60 V
  - Cold sparing capable up to ±60 V
  - Adjustable fault threshold thresholds (Vfp and Vfn) from 5 V to supplies
  - Interrupt flag feedback indicating faulted channel
  - Non-fault channels continue to operate with low leakage currents
- Latch-up immune construction
- Precision performance with 100 pA typical leakage current, 3.5 pF capacitance, and 1% Ron flatness
- Operating temperature from –55°C to +125°C
- Controlled baseline
- Gold wire
- NiPdAu lead finish
- Extended product life cycle
- Extended product-change notification
- Product traceability
- Enhanced mold compound for low outgassing
- Small, industry standard TSSOP-20 packaging

2 Applications

- Low earth orbit (LEO) space applications
- Remote interface unit (RIU)
- Remote telemetry unit (RTU)
- System monitoring for space
- Latch-up and overvoltage detection
- Power-up sequencing protection
- Satellite telemetry and telecommand for onboard data handling
- Sensor data acquisition

3 Description

The TMUX582F-SEP is a modern 8:1 multiplexer suitable for both single ended and differential operation. This latch-up immune device offers robust overvoltage protection up to ±60 V making it optimal for harsh space environments. Additionally, this protection operates in powered-on, powered-off, and floating supply conditions.

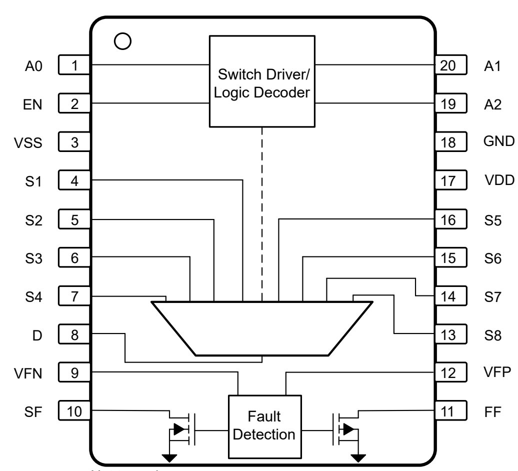
During a fault such as an overvoltage or undervoltage event, the offending channel turns OFF and the Sx pin becomes high impedance. If this fault channel is selected, the drain (D) is pulled to the fault rail that is exceeded (Vfp or Vfn). All other Sx pins which are not under fault continue to operate normally. During normal operation, when the source (Sx) does not exceed Vfp or Vfn, the switch operates with low leakage, low capacitance and an ultra-flat on-resistance. This provides high performance signal integrity with minimal distortion.

The TMUX582F-SEP is a fault protected CMOS multiplexer flexible enough to handle almost any application, from system monitoring, to power-up sequencing protection, to high precision front end data acquisition.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMUX582F-SEP	PW (TSSOP, 20)	6.5 mm × 6.4 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Revision History

DATE	REVISION	NOTES
June 2022	*	Initial Release

5 Pin Configuration and Functions

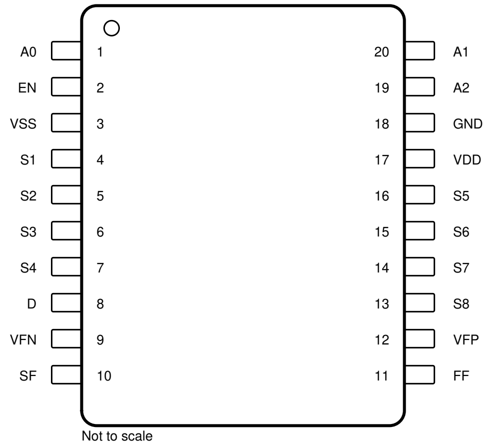

Figure 5-1. PW Package, 20-Pin TSSOP (Top View)

Table 5-1. Pin Functions: TMUX582F-SEP

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A0	1	I	Logic control input address 0 (A0). The pin has a weak internal pull-down. This pin can also be used together with the specific fault pin (SF) to indicate which input is under fault.
EN	2	I	Active high digital enable (EN) pin. The pin has a weak internal pull-down. The device is disabled and all switches become high impedance when the pin is low. When the pin is high, the Ax logic inputs determine individual switch states.
V_{SS}	3	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
S1	4	I/O	Overvoltage protected source pin 1. Can be an input or output.
S2	5	I/O	Overvoltage protected source pin 2. Can be an input or output.
S3	6	I/O	Overvoltage protected source pin 3. Can be an input or output.
S4	7	I/O	Overvoltage protected source pin 4. Can be an input or output.
D	8	I/O	Drain pin. Can be an input or output. The drain pin is not overvoltage protected and shall remain within the recommended operating range.
V_{FN}	9	P	Negative fault voltage supply that determines the overvoltage protection triggering threshold on the negative side. Connect to V_{SS} if the triggering threshold is to be the same as the device's negative supply. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{FN} and GND.
SF	10	O	Specific fault flag. This pin is an open drain output and is asserted low when overvoltage condition is detected on a specific pin, depending on the state of A0, A1, and A2 , as shown in Table 8-1. Connect this pin to an external supply (1.8 V to 5.5 V) through a 1 kΩ pull-up resistor.
FF	11	O	General fault flag. This pin is an open drain output and is asserted low when overvoltage condition is detected on any of the source (Sx) input pins. Connect this pin to an external supply (1.8 V to 5.5 V) through a 1kΩ pull-up resistor.
V_{FP}	12	P	Positive fault voltage supply that determines the overvoltage protection triggering threshold on the positive side. Connect to V_{DD} if the triggering threshold is to be the same as the device's positive supply. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{FP} and GND.
S8	13	I/O	Overvoltage protected source pin 8. Can be an input or output.
S7	14	I/O	Overvoltage protected source pin 7. Can be an input or output.
S6	15	I/O	Overvoltage protected source pin 6. Can be an input or output.
S5	16	I/O	Overvoltage protected source pin 5. Can be an input or output.
V_{DD}	17	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
GND	18	P	Ground (0 V) reference
A2	19	I	Logic control input address 2 (A2). The pin has a weak internal pull-down. This pin can also be used together with the specific fault pin (SF) to indicate which input is under fault.
A1	20	I	Logic control input address 1 (A1). The pin has a weak internal pull-down. This pin can also be used together with the specific fault pin (SF) to indicate which input is under fault.

(1) I = input, O = output, I/O = input and output, P = power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD} to V_{SS}	Supply voltage		38	V
V_{DD} to GND		–0.3	28	V
V_{SS} to GND		–18	0.3	V
V_{FP} to GND	Positive fault clamping voltage	–0.3	V_{DD} + 0.3	V
V_{FN} to GND	Negative fault clamping voltage	V_{SS} – 0.3	0.3	V
V_S to GND	Source input pin (Sx) voltage to GND	–65	65	V
V_S to V_{DD}	Source input pin (Sx) voltage to V_{DD}	–90		V
V_S to V_{SS}	Source input pin (Sx) voltage to V_{SS}		90	V
V_D	Drain pin (D or Dx) voltage	V_{FN}–0.7	V_{FP}+0.7	V
V_{SEL} or V_{EN}	Logic control input pin voltage (EN, A0, A1, A2)(2)	GND –0.7	48	V
V_{DIG_OUT}	Digital output pin (SF, FF) voltage(2)	GND –0.7	6	V
I_{SEL} or I_{EN}	Logic control input pin current (EN, A0, A1, A2)(2)	–30	30	mA
I_{DIG_OUT}	Digital output pin (SF, FF) current(2)	–10	10	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx or D)	I_{DC} ± 10 %(3)	I_{DC} ± 10 %(3)	mA
T_{stg}	Storage temperature	–65	150	°C
T_A	Ambient temperature	–55	150	°C
T_J	Junction temperature		150	°C
P_{tot} (4)	Total power dissipation		800	mW

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Stresses have to be kept at or below both voltage and current ratings at all time.
(3) Refer to Recommended Operating Conditions for I_{DC} ratings.
(4) P_{tot} derates linearly above T_A = 70°C by 12.0 mW/°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$ (1)	Power supply voltage differential	8		33	V
V_{DD}	Positive power supply voltage	5		22	V
V_{FP}	Positive fault clamping voltage	3		V_{DD}	V
V_{FN}	Negative fault clamping voltage	V_{SS}		0	V
V_S	Source pin (Sx) voltage (non-fault condition)	V_{FN}		V_{FP}	V
V_{S_FAULT} (3)	Source pin (Sx) voltage (fault condition)	–60		60	V

6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S to V_{DD} (2)	Source pin (Sx) voltage to V_{DD} or V_D (fault condition)	Source pin (Sx) voltage to V_{DD} or V_D (fault condition)	–85			V
V_S to V_{SS} (2)	Source pin (Sx) voltage to V_{SS} or V_D (fault condition)	Source pin (Sx) voltage to V_{SS} or V_D (fault condition)			85	V
V_D	Drain pin (D, Dx) voltage		V_{FN}		V_{FP}	V
V_{SEL} of V_{EN}	Logic control input pin voltage (EN, A0, A1, A2)		0		22	V
V_{DIG_OUT}	Digital output pin (SF, FF) voltage		0		5.5	V
T_A	Ambient temperature		–55		125	°C
IDC(3)	Continuous current through switch, TSSOP package	T_A = 25°C			9	mA
		T_A = 85°C			6.5	mA
		T_A = 150°C			5	mA

(1) V_{DD} and V_{SS} can be any value as long as 8 V ≤ (V_{DD} – V_{SS}) ≤ 33 V.
(2) Under a fault condition, the potential difference between source pin (Sx) and supply pins (V_{DD} and V_{SS}.) or source pin (Sx) and drain pins (D, Dx) may not exceed 85 V.
(3) Fault supplies are tied to the primary supplies (V_{FP}= V_{DD}, V_{FN} = V_{SS})

6.4 Thermal Information

THERMAL METRIC(1)		TMUX582F-SEP PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	36.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics (Global)

at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_T	Threshold voltage for fault detector		–55°C to +125°C		0.7		V
DIGITAL INPUT/ OUTPUT							
V_{IH}	High-level input voltage	EN, Ax pins	–55°C to +125°C	1.3		22	V
V_{IL}	Low-level input voltage	EN, Ax pins	–55°C to +125°C	0		0.8	V
$V_{OL(FLAG)}$	Low-level output voltage	FF and SF pins, I_O = 5 mA	–55°C to +125°C		0.1		V
POWER SUPPLY							
V_{UVLO}	Undervoltage lockout (UVLO) threshold voltage (V_{DD} – V_{SS})	single supply configuration only	–55°C to +125°C		6		V
$R_{D(OVP)}$	Drain resistance to fault rail during overvoltage event on selected source pin		25°C		40		kΩ

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6.6 Dual Supply: Electrical Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10 V to +10 V, I_S = –1 mA	–55°C to +25°C		180		Ω
			–55°C to +125°C			400	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10 V to +10 V, I_S = –1 mA	–55°C to +25°C		2.5		Ω
			–55°C to +125°C			13	
R_{FLAT}	On-resistance flatness	V_S = –10 V to +10 V, I_S = –1 mA	–55°C to +25°C		1.5		Ω
			–55°C to +125°C			4	
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V, I_S = –1 mA	–55°C to +125°C		1.2		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off, V_S = +10 V/ –10 V, V_D = –10 V/ + 10 V, V_{DD} = 16.5 V, V_{SS} = –16.5 V	–55°C to +25°C	–1	0.1	1	nA
			–55°C to +125°C	–4.5		4.5	
$I_{D(OFF)}$	Drain off leakage current(1)	Switch state is off, V_S = +10 V/ –10 V, V_D = –10 V/ + 10 V, V_{DD} = 16.5 V, V_{SS} = –16.5 V	–55°C to +25°C	–1	0.1	1	nA
			–55°C to +125°C	–15		15	
$I_{S(ON)}$, $I_{D(ON)}$	Channel on leakage current	Switch state is on, V_S = floating, V_D = –10 V/ +10 V, or V_S = –10 V/ +10 V, V_D = floating, V_{DD} = 16.5 V, V_{SS} = –16.5 V	–55°C to +25°C	–1.5	0.3	1.5	nA
			–55°C to +125°C	–23		23	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current during overvoltage	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V	–55°C to +125°C		±110		µA
	Input leakage current during overvoltage with grounded supplies	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= 0 V, V_{EN} = V_{Ax} = 0 V or floating			±135		
	Input leakage current during overvoltage with floating supplies	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= floating, V_{EN} = V_{Ax} = 0 V or floating			±135		
$I_{D(FA)}$	Output leakage current during overvoltage	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V	–55°C to +25°C		±10		nA
			–55°C to +125°C	–100		100	
	Output leakage current during overvoltage with grounded supplies	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= 0 V, V_{EN} = V_{Ax} = 0 V or floating	–55°C to +25°C	–50	±1	50	
			–55°C to +125°C	–550		550	
	Output leakage current during overvoltage with floating supplies	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= floating, V_{EN} = V_{Ax} = 0 V or floating	–55°C to +25°C		±3		µA
			–55°C to +125°C		±8		
DIGITAL INPUT/ OUTPUT							
I_{IH}	High-level input current	V_{EN} = V_{Ax} = V_{DD}	–55°C to +125°C	–2.5	± 0.6	2.5	µA
I_{IL}	Low-level input current	V_{EN} = V_{Ax} = 0 V	–55°C to +125°C	–1.5	± 0.6	1.5	µA
SWITCHING CHARACTERISTICS							
$t_{ON\ (EN)}$	Enable turn-on time	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	–55°C to +25°C		175		ns
			–55°C to +125°C		290		
$t_{OFF\ (EN)}$	Enable turn-off time	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	–55°C to +25°C		350		ns
			–55°C to +125°C		400		
t_{TRAN}	Transition time	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	–55°C to +25°C		180		ns
			–55°C to +125°C		250		
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	–55°C to +125°C		120		ns
$t_{RESPONSE}$	Fault response time	V_{FP} = 10 V, V_{FN} = –10 V, R_L = 4 kΩ, C_L= 12 pF	–55°C to +125°C		300		ns
$t_{RECOVERY}$	Fault recovery time	V_{FP} = 10 V, V_{FN} = –10 V, R_L = 4 kΩ, C_L= 12 pF	–55°C to +125°C		1.5		µs
$t_{RESPONSE(FLAG)}$	Fault flag response time	V_{FP} = 10 V, V_{FN} = –10 V, V_{PU} = 5 V, R_{PU} = 1 kΩ, C_L= 12 pF	25°C		120		ns
$t_{RECOVERY(FLAG)}$	Fault flag recovery time	V_{FP} = 10 V, V_{FN} = –10 V, V_{PU} = 5 V, R_{PU} = 1 kΩ, C_L= 12 pF	25°C		1		µs
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 1 nF, R_S = 0 Ω	25°C		-15		pC

6.6 Dual Supply: Electrical Characteristics (continued)

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
O_{ISO}	Off-isolation	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–80		dB
X_{TALK}	Intra-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–95		dB
BW	–3 dB bandwidth	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V	25°C		150		MHz
I_{LOSS}	Insertion loss	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–9		dB
THD+N	Total harmonic distortion plus noise	R_S = 40 Ω, R_L = 10 kΩ, V_S = 15 V_{PP}, V_{BIAS} = 0 V, f = 20 Hz to 20 kHz	25°C		0.0015		%
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 0 V	25°C		3.5		pF
$C_{D(OFF)}$	Output off-capacitance	f = 1 MHz, V_S = 0 V	25°C		28		pF
$C_{S(ON)}$, $C_{D(ON)}$	Input/Output on-capacitance	f = 1 MHz, V_S = 0 V	25°C		30		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}, V_S = 0 V	25°C		0.25		mA
			–55°C to +125°C			0.6	
I_{SS}	V_{SS} supply current	V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}, V_S = 0 V	25°C		0.15		mA
			–55°C to +125°C			0.5	
I_{GND}	GND current	V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}, V_S = 0 V	25°C		0.075		mA
I_{FP}	V_{FP} supply current	V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}, V_S = 0 V	25°C		10		µA
I_{FN}	V_{FN} supply current	V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}, V_S = 0 V	25°C		10		µA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.25		mA
			–55°C to +125°C			1.25	
$I_{SS(FA)}$	V_{SS} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15		mA
			–55°C to +125°C			0.75	
$I_{GND(FA)}$	GND current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.2		mA
$I_{FP(FA)}$	V_{FP} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		20		µA
$I_{FN(FA)}$	V_{FN} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		20		µA
$I_{DD(DISABLE)}$	V_{DD} supply current (disable mode)	V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V, V_S = 0 V	25°C		0.15		mA
			–55°C to +125°C			0.6	
$I_{SS(DISABLE)}$	V_{SS} supply current (disable mode)	V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V, V_S = 0 V	25°C		0.1		mA
			–55°C to +125°C			0.5	

(1) When V_S is positive,V_D is negative, and vice versa.

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6.7 Single Supply: Electrical Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 7.8 V, I_S = –1 mA	–55°C to +25°C		180		Ω
			–55°C to +125°C			400	
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 7.8 V, I_S = –1 mA	–55°C to +25°C		2.5		Ω
			–55°C to +125°C			13	
R_{FLAT}	On-resistance flatness	V_S = 0 V to 7.8 V, I_S = –1 mA	–55°C to +25°C		7		Ω
R_{FLAT}	On-resistance flatness	V_S = 0 V to 7.8 V, I_S = –1 mA	–55°C to +125°C			80	Ω
R_{FLAT}	On-resistance flatness	V_S = 1 V to 7.8 V, I_S = –1 mA	–55°C to +25°C		1.5		Ω
			–55°C to +125°C			8	
R_{ON_DRIFT}	On-resistance drift	V_S = 6 V, I_S = –1 mA	–55°C to +125°C		1.2		Ω/°C
$I_{S(OFF)}$	Source off leakage current[(1)]	Switch state is off, V_S = 1 V/ 10 V, V_D = 10 V/ 1 V, V_{DD} = 13.2 V	–55°C to +25°C	–1	0.1	1	nA
			–55°C to +125°C	–4.5		4.5	
$I_{D(OFF)}$	Drain off leakage current[(1)]	Switch state is off, V_S = 1 V/ 10 V, V_D = 10 V/ 1 V, V_{DD} = 13.2 V	–55°C to +25°C	–1	0.1	1	nA
			–55°C to +125°C	–15		15	
$I_{S(ON)}$, $I_{,D(ON)}$	Channel on leakage current	Switch state is on, V_S = floating, V_D = 1 V/ 10 V, V_{DD} = 13.2	–55°C to +25°C	–1.5	0.3	1.5	nA
			–55°C to +125°C	–23		23	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current during overvoltage	V_S = ± 60 V, GND = 0V, V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V	–55°C to +125°C		±145		µA
	Input leakage current during overvoltage with grounded supplies	V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= 0 V, V_{EN} = V_{Ax} = 0 V or floating			±135		
	Input leakage current during overvoltage with floating supplies	V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= floating, V_{EN} = V_{Ax} = 0 V or floating			±135		
$I_{D(FA)}$	Output leakage current during overvoltage	V_S = ± 60 V, GND = 0V, V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V	–55°C to +25°C		±10		nA
			–55°C to +125°C	–100		100	
	Output leakage current during overvoltage with grounded supplies	V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= 0 V, V_{EN} = V_{Ax} = 0 V or floating	–55°C to +25°C	–50	±1	50	
			–55°C to +125°C	–550		550	
	Output leakage current during overvoltage with floating supplies	V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= floating, V_{EN} = V_{Ax} = 0 V or floating	–55°C to +25°C		±3		µA
			–55°C to +125°C		±8		
DIGITAL INPUT/ OUTPUT							
I_{IH}	High-level input current	V_{EN} = V_{Ax} = V_{DD}	–55°C to +125°C	–2.5	± 0.6	2.5	µA
I_{IL}	Low-level input current	V_{EN} = V_{Ax} = 0 V	–55°C to +125°C	–1.5	± 0.6	1.5	µA
SWITCHING CHARACTERISTICS							
$t_{ON\ (EN)}$	Enable turn-on time	V_S = 8 V, R_L = 4 kΩ, C_L= 12 pF	–55°C to +25°C		160		ns
			–55°C to +125°C		300		
$t_{OFF\ (EN)}$	Enable turn-off time	V_S = 8 V, R_L = 4 kΩ, C_L= 12 pF	–55°C to +25°C		420		ns
			–55°C to +125°C		500		
t_{TRAN}	Transition time	V_S = 8 V, R_L = 4 kΩ, C_L= 12 pF	–55°C to +25°C		160		ns
			–55°C to +125°C		240		
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 4 kΩ, C_L= 12 pF	–55°C to +125°C		90		ns
$t_{RESPONSE}$	Fault response time	V_{FP} = 8 V, V_{FN} = 0 V, R_L = 4 kΩ, C_L= 12 pF	–55°C to +125°C		225		ns
$t_{RECOVERY}$	Fault recovery time	V_{FP} = 8 V, V_{FN} = 0 V, R_L = 4 kΩ, C_L= 12 pF	–55°C to +125°C		0.75		µs
$t_{RESPONSE(FLAG)}$	Fault flag response time	V_{FP} = 8 V, V_{FN} = 0 V, V_{PU} = 5 V, R_{PU} = 1 kΩ, C_L= 12 pF	25°C		120		ns

6.7 Single Supply: Electrical Characteristics (continued)

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$t_{RECOVERY(FLAG)}$	Fault flag recovery time	V_{FP} = 8 V, V_{FN} = 0 V, V_{PU} = 5 V, R_{PU} = 1 kΩ, C_L= 12 pF	25°C		0.75		μs
Q_{INJ}	Charge injection	V_S = 6 V, C_L = 1 nF, R_S = 0 Ω	25°C		-11		pC
O_{ISO}	Off-isolation	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 2 V, f = 1 MHz	25°C		–75		dB
X_{TALK}	Intra-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 2 V, f = 1 MHz	25°C		–90		dB
BW	–3 dB bandwidth	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 2 V, f = 1 MHz	25°C		130		MHz
I_{LOSS}	Insertion loss	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 2 V, f = 1 MHz	25°C		–9		dB
THD+N	Total harmonic distortion plus noise	R_S = 40 Ω, R_L = 10k Ω, V_S = 6 V_{PP}, V_{BIAS} = 6 V, f = 20 Hz to 20 kHz	25°C		0.0025		%
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 6 V	25°C		4		pF
$C_{D(OFF)}$	Output off-capacitance	f = 1 MHz, V_S = 6 V	25°C		31		pF
$C_{S(ON)}$, $C_{D(ON)}$	Input/Output on-capacitance	f = 1 MHz, V_S = 6 V	25°C		34		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{EN}/ V_{Ax} = 0 V, 5 V, or V_{DD}, V_S = 6 V	25°C		0.25		mA
			–55°C to +125°C			0.6	
I_{SS}	V_{SS} supply current	V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{EN}/ V_{Ax} = 0 V, 5 V, or V_{DD}, V_S = 6 V	25°C		0.15		mA
			–55°C to +125°C			0.5	
I_{GND}	GND current	V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{EN}/ V_{Ax} = 0 V, 5 V, or V_{DD}, V_S = 6 V	25°C		0.075		mA
I_{FP}	V_{FP} supply current	V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{EN}/ V_{Ax} = 0 V, 5 V, or V_{DD}, V_S = 6 V	25°C		10		μA
I_{FN}	V_{FN} supply current	V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{EN}/ V_{Ax} = 0 V, 5 V, or V_{DD}, V_S = 6 V	25°C		10		μA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{EN}/ V_{Ax} = 0 V, 5 V, or V_{DD}	25°C		0.25		mA
			–55°C to +125°C			1.25	
$I_{SS(FA)}$	V_{SS} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{EN}/ V_{Ax} = 0 V, 5 V, or V_{DD}	25°C		0.15		mA
			–55°C to +125°C			0.75	
$I_{GND(FA)}$	GND current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{EN}/ V_{Ax} = 0 V, 5 V, or V_{DD}	25°C		0.2		mA
$I_{FP(FA)}$	V_{FP} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{EN}/ V_{Ax} = 0 V, 5 V, or V_{DD}	25°C		20		μA
$I_{FN(FA)}$	V_{FN} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{EN}/ V_{Ax} = 0 V, 5 V, or V_{DD}	25°C		20		μA
$I_{DD(DISABLE)}$	V_{DD} supply current (disable mode)	V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V, V_S = 0 V	25°C		0.15		mA
			–55°C to +125°C			0.6	
$I_{SS(DISABLE)}$	V_{SS} supply current (disable mode)	V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V, V_S = 0 V	25°C		0.1		mA
			–55°C to +125°C			0.5	

(1) When V_S is positive, V_D is negative, and vice versa.

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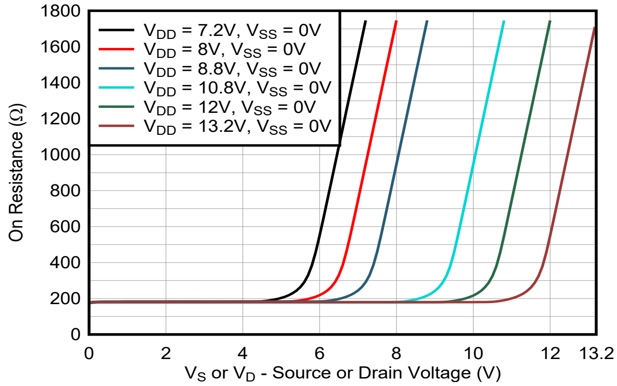
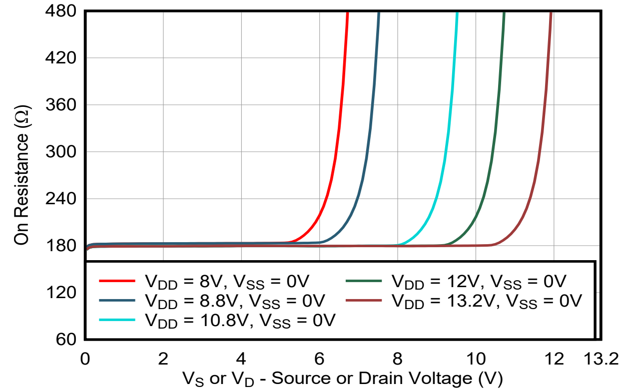
6.8 Typical Characteristics

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



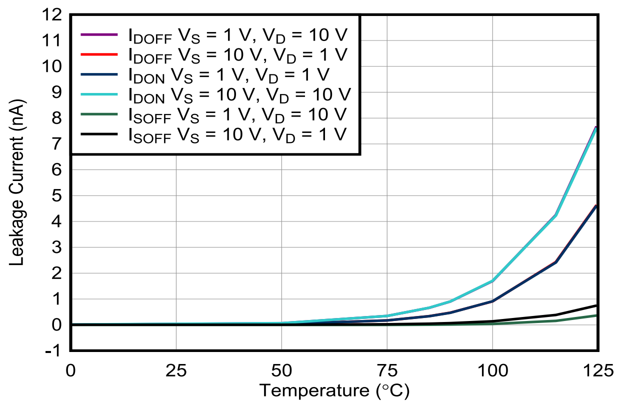
Single Supply Voltages

Figure 6-1. On-Resistance vs Source or Drain Voltage



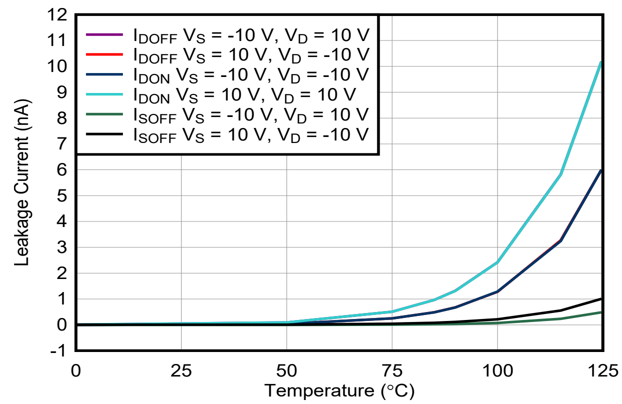
Single Supply Flat R_{ON} Region

Figure 6-2. On-Resistance vs Source or Drain Voltage



V_{DD} = 12 V, V_{SS} = 0 V

Figure 6-3. Leakage Current vs Temperature



V_{DD} = 15 V, V_{SS} = -15 V

Figure 6-4. Leakage Current vs Temperature

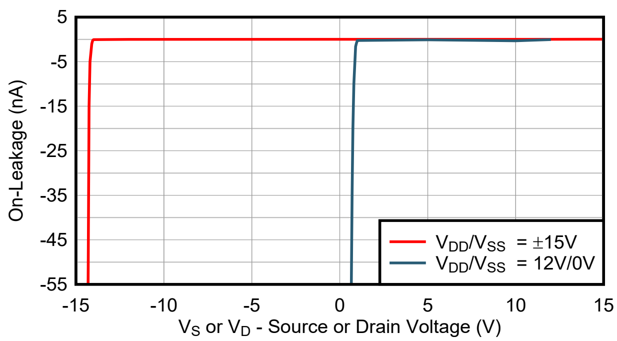
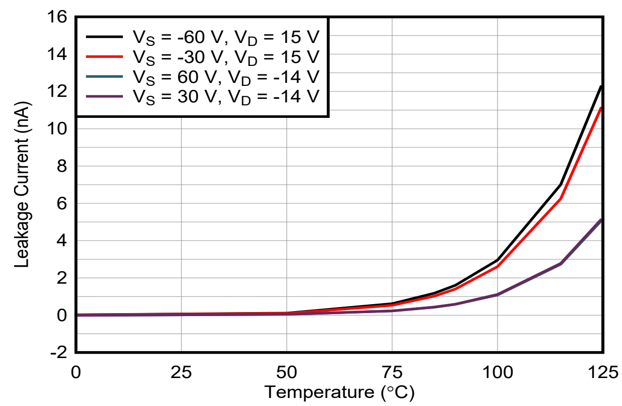


Figure 6-5. On-Leakage Current vs Input Voltage

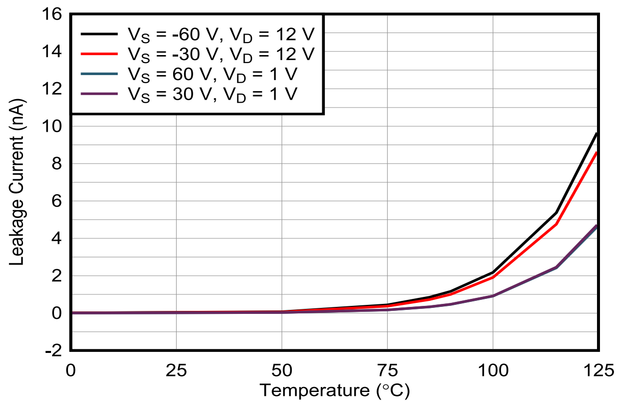


V_{DD} = 15 V, V_{SS} = -15 V

Figure 6-6. $I_{D(FA)}$ Overvoltage Leakage Current vs Temperature

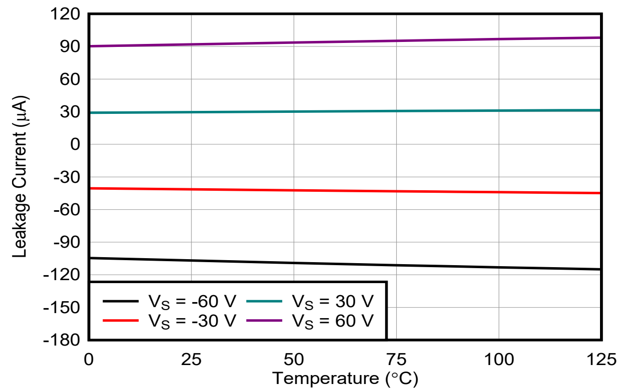
6.8 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



V_{DD} = 12 V, V_{SS} = 0 V

Figure 6-7. $I_{D(FA)}$ Overvoltage Leakage Current vs Temperature



V_{DD} = 15 V, V_{SS} = -15 V

Figure 6-8. $I_{S(FA)}$ Overvoltage Leakage Current vs Temperature

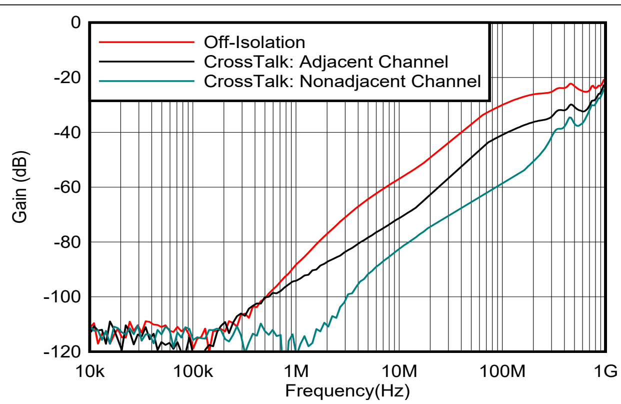


Figure 6-9. Off Isolation and Crosstalk vs Frequency

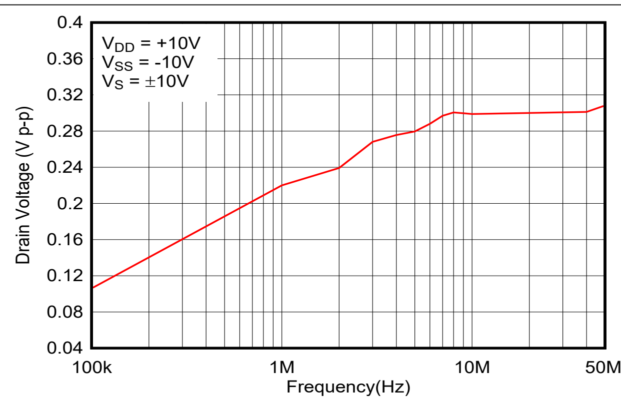


Figure 6-10. Large Signal Voltage Off Isolation vs Frequency

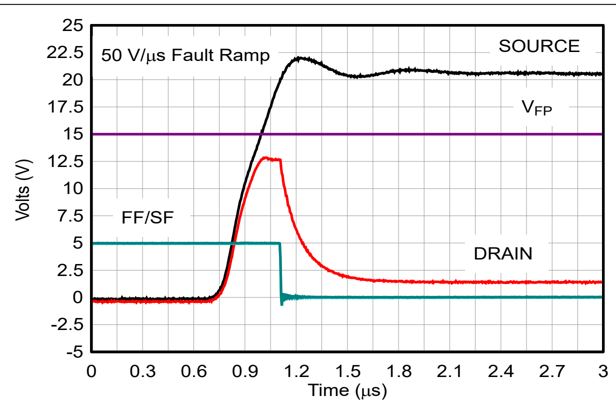


Figure 6-11. Drain Output Response – Positive Overvoltage

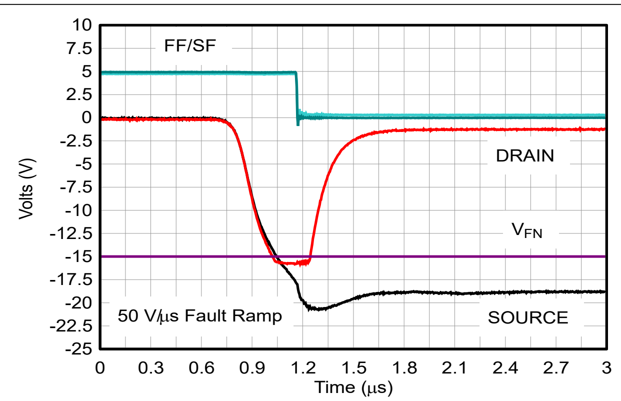


Figure 6-12. Drain Output Response – Negative Overvoltage

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6.8 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

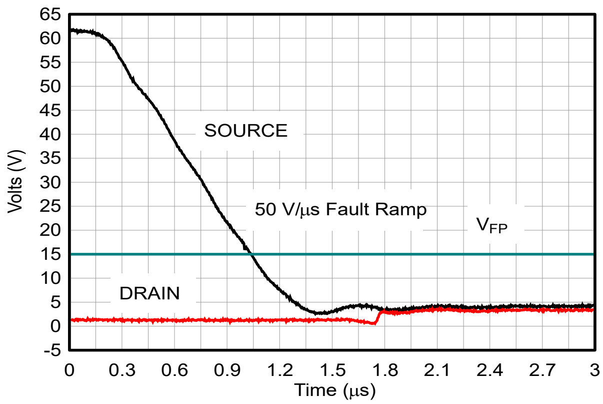

Figure 6-13. Drain Output Recovery – Positive Overvoltage

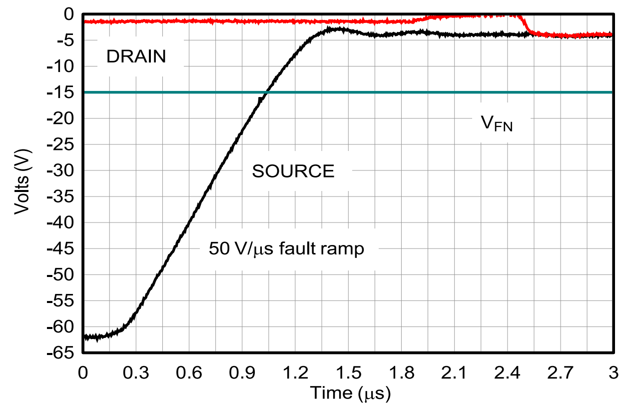

Figure 6-14. Drain Output Recovery – Negative Overvoltage

7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of the TMUX582F-SEP is the ohmic resistance across the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in Figure 7-1. ΔR_{ON} represents the difference between the R_{ON} of any two channels, while R_{ON_FLAT} denotes the flatness that is defined as the difference between the maximum and minimum value of on-resistance measured over the specified analog signal range.

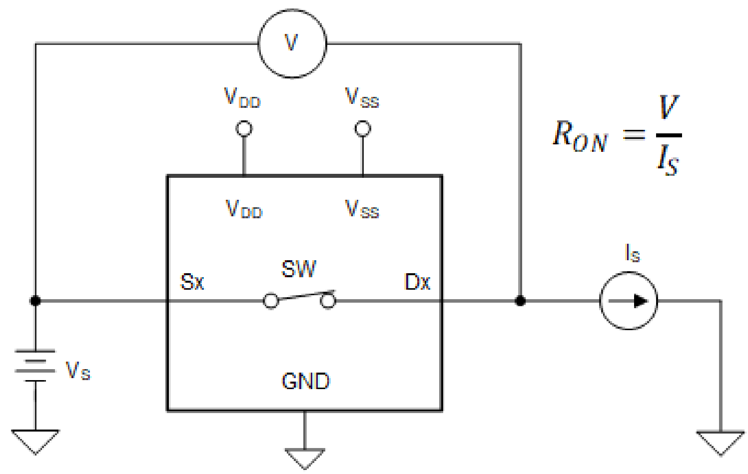

Figure 7-1. On-Resistance Measurement Setup

7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current $I_{S(OFF)}$: the leakage current flowing into or out of the source pin when the switch is off.
2. Drain off-leakage current $I_{D(OFF)}$: the leakage current flowing into or out of the drain pin when the switch is off.

Figure 7-2 shows the setup used to measure both off-leakage currents.

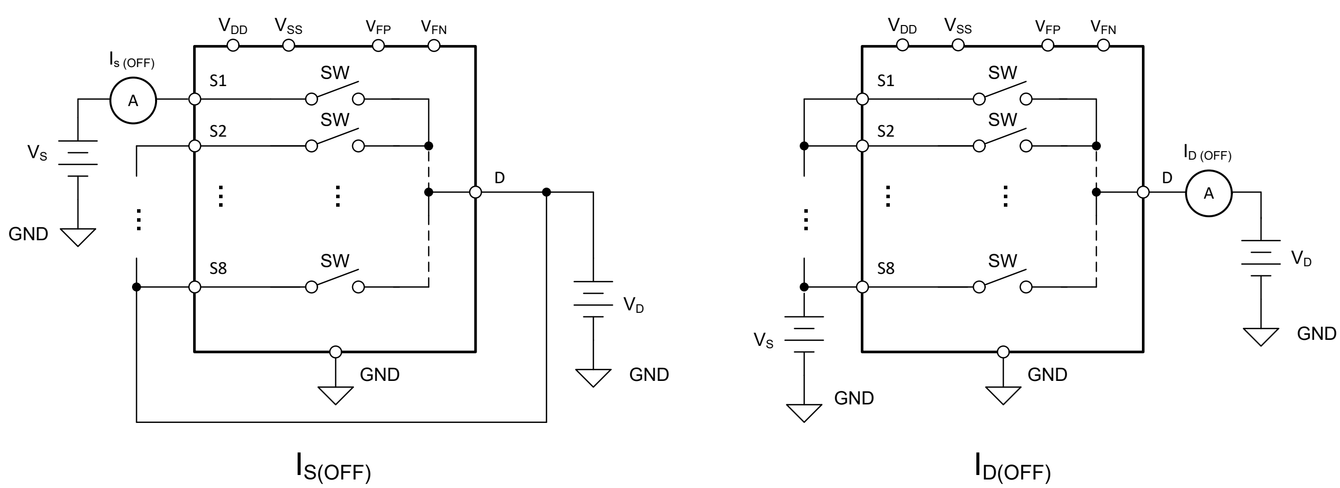

Figure 7-2. Off-Leakage Measurement Setup

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7.3 On-Leakage Current

Source on-leakage current ($I_{S(ON)}$) and drain on-leakage current ($I_{D(ON)}$) denote the channel leakage currents when the switch is in the on state. $I_{S(ON)}$ is measured with the drain floating, while $I_{D(ON)}$ is measured with the source floating. Figure 7-3 shows the circuit used for measuring the on-leakage currents.

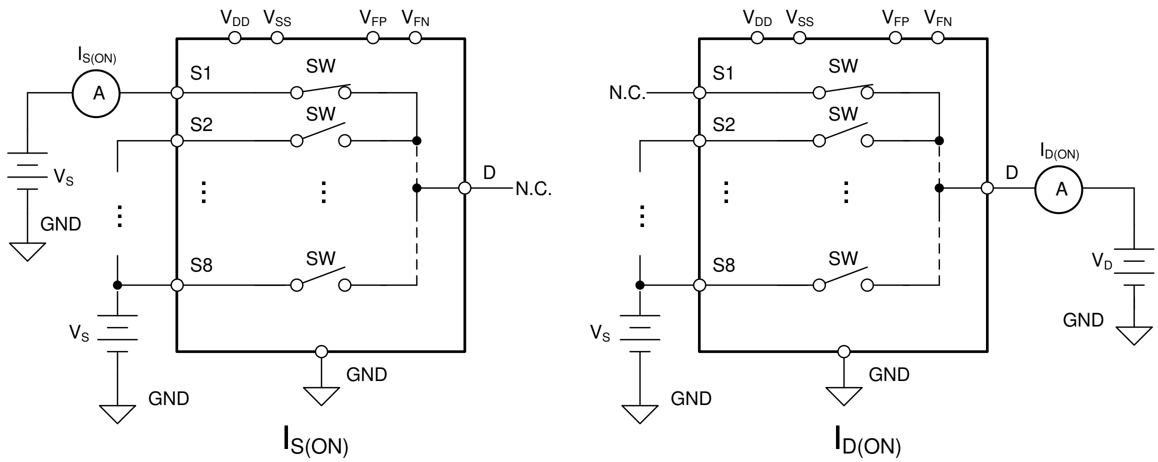

Figure 7-3. On-Leakage Measurement Setup

7.4 Input and Output Leakage Current Under Overvoltage Fault

If any of the source pin voltage goes above the fault supplies (V_{FP} or V_{FN}), the overvoltage protection feature of the TMUX582F-SEP is triggered to turn off the switch under fault, keeping the fault channel in high-impedance state. $I_{S(FA)}$ and $I_{D(FA)}$ denotes the input and output leakage current under overvoltage fault conditions, respectively. For $I_{D(FA)}$ the device is disabled to measure leakage current on the drain pin without being impacted by the 40 kΩ impedance to the fault supply. When the overvoltage fault occurs, the supply (or supplies) can either be in normal operating condition (Figure 7-5) or abnormal operating condition (Figure 7-5). During abnormal operating condition, the supply (or supplies) can either be unpowered (V_{DD}= VSS = V_{FN} = V_{FP} = 0 V) or floating (V_{DD}= VSS = V_{FN} = V_{FP} = No Connection), and remains within the leakage performance specifications.

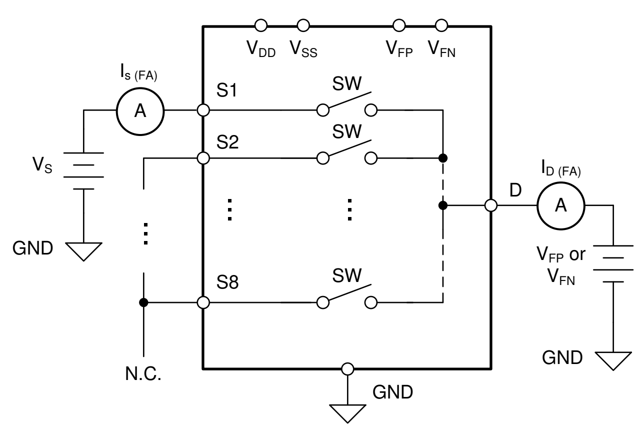

Figure 7-4. Measurement Setup for Input and Output Leakage Current under Overvoltage Fault with Normal Supplies

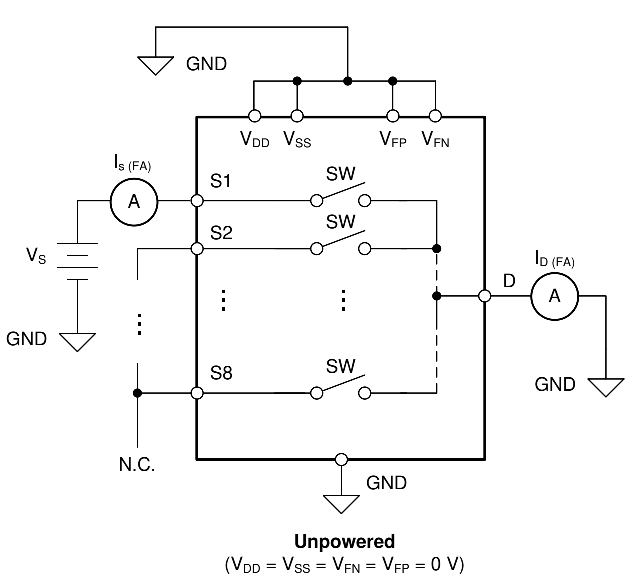

Figure 7-5. Measurement Setup for Input and Output Leakage Current Under Overvoltage Fault with Unpowered or Floating Supplies

7.5 Break-Before-Make Delay

The break-before-make delay is a safety feature of the TMUX582F-SEP. The ON switches first break the connection before the OFF switches make connection. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 7-6 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM}.

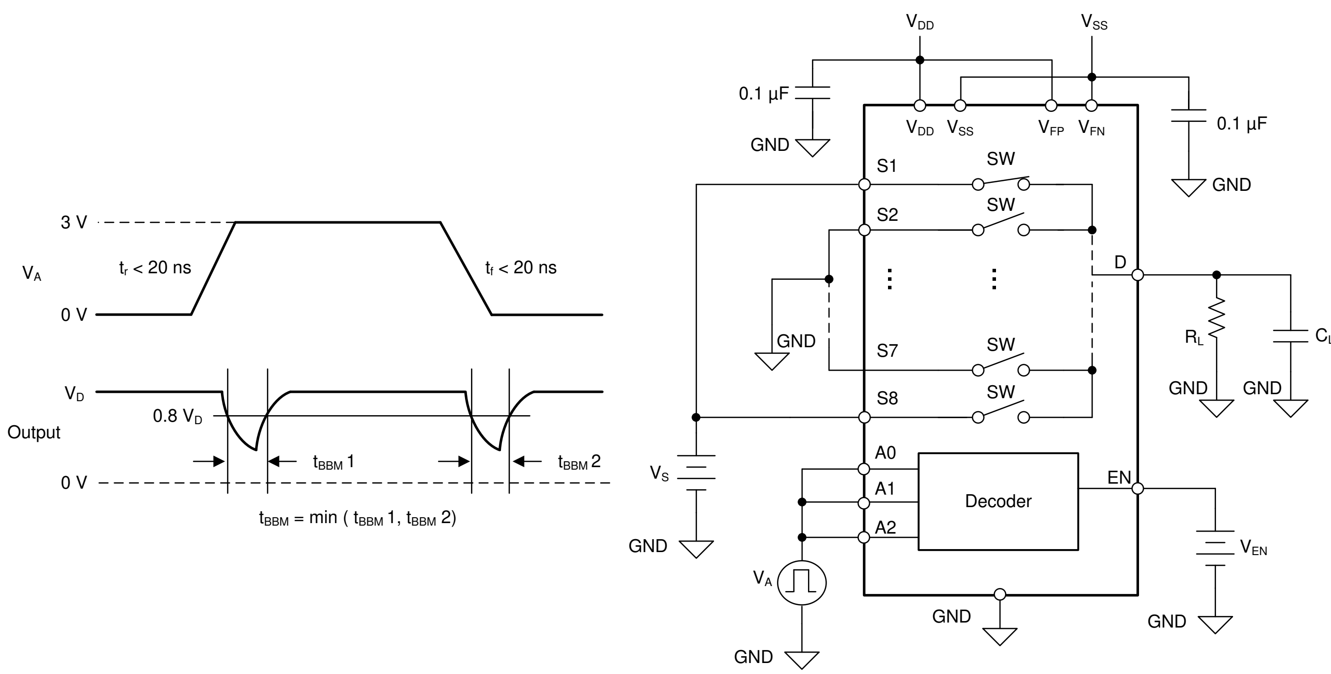

Figure 7-6. Break-Before-Make Delay Measurement Setup

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7.6 Enable Delay Time

$t_{ON(EN)}$ time is defined as the time taken by the output of the TMUX582F-SEP to rise to a 90% final value after the EN signal has risen to a 50% final value. $t_{OFF(EN)}$ is defined as the time taken by the output of the TMUX582F-SEP to fall to a 10% initial value after the EN signal has fallen to a 50% initial value. Figure 7-7 shows the setup used to measure the enable delay time.

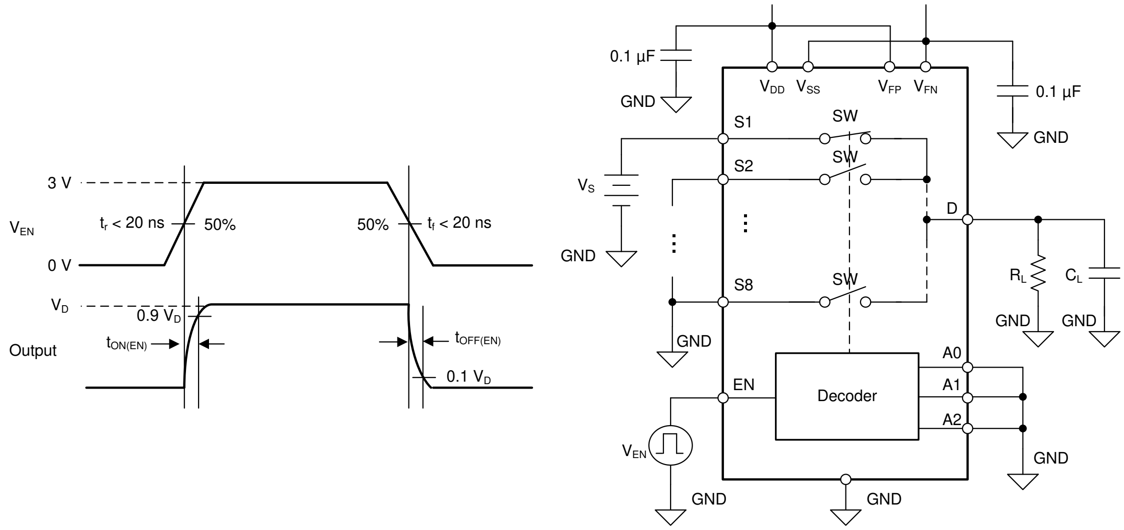

Figure 7-7. Enable Delay Measurement Setup

7.7 Transition Time

Transition time is defined as the time taken by the output of the device to rise (to 90% of the transition) or fall (to 10% of the transition) after the address signal (Ax) has fallen or risen to 50% of the transition. Figure 7-8 shows the setup used to measure transition time, denoted by the symbol t_{TRAN}.

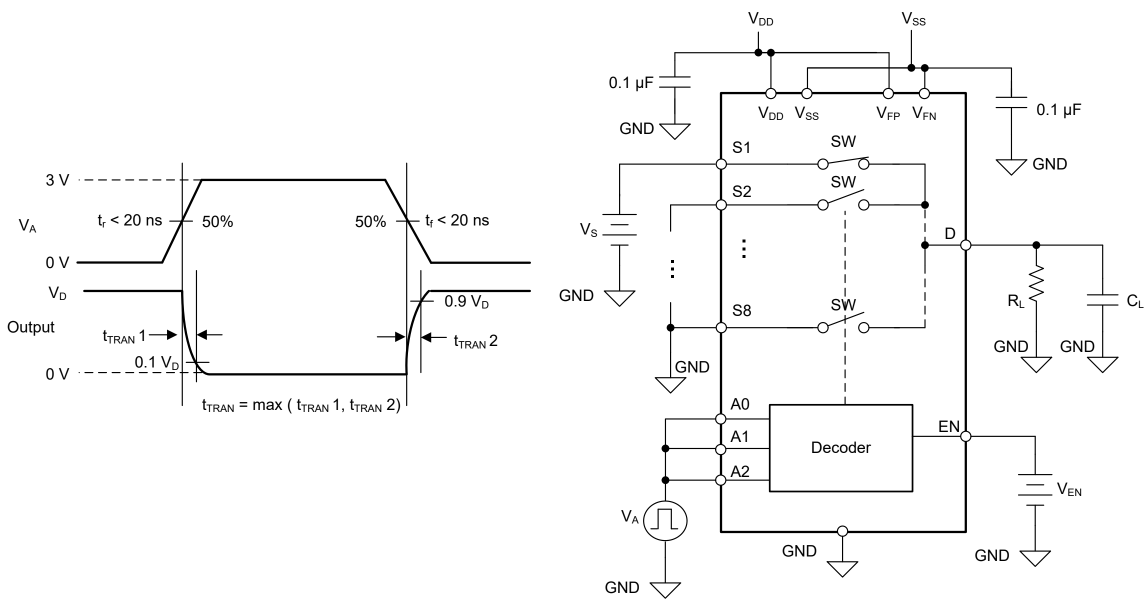

Figure 7-8. Transition Time Measurement Setup

7.8 Fault Response Time

Fault response time ($t_{RESPONSE}$) measures the delay between the source voltage exceeding the fault supply voltage (V_{FP} or V_{FN}) by 0.5 V and the drain voltage failing to 50% of the maximum output voltage. Figure 7-9 shows the setup used to measure $t_{RESPONSE}$.

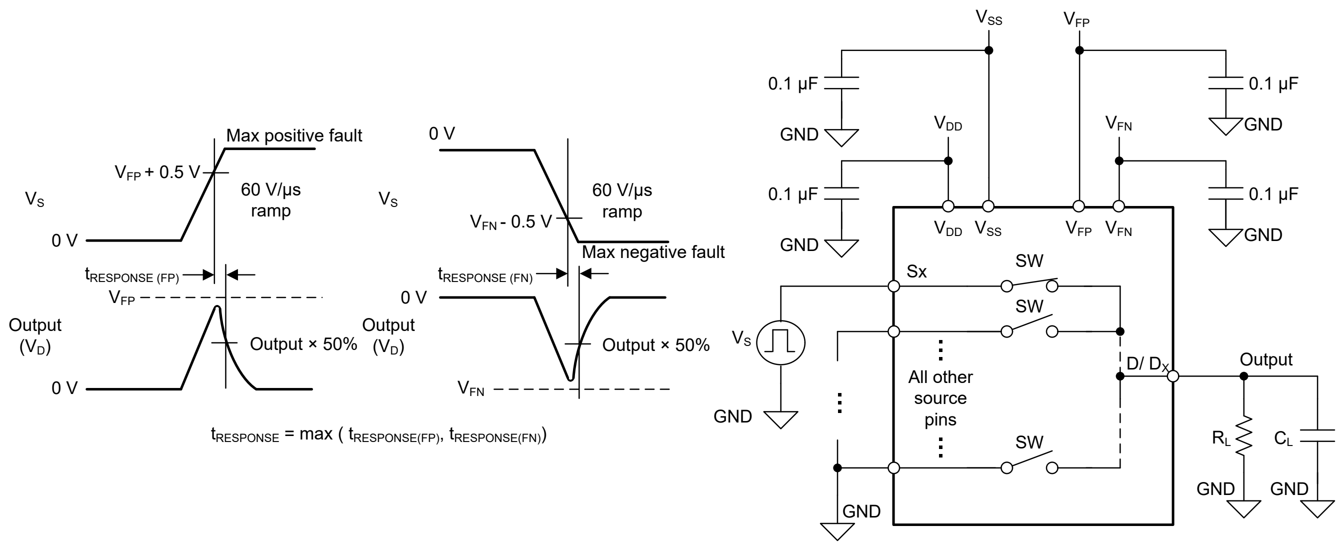

Figure 7-9. Fault Response Time Measurement Setup

7.9 Fault Recovery Time

Fault recovery time ($t_{RECOVERY}$) measures the delay between the source voltage falling from overvoltage condition to below fault supply voltage (V_{FP} or V_{FN}) plus 0.5 V and the drain voltage rising from 0 V to 50% of the final output voltage. Figure 7-10 shows the setup used to measure $t_{RECOVERY}$.

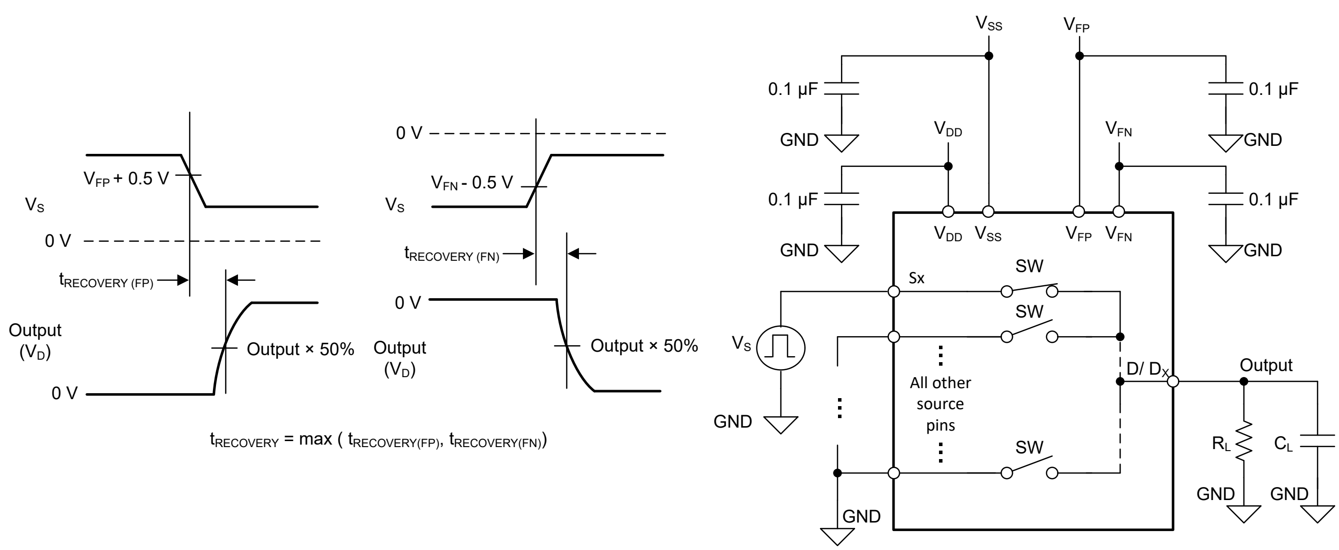

Figure 7-10. Fault Recovery Time Measurement Setup

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7.10 Fault Flag Response Time

Fault flag response time ($t_{RESPONSE(FLAG)}$) measures the delay between the source voltage exceeding the fault supply voltage (V_{FP} or V_{FN}) by 0.5 V and the general fault flag (FF) pin or specific fault flag (SF) pin to go below 10% of its original value. Figure 7-11 shows the setup used to measure $t_{RESPONSE(FLAG)}$.

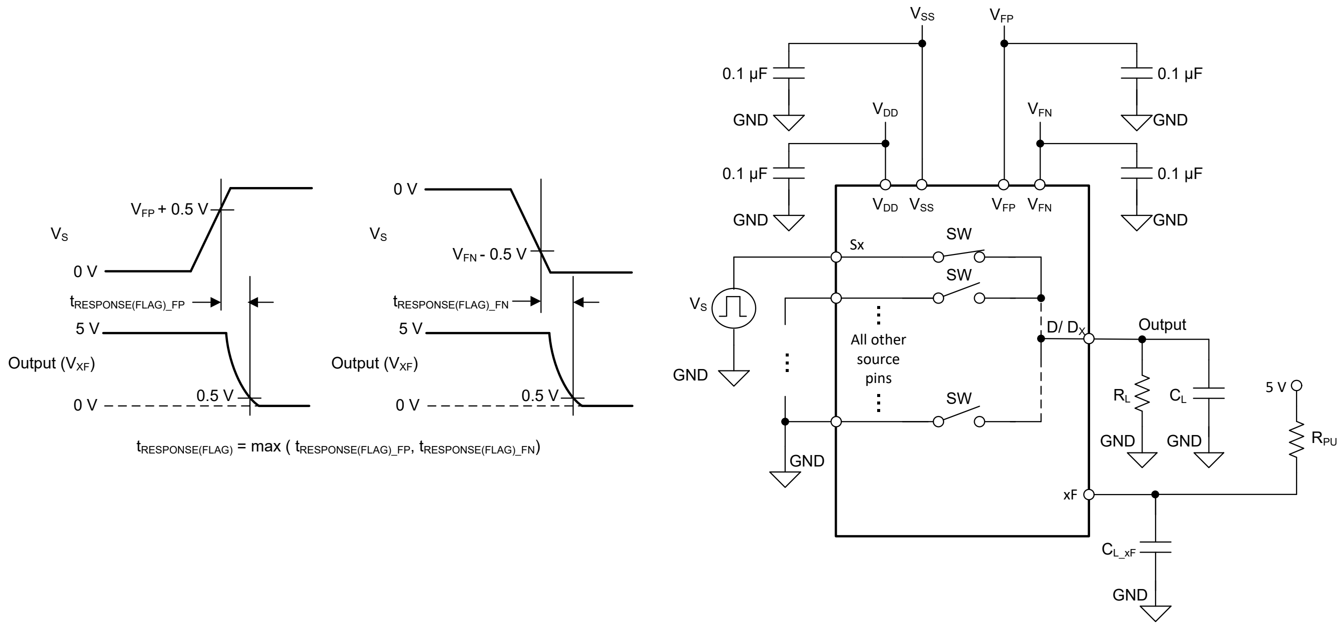

Figure 7-11. Fault Flag Response Time Measurement Setup

7.11 Fault Flag Recovery Time

Fault flag recovery time ($t_{RECOVERY(FLAG)}$) measures the delay between the source voltage falling from overvoltage condition to below fault supply voltage (V_{FP} or V_{FN}) plus 0.5 V and the general fault flag (FF) pin or the specific fault flag (SF) pin to rise above 3 V with 5 V external pull-up. Figure 7-12 shows the setup used to measure $t_{RECOVERY(FLAG)}$.

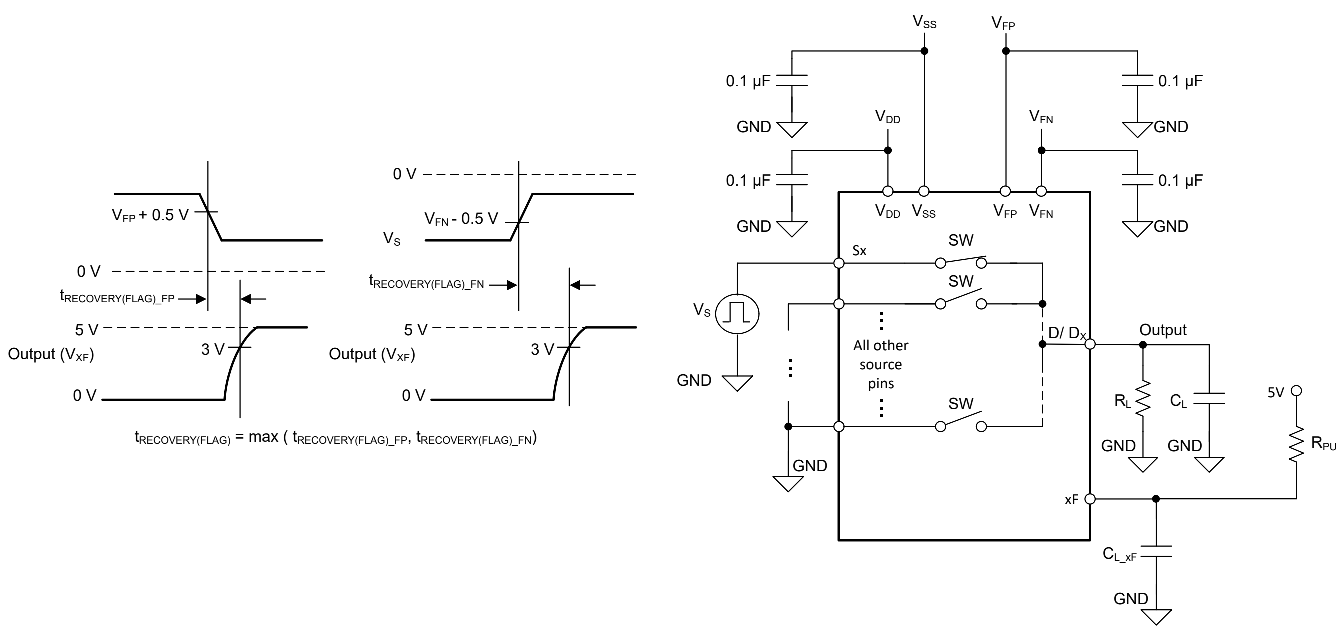

Figure 7-12. Fault Flag Recovery Time Measurement Setup

7.12 Charge Injection

Charge injection is a measure of the glitch impulse transferred from the logic input to the analog output during switching, and is denoted by the symbol Q_{INJ}. Figure 7-13 shows the setup used to measure charge injection from the source to drain.

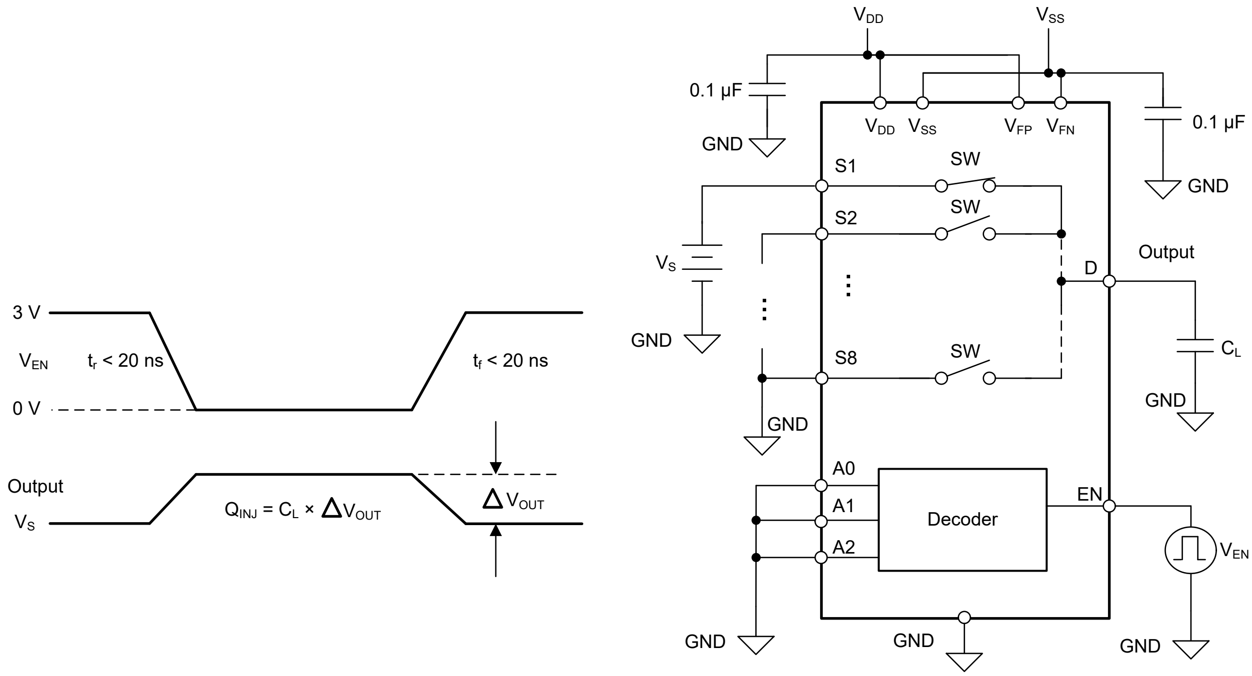

Figure 7-13. Charge-Injection Measurement Setup

7.13 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. Figure 7-14 and Equation 1 shows the setup used to measure, and the equation used to calculate off isolation.

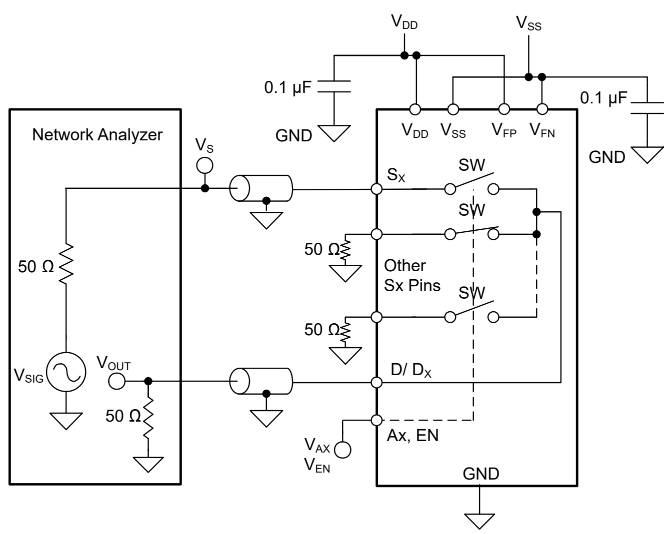

Figure 7-14. Off Isolation Measurement Setup

$$Off\ Isolation = 20 \times Log \frac{V_{OUT}}{V_S} \tag{1}$$

7.14 Crosstalk

Crosstalk (X_{TALK}) is defined as the voltage at the source pin (Sx) of an off-switch input, when a signal is applied at the source pin of an on-switch input in the same channel, as shown in Figure 7-15 and Equation 2.

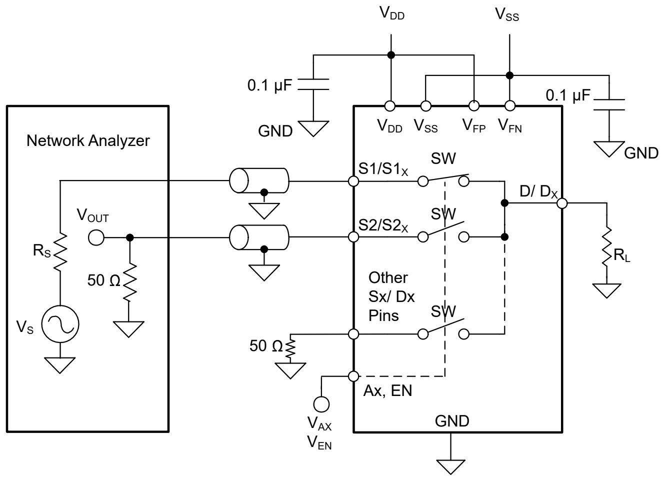

Figure 7-15. Intra-Channel Crosstalk Measurement Setup

$$Intra - channel\ Crosstalk = 20 \times Log \frac{V_{OUT}}{V_S} \quad (2)$$

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7.15 Bandwidth

Bandwidth (BW) is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the TMUX582F-SEP. Figure 7-16 and Equation 3 shows the setup used to measure bandwidth of the switch.

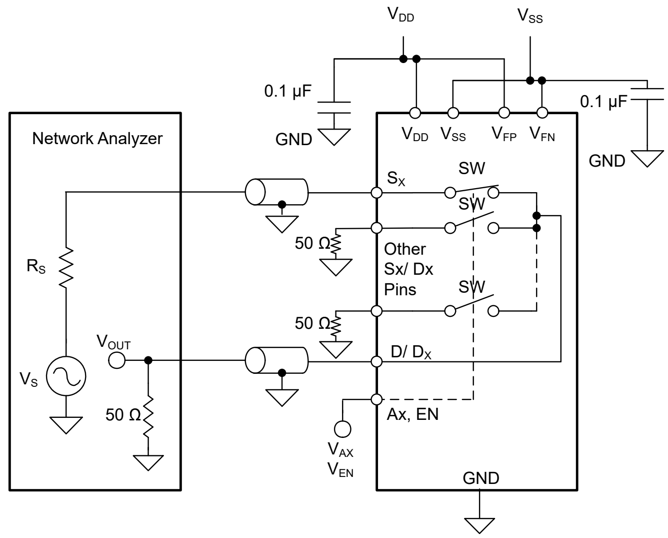

Figure 7-16. Bandwidth Measurement Setup

$$Bandwidth = 20 \times Log \frac{V_{OUT}}{V_S} \quad (3)$$

7.16 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the multiplexer output. The on-resistance of the TMUX582F-SEP varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. Figure 7-17 shows the setup used to measure THD+N of the devices.

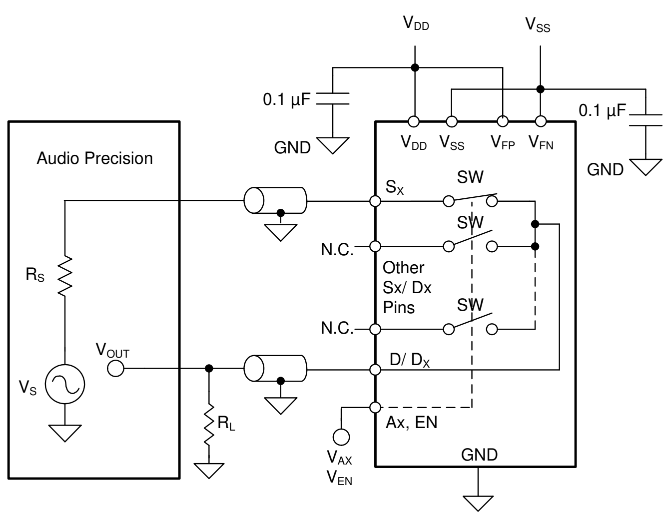

Figure 7-17. THD+N Measurement Setup

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8 Truth Table

Table 8-1 provides the truth tables for the TMUX582F-SEP under normal and fault conditions.

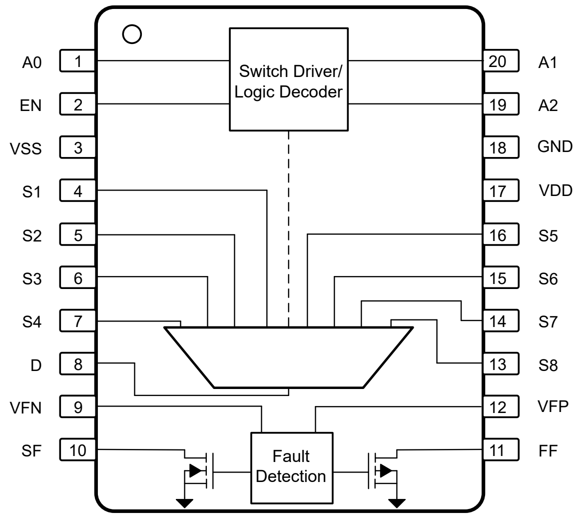
Table 8-1. TMUX582F-SEP Truth Table

EN	A2	A1	A0	Normal Condition	Fault Condition							
					State of Specific Flag (SF) when fault occurs on							
				On Switch	S1	S2	S3	S4	S5	S6	S7	S8
0	0	0	0	None	0	1	1	1	1	1	1	1
0	0	0	1	None	1	0	1	1	1	1	1	1
0	0	1	0	None	1	1	0	1	1	1	1	1
0	0	1	1	None	1	1	1	0	1	1	1	1
0	1	0	0	None	1	1	1	1	0	1	1	1
0	1	0	1	None	1	1	1	1	1	0	1	1
0	1	1	0	None	1	1	1	1	1	1	0	1
0	1	1	1	None	1	1	1	1	1	1	1	0
1	0	0	0	S1	0	1	1	1	1	1	1	1
1	0	0	1	S2	1	0	1	1	1	1	1	1
1	0	1	0	S3	1	1	0	1	1	1	1	1
1	0	1	1	S4	1	1	1	0	1	1	1	1
1	1	0	0	S5	1	1	1	1	0	1	1	1
1	1	0	1	S6	1	1	1	1	1	0	1	1
1	1	1	0	S7	1	1	1	1	1	1	0	1
1	1	1	1	S8	1	1	1	1	1	1	1	0

9 Detailed Description

The TMUX582F-SEP and TMUX582F-SEP are a modern complementary metal-oxide semiconductor (CMOS) analog multiplexers in a 8:1 configuration. The devices work well with dual supplies (±5 V to ±16.5 V), a single supply (8 V to 22 V), or asymmetric supplies (such as V_{DD} = 12 V, V_{SS} = –5 V). The devices feature a number of protection features, allowing them to be used in harsh industrial environments.

9.1 Functional Block Diagram



ADVANCE INFORMATION

9.2 Feature Description

9.2.1 Flat ON- Resistance

The TMUX582F-SEP are designed with a special switch architecture to produce ultra-flat on-resistance (R_{ON}) across most of the switch input operation region. The flat R_{ON} response allows the device to be used in precision sensor applications since the R_{ON} is controlled regardless of the signals sampled. The architecture is implemented without a charge pump, so no unwanted noise is produced from the device to affect sampling accuracy.

9.2.2 Protection Features

The TMUX582F-SEP offer a number of protection features to enable robust system implementations.

9.2.2.1 Input Voltage Tolerance

The maximum voltage that can be applied to any source input pin is +60 V or -60 V, which allows the device to handle typical voltage fault condition in industrial applications. Take caution: the device is rated to handle a maximum stress of 85 V across different pins:

1. **Between source pins and supply rails:**

   For example, if the device is powered by V_{DD} supply of 20 V, the maximum negative signal level on any source pin is –60 V. If the device is powered by V_{DD} supply of 40 V, the maximum negative signal level on any source pin is reduced to –45 V to maintain the 85 V maximum rating across the source pin and the supply.
2. **Between source pins and one or more of the drain pins:**

   For example, if channel S1 is ON and the voltage on S1(A) pin is 40 V. In this case, the drain voltage is also 40 V. The maximum negative voltage on any of the other source pins is –45 V to maintain the 85 V maximum rating across the source pin and the drain pin.

9.2.2.2 Powered-Off Protection

When the supplies of TMUX582F-SEP are removed (V_{DD}/ V_{SS} = 0 V or floating), the source (Sx) pins of the device remain in the high impedance (Hi-Z) state, and the source (Sx) and drain (Dx) pins of the device remain within the leakage performance mentioned in the Electrical Specifications. Powered-off protection minimizes system complexity by removing the need to control the power supply sequencing of the system. The feature prevents errant voltages on the input source pins from reaching the rest of the system and maintains isolation when the system is powering up. Without powered-off protection, the signal on the input source pins can back-power the supply rails through the internal ESD diodes and potentially cause damage to the system. For more information on powered-off protection refer to *Eliminate Power Sequencing With Powered-Off Protection Signal Switches*.

The switch remains OFF regardless of whether the V_{DD} and V_{SS} supplies are 0 V or floating. A GND reference must always be present to allow proper operation. Source and drain voltage levels of up to ±60 V are blocked in the powered-off condition.

9.2.2.3 Fail-Safe Logic

Fail-safe logic circuitry allows voltages on the logic control pins to be applied before the supply pins, protecting the device from potential damage. The switch is specified to be in the OFF state, regardless of the state of the logic signals. The logic inputs are protected against positive faults of up to +24 V in the powered-off condition, but do not offer protection against the negative overvoltage condition.

Fail-safe logic also allows the TMUX582F-SEP devices to interface with a voltage greater than V_{DD} during normal operation to add maximum flexibility in system design. For example, with a V_{DD} of 15 V, the logic control pins could be connected to +24 V for a logic high signal which allows different types of signals, such as analog feedback voltages, to be used when controlling the logic inputs. Regardless of the supply voltage, the logic inputs can be interfaced as high as 24 V.

9.2.2.4 Overvoltage Protection and Detection

The TMUX582F-SEP detects overvoltage inputs by comparing the voltage on a source pin (Sx) with the fault supplies (V_{FP} and V_{FN}). A signal is considered overvoltage if it exceeds the fault supply voltages by the threshold voltage (V_T).

When an overvoltage is detected, the switch automatically turns OFF regardless of the logic controls. The source pin becomes high impedance and allows only a small leakage current through the switch and the overvoltage does not appear on the drain. When the overvoltage channel is selected by the logic control, the drain pin (D) is pulled to the supply that was exceeded. For example, if the source voltage exceeds V_{FP}, the drain output is pulled to V_{FP}. If the source voltage exceeds V_{FN}, the drain output is pulled to V_{FN}. The pull-up impedance is approximately 40 kΩ, and as a result, the drain current is limited to roughly 1 mA during a shorted load (to GND) condition.

Figure 9-1 shows a detailed view of how the pullup/down controls the output state of the drain pin under a fault scenario.

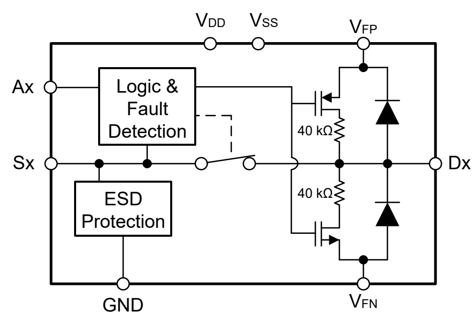


Figure 9-1. Detailed Functional Diagram

V_{FP} and V_{FN} are required fault supplies that set the level at which the overvoltage protection is engaged. V_{FP} can be supplied from 3 V to V_{DD}, while the V_{FN} can be supplied from V_{SS} to 0 V. If the fault supplies are not available in the system, the V_{FP} pin must be connected to V_{DD}, while the V_{FN} pin must be connected to V_{SS}. In this case, overvoltage protection then engages at the primary supply voltages V_{DD} and V_{SS}.

9.2.2.5 Adjacent Channel Operation During Fault

When the logic pins are set to a channel under a fault, the overvoltage detection will trigger, the switch will open, and the drain pin will be pulled up or down as described in Section 9.2.2.4. During such an event, all other channels not under a fault can continue to operate as normal. For example, if S1 voltage exceeds V_{FP}, and the logic pins are set to S1, the drain output is pulled to V_{FP}. Then if the logic pins are changed to set S4, which is not in overvoltage or undervoltage, the drain will disconnect from the pullup to V_{FP} and the S4 switch will be enabled and connected to the drain, operating as normal. If the logic pins are switched back to S1, the S4 switch will be disabled, the drain pin will be pulled up to V_{FP} again, and the switch from S1 to drain will not be enabled until the overvoltage fault is removed.

9.2.2.6 ESD Protection

All pins on the TMUX582F-SEP support HBM ESD protection level up to ±3.5 kV, which helps the device from getting ESD damages during the manufacturing process.

The drain pins (D) have internal ESD protection diodes to the fault supplies V_{FP} and V_{FN}. Therefore, the voltage at the drain pins must not exceed the fault supply voltages to prevent excessive diode current. The source pins have specialized ESD protection that allows the signal voltage to reach ±60 V regardless of the supply voltage level. Exceeding ±60 V on any source input may damage the ESD protection circuitry on the device and cause the device to malfunction if the damage is excessive.

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9.2.2.7 Latch-Up Immunity

Latch-up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The latch-up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX582F-SEP devices are constructed on silicon on insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX582F-SEP to be used in harsh environments. For more information on latch-up immunity, refer to *Using Latch Up Immune Multiplexers to Help Improve System Reliability*.

9.2.2.8 EMC Protection

The TMUX582F-SEP are not intended for standalone electromagnetic compatibility (EMC) protection in industrial applications. There are three common high voltage transient specifications that govern industrial high voltage transient specification: IEC61000-4-2 (ESD), IEC61000-4-4 (EFT), and IEC61000-4-5 (surge immunity). A transient voltage suppressor (TVS), along with some low-value series current limiting resistors, are required to prevent source input voltages from going above the rated ±60 V limits.

When selecting a TVS protection device, it is critical to confirm that the maximum working voltage is greater than both the normal operating range of the input source pins to be protected and any known system common-mode overvoltage that may be present due to incorrect wiring, loss of power, or short circuit. Figure 9-2 shows an example of the proper design window when selecting a TVS device.

Region 1 denotes normal operation region of TMUX582F-SEP where the input source voltages stay below the fault supplies V_{FP} and V_{FN}. Region 2 represents the range of possible persistent DC (or long duration AC overvoltage fault) presented on the source input pins. Region 3 represents the margin between any known DC overvoltage level and the absolute maximum rating of the TMUX582F-SEP. The TVS breakdown voltage must be selected to be less than the absolute maximum rating of the TMUX582F-SEP, but greater than any known possible persistent DC or long duration AC overvoltage fault to avoid triggering the TVS inadvertently. Region 4 represents the margin system designers must impose when selecting the TVS protection device to prevent accidental triggering of ESD cells of the TMUX582F-SEP devices.

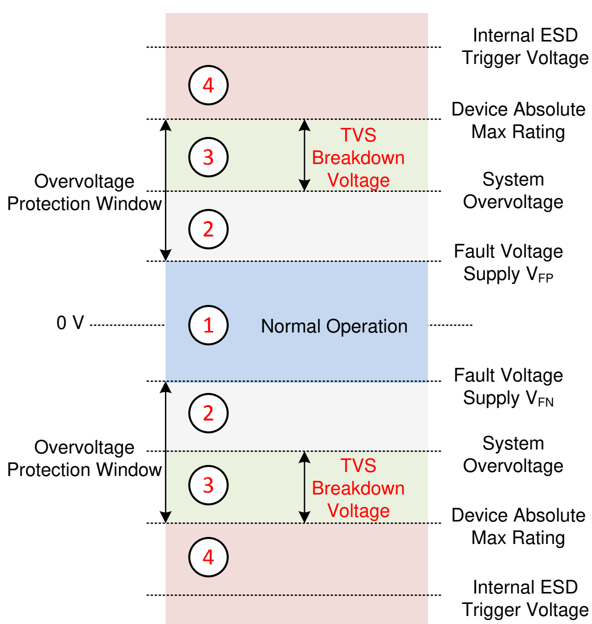

Figure 9-2. System Operation Regions and Proper Region of Selecting a TVS Protection Device

9.2.3 Overvoltage Fault Flags

The voltages on the source input pins of the TMUX582F-SEP is continuously monitored, and the status of whether an overvoltage condition occurs is indicated by an active low general fault flag (FF).The voltage on the FF pin indicates if any of the source input pins are experiencing an overvoltage condition. If any source pin voltage exceeds the fault supply voltages b V_T, then the FF output is pulled-down to below V_{OL}.

The specific fault (SF) output pins, on the other hand, can be used to decode which inputs are experiencing an overvoltage condition. The SF pin is pulled-down to below V_{OL} when an overvoltage condition is detected on a specific source input pin, depending on the state of the A0, A1, A2, and EN logic pins (Table 8-1 provides more details).

Both the FF pin and SF pin are open-drain output and external pull-up resistors of 1 kΩ are recommended. The pull-up voltage can be in the range of 1.8 V to 5.5 V, depending on the controller voltage the device interfaces with.

9.2.4 Bidirectional and Rail-to-Rail Operation

The TMUX582F-SEP conducts equally well from source (Sx) to drain (D or Dx) or from drain (D or Dx) to source (Sx). Each signal path has very similar characteristics in both directions. It is important to note, however, that the overvoltage protection is implemented only on the source (Sx) side. The voltage on the drain is only allowed to swing between V_{FP} and V_{FN} and no overvoltage protection is available on the drain side.

The primary supplies (V_{DD} and V_{SS}) define the on-resistance profile of the switch channel, whereas the fault voltage supplies (V_{FP} and V_{FN}) define the signal range that can be passed through from source to drain of the device. It is good practice to use voltages on V_{FP} and V_{FN} that are lower than V_{DD} and V_{SS} to take advantage of the flat on-resistance region of the device for better input-to-output linearity. The flattest on-resistance region extends from V_{SS} to roughly 3 V below V_{DD}. Once the signal is within 3 V of V_{DD} the on-resistance will exponentially increase and may impact desired signal transmission.

9.2.5 1.8 V Logic Compatible Inputs

The TMUX582F-SEP devices have 1.8 V logic compatible control for all logic control inputs. 1.8 V logic level inputs allows the TMUX582F-SEP to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations, refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

9.2.6 Integrated Pull-Down Resistor on Logic Pins

The TMUX582F-SEP have internal weak pull-down resistors to GND to confirm the logic pins are not left floating. The value of this pull-down resistor is approximately 4 MΩ, but is clamped to about 1 µA at higher voltages. This feature integrates up to four external components and reduces system size and cost.

9.3 Device Functional Modes

The TMUX582F-SEP offer two modes, Normal mode and Fault mode, of operation depending on whether any of the input pins experience overvoltage condition.

9.3.1 Normal Mode

In Normal mode operation, signals of up to V_{FP} and V_{FN} can be passed through the switch from source (Sx) to drain (D or Dx) or from drain (D or Dx) to source (Sx). As provided in Table 8-1, the address (Ax) pins and the enable (EN) pin determine which switch path to turn on, The following conditions must be satisfied for the switch to stay in the ON condition:

- The difference between the primary supplies (V_{DD} – V_{SS}) must be higher or equal to 8 V. With a minimum V_{DD} of 5 V.
- V_{FP} must between 3 V and V_{DD}, and V_{FN} must between V_{SS} and 0 V.
- The input signals on the source (Sx) or the drain (D or Dx) must be between V_{FP}+ V_T and V_{FN} – V_T.
- The logic control (Ax and EN) must have selected the switch.

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9.3.2 Fault Mode

The TMUX582F-SEP enters into Fault mode when any of the input signals on the source (Sx) pins exceed V_{FP} or V_{FN} by a threshold voltage V_T. Under the overvoltage condition, the switch input experiencing the fault automatically turns OFF regardless of the digital logic status, and the source pin becomes high impedance with a negligible amount of leakage current flowing through the switch. When the fault channel is selected by the digital logic control, the drain pin (D or Dx) is pulled to the supply that was exceeded through a 40 kΩ internal resistor.

In the Fault Mode, the general fault flag (FF) is asserted low. The specific flag (SF) is asserted low when a specific input path is selected, as provided in Table 8-1.

The overvoltage protection is provided only for the source (Sx) input pins. The drain (D or Dx) pin, if used as signal input, must stay in between V_{FP} and V_{FN} at all time since no overvoltage protection is implemented on the drain pin.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The TMUX582F-SEP is part of the fault protected switches and multiplexers family of devices. The ability to protect downstream components from overvoltage events up to ±60 V makes these switches and multiplexers suitable for harsh aerospace environments.

10.2 Typical Application

10.2.1 System Diagnostics – Telemetry

In large remote systems, on-board diagnostics is essential to correct fault scenarios. Through measuring subsystem voltage, current consumption, or a fault pin directly, the system MCU can easily detect where a potential issue surfaces and automatically correct it; however, this requires many ADC channels to accomplish. TMUX582F-SEP allows a significant reduction in ADC channels. Low distortion, charge injection and off-isolation increases measurement accuracy and helps reduce the likelihood of false positives or negatives. In addition, overvoltage and power-off or cold sparing protection helps prevent faults from the subsystems propagating throughout the system.

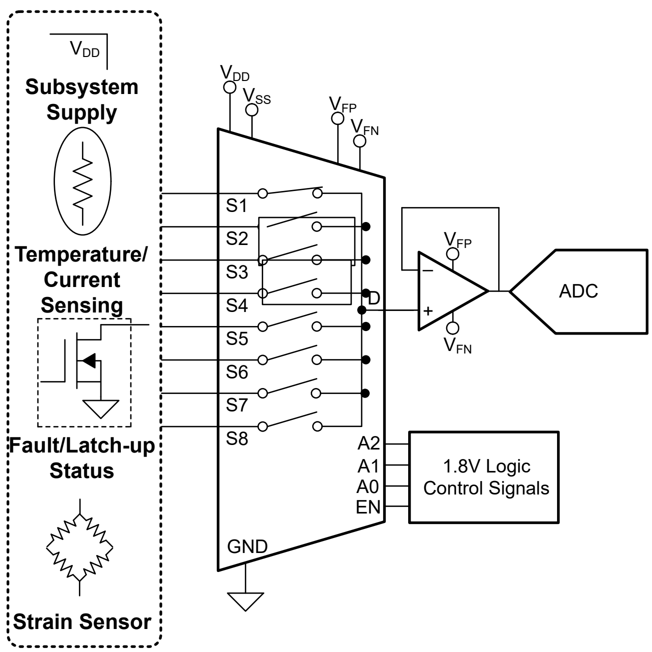


Figure 10-1. System Diagnostics - Telemetry

ADVANCE INFORMATION

10.2.2 Design Requirements

Table 10-1. Design Parameters

PARAMETER	VALUE
Positive supply (V_{DD}) mux	+12 V
Negative supply (V_{SS}) mux	-5 V
Positive fault voltage supply (V_{FP}) mux and ADC	+5 V
Negative fault voltage supply (V_{FN}) mux and ADC	0 V
Max power supply voltage on board	+24 V
Input / output signal range non-faulted	+5 V to 0 V
Overvoltage protection levels	-60 V to 60 V
Control logic thresholds	1.8 V compatible
Temperature range	-55°C to +125°C

10.2.3 Detailed Design Procedure

The TMUX582F-SEP is built on a latch-up immune process that can support telemetry applications by decreasing the number of ADC channels used while also reducing distortions in sampled inputs by maintaining an ultra low Ron flatness response that helps prevent false positives and negatives. TMUX582F-SEP also utilizes overvoltage and power-off protection (cold sparing capable up to ±60 V) which can help prevent downstream devices from experiencing these events.

10.2.4 Application Curves

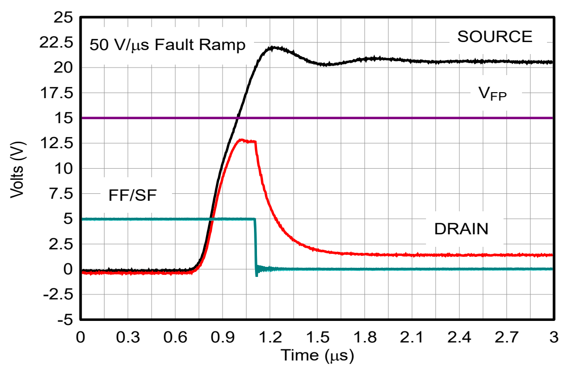


Figure 10-2. Positive Overvoltage Response

11 Power Supply Recommendations

The TMUX582F-SEP operates across a wide supply range of ±5 V to ±16.5 V (8 V to 22 V in single-supply mode). They also perform well with asymmetrical supplies such as V_{DD} = 12 V and V_{SS}= –5 V. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF at both the V_{DD} and V_{SS} pins to ground. Always ensure the ground (GND) connection is established before supplies are ramped. As a best practice, it is recommended to ramp V_{SS} first before V_{DD} in dual or asymmetrical supply applications.

The fault supplies (V_{FP} and V_{FN}) provide the current required to operate the fault protection, and thus, must be low impedance supplies. They can be derived from the primary supplies by using a resistor divider and buffer. The fault supplies must not exceed the primary supplies as it might cause unexpected behavior of the switch.

12 Layout

12.1 Layout Guidelines

The following image illustrates an example of a PCB layout with the TMUX582F-SEP. Some key considerations are:

- Decouple the V_{DD} and V_{SS} pins with a 0.1-μF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} and V_{SS} supplies.
- Keep the input lines as short as possible.
- Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

12.2 Layout Example

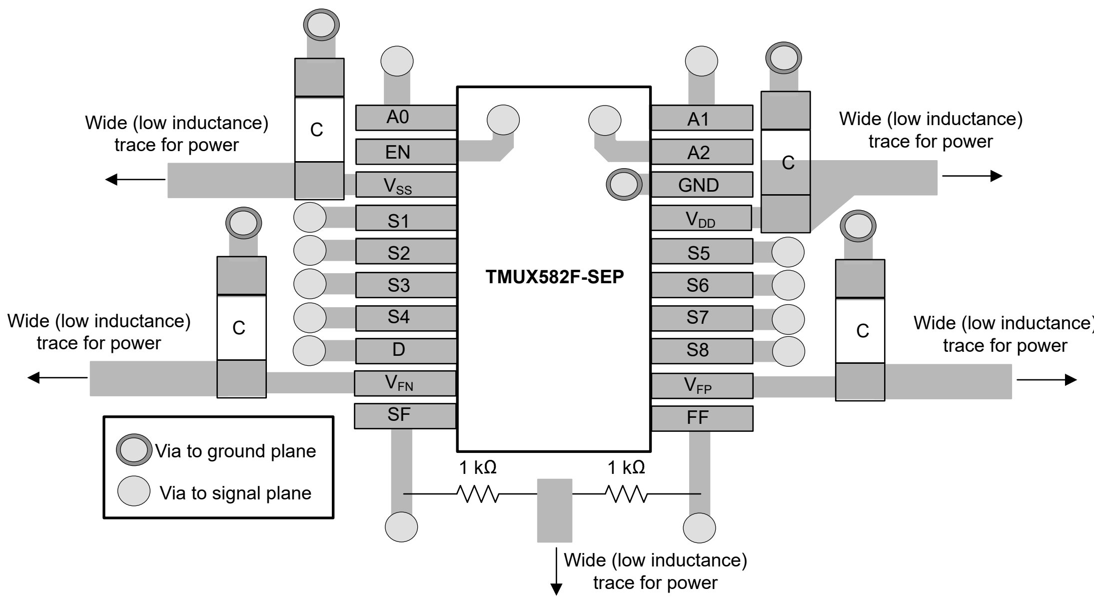


Figure 12-1. TMUX582F-SEP PW Layout Example

ADVANCE INFORMATION

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ADS866x 12-Bit, 500-kSPS, 4- and 8-Channel, Single-Supply, SAR ADCs with Bipolar Input Ranges*
- Texas Instruments, *OPAx140 High-Precision, Low-Noise, Rail-to-Rail Output, 11-MHz, JFET Op Amp*
- Texas Instruments, *OPAx192 36-V, Precision, Rail-to-Rail Input/Output, Low Offset Voltage, Low Input Bias Current Op Amp with e-trim™*

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

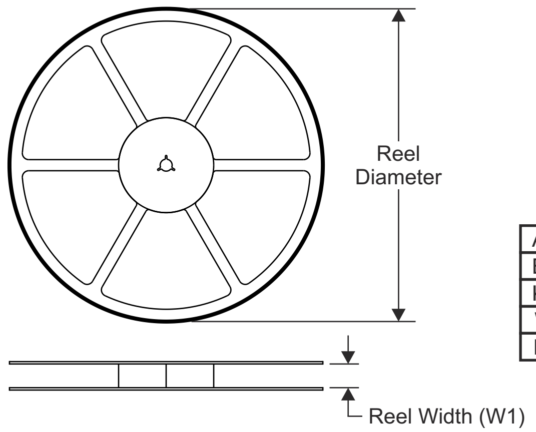
TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

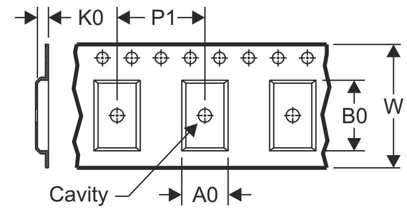
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

14.1 Tape and Reel Information

REEL DIMENSIONS

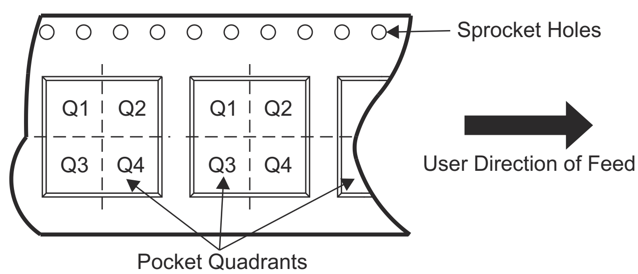


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

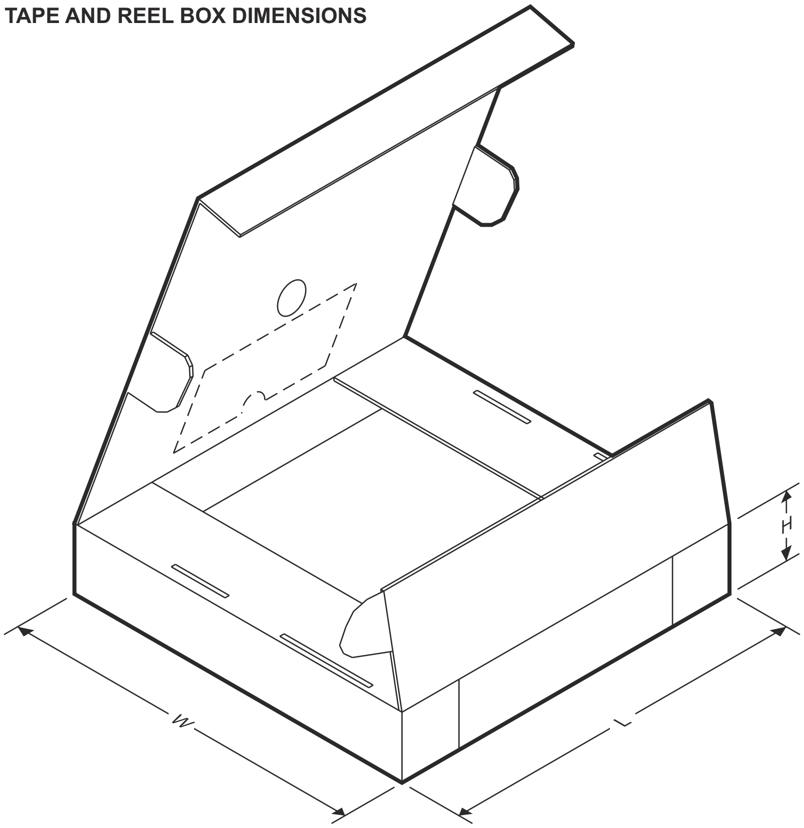
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX582FSEPPWR	TSSOP	PW	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



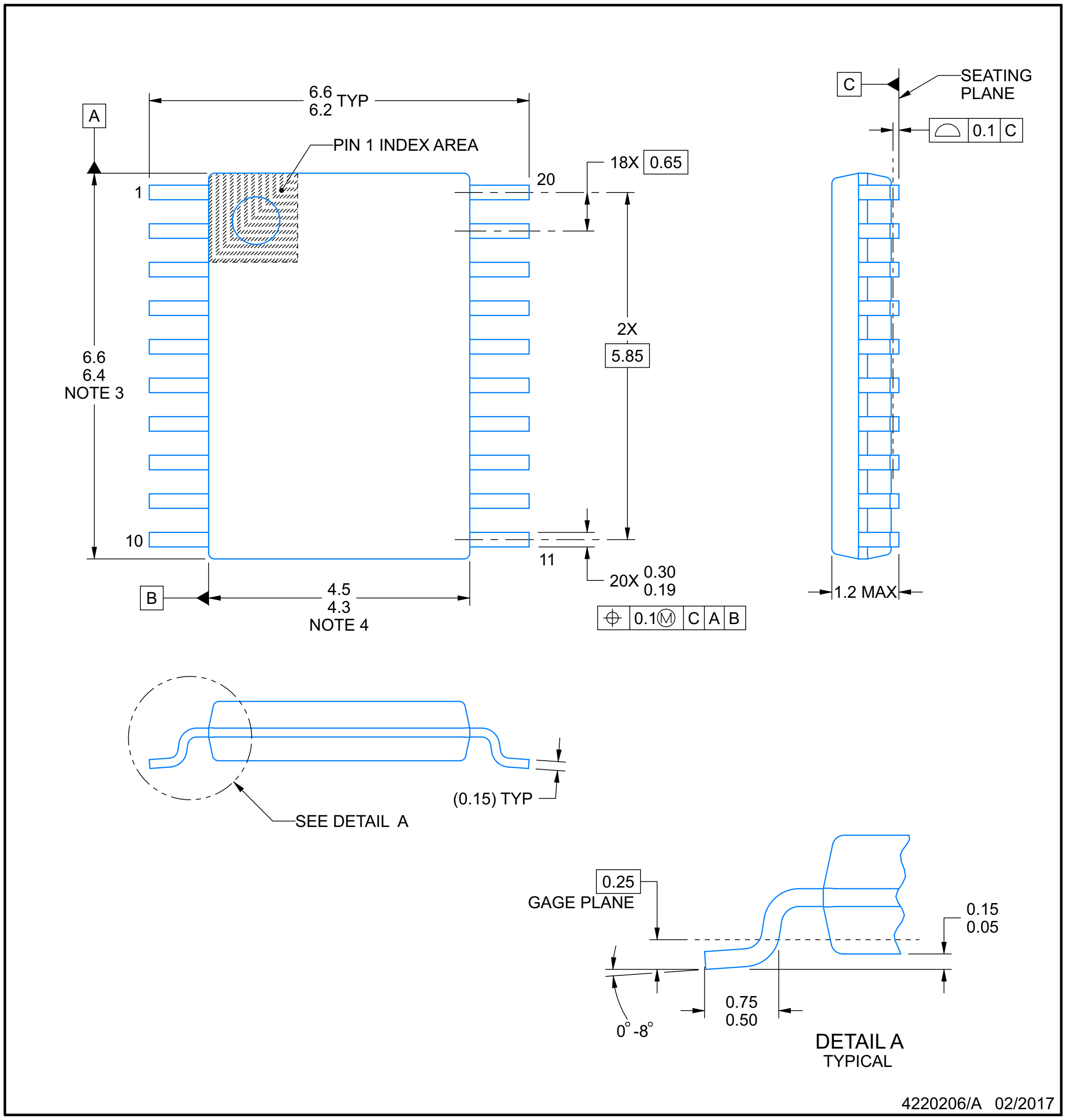
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX582FSEPPWR	TSSOP	PW	20	3000	367.0	367.0	35.0

14.2 Mechanical Data

PACKAGE OUTLINE

PW0020A **TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

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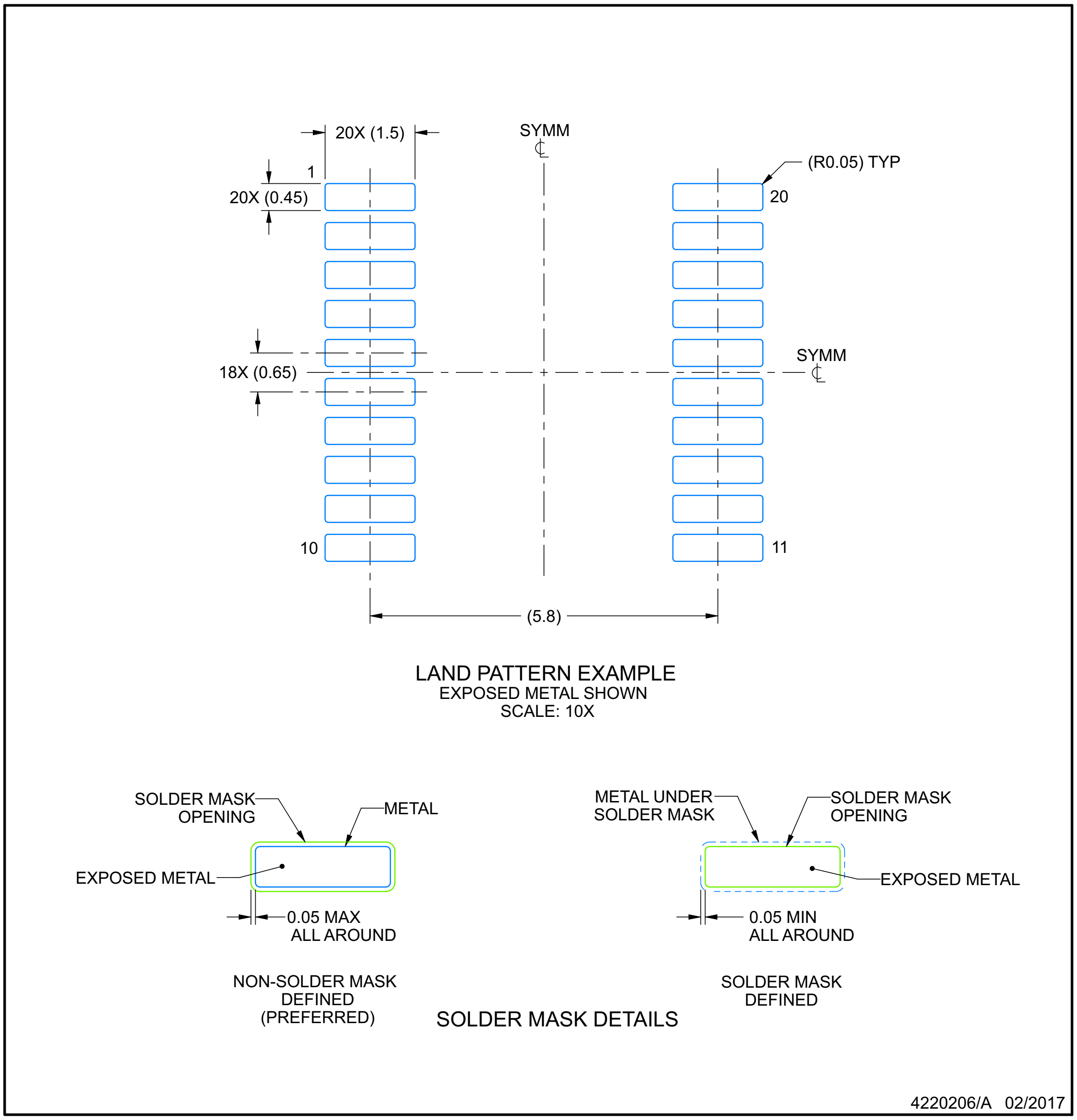
EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

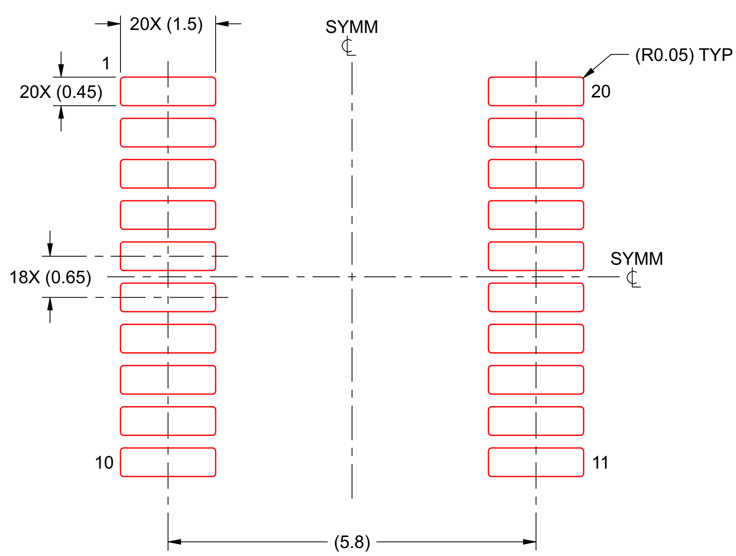
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PMUX582FPWTSEP	ACTIVE	TSSOP	PW	20	250	TBD	Call TI	Call TI	-55 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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