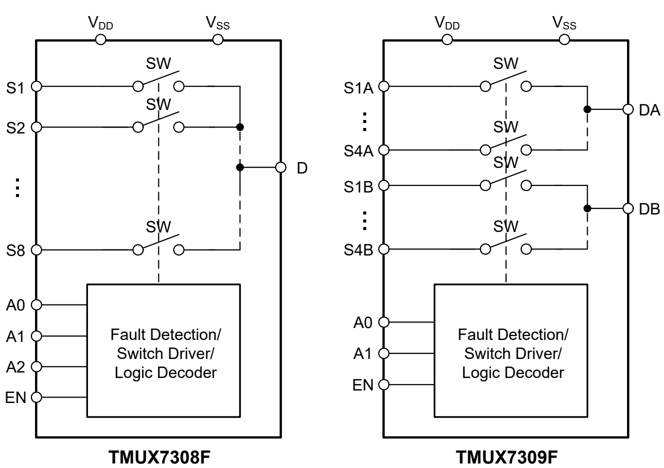
TMUX730xF ±60-V Fault-Protected, 8:1 and Dual 4:1 Multiplexers with Latch-Up Immunity and 1.8-V Logic

1 Features

- Wide supply range:
  - Dual supply: ±5 V to ±22 V
  - Single supply: 8 V to 44 V
- Integrated fault protection:
  - Overvoltage protection, source to supplies or source to drain: ±85 V
  - Overvoltage protection: ±60 V
  - Powered-off protection: ±60 V
  - Non-fault channels continue to operate
  - Known state without logic inputs present
  - Output clamped to the supply in overvoltage condition
- Latch-up immune
- 1.8-V Logic capable
- Fail-safe logic: up to 44 V independent of supply
- Integrated pull-down resistor on logic pins
- Break-before-make switching
- Industry standard TSSOP and smaller WQFN packages

2 Applications

- Factory automation and control
- Programmable logic controllers (PLC)
- Analog input modules
- Semiconductor test equipment
- Battery test equipment
- Servo drive control module
- Data acquisition systems (DAQ)



Functional Block Diagram

3 Description

The TMUX7308F and TMUX7309F are modern complementary metal-oxide semiconductor (CMOS) analog multiplexers in 8:1 (single ended) and 4:1 (differential) configurations. The devices work well with dual supplies (±5 V to ±22 V), a single supply (8 V to 44 V), or asymmetric supplies (such as V_{DD} = 12 V, V_{SS} = –5 V). The overvoltage protection is available in powered and powered-off conditions, making the TMUX7308F and TMUX7309F devices suitable for applications where power supply sequencing cannot be precisely controlled.

The device blocks fault voltage up to +60 V or –60 V relative to ground in both powered and powered-off conditions. When no power supplies are present, the switch channels remain in the OFF state regardless of switch input conditions and logic control status. Under normal operation conditions, if the analog input signal level on any Sx pin exceeds the supply voltage (V_{DD} or V_{SS}) by a threshold voltage (V_T), the channel turns OFF and the Sx pin becomes high impedance. When the fault channel is selected, the drain pin (D or Dx) is pulled to the supply (V_{DD} or V_{SS}) that was exceeded.

The low capacitance, low charge injection, and integrated fault protection enables the TMUX7308F and TMUX7309F devices to be used in front end data acquisition applications where high performance and high robustness are both critical. The devices are available in a standard TSSOP package and smaller WQFN package (ideal if PCB space is limited).

Device Information

PART NUMBER	CONFIGURATION(1)	PACKAGE(2)	PACKAGE SIZE(3)
TMUX7308F TMUX7309F	1 Channel 8:1 2 Channel 4:1	PW (TSSOP, 16)	5 mm × 6.4 mm
		RRP (WQFN, 16)	4 mm × 4 mm

(1) See the *Device Comparison Table*.
(2) For all available packages, see the package option addendum at the end of the data sheet.
(3) The package size (length × width) is a nominal value and includes pins, where applicable.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (December 2021) to Revision C (July 2023)	Page
• Changed the status of the PW package from: *preview* to: *active*	1
• Updated the *Device Information* table to include configuration and package size	1

Changes from Revision A (October 2021) to Revision B (December 2021)	Page
• Changed the status of the data sheet from: *Advanced Information* to: *Production Data*	1

5 Device Comparison Table

PRODUCT	DESCRIPTION
TMUX7308F	+60 V/ –60 V Tolerant, Fault-protected, Latch-up Immune, Single-Ended 8:1 Multiplexer
TMUX7309F	+60 V/ –60 V Tolerant, Fault-protected, Latch-up Immune, 4:1, 2-Channel Multiplexer

6 Pin Configuration and Functions

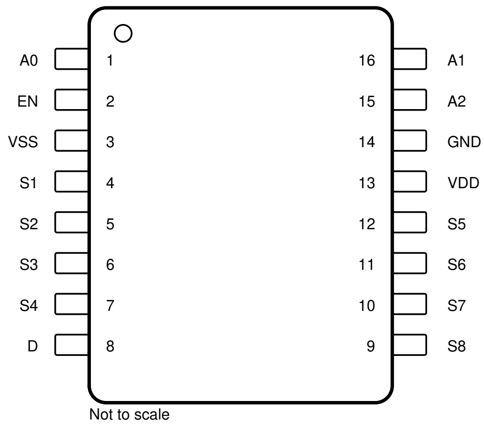


Figure 6-1. PW Package, 16-Pin TSSOP (Top View)

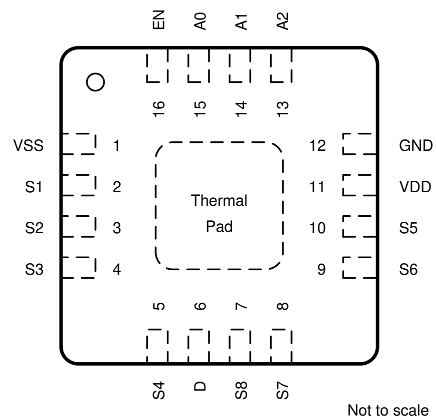


Figure 6-2. RRP Package, 16-Pin WQFN (Top View)

Table 6-1. Pin Functions: TMUX7308F

PIN			TYPE[(1)]	DESCRIPTION
NAME	TSSOP	WQFN		
A0	1	15	I	Logic control input address 0 (A0), has internal 4 MΩ pull-down resistor. Controls switch state as shown in Section 9.4.3.
EN	2	16	I	Active high logic enable (EN) pin, has internal 4 MΩ pull-down resistor. The device is disabled and all switches become high impedance when the pin is low. When the pin is high, the Ax logic inputs determine individual switch states as shown in Section 9.4.3.
V_{SS}	3	1	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
S1	4	2	I/O	Overvoltage protected source pin 1. Can be an input or output.
S2	5	3	I/O	Overvoltage protected source pin 2. Can be an input or output.
S3	6	4	I/O	Overvoltage protected source pin 3. Can be an input or output.
S4	7	5	I/O	Overvoltage protected source pin 4. Can be an input or output.
D	8	6	I/O	Drain pin. Can be an input or output. The drain pin is not overvoltage protected.
S8	9	7	I/O	Overvoltage protected source pin 8. Can be an input or output.
S7	10	8	I/O	Overvoltage protected source pin 7. Can be an input or output.
S6	11	9	I/O	Overvoltage protected source pin 6. Can be an input or output.
S5	12	10	I/O	Overvoltage protected source pin 5. Can be an input or output.
V_{DD}	13	11	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
GND	14	12	P	Ground (0 V) reference
A2	15	13	I	Logic control input address 2 (A2), has internal 4 MΩ pull-down resistor. Controls switch state as shown in Section 9.4.3.
A1	16	14	I	Logic control input address 1 (A1), has internal 4 MΩ pull-down resistor. Controls switch state as shown in Section 9.4.3.
Thermal Pad			P	The thermal pad is not connected internally. It is recommended that the pad be tied to GND or V_{SS} for best performance.

(1) I = input, O = output, I/O = input and output, P = power

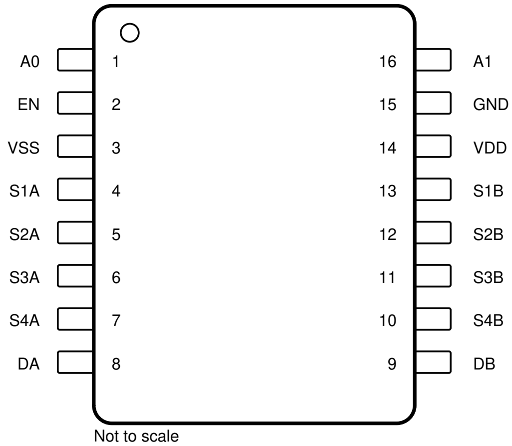


Figure 6-3. PW Package, 16-Pin TSSOP (Top View)

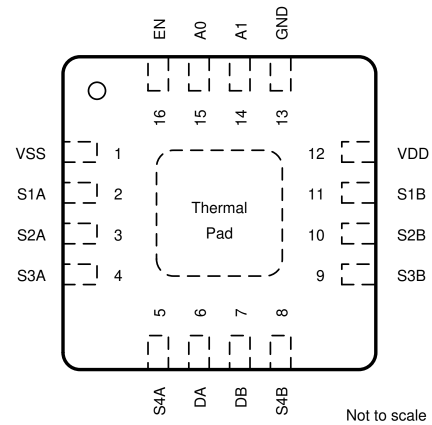


Figure 6-4. RRP Package, 16-Pin WQFN (Top View)

Table 6-2. Pin Functions: TMUX7309F

PIN			TYPE[(1)]	DESCRIPTION
NAME	TSSOP	WQFN		
A0	1	15	I	Logic control input address 0 (A0), has internal 4 MΩ pull-down resistor. Controls switch state as shown in Section 9.4.3.
EN	2	16	I	Active high logic enable (EN) pin, has internal 4 MΩ pull-down resistor. The device is disabled and all switches become high impedance when the pin is low. When the pin is high, the Ax logic inputs determine individual switch states as shown in Section 9.4.3.
V_{SS}	3	1	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
S1A	4	2	I/O	Overvoltage protected source pin 1A. Can be an input or output.
S2A	5	3	I/O	Overvoltage protected source pin 2A. Can be an input or output.
S3A	6	4	I/O	Overvoltage protected source pin 3A. Can be an input or output.
S4A	7	5	I/O	Overvoltage protected source pin 4A. Can be an input or output.
DA	8	6	I/O	Drain terminal A. Can be an input or output. The drain pin is not overvoltage protected.
DB	9	7	I/O	Drain terminal B. Can be an input or output. The drain pin is not overvoltage protected.
S4B	10	8	I/O	Overvoltage protected source pin 4B. Can be an input or output.
S3B	11	9	I/O	Overvoltage protected source pin 3B. Can be an input or output.
S2B	12	10	I/O	Overvoltage protected source pin 2B. Can be an input or output.
S1B	13	11	I/O	Overvoltage protected source pin 1B. Can be an input or output.
V_{DD}	14	12	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
GND	15	13	P	Ground (0 V) reference
A1	16	14	I	Logic control input address 1 (A1), has internal 4 MΩ pull-down resistor. Controls switch state as shown in Section 9.4.3.
Thermal Pad			P	The thermal pad is not connected internally. It is recommended that the pad be tied to GND or V_{SS} for best performance.

(1) I = input, O = output, I/O = input and output, P = power

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{DD} to V_{SS}	Supply voltage		48	V
V_{DD} to GND		–0.3	48	V
V_{SS} to GND		–48	0.3	V
V_S to GND	Source input pin (Sx) voltage to GND	–65	65	V
V_S to V_{DD}	Source input pin (Sx) voltage to V_{DD}	–90		V
V_S to V_{SS}	Source input pin (Sx) voltage to V_{SS}		90	V
V_D	Drain pin (D or Dx) voltage	V_{SS}–0.7	V_{DD}+0.7	V
V_{EN} or V_{Ax}	Logic control input pin voltage (EN, A0, A1, A2)[2]	GND –0.7	48	V
I_{EN} or I_{Ax}	Logic control input pin current (EN, A0, A1, A2)[2]	–30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx or D)	I_{DC} ± 10 %[3]	I_{DC} ± 10 %[3]	mA
T_{stg}	Storage temperature	–65	150	°C
T_A	Ambient temperature	–55	150	°C
T_J	Junction temperature		150	°C
P_{tot} [4]	Total power dissipation (QFN)		1600	mW
P_{tot} [5]	Total power dissipation (TSSOP)		650	mW

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Stresses have to be kept at or below both voltage and current ratings at all time.
(3) Refer to Recommended Operating Conditions for I_{DC} ratings.
(4) For QFN package: P_{tot} derates linearly above T_A = 70°C by 23.5 mW/°C
(5) For TSSOP package: P_{tot} derates linearly above T_A = 70°C by 10.1 mW/°C

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±3500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002[2]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible if necessary precautions are taken.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible if necessary precautions are taken.

7.3 Thermal Information

THERMAL METRIC[1]		TMUX7308F/ TMUX7309F PW (TSSOP) 16 PINS	TMUX7308F/ TMUX7309F RRP (QFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100.4	43.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.3	28.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.4	17.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.7	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	45.8	17.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	4.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$ [1]	Power supply voltage differential		8		44	V
V_{DD}	Positive power supply voltage		5		44	V
V_S	Source pin (Sx) voltage (non-fault condition)		V_{SS}		V_{DD}	V
V_S to GND	Source pin (Sx) voltage to GND (fault condition)		–60		60	V
V_S to V_{DD} [2]	Source pin (Sx) voltage to V_{DD} or V_D (fault condition)		–85			V
V_S to V_{SS} [2]	Source pin (Sx) voltage to V_{SS} or V_D (fault condition)				85	V
V_D	Drain pin (D, Dx) voltage		V_{SS}		V_{DD}	V
V_{EN} or V_{Ax}	Logic control input pin voltage (EN, A0, A1, A2)		0		44	V
T_A	Ambient temperature		–40		125	°C
I_{DC}	Continuous current through switch	T_A = 25°C			9	mA
		T_A = 85°C			6.5	mA
		T_A = 125°C			5	mA

(1) V_{DD} and V_{SS} can be any value as long as 8 V ≤ ($V_{DD} – V_{SS}$) ≤ 44 V, and the minimum V_{DD} is met.
(2) Under a fault condition, the potential difference between source pin (Sx) and supply pins (V_{DD} and V_{SS}.) or source pin (Sx) and drain pins (D, Dx) may not exceed 85 V.

7.5 Electrical Characteristics (Global)

at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_T	Threshold voltage for fault detector		25°C		0.7		V
LOGIC INPUT/ OUTPUT							
V_{IH}	High-level input voltage	EN, Ax pins	–40°C to +125°C	1.3		44	V
V_{IL}	Low-level input voltage	EN, Ax pins	–40°C to +125°C	0		0.8	V
POWER SUPPLY							
V_{UVLO}	Undervoltage lockout (UVLO) threshold voltage ($V_{DD} – V_{SS}$)	Rising edge, single supply	–40°C to +125°C	5.1	6	6.4	V
	Undervoltage lockout (UVLO) threshold voltage ($V_{DD} – V_{SS}$)	Falling edge, single supply	–40°C to +125°C	5	5.8	6.3	V
V_{HYS}	V_{DD} Undervoltage lockout (UVLO) hysteresis	Single supply	–40°C to +125°C		0.2		V
$R_{D(OVP)}$	Drain resistance to supply rail during overvoltage event on selected source pin		25°C		40		kΩ

7.6 ±15 V Dual Supply: Electrical Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10 V to +10 V, I_S = –1 mA	25°C		180	250	Ω
			–40°C to +85°C			330	
			–40°C to +125°C			390	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10 V to +10 V, I_S = –1 mA	25°C		2.5	8	Ω
			–40°C to +85°C			12	
			–40°C to +125°C			13	
R_{FLAT}	On-resistance flatness	V_S = –10 V to +10 V, I_S = –1 mA	25°C		1.5	3.5	Ω
			–40°C to +85°C			4	
			–40°C to +125°C			4	
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V, I_S = –1 mA	–40°C to +125°C		1		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V	25°C	–1	0.1	1	nA
			–40°C to +85°C	–1		1	
			–40°C to +125°C	–4		4	
$I_{D(OFF)}$	Drain off leakage current[1]	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V	25°C	–1	0.1	1	nA
			–40°C to +85°C	–3		3	
			–40°C to +125°C	–14		14	
$I_{S(ON)}$ $I_{D(ON)}$	Output on leakage current[2]	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is on V_S = V_D = ±10 V	25°C	–1.5	0.3	1.5	nA
			–40°C to +85°C	–5		5	
			–40°C to +125°C	–22		22	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current during overvoltage	V_S = ± 60 V, GND = 0 V, V_{DD} = 16.5 V, V_{SS} = –16.5 V	–40°C to +125°C		±110		µA
$I_{S(FA)\ Grounded}$	Input leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V V_{DD} = V_{SS} = 0 V	–40°C to +125°C		±135		µA
$I_{S(FA)\ Floating}$	Input leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = floating	–40°C to +125°C		±135		µA
$I_{D(FA)}$	Output leakage current during overvoltage	V_S = ± 60 V, GND = 0 V, V_{DD} = 16.5 V, V_{SS} = –16.5 V, –15.5V ≤ V_D ≤ 16.5V	25°C	–50	±10	50	nA
			–40°C to +85°C	–70		70	
			–40°C to +125°C	–90		90	
$I_{D(FA)\ Grounded}$	Output leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = 0 V	25°C	–50	±1	50	nA
			–40°C to +85°C	–100		100	
			–40°C to +125°C	–500		500	
$I_{D(FA)\ Floating}$	Output leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = floating	25°C		±3		µA
			–40°C to +85°C		±5		
			–40°C to +125°C		±8		
LOGIC INPUT/ OUTPUT							
I_{IH}	High-level input current	V_{EN} = V_{Ax} = V_{DD}	25°C	–2	± 0.6	2	µA
			–40°C to +125°C	–2		2	
I_{IL}	Low-level input current	V_{EN} = V_{Ax} = 0 V	25°C	–1.1	± 0.6	1.1	µA
			–40°C to +125°C	–1.2		1.2	

7.6 ±15 V Dual Supply: Electrical Characteristics (continued)

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
$t_{ON (EN)}$	Enable turn-on time	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	25°C		165	265	ns
			–40°C to +85°C			285	
			–40°C to +125°C			300	
$t_{OFF (EN)}$	Enable turn-off time	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	25°C		350	400	ns
			–40°C to +85°C			400	
			–40°C to +125°C			420	
t_{TRAN}	Transition time	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	25°C		170	225	ns
			–40°C to +85°C			245	
			–40°C to +125°C			260	
$t_{RESPONSE}$	Fault response time	R_L = 4 kΩ, C_L= 12 pF	25°C		300		ns
$t_{RECOVERY}$	Fault recovery time	R_L = 4 kΩ, C_L= 12 pF	25°C		1.2		µs
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	–40°C to +125°C	50	120		ns
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 1 nF	25°C		–15		pC
O_{ISO}	Off-isolation	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–82		dB
X_{TALK}	Intra-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–95		dB
	Inter-channel crosstalk (TMUX7309F)				–103		
BW	–3 dB bandwidth (TMUX7308F)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V	25°C		150		MHz
	–3 dB bandwidth (TMUX7309F WQFN Package)				280		
	–3 dB bandwidth (TMUX7309F TSSOP Package)				240		
I_{LOSS}	Insertion loss	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–9		dB
THD+N	Total harmonic distortion plus noise	R_S = 40 Ω, R_L = 10 kΩ, V_S = 15 V_{PP}, V_{BIAS} = 0 V, f = 20 Hz to 20 kHz	25°C		0.0015		%
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 0 V	25°C		3.5		pF
$C_{D(OFF)}$	Output off-capacitance (TMUX7308F)	f = 1 MHz, V_S = 0 V	25°C		28		pF
	Output off-capacitance (TMUX7309F)	f = 1 MHz, V_S = 0 V	25°C		15		pF
$C_{S(ON)}$ $C_{D(ON)}$	Input/Output on-capacitance (TMUX7308F)	f = 1 MHz, V_S = 0 V	25°C		30		pF
	Input/Output on-capacitance (TMUX7309F)	f = 1 MHz, V_S = 0 V	25°C		17		pF

7.6 ±15 V Dual Supply: Electrical Characteristics (continued)

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.25	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
I_{SS}	V_{SS} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15	0.4	mA
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.4	
I_{GND}	GND current	V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.075		mA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = ± 60 V, V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.25	1	mA
			–40°C to +85°C			1	
			–40°C to +125°C			1	
$I_{SS(FA)}$	V_{SS} supply current under fault	V_S = ± 60 V, V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
$I_{GND(FA)}$	GND current under fault	V_S = ± 60 V, V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15		mA
$I_{DD(DISABLE)}$	V_{DD} supply current (disable mode)	V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
$I_{SS(DISABLE)}$	V_{SS} supply current (disable mode)	V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.1	0.4	mA
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.4	

(1) When V_S is positive, V_D is negative. And when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating. And when V_D is at a voltage potential, V_S is floating.

7.7 ±20 V Dual Supply: Electrical Characteristics

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –15 V to +15 V, I_S = –1 mA	25°C		180	250	Ω
			–40°C to +85°C			330	
			–40°C to +125°C			390	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –15 V to +15 V, I_S = –1 mA	25°C		2.5	8	Ω
			–40°C to +85°C			12	
			–40°C to +125°C			13	
R_{FLAT}	On-resistance flatness	V_S = –15 V to +15 V, I_S = –1 mA	25°C		8	10	Ω
			–40°C to +85°C			12	
			–40°C to +125°C			12	
R_{FLAT}	On-resistance flatness	V_S = –13.5 V to +13.5 V, I_S = –1 mA	25°C		1.5	3.5	Ω
			–40°C to +85°C			4	
			–40°C to +125°C			4	
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V, I_S = –1 mA	–40°C to +125°C		1		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V	25°C	–1	0.1	1	nA
			–40°C to +85°C	–1		1	
			–40°C to +125°C	–4		4	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is off V_S = +15 V / –15 V V_D = –15 V / + 15 V	25°C	–1	0.1	1	nA
			–40°C to +85°C	–3		3	
			–40°C to +125°C	–14		14	
$I_{S(ON)}$ $I_{D(ON)}$	Output on leakage current(2)	V_{DD} = 22 V, V_{SS} = –22 V Switch state is on V_S = V_D = ±15 V	25°C	–1.5	0.3	1.5	nA
			–40°C to +85°C	–5		5	
			–40°C to +125°C	–22		22	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current during overvoltage	V_S = ± 60 V, GND = 0 V, V_{DD} = 22 V, V_{SS} = –22 V	–40°C to +125°C		±95		µA
$I_{S(FA)\ Grounded}$	Input leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = 0 V	–40°C to +125°C		±135		µA
$I_{S(FA)\ Floating}$	Input leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = floating	–40°C to +125°C		±135		µA
$I_{D(FA)}$	Output leakage current during overvoltage	V_S = ± 60 V, GND = 0V, V_{DD} = 22 V, V_{SS} = –22 V, –21V ≤ V_D ≤ 22V	25°C	–50	±10	50	nA
			–40°C to +85°C	–70		70	
			–40°C to +125°C	–90		90	
$I_{D(FA)\ Grounded}$	Output leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = 0 V	25°C	–50	±1	50	nA
			–40°C to +85°C	–100		100	
			–40°C to +125°C	–500		500	
$I_{D(FA)\ Floating}$	Output leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = floating	25°C		±3		µA
			–40°C to +85°C		±5		
			–40°C to +125°C		±8		
LOGIC INPUT/ OUTPUT							
I_{IH}	High-level input current	V_{EN} = V_{Ax} = V_{DD}	25°C	–2.2	± 0.6	2.2	µA
			–40°C to +125°C	–2.2		2.2	
I_{IL}	Low-level input current	V_{EN} = V_{Ax} = 0 V	25°C	–1.1	± 0.6	1.1	µA
			–40°C to +125°C	–1.2		1.2	

7.7 ±20 V Dual Supply: Electrical Characteristics (continued)

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
$t_{ON\ (EN)}$	Enable turn-on time	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	25°C		175	300	ns
			–40°C to +85°C			325	ns
			–40°C to +125°C			350	ns
$t_{OFF\ (EN)}$	Enable turn-off time	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	25°C		350	400	ns
			–40°C to +85°C			400	ns
			–40°C to +125°C			420	ns
t_{TRAN}	Transition time	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	25°C		170	245	ns
			–40°C to +85°C			270	ns
			–40°C to +125°C			285	ns
$t_{RESPONSE}$	Fault response time	R_L = 4 kΩ, C_L= 12 pF	25°C		300		ns
$t_{RECOVERY}$	Fault recovery time	R_L = 4 kΩ, C_L= 12 pF	25°C		1.2		μs
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	–40°C to +125°C	50	120		ns
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 1 nF	25°C		–17		pC
O_{ISO}	Off-isolation	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–85		dB
X_{TALK}	Intra-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–95		dB
	Inter-channel crosstalk (TMUX7309F)				–103		dB
BW	–3 dB bandwidth (TMUX7308F)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V	25°C		150		MHz
	–3 dB bandwidth (TMUX7309F WQFN Package)				285		MHz
	–3 dB bandwidth (TMUX7309F TSSOP Package)				245		MHz
I_{LOSS}	Insertion loss	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–9		dB
THD+N	Total harmonic distortion plus noise	R_S = 40 Ω, R_L = 10 kΩ, V_S = 20 V_{PP}, V_{BIAS} = 0 V, f = 20 Hz to 20 kHz	25°C		0.0015		%
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 0 V	25°C		3.5		pF
$C_{D(OFF)}$	Output off-capacitance (TMUX7308F)	f = 1 MHz, V_S = 0 V	25°C		28		pF
	Output off-capacitance (TMUX7309F)	f = 1 MHz, V_S = 0 V	25°C		14		pF
$C_{S(ON)}$ $C_{D(ON)}$	Input/Output on-capacitance (TMUX7308F)	f = 1 MHz, V_S = 0 V	25°C		30		pF
	Input/Output on-capacitance (TMUX7309F)	f = 1 MHz, V_S = 0 V	25°C		16		pF

7.7 ±20 V Dual Supply: Electrical Characteristics (continued)

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 22 V, V_{SS} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.25	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
I_{SS}	V_{SS} supply current	V_{DD} = 22 V, V_{SS} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15	0.4	mA
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.4	
I_{GND}	GND current	V_{DD} = 22 V, V_{SS} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.075		mA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = ± 60 V, V_{DD} = 22 V, V_{SS} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.25	1	mA
			–40°C to +85°C			1	
			–40°C to +125°C			1	
$I_{SS(FA)}$	V_{SS} supply current under fault	V_S = ± 60 V, V_{DD} = 22 V, V_{SS} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
$I_{GND(FA)}$	GND current under fault	V_S = ± 60 V, V_{DD} = 22 V, V_{SS} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15		mA
$I_{DD(DISABLE)}$	V_{DD} supply current (disable mode)	V_{DD} = 22 V, V_{SS} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	mA
			–40°C to +125°C			0.5	mA
$I_{SS(DISABLE)}$	V_{SS} supply current (disable mode)	V_{DD} = 22 V, V_{SS} = –22 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.1	0.4	mA
			–40°C to +85°C			0.4	mA
			–40°C to +125°C			0.4	mA

(1) When V_S is positive,V_D is negative. And when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating. And when V_D is at a voltage potential, V_S is floating.

7.8 12 V Single Supply: Electrical Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 7.8 V, I_S = –1 mA	25°C		180	250	Ω
			–40°C to +85°C			330	Ω
			–40°C to +125°C			390	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 7.8 V, I_S = –1 mA	25°C		2.5	8	Ω
			–40°C to +85°C			12	
			–40°C to +125°C			13	
R_{FLAT}	On-resistance flatness	V_S = 0 V to 7.8 V, I_S = –1 mA	25°C		7	30	Ω
			–40°C to +85°C			45	
			–40°C to +125°C			75	
R_{FLAT}	On-resistance flatness	V_S = 1 V to 7.8 V, I_S = –1 mA	25°C		1.5	7	Ω
			–40°C to +85°C			8	
			–40°C to +125°C			8	
R_{ON_DRIFT}	On-resistance drift	V_S = 6 V, I_S = –1 mA	–40°C to +125°C		1		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V	25°C	–1	0.1	1	nA
			–40°C to +85°C	–1		1	
			–40°C to +125°C	–4		4	
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V	25°C	–1	0.1	1	nA
			–40°C to +85°C	–3		3	
			–40°C to +125°C	–14		14	
$I_{S(ON)}$ $I_{D(ON)}$	Output on leakage current(2)	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is on V_S = V_D = 10 V or 1 V	25°C	–1.5	0.3	1.5	nA
			–40°C to +85°C	–5		5	
			–40°C to +125°C	–22		22	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current during overvoltage	V_S = ± 60 V, GND = 0 V, V_{DD} = 13.2 V, V_{SS} = 0 V	–40°C to +125°C		±145		µA
$I_{S(FA)\ Grounded}$	Input leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = 0 V	–40°C to +125°C		±135		µA
$I_{S(FA)\ Floating}$	Input leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = floating	–40°C to +125°C		±135		µA
$I_{D(FA)}$	Output leakage current during overvoltage	V_S = ± 60 V, GND = 0 V, V_{DD} = 13.2 V, V_{SS} = 0 V, 1V ≤ V_D ≤ 13.2V	25°C	–50	±10	50	nA
			–40°C to +85°C	–70		70	
			–40°C to +125°C	–90		90	
$I_{D(FA)\ Grounded}$	Output leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = 0 V	25°C	–50	±1	50	nA
			–40°C to +85°C	–100		100	
			–40°C to +125°C	–500		500	
$I_{D(FA)\ Floating}$	Output leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = floating	25°C		±3		µA
			–40°C to +85°C		±5		
			–40°C to +125°C		±8		
LOGIC INPUT/ OUTPUT							
I_{IH}	High-level input current	V_{EN} = V_{Ax} = V_{DD}	25°C	–2	± 0.6	2	µA
			–40°C to +125°C	–2		2	
I_{IL}	Low-level input current	V_{EN} = V_{Ax} = 0 V	25°C	–1.1	± 0.6	1.1	µA
			–40°C to +125°C	–1.2		1.2	

7.8 12 V Single Supply: Electrical Characteristics (continued)

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
$t_{ON\ (EN)}$	Enable turn-on time	V_S = 8 V, R_L = 4 kΩ, C_L= 12 pF	25°C		160	265	ns
			–40°C to +85°C			285	
			–40°C to +125°C			300	
$t_{OFF\ (EN)}$	Enable turn-off time	V_S = 8 V, R_L = 4 kΩ, C_L= 12 pF	25°C		420	485	ns
			–40°C to +85°C			485	
			–40°C to +125°C			500	
t_{TRAN}	Transition time	V_S = 8 V, R_L = 4 kΩ, C_L= 12 pF	25°C		160	215	ns
			–40°C to +85°C			230	
			–40°C to +125°C			240	
$t_{RESPONSE}$	Fault response time	R_L = 4 kΩ, C_L= 12 pF	25°C		220		ns
$t_{RECOVERY}$	Fault recovery time	R_L = 4 kΩ, C_L= 12 pF	25°C		0.63		µs
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 4 kΩ, C_L= 12 pF	–40°C to +125°C	30	90		ns
Q_{INJ}	Charge injection	V_S = 6 V, C_L = 1 nF	25°C		–11		pC
O_{ISO}	Off-isolation	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–76		dB
X_{TALK}	Intra-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–93		dB
	Inter-channel crosstalk (TMUX7309F)				–103		
BW	–3 dB bandwidth (TMUX7308F)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V	25°C		130		MHz
	–3 dB bandwidth (TMUX7309F WQFN Package)				250		
	–3 dB bandwidth (TMUX7309F TSSOP Package)				218		
I_{LOSS}	Insertion loss	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–9		dB
THD+N	Total harmonic distortion plus noise	R_S = 40 Ω, R_L = 10 kΩ, V_S = 6 V_{PP}, V_{BIAS} = 6 V, f = 20 Hz to 20 kHz	25°C		0.002		%
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 6 V	25°C		4		pF
$C_{D(OFF)}$	Output off-capacitance (TMUX7308F)	f = 1 MHz, V_S = 6 V	25°C		31		pF
	Output off-capacitance (TMUX7309F)	f = 1 MHz, V_S = 6 V	25°C		16		
$C_{S(ON)}$ $C_{D(ON)}$	Input/Output on-capacitance (TMUX7308F)	f = 1 MHz, V_S = 6 V	25°C		34		pF
	Input/Output on-capacitance (TMUX7309F)	f = 1 MHz, V_S = 6 V	25°C		20		

7.8 12 V Single Supply: Electrical Characteristics (continued)

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.25	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
I_{SS}	V_{SS} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15	0.4	mA
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.4	
I_{GND}	GND current	V_{DD} = 13.2 V, V_{SS} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.075		mA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = ± 60 V, V_{DD} = 13.2 V, V_{SS} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.25	1	mA
			–40°C to +85°C			1	
			–40°C to +125°C			1	
$I_{SS(FA)}$	V_{SS} supply current under fault	V_S = ± 60 V, V_{DD} = 13.2 V, V_{SS} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
$I_{GND(FA)}$	GND current under fault	V_S = ± 60 V, V_{DD} = 13.2 V, V_{SS} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.17		mA
$I_{DD(DISABLE)}$	V_{DD} supply current (disable mode)	V_{DD} = 13.2 V, V_{SS} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
$I_{SS(DISABLE)}$	V_{SS} supply current (disable mode)	V_{DD} = 13.2 V, V_{SS} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.1	0.4	mA
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.4	

(1) When V_S is 10 V, V_D is 1 V. Or when V_S is 1 V, V_D is 10 V.
(2) When V_S is at a voltage potential, V_D is floating. Or when V_D is at a voltage potential, V_S is floating.

7.9 36 V Single Supply: Electrical Characteristics

V_{DD} = +36 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +36 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 28 V, I_S = –1 mA	25°C		180	250	Ω
			–40°C to +85°C			330	
			–40°C to +125°C			390	
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 28 V, I_S = –1 mA	25°C		2.5	8	Ω
			–40°C to +85°C			12	
			–40°C to +125°C			13	
R_{FLAT}	On-resistance flatness	V_S = 0 V to 30 V, I_S = –1 mA	25°C		8	65	Ω
			–40°C to +85°C			75	
			–40°C to +125°C			90	
R_{FLAT}	On-resistance flatness	V_S = 1 V to 28 V, I_S = –1 mA	25°C		1.5	3	Ω
			–40°C to +85°C			4	
			–40°C to +125°C			4	
R_{ON_DRIFT}	On-resistance drift	V_S = 18 V, I_S = –1 mA	–40°C to +125°C		1		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 39.6 V, V_{SS} = 0 V Switch state is off V_S = 30 V / 1 V V_D = 1 V / 30 V	25°C	–1	0.1	1	nA
			–40°C to +85°C	–1		1	
			–40°C to +125°C	–4		4	
$I_{D(OFF)}$	Output on leakage current[2]	V_{DD} = 39.6 V, V_{SS} = 0 V Switch state is off V_S = 30 V / 1 V V_D = 1 V / 30 V	25°C	–1	0.1	1	nA
			–40°C to +85°C	–3		3	
			–40°C to +125°C	–14		14	
$I_{S(ON)}$ $I_{D(ON)}$	Output on leakage current[1]	V_{DD} = 39.6 V, V_{SS} = 0 V Switch state is on V_S = V_D = 30 V or 1 V	25°C	–1.5	0.3	1.5	nA
			–40°C to +85°C	–5		5	
			–40°C to +125°C	–22		22	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current during overvoltage	V_S = 60 / –40 V, GND = 0 V V_{DD} = 39.6 V, V_{SS} = 0 V	–40°C to +125°C		±110		µA
$I_{S(FA)\ Grounded}$	Input leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V V_{DD} = V_{SS} = 0 V	–40°C to +125°C		±135		µA
$I_{S(FA)\ Floating}$	Input leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V V_{DD} = V_{SS} = floating	–40°C to +125°C		±135		µA
$I_{D(FA)}$	Output leakage current during overvoltage	V_S = 60 / –40 V, GND = 0V, V_{DD} = 39.6 V, V_{SS} = 0 V, 1V ≤ V_D ≤ 39.6V	25°C	–50	±10	50	nA
			–40°C to +85°C	–70		70	
			–40°C to +125°C	–90		90	
$I_{D(FA)\ Grounded}$	Output leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = 0 V	25°C	–50	±1	50	nA
			–40°C to +85°C	–100		100	
			–40°C to +125°C	–500		500	
$I_{D(FA)\ Floating}$	Output leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = floating	25°C		±3		µA
			–40°C to +85°C		±5		
			–40°C to +125°C		±8		
LOGIC INPUT/ OUTPUT							
I_{IH}	High-level input current	V_{EN} = V_{Ax} = V_{DD}	25°C	–3.2	± 0.6	3.2	µA
			–40°C to +125°C	–3.2		3.2	
I_{IL}	Low-level input current	V_{EN} = V_{Ax} = 0 V	25°C	–1.1	± 0.6	1.1	µA
			–40°C to +125°C	–1.2		1.2	

7.9 36 V Single Supply: Electrical Characteristics (continued)

V_{DD} = +36 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +36 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
$t_{ON\ (EN)}$	Enable turn-on time	V_S = 18 V, R_L = 4 kΩ, C_L= 12 pF	25°C		185	390	ns
			–40°C to +85°C			460	
			–40°C to +125°C			530	
$t_{OFF\ (EN)}$	Enable turn-off time	V_S = 18 V, R_L = 4 kΩ, C_L= 12 pF	25°C		380	450	ns
			–40°C to +85°C			450	
			–40°C to +125°C			450	
t_{TRAN}	Transition time	V_S = 18 V, R_L = 4 kΩ, C_L= 12 pF	25°C		185	230	ns
			–40°C to +85°C			245	
			–40°C to +125°C			255	
$t_{RESPONSE}$	Fault response time	R_L = 4 kΩ, C_L= 12 pF	25°C		210		ns
$t_{RECOVERY}$	Fault recovery time	R_L = 4 kΩ, C_L= 12 pF	25°C		0.63		μs
t_{BBM}	Break-before-make time delay	V_S = 18 V, R_L = 4 kΩ, C_L= 12 pF	–40°C to +125°C	50	100		ns
Q_{INJ}	Charge injection	V_S = 18 V, C_L = 1 nF	25°C		–16		pC
O_{ISO}	Off-isolation	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–78		dB
X_{TALK}	Intra-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–95		dB
	Inter-channel crosstalk (TMUX7309F)				–103		
BW	–3 dB bandwidth (TMUX7308F)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V	25°C		130		MHz
	–3 dB bandwidth (TMUX7309F WQFN Package)				255		
	–3 dB bandwidth (TMUX7309F TSSOP Package)				220		
I_{LOSS}	Insertion loss	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 6 V, f = 1 MHz	25°C		–9		dB
THD+N	Total harmonic distortion plus noise	R_S = 40 Ω, R_L = 10 kΩ, V_S = 18 V_{PP}, V_{BIAS} = 18 V, f = 20 Hz to 20 kHz	25°C		0.0015		%
$C_{S(OFF)}$	Input off-capacitance	f = 1 MHz, V_S = 18 V	25°C		4		pF
$C_{D(OFF)}$	Output off-capacitance (TMUX7308F)	f = 1 MHz, V_S = 18 V	25°C		31		pF
	Output off-capacitance (TMUX7309F)	f = 1 MHz, V_S = 18 V	25°C		16		
$C_{S(ON)}$ $C_{D(ON)}$	Input/Output on-capacitance (TMUX7308F)	f = 1 MHz, V_S = 18 V	25°C		34		pF
	Input/Output on-capacitance (TMUX7309F)	f = 1 MHz, V_S = 18 V	25°C		19		

7.9 36 V Single Supply: Electrical Characteristics (continued)

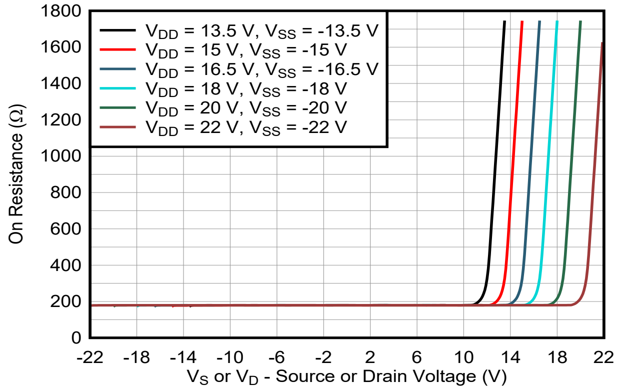
V_{DD} = +36 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +36 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 39.6 V, V_{SS} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.25	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
I_{SS}	V_{SS} supply current	V_{DD} = 39.6 V, V_{SS} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15	0.4	mA
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.4	
I_{GND}	GND current	V_{DD} = 39.6 V, V_{SS} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.075		mA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = 60 / –40 V, V_{DD} = 39.6 V, V_{SS} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.25	1	mA
			–40°C to +85°C			1	
			–40°C to +125°C			1	
$I_{SS(FA)}$	V_{SS} supply current under fault	V_S = 60 / –40 V, V_{DD} = 39.6 V, V_{SS} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
$I_{GND(FA)}$	GND current under fault	V_S = 60 / –40 V, V_{DD} = 39.6 V, V_{SS} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 5 V or V_{DD}	25°C		0.15		mA
$I_{DD(DISABLE)}$	V_{DD} supply current (disable mode)	V_{DD} = 39.6 V, V_{SS} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.15	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
$I_{SS(DISABLE)}$	V_{SS} supply current (disable mode)	V_{DD} = 39.6 V, V_{SS} = 0 V, V_{Ax} = 0 V, 5 V, or V_{DD}, V_{EN} = 0 V	25°C		0.1	0.4	mA
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.4	

(1) When V_S is 30 V, V_D is 1 V. Or when V_S is 1 V, V_D is 30 V.
(2) When V_S is at a voltage potential, V_D is floating. Or when V_D is at a voltage potential, V_S is floating.

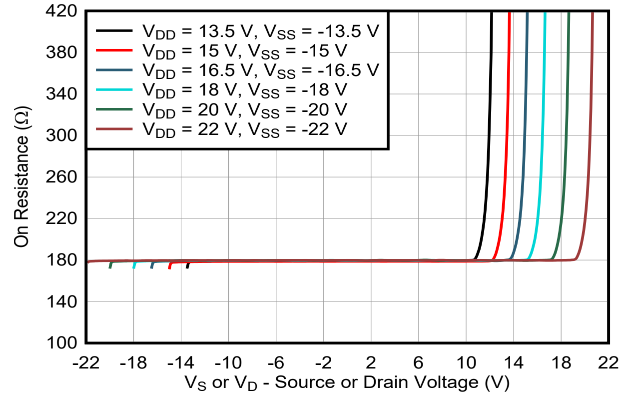
7.10 Typical Characteristics

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



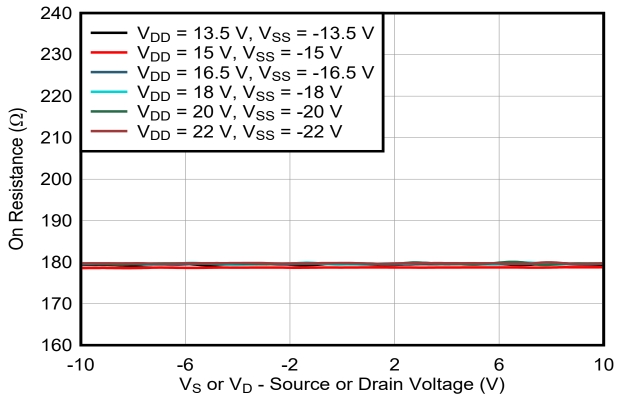
Dual Supply Voltages

Figure 7-1. On-Resistance vs Source or Drain Voltage



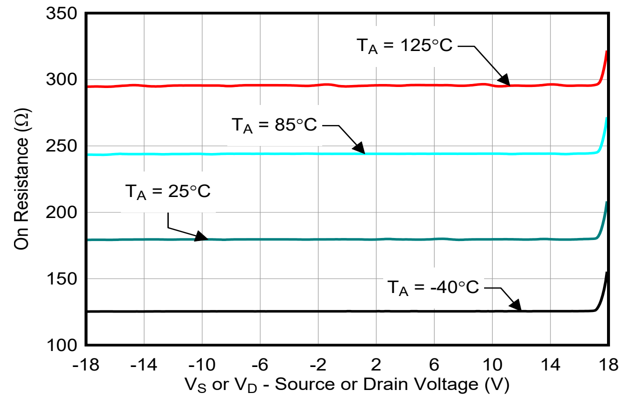
Dual Supply Flat R_{ON} Region

Figure 7-2. On-Resistance vs Source or Drain Voltage



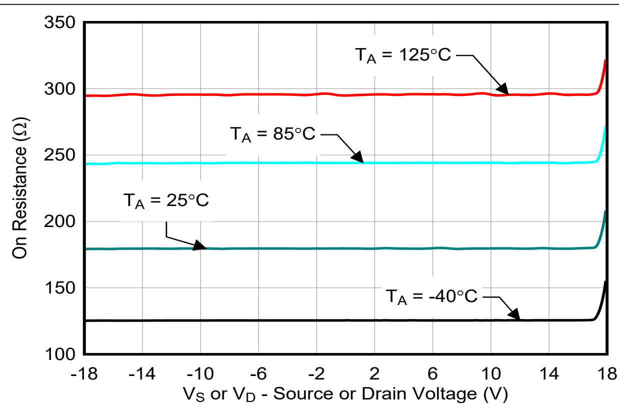
Flattest R_{ON} region for all supply voltages shown

Figure 7-3. On-Resistance vs Source or Drain Voltage



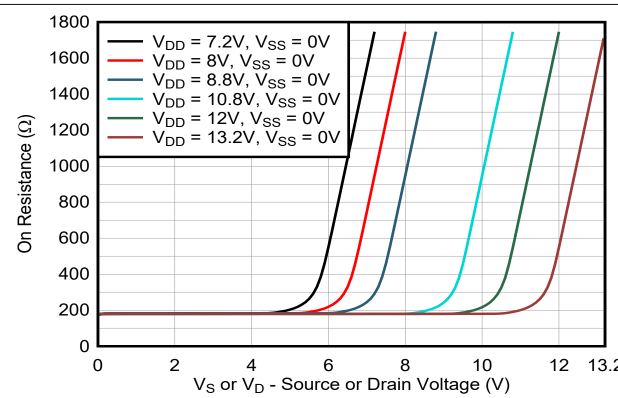
±15 V Supply Flattest R_{ON} Region

Figure 7-4. On-Resistance vs Source or Drain Voltage



±20 V Supply Flattest R_{ON} Region

Figure 7-5. On-Resistance vs Source or Drain Voltage



Single Supply Voltages

Figure 7-6. On-Resistance vs Source or Drain Voltage

7.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

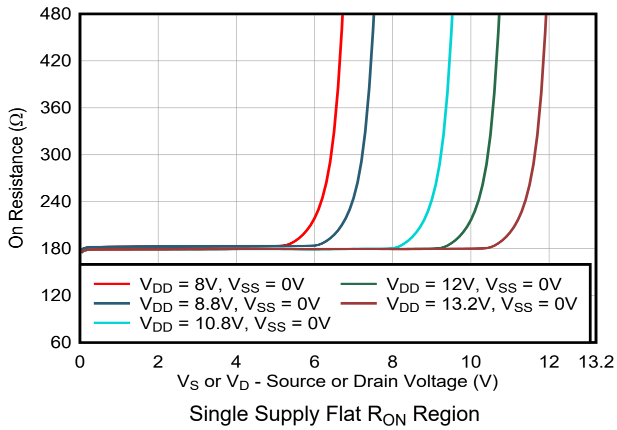


Figure 7-7. On-Resistance vs Source or Drain Voltage

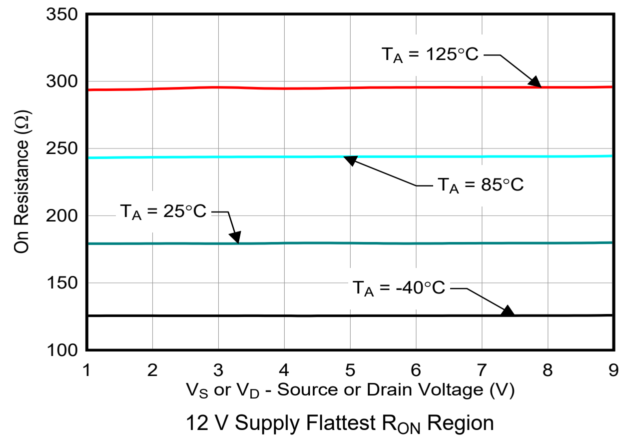


Figure 7-8. On-Resistance vs Source or Drain Voltage

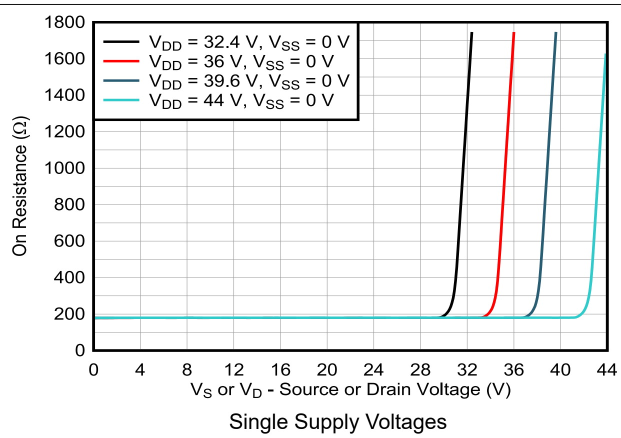


Figure 7-9. On-Resistance vs Source or Drain Voltage

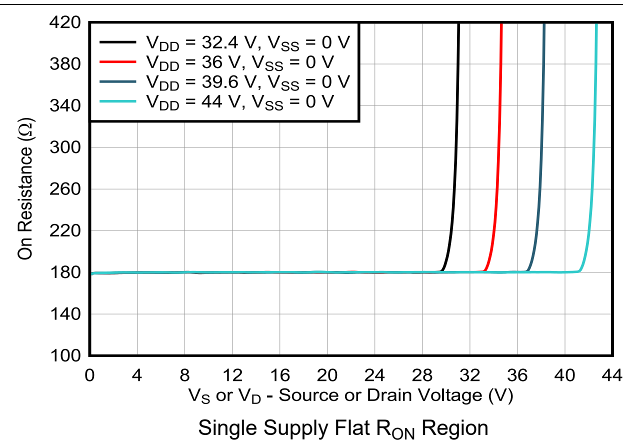


Figure 7-10. On-Resistance vs Source or Drain Voltage

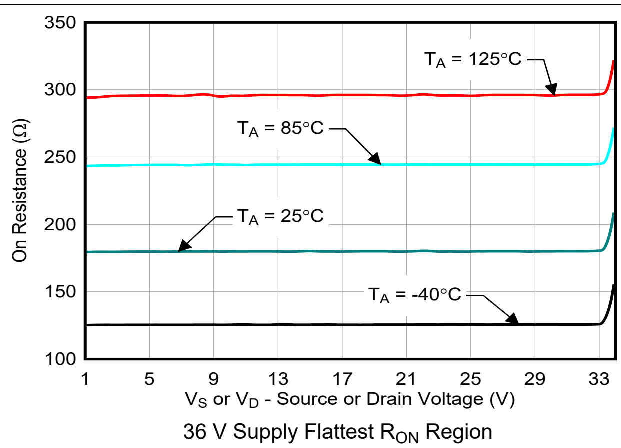


Figure 7-11. On-Resistance vs Source or Drain Voltage

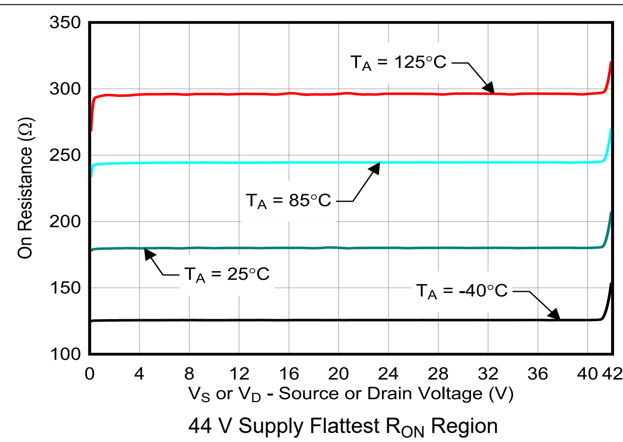
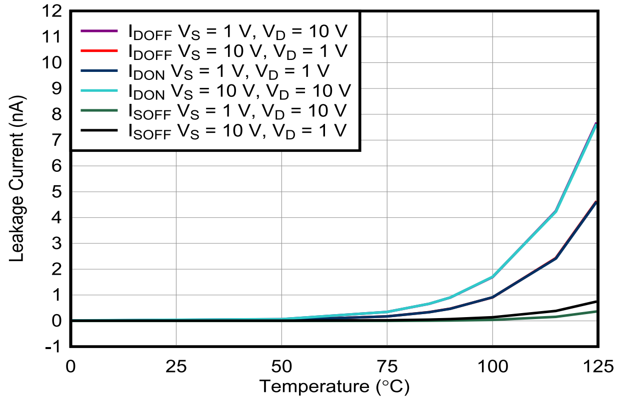


Figure 7-12. On-Resistance vs Source or Drain Voltage

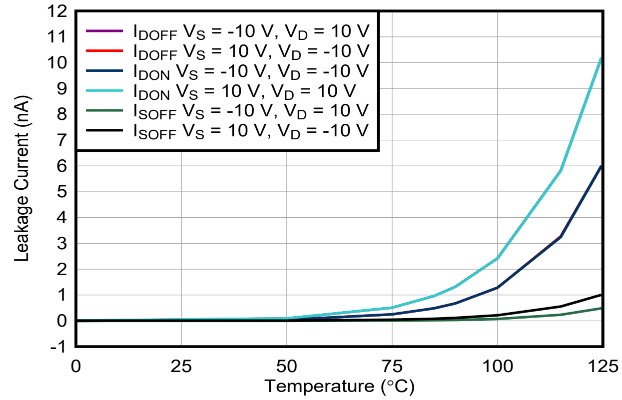
7.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



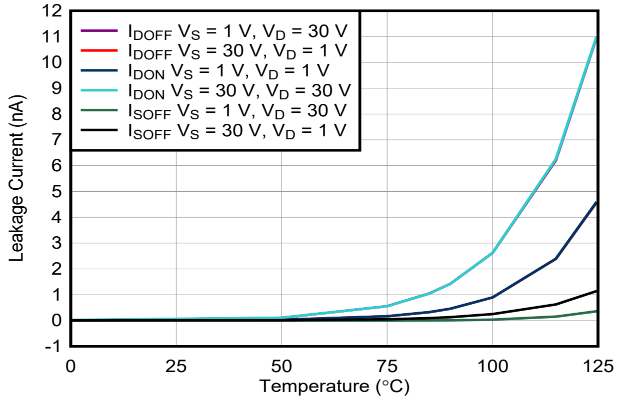
V_{DD} = 12 V, V_{SS} = 0 V

Figure 7-13. Leakage Current vs Temperature



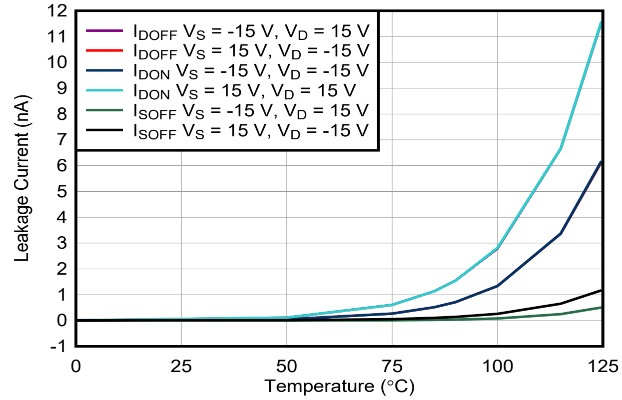
V_{DD} = 15 V, V_{SS} = -15 V

Figure 7-14. Leakage Current vs Temperature



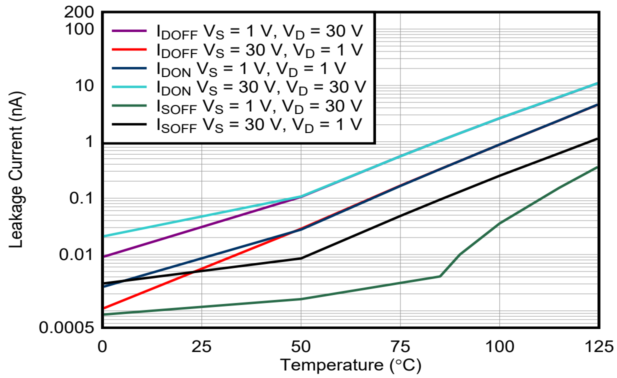
V_{DD} = 36 V, V_{SS} = 0 V

Figure 7-15. Leakage Current vs Temperature



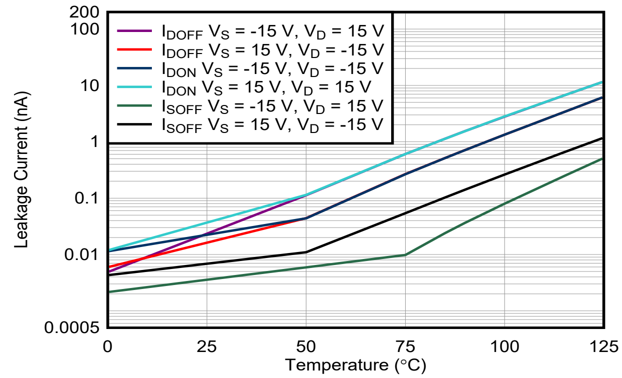
V_{DD} = 20 V, V_{SS} = -20 V

Figure 7-16. Leakage Current vs Temperature



V_{DD} = 36 V, V_{SS} = 0 V

Figure 7-17. Leakage Current vs Temperature

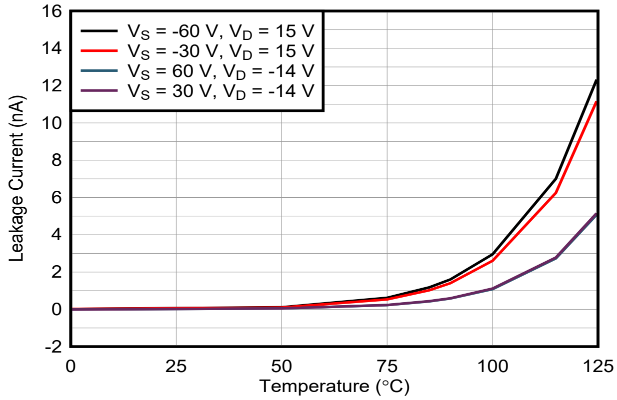


V_{DD} = 20 V, V_{SS} = -20 V

Figure 7-18. Leakage Current vs Temperature

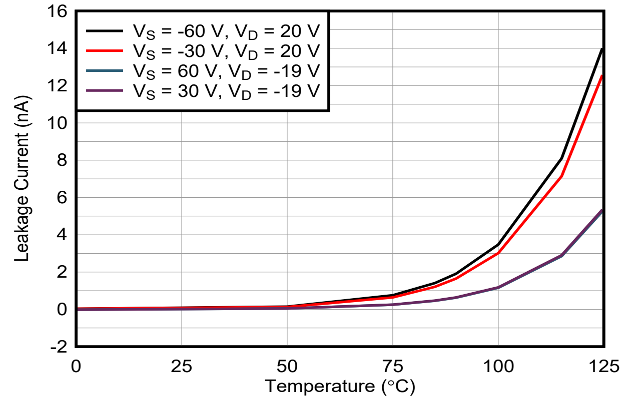
7.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



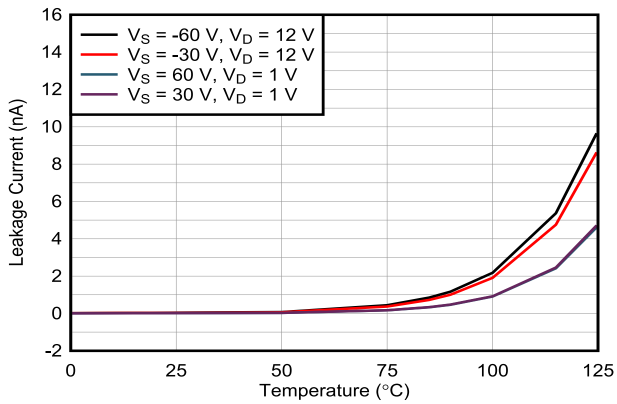
V_{DD} = 15 V, V_{SS} = -15 V

Figure 7-19. $I_{D(FA)}$ Overvoltage Leakage Current vs Temperature



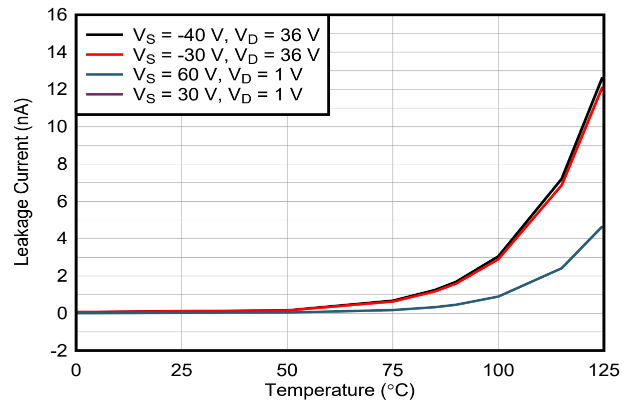
V_{DD} = 20 V, V_{SS} = -20 V

Figure 7-20. $I_{D(FA)}$ Overvoltage Leakage Current vs Temperature



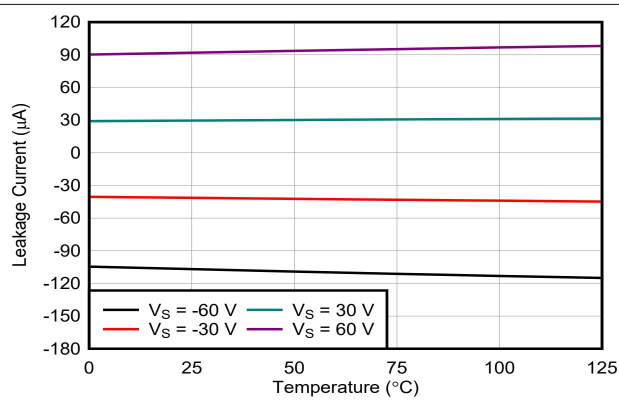
V_{DD} = 12 V, V_{SS} = 0 V

Figure 7-21. $I_{D(FA)}$ Overvoltage Leakage Current vs Temperature



V_{DD} = 36 V, V_{SS} = 0 V

Figure 7-22. $I_{D(FA)}$ Overvoltage Leakage Current vs Temperature



V_{DD} = 15 V, V_{SS} = -15 V

Figure 7-23. $I_{S(FA)}$ Overvoltage Leakage Current vs Temperature

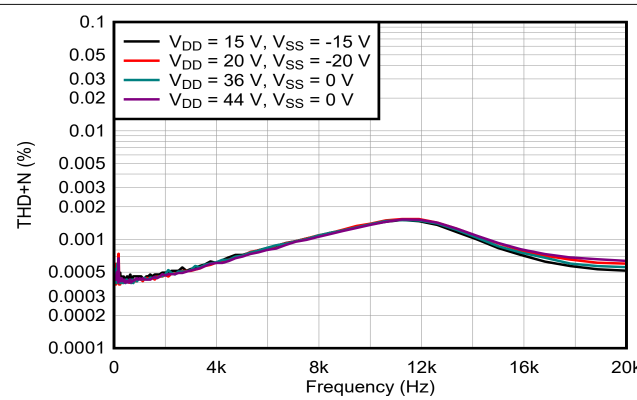


Figure 7-24. THD+N vs Frequency

7.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

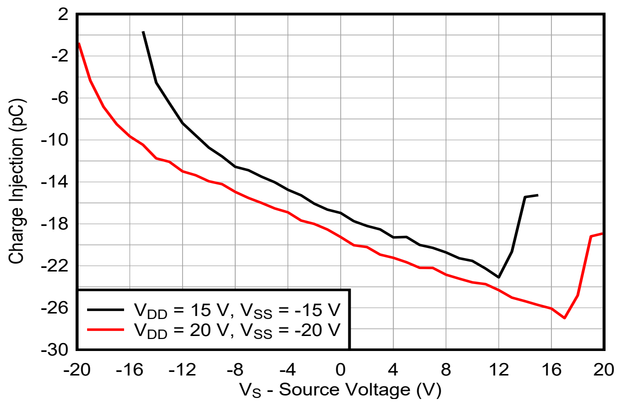


Figure 7-25. Charge Injection vs Source Voltage – Dual Supply

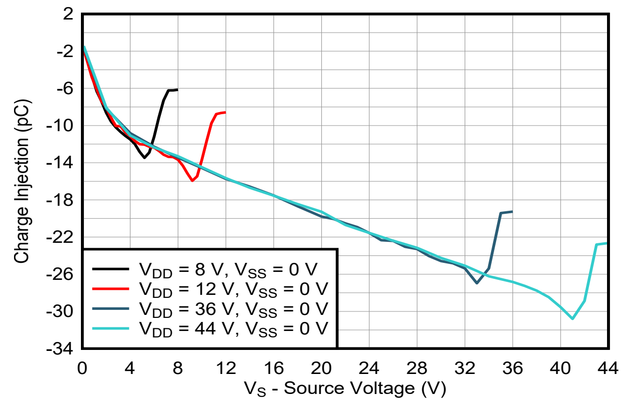


Figure 7-26. Charge Injection vs Source Voltage – Single Supply

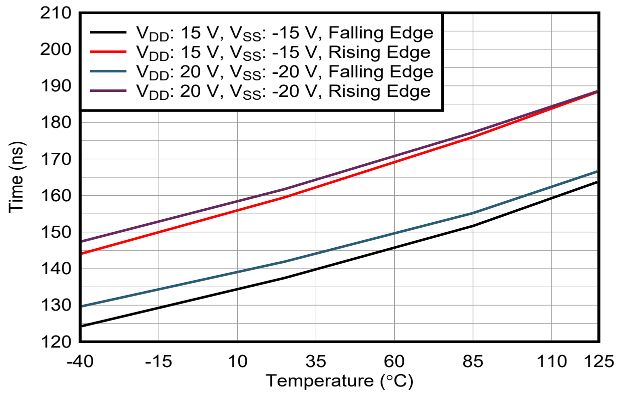


Figure 7-27. Transition Times vs Temperature

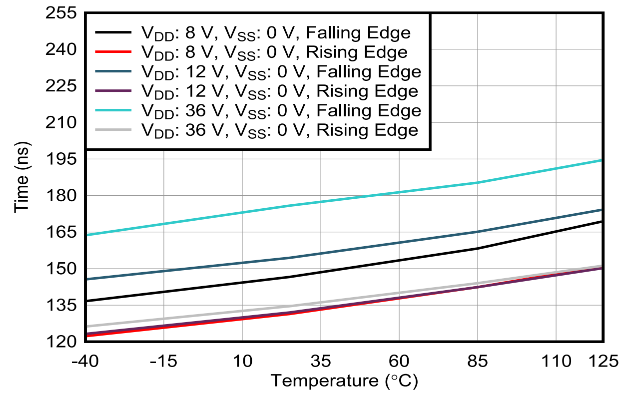


Figure 7-28. Transition Times vs Temperature

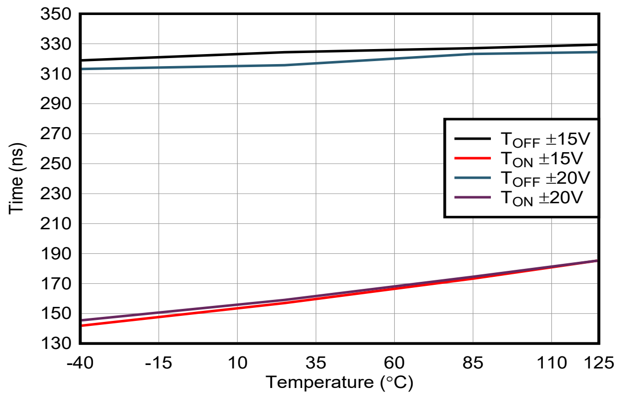


Figure 7-29. Turn-On and Turn-Off Times vs Temperature

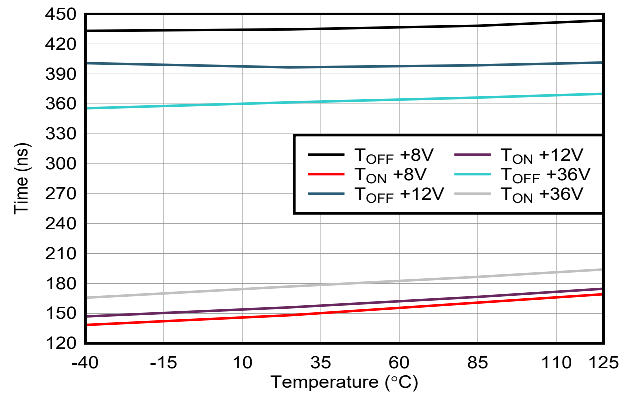


Figure 7-30. Turn-On and Turn-Off Times vs Temperature

7.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

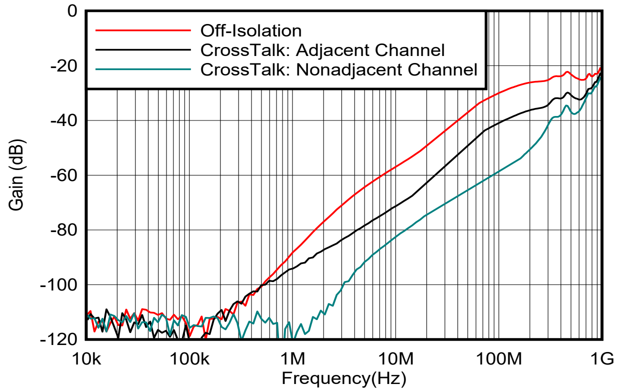


Figure 7-31. Off Isolation and Crosstalk vs Frequency

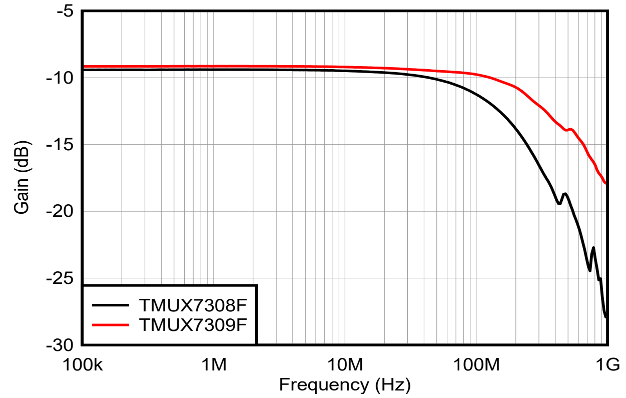
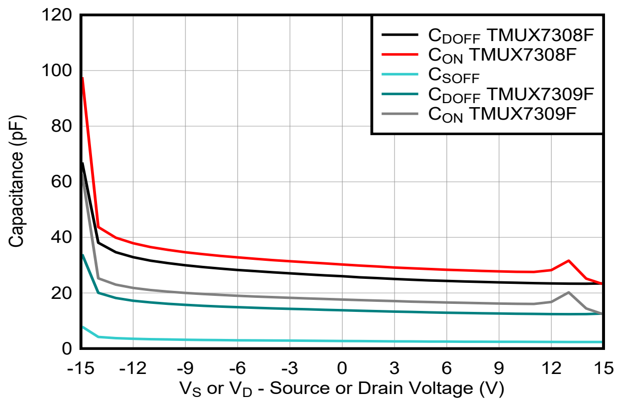
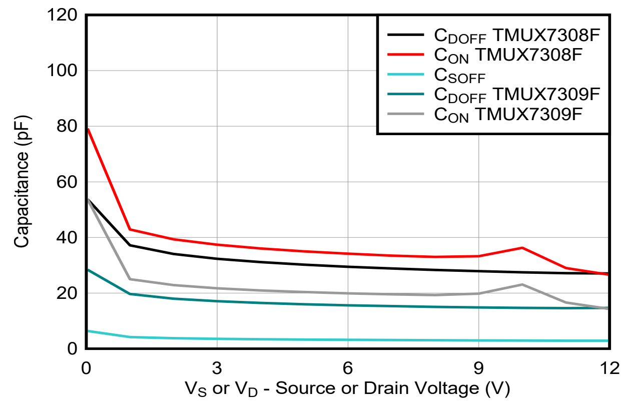


Figure 7-32. On Response vs Frequency



V_{DD} = 15 V, V_{SS} = -15 V

Figure 7-33. Capacitance vs Source or Drain Voltage



V_{DD} = 12 V, V_{SS} = 0 V

Figure 7-34. Capacitance vs Source or Drain Voltage

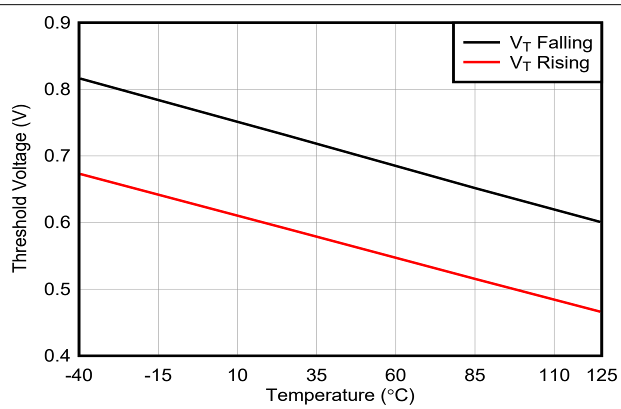


Figure 7-35. Threshold Voltage vs Temperature

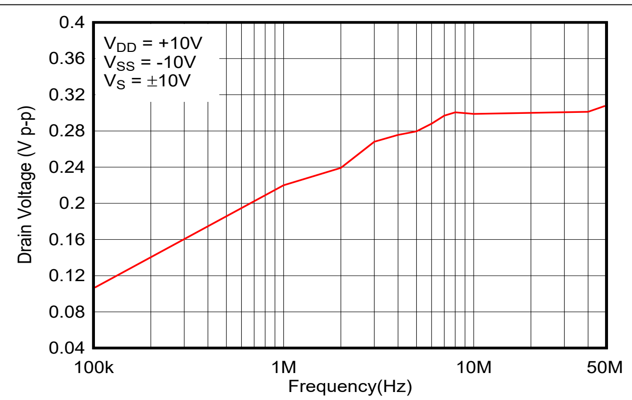


Figure 7-36. Large Signal Voltage Off Isolation vs Frequency

7.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

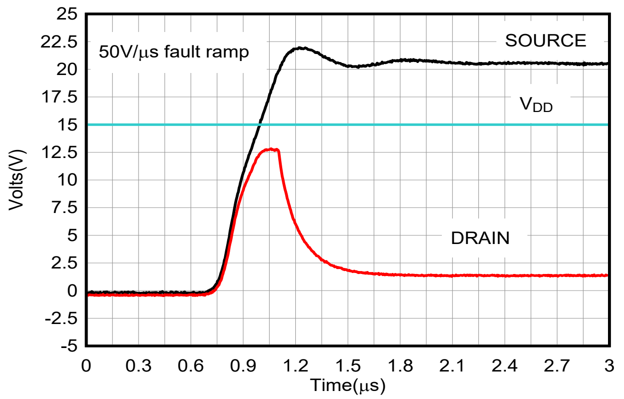


Figure 7-37. Drain Output Response – Positive Overvoltage

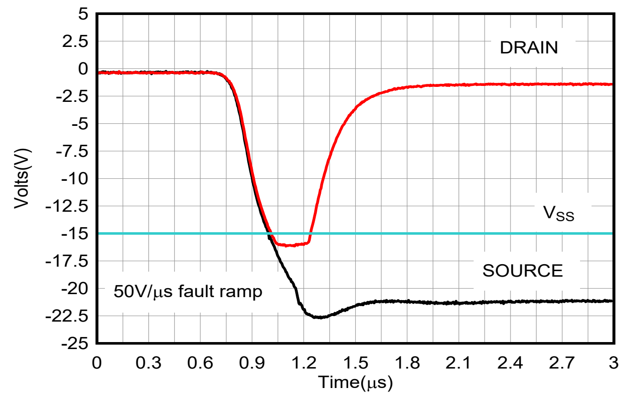


Figure 7-38. Drain Output Response – Negative Overvoltage

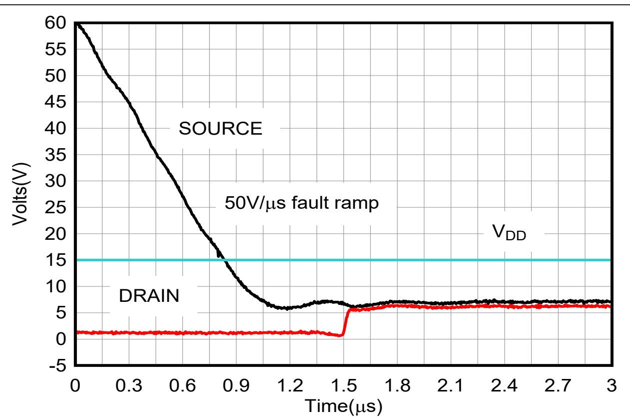


Figure 7-39. Drain Output Recovery – Positive Overvoltage

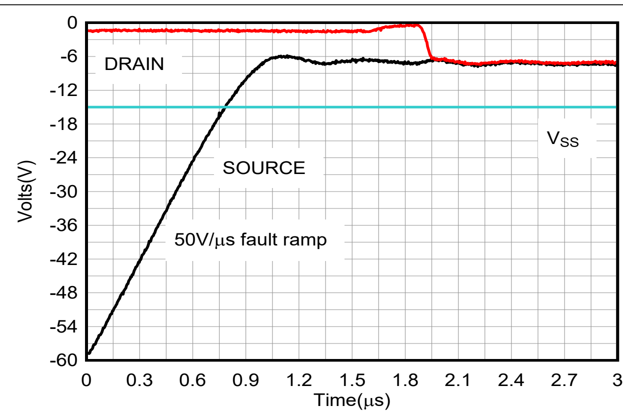


Figure 7-40. Drain Output Recovery – Negative Overvoltage

8 Parameter Measurement Information

8.1 On-Resistance

The on-resistance of the TMUX7308F and TMUX7309F is the ohmic resistance across the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. Figure 8-1 shows the measurement setup used to measure R_{ON}. ΔR_{ON} represents the difference between the R_{ON} of any two channels, while R_{ON_FLAT} denotes the flatness that is defined as the difference between the maximum and minimum value of the on-resistance measured over the specified analog signal range.

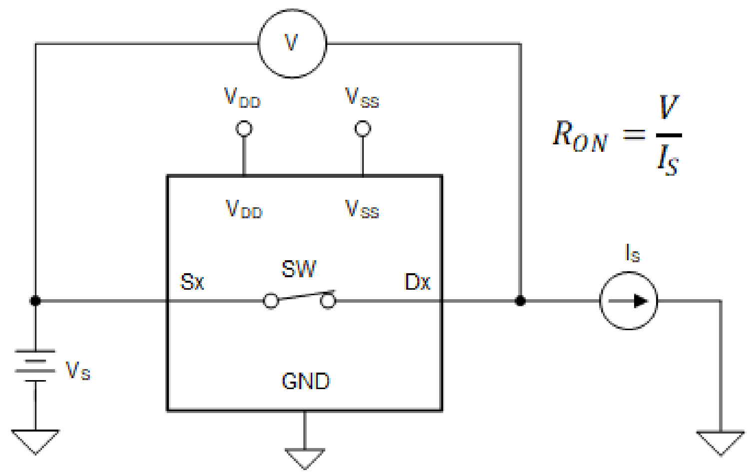


Figure 8-1. On-Resistance Measurement Setup

8.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state, which follows:

1. Source off-leakage current $I_{S(OFF)}$: the leakage current flowing into or out of the source pin when the switch is off.
2. Drain off-leakage current $I_{D(OFF)}$: the leakage current flowing into or out of the drain pin when the switch is off.

Figure 8-2 shows the setup used to measure both off-leakage currents.

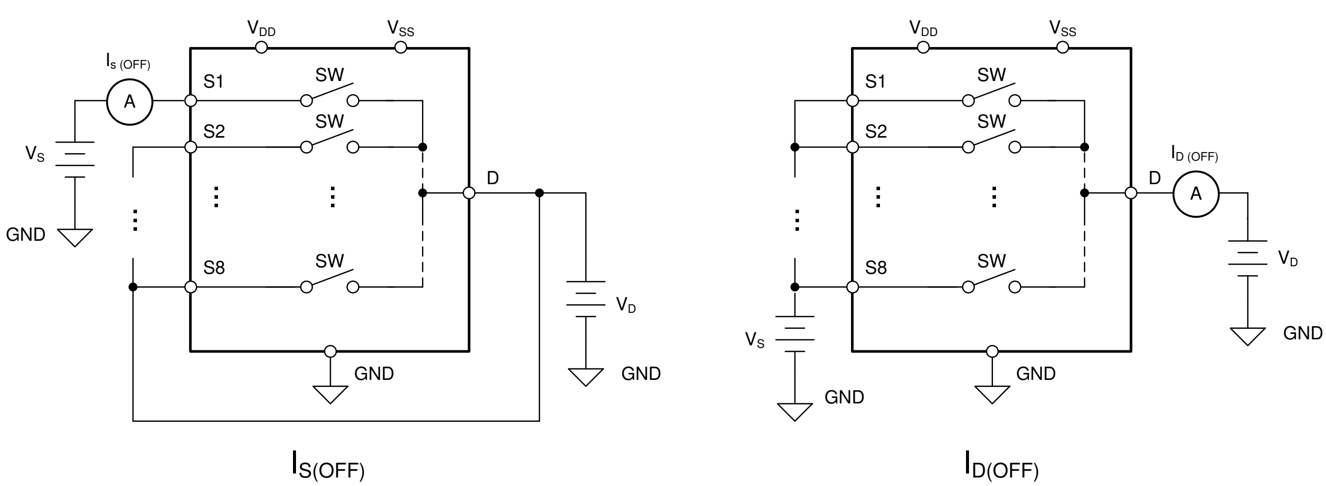


Figure 8-2. Off-Leakage Measurement Setup

8.3 On-Leakage Current

Source on-leakage current ($I_{S(ON)}$) and drain on-leakage current ($I_{D(ON)}$) denote the channel leakage currents when the switch is in the on state. $I_{S(ON)}$ is measured with the drain floating, while $I_{D(ON)}$ is measured with the source floating. Figure 8-3 shows the circuit used for measuring the on-leakage currents.

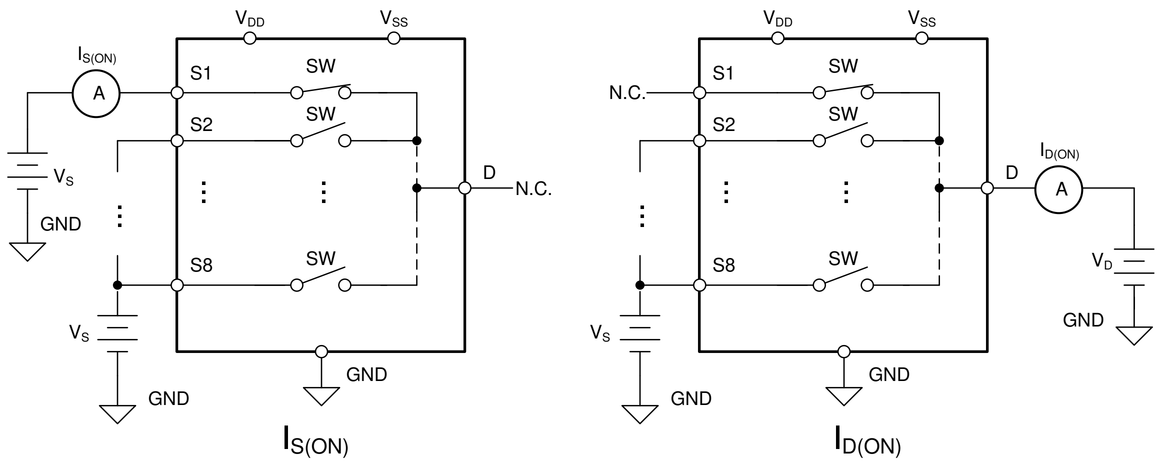


Figure 8-3. On-Leakage Measurement Setup

8.4 Input and Output Leakage Current Under Overvoltage Fault

If the voltage on any source pin goes above the supplies (V_{DD} or V_{SS}) by one threshold voltage (V_T), the overvoltage protection feature of the TMUX7308F and TMUX7309F is triggered to turn off the switch under fault, keeping the fault channel in a high-impedance state. $I_{S(FA)}$ and $I_{D(FA)}$ denotes the input and output leakage current under overvoltage fault conditions, respectively. For $I_{D(FA)}$ the device is disabled to measure leakage current on the drain pin without being impacted by the 40 kΩ impedance to the fault supply. When the overvoltage fault occurs, the supply (or supplies) can either be in normal operating condition (Figure 8-4) or abnormal operating condition (Figure 8-5). During abnormal operating condition, the supply (or supplies) can either be unpowered (V_{DD}= V_{SS} = 0 V) or floating (V_{DD}= V_{SS} = no connection), and remains within the leakage performance specifications.

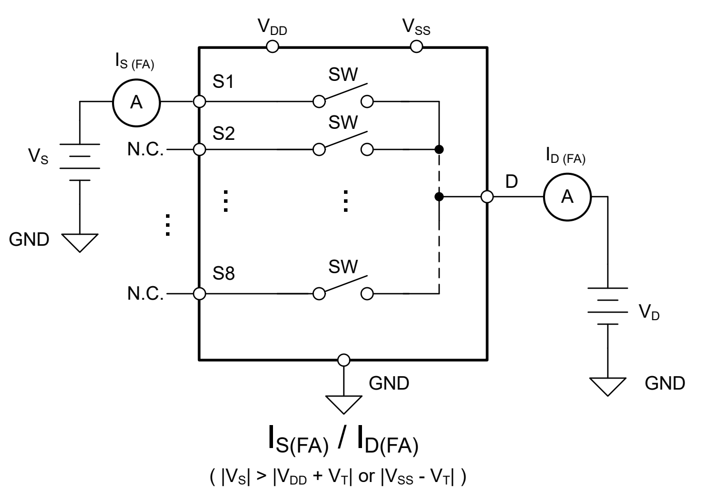


Figure 8-4. Measurement Setup for Input and Output Leakage Current under Overvoltage Fault with Normal Supplies

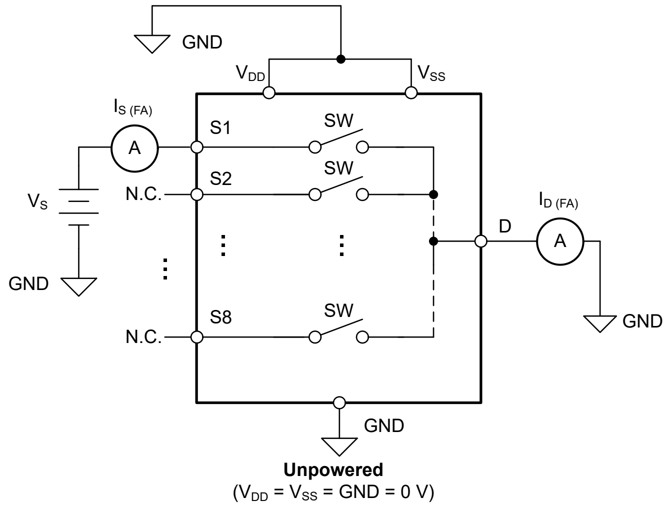


Figure 8-5. Measurement Setup for Input and Output Leakage Current under Overvoltage Fault with Unpowered or Floating Supplies

8.5 Break-Before-Make Delay

The break-before-make delay is a safety feature of the TMUX7308F and TMUX7309F. The ON switches first break the connection before the OFF switches make connection. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 8-6 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM}.

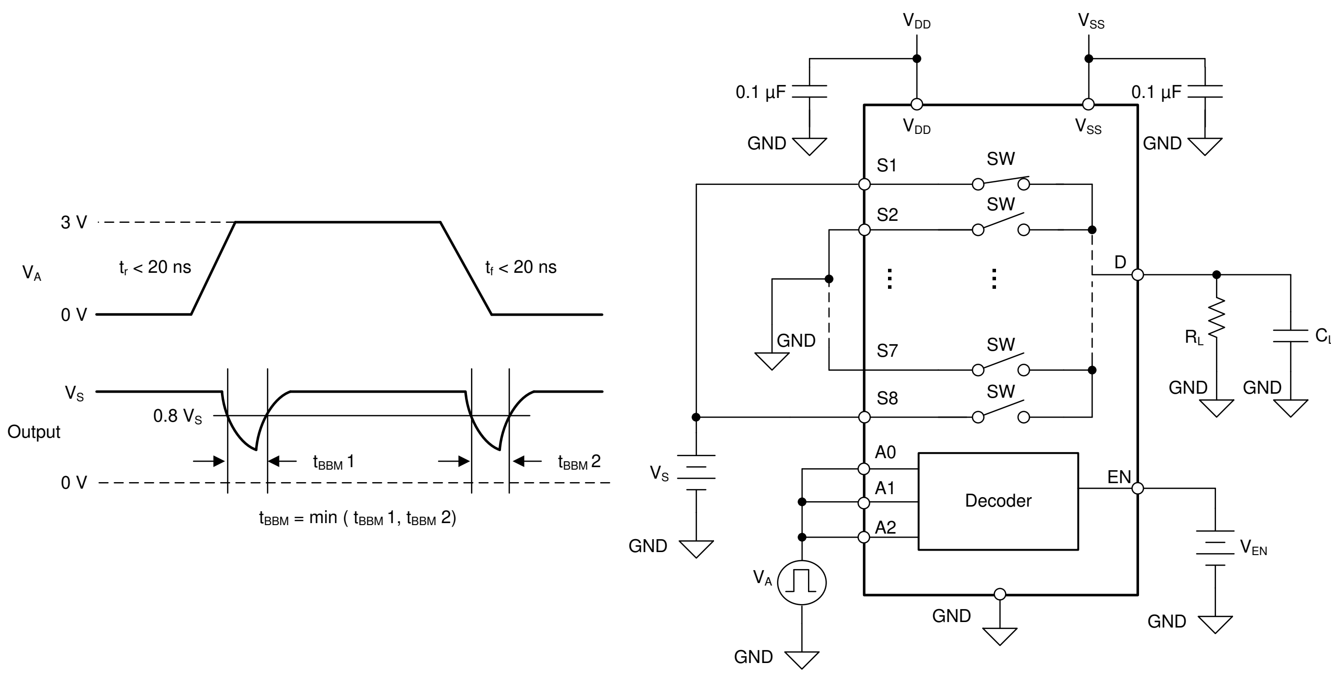


Figure 8-6. Break-Before-Make Delay Measurement Setup

8.6 Enable Delay Time

$t_{ON(EN)}$ time is defined as the time taken by the output of the TMUX7308F and TMUX7309F to rise to a 90% final value after the EN signal has risen to a 50% final value. $t_{OFF(EN)}$ is defined as the time taken by the output of the TMUX7308F and TMUX7309F to fall to a 10% initial value after the EN signal has fallen to a 50% initial value. Figure 8-7 shows the setup used to measure the enable delay time.

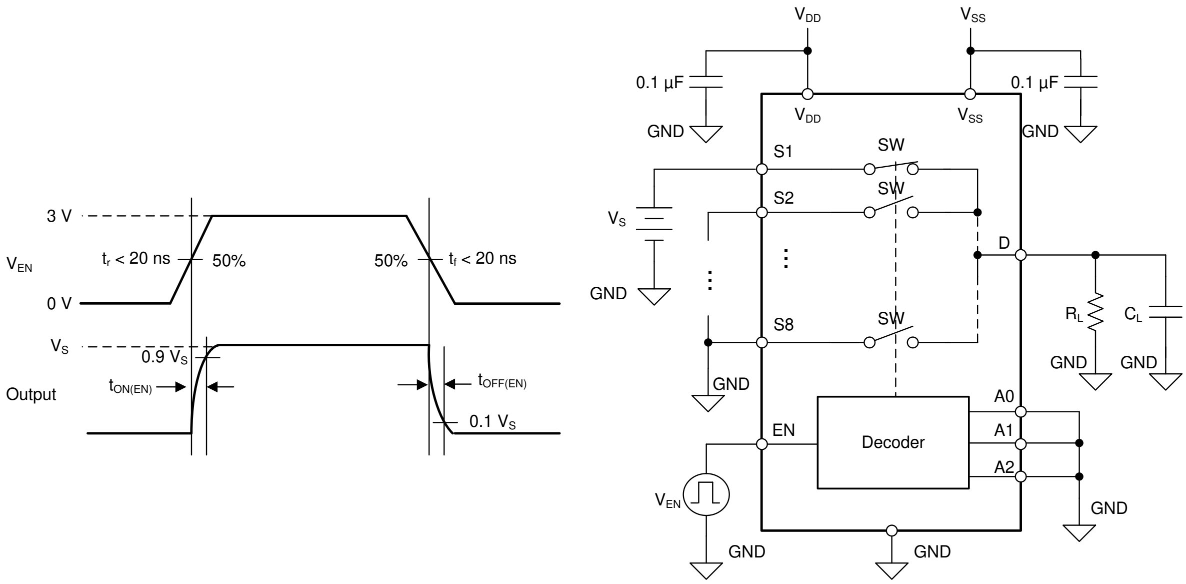


Figure 8-7. Enable Delay Measurement Setup

8.7 Transition Time

Transition time is defined as the time taken by the output of the device to rise (to 90% of the transition) or fall (to 10% of the transition) after the address signal (Ax) has fallen or risen to 50% of the transition. Figure 8-8 shows the setup used to measure transition time, denoted by the symbol t_{TRAN}.

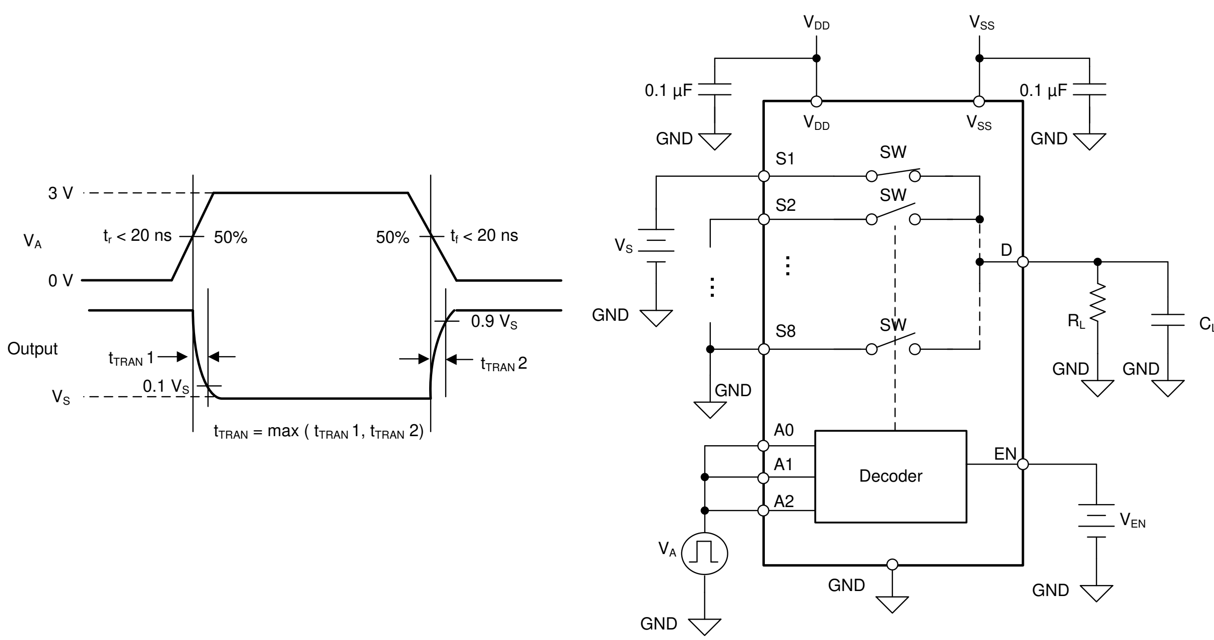


Figure 8-8. Transition Time Measurement Setup

8.8 Fault Response Time

Fault response time ($t_{REPONSE}$) measures the delay between the source voltage exceeding the supply voltage (V_{DD} or V_{SS}) by 0.5 V and the drain voltage failing to 50% of the maximum output voltage. Figure 8-9 shows the setup used to measure $t_{RESPONSE}$.

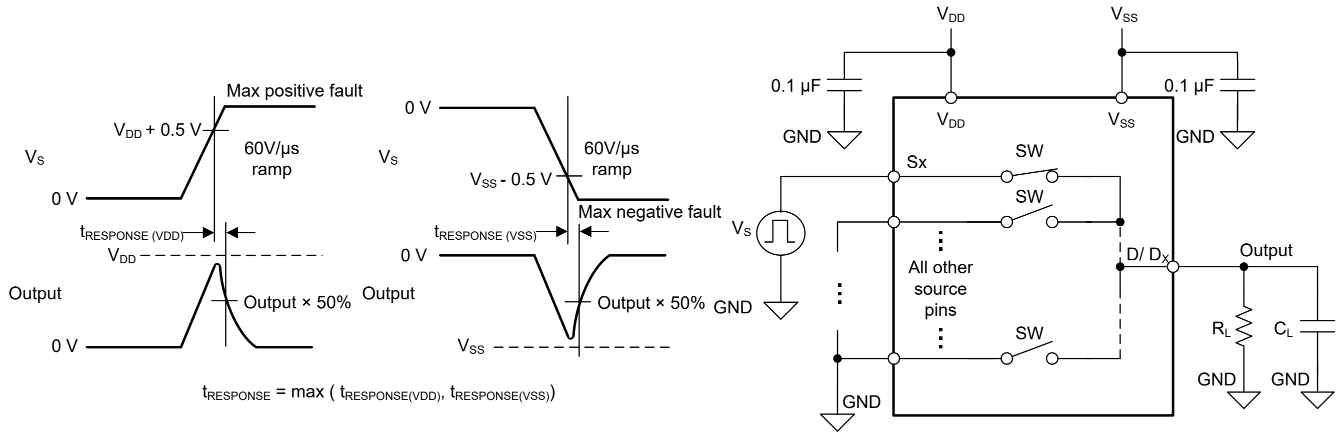


Figure 8-9. Fault Response Time Measurement Setup

8.9 Fault Recovery Time

Fault recovery time ($t_{RECOVERY}$) measures the delay between the source voltage falling from overvoltage condition to below supply voltage (V_{DD} or V_{SS}) plus 0.5 V and the drain voltage rising from 0 V to 50% of the final output voltage. Figure 8-10 shows the setup used to measure $t_{RECOVERY}$.

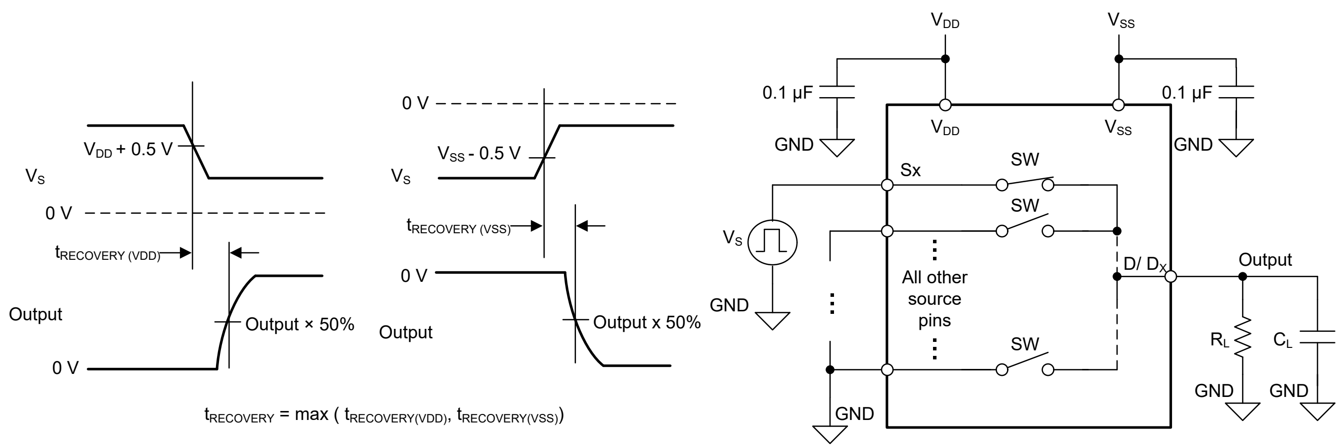


Figure 8-10. Fault Recovery Time Measurement Setup

8.10 Charge Injection

Charge injection is a measure of the glitch impulse transferred from the logic input to the signal path during logic pin switching, and is denoted by the symbol Q_{INJ}. Figure 8-11 shows the setup used to measure charge injection from the source to drain.

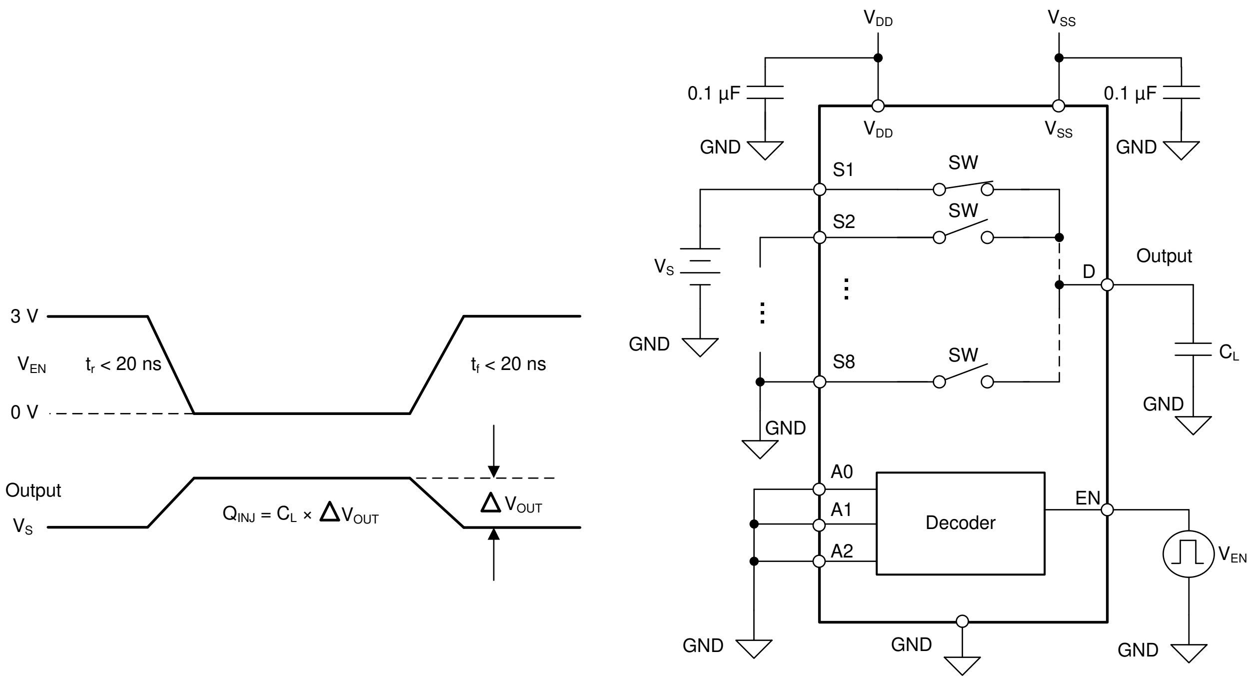
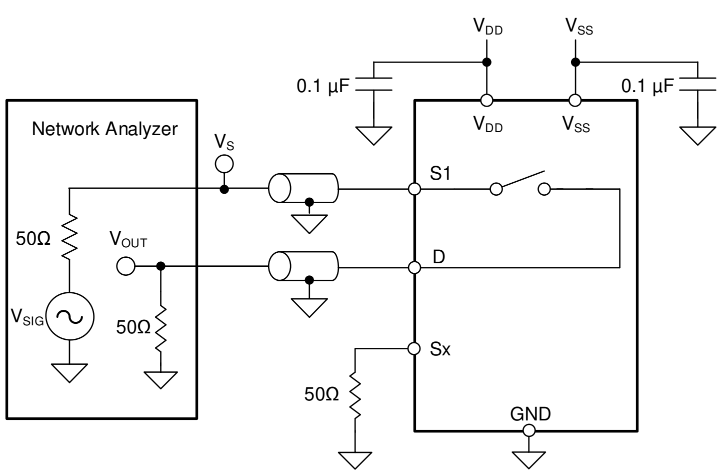


Figure 8-11. Charge-Injection Measurement Setup

8.11 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. Figure 8-12 shows the setup used to measure, and the equation used to calculate off isolation.



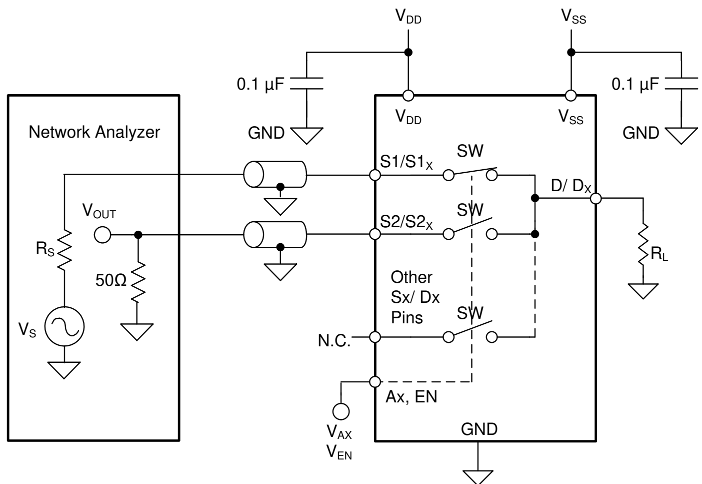
$$Off\ Isolation = 20 \times Log\frac{V_{OUT}}{V_S}$$

Figure 8-12. Off Isolation Measurement Setup

8.12 Crosstalk

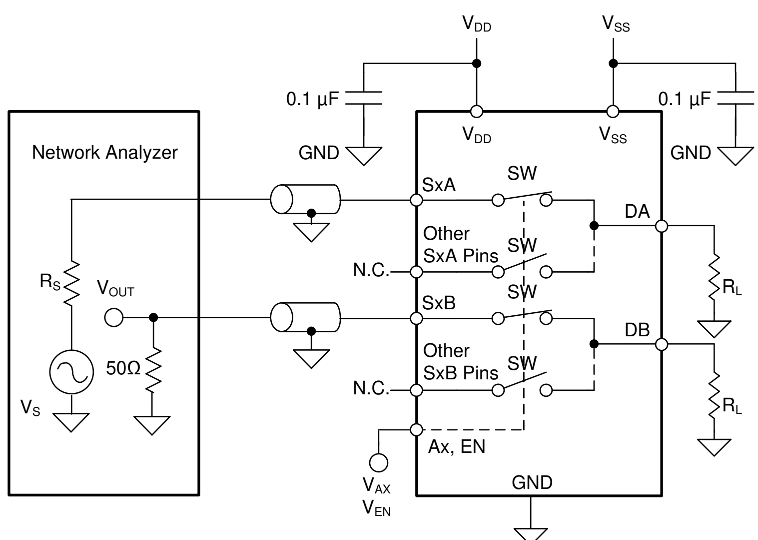
The following are two types of crosstalk that can be defined for the devices:

1. Intra-channel crosstalk ($X_{TALK(INTRA)}$): the voltage at the source pin (Sx) of an off-switch input, when a 1-V_{RMS} signal is applied at the source pin of an on-switch input in the same channel, as shown in Figure 8-13.
2. Inter-channel crosstalk ($X_{TALK(INTER)}$): the voltage at the source pin (Sx) of an on-switch input, when a 1-V_{RMS} signal is applied at the source pin of an on-switch input in a different channel, as shown in Figure 8-14. Inter-channel crosstalk applies only to the TMUX7309F device.



$$Intra - channel\ Crosstalk = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 8-13. Intra-channel Crosstalk Measurement Setup

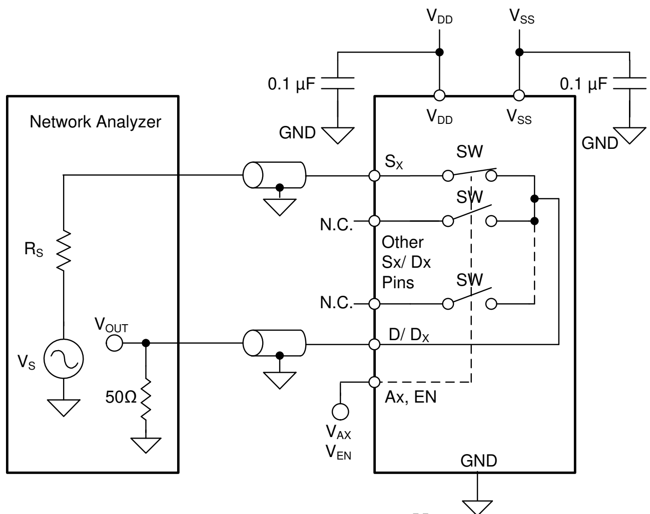


$$Inter - channel\ Crosstalk = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 8-14. Inter-channel Crosstalk Measurement Setup

8.13 Bandwidth

Bandwidth (BW) is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D or Dx) of the TMUX730xF. Figure 8-15 shows the setup used to measure bandwidth of the switch.



$$Bandwidth = 20 \times Log \frac{V_{OUT}}{V_S}$$

Figure 8-15. Bandwidth Measurement Setup

8.14 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the multiplexer output. The on-resistance of the TMUX7308F and TMUX7309F varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. Figure 8-16 shows the setup used to measure THD+N of the devices.

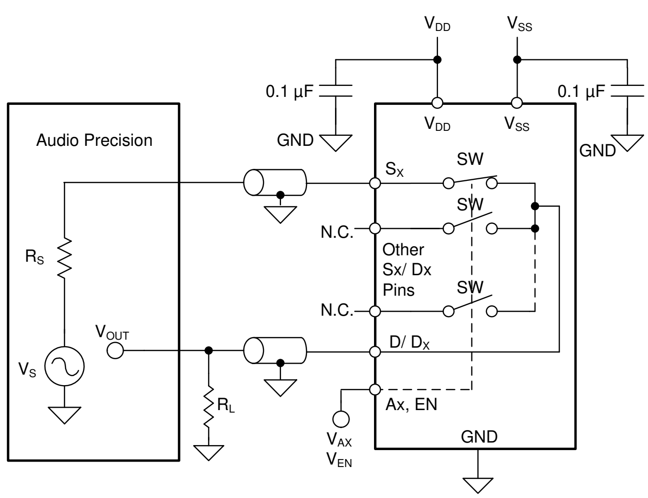


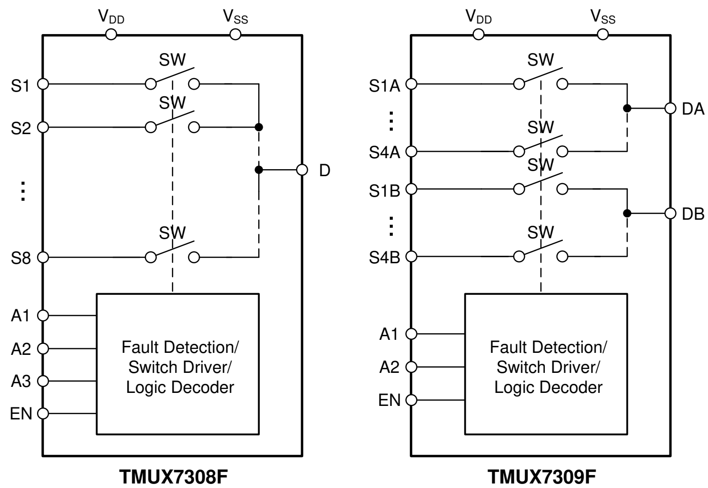
Figure 8-16. THD+N Measurement Setup

9 Detailed Description

9.1 Overview

The TMUX7308F and TMUX7309F are a modern complementary metal-oxide semiconductor (CMOS) analog multiplexers in 8:1 (single ended) and 4:1 (differential) configurations. The devices work well with dual supplies (±5 V to ±22 V), a single supply (8 V to 44 V), or asymmetric supplies (such as V_{DD} = 15 V, V_{SS} = –5 V). The devices have an overvoltage protection feature on the source pins under powered and powered-off conditions, allowing them to be used in harsh industrial environments.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Flat On – Resistance

The TMUX7308F and TMUX7309F are designed with a special switch architecture to produce ultra-flat on-resistance (R_{ON}) across most of the switch input operation region. The flat R_{ON} response allows the device to be used in precision sensor applications since the R_{ON} is controlled regardless of the signals sampled. The architecture is implemented without a charge pump so no unwanted noise is produced from the device to affect sampling accuracy.

9.3.2 Protection Features

The TMUX7308F and TMUX7309F offer a number of protection features to enable robust system implementations.

9.3.2.1 Input Voltage Tolerance

The maximum voltage that can be applied to any source input pin is +60 V or -60 V, regardless of supply voltage. This allows the device to handle typical voltage fault conditions in industrial applications. It shall be cautioned that the device is rated to handle maximum stress of 85 V across different pins, such as the following:

1. **Between the source pins and supply rails:**

   For example, if the device is powered by V_{DD} supply of 20 V, then the maximum negative signal level on any source pin is –60 V to maintain the 60 V maximum rating on any source pin. If the device is powered by V_{DD} supply of 40 V, then the maximum negative signal level on any source pin is reduced to –45 V to maintain the 85 V maximum rating across the source pin and the supply.
2. **Between the source pins and one or more drain pins:**

   For example, if channel S1(A) is ON and the voltage on S1(A) pin is 40 V. In this case, the drain voltage is also 40 V. The maximum negative voltage on any of the other source pins is –45 V to maintain the 85 V maximum rating across the source pin and the drain pin.

9.3.2.2 Powered-Off Protection

When the supplies of TMUX7308F and TMUX7309F are removed (V_{DD} / V_{SS} = 0 V or floating), the source (Sx) pins of the device remain in the high impedance (Hi-Z) state, and the source (Sx) and drain (Dx) pins of the device remain within the leakage performance mentioned in the Electrical Specifications. Powered-off protection minimizes system complexity by removing the need to control power supply sequencing of the system. The feature prevents errant voltages on the input source pins from reaching the rest of the system and maintains isolation when the system is powering up. Without powered-off protection, signal on the input source pins can back-power the supply rails through internal ESD diodes and cause potential damage to the system. For more information on powered-off protection refer to *Eliminate Power Sequencing With Powered-Off Protection Signal Switches*.

The switch remains OFF regardless of whether the V_{DD} and V_{SS} supplies are 0 V or floating. A GND reference must always be present for proper operation. Source and drain voltage levels of up to ±60 V are blocked in the powered-off condition.

9.3.2.3 Fail-Safe Logic

Fail-safe logic circuitry allows voltages on the logic control pins to be applied before the supply pins, protecting the device from potential damage. The switch is specified to be in the OFF state, regardless of the state of the logic signals. The logic inputs are protected against positive faults of up to +44 V in the powered-off condition, but do not offer protection against the negative overvoltage condition.

Fail-safe logic also allows the TMUX7308F and TMUX7309F devices to interface with a voltage greater than V_{DD} during normal operation to add maximum flexibility in system design. For example, with a V_{DD} of = 15 V, the logic control pins could be connected to +24 V for a logic high signal which allows different types of signals, such as analog feedback voltages, to be used when controlling the logic inputs. Regardless of the supply voltage, the logic inputs can be interfaced as high as 44 V.

9.3.2.4 Overvoltage Protection and Detection

The TMUX7308F and TMUX7309F detect overvoltage inputs by comparing the voltage on a source pin (Sx) with the supplies (V_{DD} and V_{SS}). A signal is considered overvoltage if it exceeds the supply voltages by the threshold voltage (V_T).

When an overvoltage is detected, the switch with the overvoltage automatically turns OFF, and stays OFF regardless of the logic controls. The source pin becomes high impedance and allows only a small leakage current to flow through the switch and the overvoltage does not appear on the drain. When the overvoltage channel is selected by the logic control, the drain pin (D or Dx) is pulled to the supply that was exceeded. For example, if the source voltage exceeds V_{DD}, the drain output is pulled to V_{DD}. If the source voltage exceeds V_{SS}, the drain output is pulled to V_{SS}. The pull-up impedance is approximately 40 kΩ, and as a result, the drain current is limited to roughly 1 mA during a shorted load (to GND) condition.

Figure 9-1 shows a detailed view of the how the pullup/down controls the output state of the drain pin under a fault scenario.

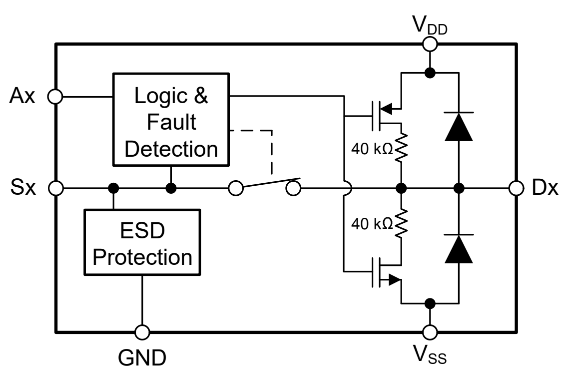


Figure 9-1. Detailed Functional Diagram

9.3.2.5 Adjacent Channel Operation During Fault

When the logic pins are set to a channel under a fault, the overvoltage detection will trigger, the switch will open, and the drain pin will be pulled up/down as described in Section 9.3.2.4. During such an event, all other channels not under a fault can continue to operate as normal. For example, if S1 voltage exceeds V_{DD}, and the logic pins are set to S1, the drain output is pulled to V_{DD}. If then the logic pins are changed to set S4, which is not in overvoltage or undervoltage, the drain will disconnect from the pullup to V_{DD} and the S4 switch will be enabled and connected to the drain, operating as normal. If the logic pins are switched back to S1, the S4 switch will be disabled, the drain pin will be pulled up to V_{DD} again, and the switch from S1 to drain will not be enabled until the overvoltage fault is removed.

9.3.2.6 ESD Protection

All pins on the TMUX7308F and TMUX7309F support HBM ESD protection level up to ±3.5 kV, which helps the device from getting ESD damages during manufacturing process.

The drain pins (D or Dx) have internal ESD protection diodes to the supplies V_{DD} and V_{SS}, therefore the voltage at the drain pins must not exceed the supply voltages to prevent excessive diode current. The source pins have specialized ESD protection that allows the signal voltage to reach ±60 V regardless of supply voltage level. Exceeding ±60 V on any source input may damage the ESD protection circuitry on the device and cause the device to malfunction if the damage is excessive.

9.3.2.7 Latch-Up Immunity

Latch-up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The latch-up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX7308F and TMUX7309F devices are constructed on silicon on insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX7308F and TMUX7309F to be used in harsh environments. For more information on latch-up immunity refer to *Using Latch Up Immune Multiplexers to Help Improve System Reliability*.

9.3.2.8 EMC Protection

The TMUX7308F and TMUX7309F are not intended for standalone electromagnetic compatibility (EMC) protection in industrial applications. There are three common high voltage transient specifications that govern industrial high voltage transient specification: IEC61000-4-2 (ESD), IEC61000-4-4 (EFT), and IEC61000-4-5 (surge immunity). A transient voltage suppressor (TVS), along with some low-value series current limiting resistor, are required to prevent source input voltages from going above the rated ±60 V limits.

When selecting a TVS protection device, it is critical to ensure that the maximum working voltage is greater than both the normal operating range of the input source pins to be protected and any known system common-mode overvoltage that may be present due to incorrect wiring, loss of power, or short circuit. Figure 9-2 shows one example of the proper design window when selecting a TVS device.

Region 1 denotes the normal operation region of TMUX7308F and TMUX7309F where the input source voltages stay below the fault supplies V_{DD} and V_{SS}. Region 2 represents the range of possible persistent DC (or long duration AC overvoltage fault) presented on the source input pins. Region 3 represents the margin between any known DC overvoltage level and the absolute maximum rating of the TMUX7308F and TMUX7309F. The selected TVS breakdown voltage must be less than the absolute maximum rating of the TMUX730xF but greater than any known possible persistent DC or long duration AC overvoltage fault to avoid triggering the TVS inadvertently. Region 4 represents the margin that system designers must impose when selecting the TVS protection device to prevent accidental triggering of the ESD cells of the TMUX7308F and TMUX7309F devices.

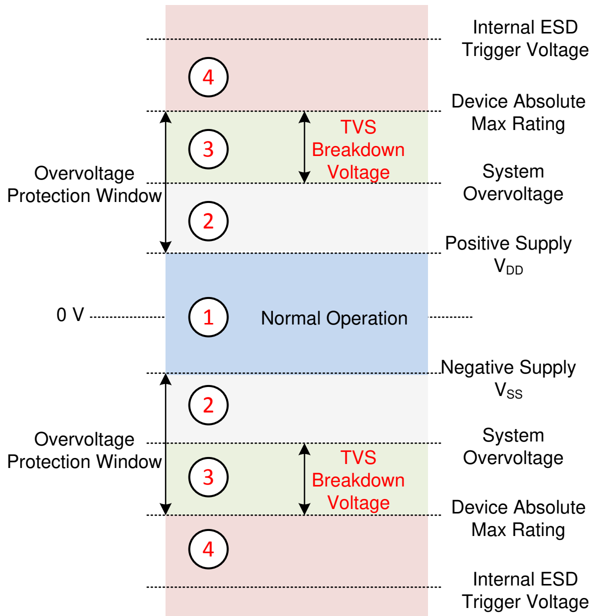


Figure 9-2. System Operation Regions and Proper Region of Selecting a TVS Protection Device

9.3.3 Bidirectional Operation

The TMUX7308F and TMUX7309F conducts equally well from source (Sx) to drain (D or Dx) or from drain (D or Dx) to source (Sx). Each signal path has very similar characteristics in both directions. However, take note that the overvoltage protection is implemented only on the source (Sx) side. The voltage on the drain is only allowed to swing between V_{DD} and V_{SS} and no overvoltage protection is available on the drain side.

The flattest on-resistance region extends from V_{SS} to roughly 3 V below V_{DD}. Once the signal is within 3 V of V_{DD} the on-resistance will exponentially increase and may impact desired signal transmission.

9.3.4 1.8 V Logic Compatible Inputs

The TMUX7308F and TMUX7309F devices have 1.8 V logic compatible control for all logic control inputs. 1.8 V logic level inputs allows the TMUX7308F and TMUX7309F to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

9.3.5 Integrated Pull-Down Resistor on Logic Pins

The TMUX7308F and TMUX7309F have internal weak pull-down resistors to GND so that the logic pins are not left floating. The value of this pull-down resistor is approximately 4 MΩ, but is clamped to about 1 µA at higher voltages. This feature integrates up to four external components and reduces system size and cost.

9.4 Device Functional Modes

The TMUX7308F and TMUX7309F offers two modes of operation (Normal mode and Fault mode) depending on whether any of the input pins experience an overvoltage condition.

9.4.1 Normal Mode

In Normal mode operation, signals of up to V_{DD} and V_{SS} can be passed through the switch from source (Sx) to drain (D or Dx) or from drain (D or Dx) to source (Sx). The address (Ax) pins and the enable (EN) pin determines which switch path to turn on, according to Table 9-1 and Table 9-2. The following conditions must be satisfied for the switch to stay in the ON condition:

- The difference between the primary supplies (V_{DD} – V_{SS}) must be greater than or equal to 8 V. With a minimum V_{DD} of 5 V.
- The input signals on the source (Sx) or the drain (D or Dx) must be between V_{DD}+ V_T and V_{SS} – V_T.
- The logic control (Ax and EN) must have selected the switch.

9.4.2 Fault Mode

The TMUX7308F and TMUX7309F enter into the Fault mode when any of the input signals on the source (Sx) pins exceed V_{DD} or V_{SS} by a threshold voltage V_T. Under the overvoltage condition, the switch input experiencing the fault automatically turns OFF regardless of the logic status, and the source pin becomes high impedance with a negligible amount of leakage current flowing through the switch. When the fault channel is selected by the logic control, the drain pin (D or Dx) is pulled to the supply that was exceeded through a 40 kΩ internal resistor.

The overvoltage protection is provided only for the source (Sx) input pins. The drain (D or Dx) pin, if used as a signal input, must stay in between V_{DD} and V_{SS} at all times since no overvoltage protection is implemented on the drain pin.

9.4.3 Truth Tables

Table 9-1 shows the truth tables for the TMUX7308F.

Table 9-1. TMUX7308F Truth Table

EN	A2	A1	A0	Selected Source Connected to Drain Pin (D)
0	X(1)	X(1)	X(1)	All sources are off (HI-Z)
1	0	0	0	S1
1	0	0	1	S2
1	0	1	0	S3
1	0	1	1	S4
1	1	0	0	S5
1	1	0	1	S6
1	1	1	0	S7
1	1	1	1	S8

(1) "X" means "do not care."

Table 9-2 shows the truth tables for the TMUX7309F.

Table 9-2. TMUX7309F Truth Table

EN	A1	A0	Selected Source Connected to Drain Pins (DA, DB)
0	X(1)	X(1)	All sources are off (HI-Z)
1	0	0	S1A and S1B
1	0	1	S2A and S2B
1	1	0	S3A and S3B
1	1	1	S4A and S4B

(1) "X" means "do not care."

If unused, Ax pins must be tied to GND so that the device does not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (Sx or Dx) should be connected to GND.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The TMUX7308F and TMUX7309F are part of the fault protected switches and multiplexers family of devices. The ability to protect downstream components from overvoltage events up to ±60 V makes these switches and multiplexers suitable for harsh environments.

10.2 Typical Application

In analog input programmable logic controllers (PLC) a multiplexer is often used to switch multiple sensors to a single ADC. By using a multiplexer, the number of components in the system can be reduced to save system cost and size. In a PLC module a ±10 V input signal range is common for interfacing with external field transmitters and sensors; however, there are a number of fault cases that may occur that can be damaging to many of the integrated circuits. Such fault conditions may include, but are not limited to, human error from wiring connections incorrectly, component failure or wire shorts, electromagnetic interference (EMI) or transient disturbances, and so forth.

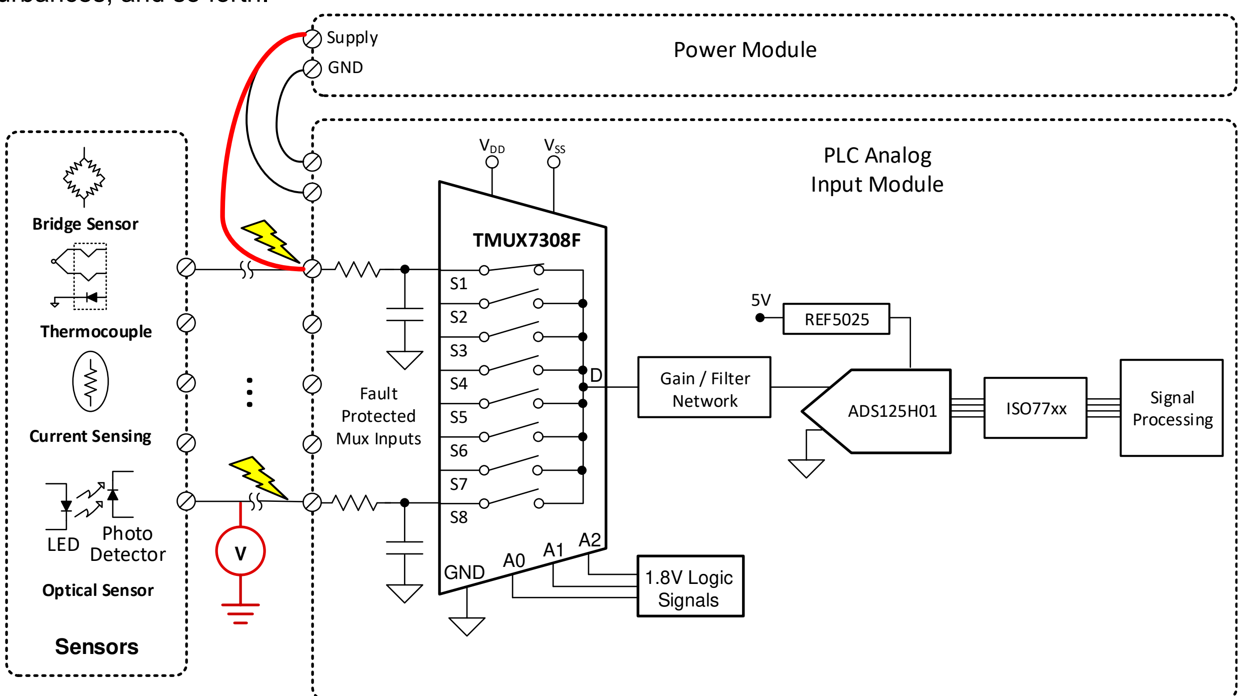


Figure 10-1. Typical Application

10.2.1 Design Requirements

Table 10-1. Design Parameters

PARAMETER	VALUE
Positive supply (V_{DD}) mux and ADC	+15 V
Negative supply (V_{SS}) mux and ADC	-15 V
Power board supply voltage	24 V
Input / output signal range non-faulted	-15 V to 15 V
Overvoltage protection levels	-60 V to 60 V
Control logic thresholds	1.8 V compatible, up to 44 V
Temperature range	-40°C to +125°C

10.2.2 Detailed Design Procedure

The image shows the case where an incorrect wiring condition occurred and one of the input connectors has been shorted to the power board supply voltage. If the board supply voltage is higher than the power supply of the multiplexer, then the TMUX7308F or TMUX7309F will disconnect the source input from passing the signal to protect the downstream ADC. The drain pin of the mux will be pulled up to the supply voltage VDD through a 40 kΩ resistor to allow the ADC to determine a fault condition has occurred.

10.2.3 Application Curves

The example application utilizes the fault protection of the TMUX7308F or TMUX7309F to protect downstream components from potential miswiring conditions from the Power Module board. Figure 10-2 shows an example of positive overvoltage fault response with a fast fault ramp rate of 50 V/µs. Figure 10-3 shows the extremely flat on-resistance across source voltage while operating within a common signal range of ±10 V. These features make the TMUX7308F or TMUX7309F an ideal solution for factory automation applications that may face various fault conditions but also require excellent linearity and low distortion.

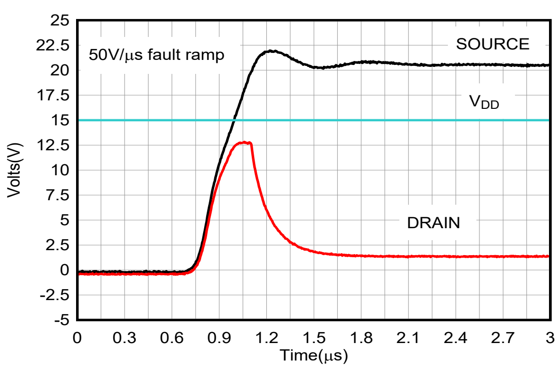


Figure 10-2. Positive Overvoltage Response

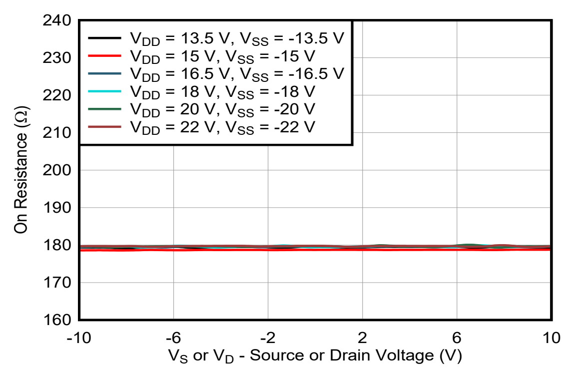


Figure 10-3. R_{ON} Flatness in Non-Fault Region

10.3 Power Supply Recommendations

The TMUX7308F and TMUX7309F operate across a wide supply range of ±5 V to ±22 V (8 V to 44 V in single-supply mode). They also perform well with asymmetrical supplies such as V_{DD} = 15 V and V_{SS}= –5 V. For improved supply noise immunity, use a supply decoupling capacitor ranging from 1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground. Always ensure the ground (GND) connection is established before supplies are ramped.

10.4 Layout

10.4.1 Layout Guidelines

The image below illustrates an example of a PCB layout with the TMUX7308F and TMUX7309F. Some key considerations are:

- For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and V_{SS} to GND. We recommend a 0.1 µF and 1 µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

10.4.2 Layout Example

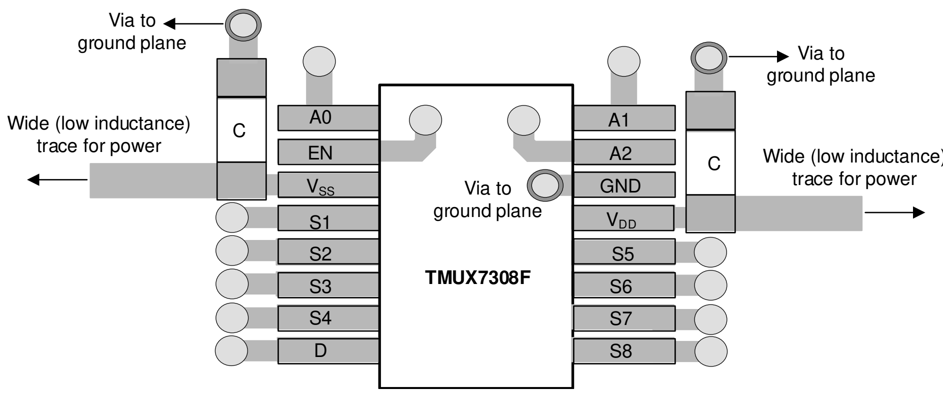


Figure 10-4. TMUX7308FPW Layout Example

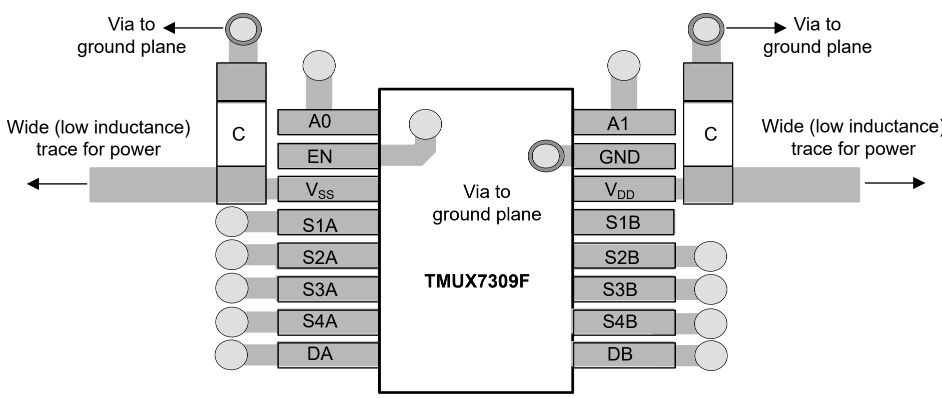


Figure 10-5. TMUX7309FPW Layout Example

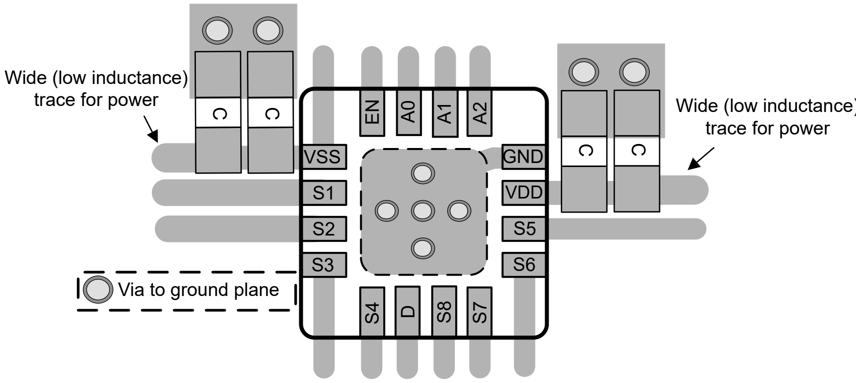


Figure 10-6. TMUX7308FQFN Layout Example

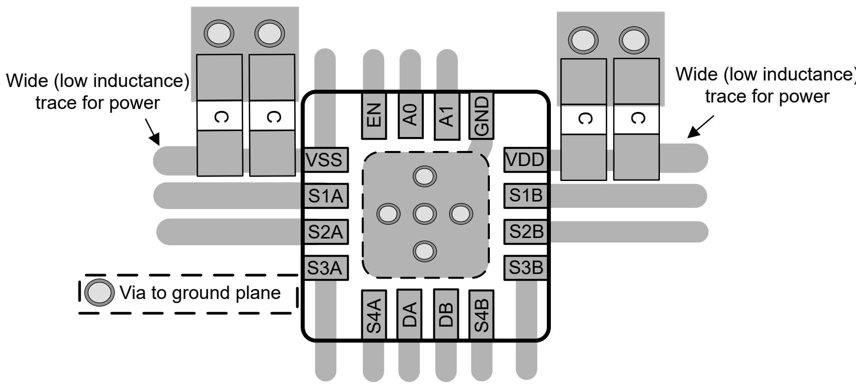


Figure 10-7. TMUX7309FQFN Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note
- Texas Instruments, *Improving Analog Input Modules Reliability Using Fault Protected Multiplexers* application report
- Texas Instruments, *Multiplexers and Signal Switches Glossary* application report
- Texas Instruments, *Protection Against Overvoltage Events, Miswiring, and Common Mode Voltages* application report
- Texas Instruments, *Using Latch-Up Immune Multiplexers to Help Improve System Reliability* application report

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX7308FPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM7308F
TMUX7308FPWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM7308F
TMUX7308FPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM7308F
TMUX7308FPWRG4.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM7308F
TMUX7308FRRPR	Active	Production	WQFN (RRP) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX 7308F
TMUX7308FRRPR.B	Active	Production	WQFN (RRP) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX 7308F
TMUX7308FRRPRG4	Active	Production	WQFN (RRP) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX 7308F
TMUX7308FRRPRG4.B	Active	Production	WQFN (RRP) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX 7308F
TMUX7309FPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM7309F
TMUX7309FPWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM7309F
TMUX7309FRRPR	Active	Production	WQFN (RRP) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX 7309F
TMUX7309FRRPR.B	Active	Production	WQFN (RRP) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX 7309F

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

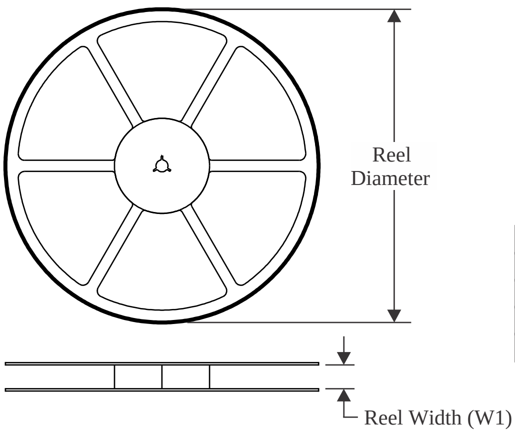
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

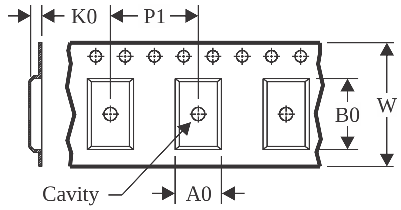
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

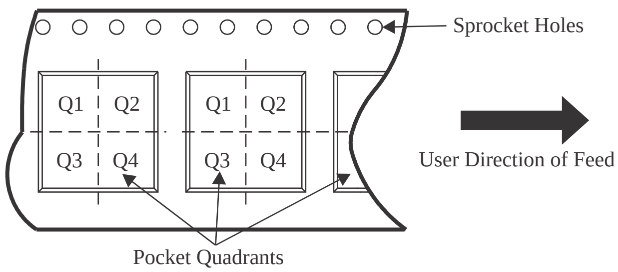


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

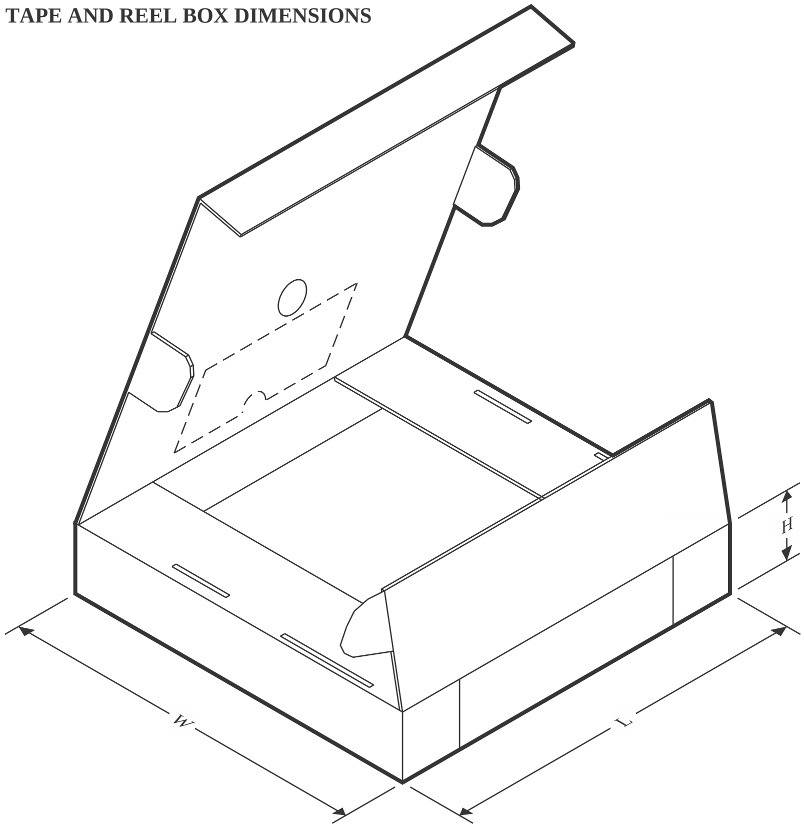
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

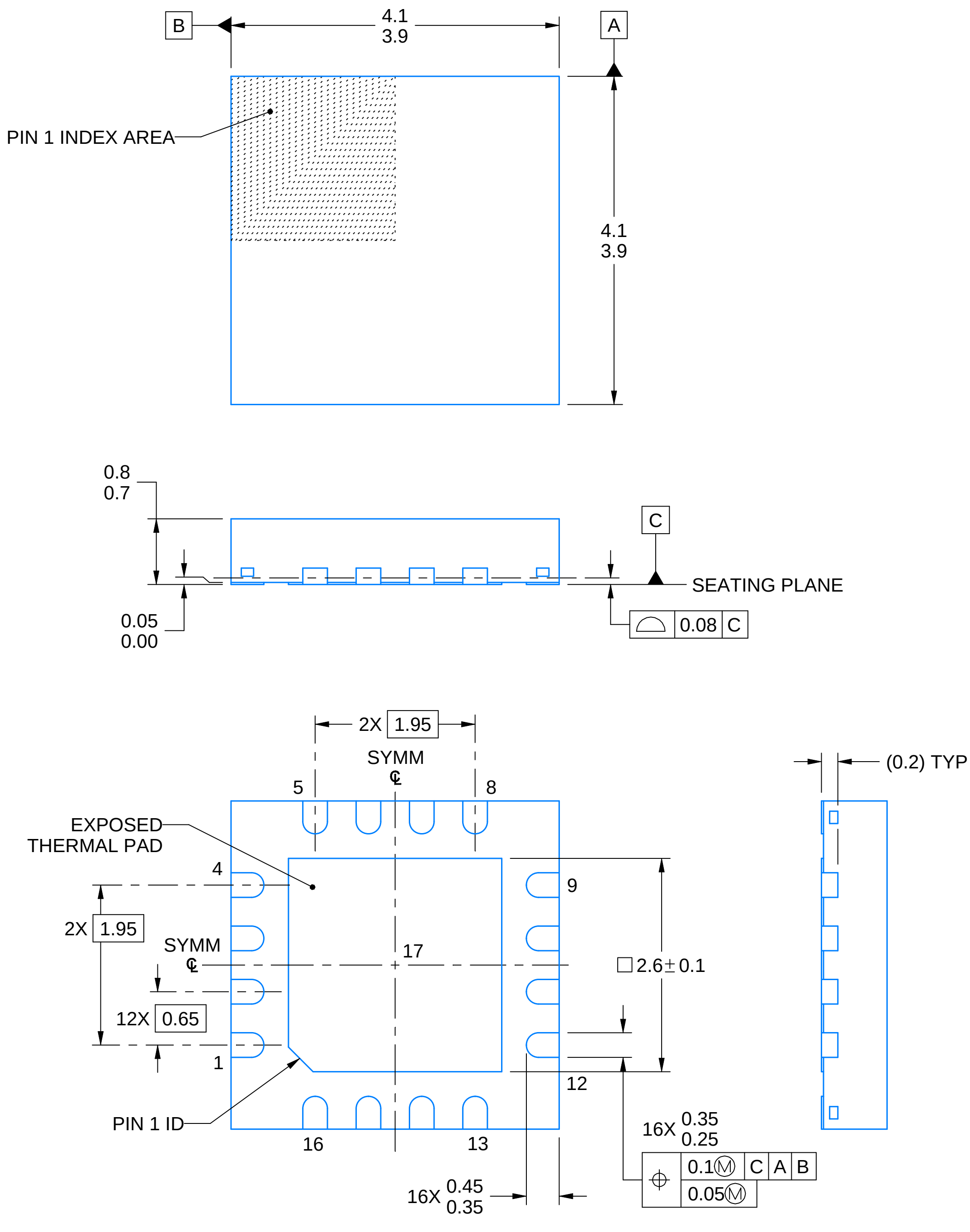
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX7308FPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX7308FPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX7308FRRPR	WQFN	RRP	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TMUX7308FRRPRG4	WQFN	RRP	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TMUX7309FPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX7309FRRPR	WQFN	RRP	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

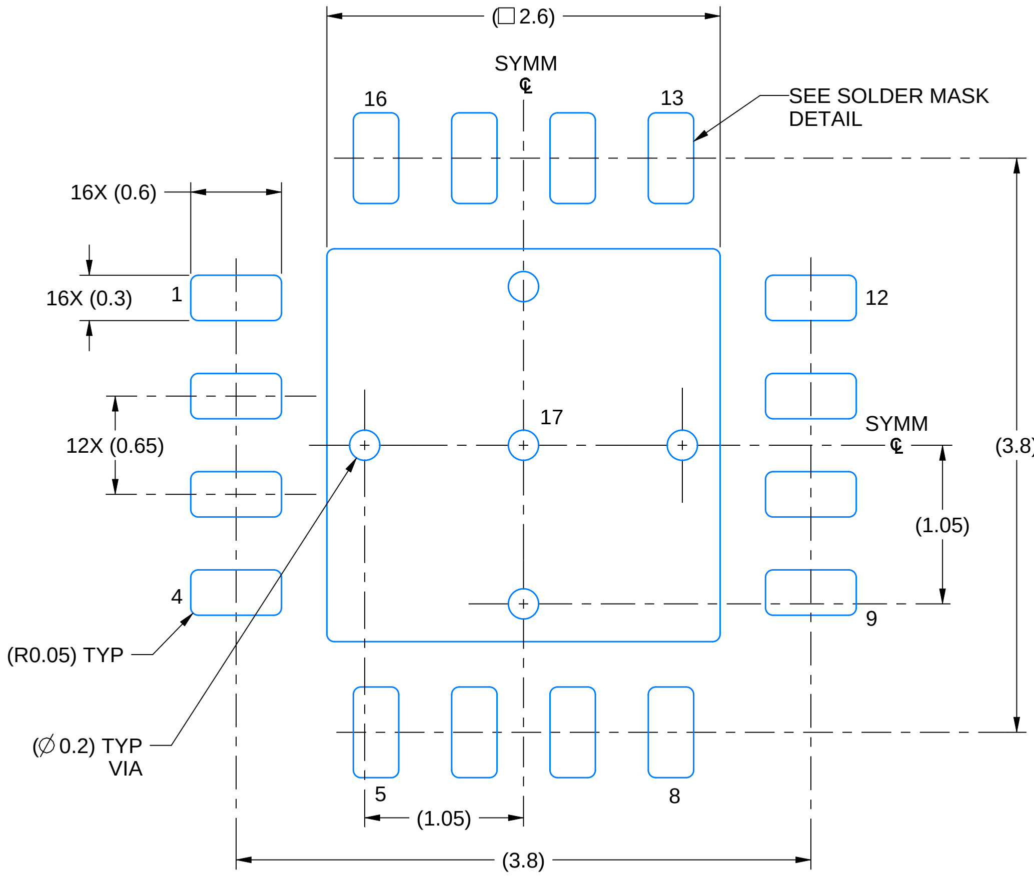
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX7308FPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TMUX7308FPWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
TMUX7308FRRPR	WQFN	RRP	16	3000	367.0	367.0	35.0
TMUX7308FRRPRG4	WQFN	RRP	16	3000	367.0	367.0	35.0
TMUX7309FPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TMUX7309FRRPR	WQFN	RRP	16	3000	367.0	367.0	35.0



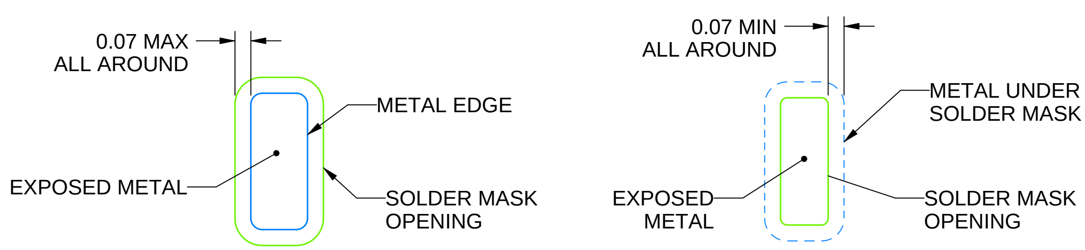
4224816/A 02/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

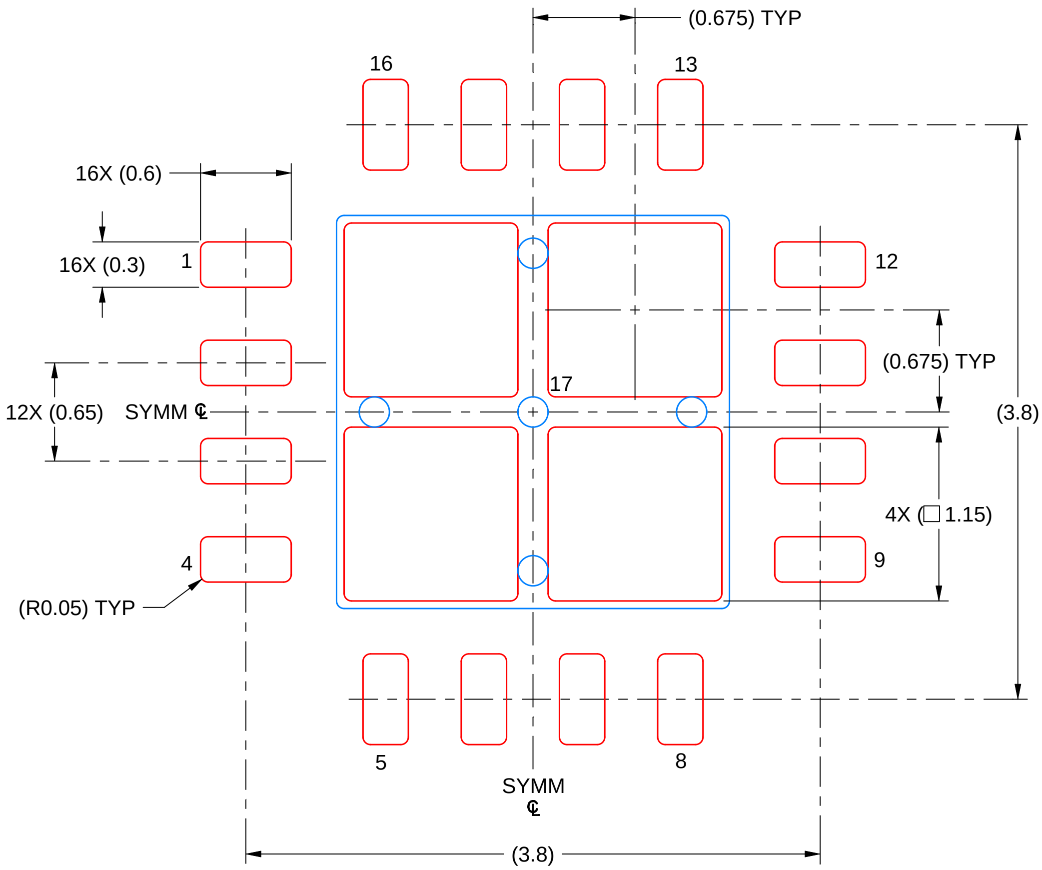
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4224816/A 02/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224816/A 02/2019

NOTES: (continued)

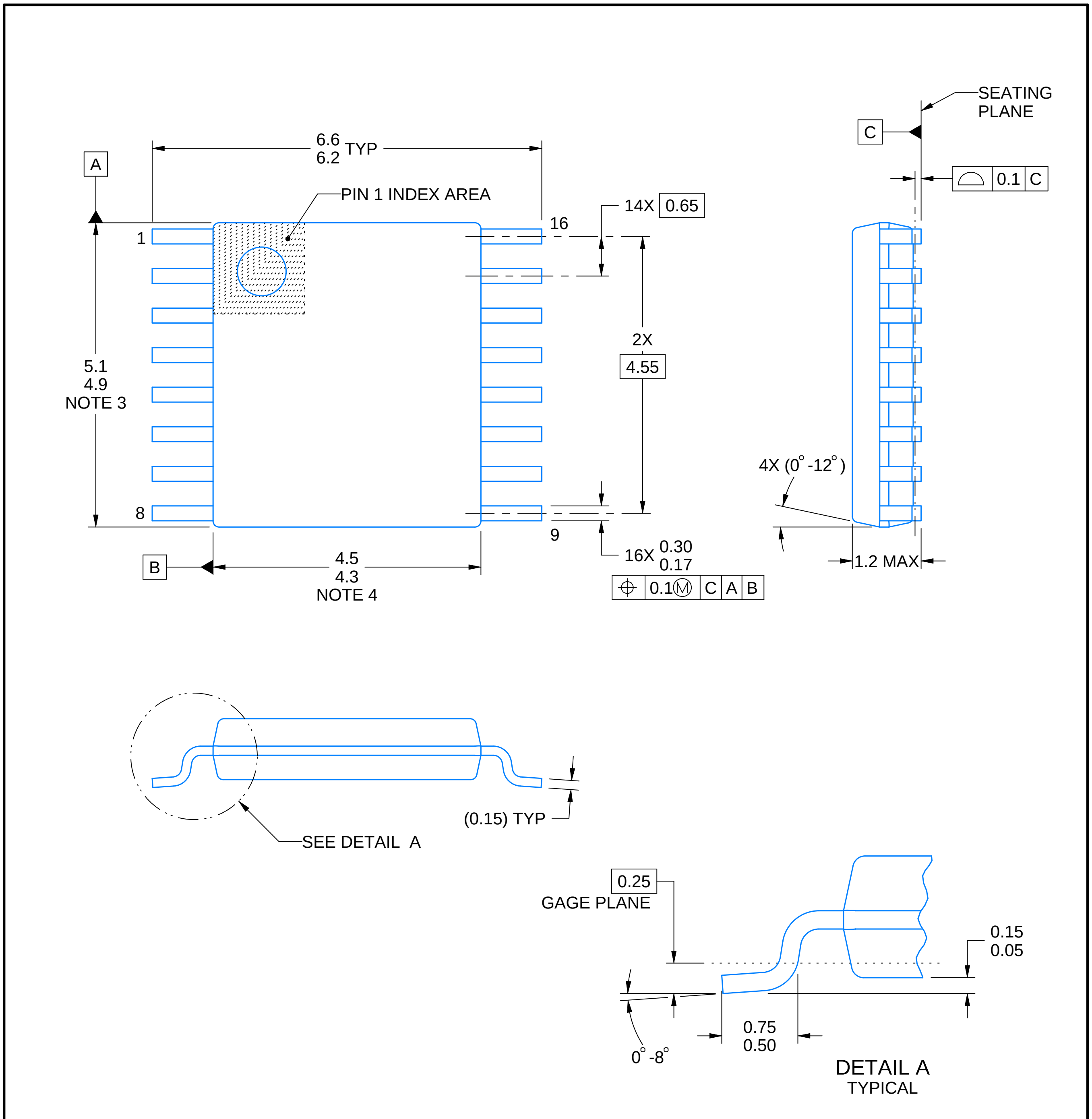
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PW0016A

PACKAGE OUTLINE

TSSOP - 1.2 mm max height

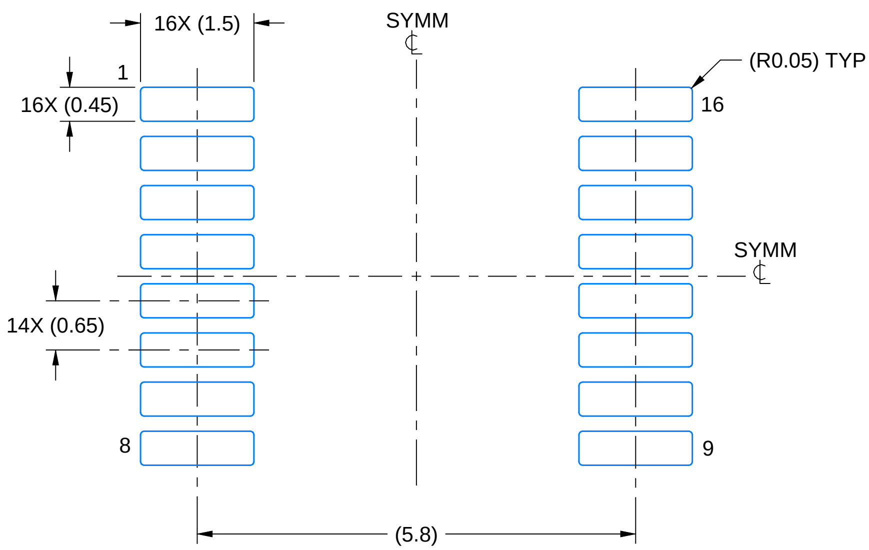
SMALL OUTLINE PACKAGE



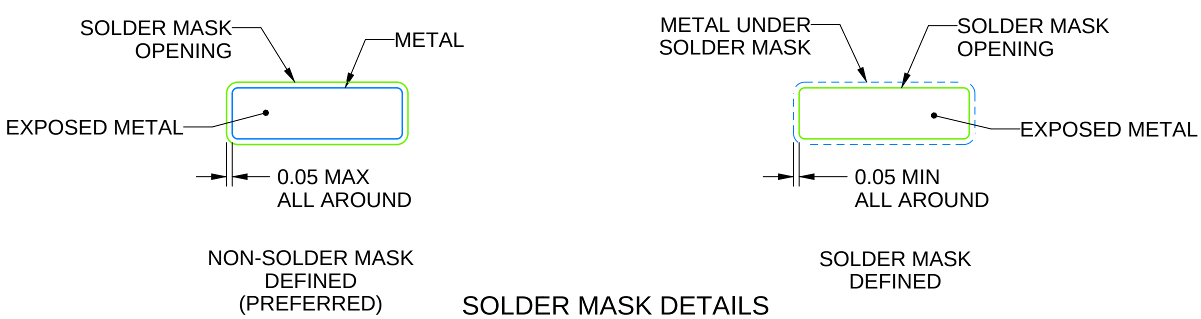
4220204/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

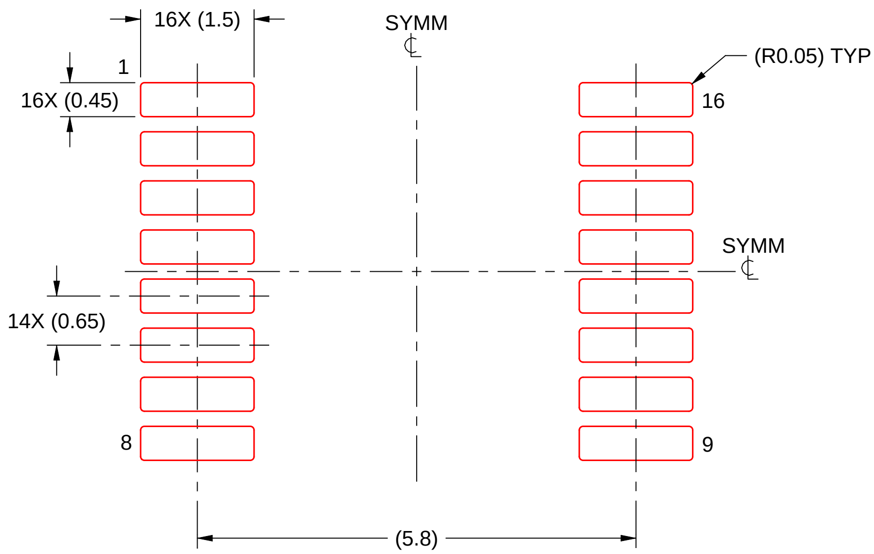


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.