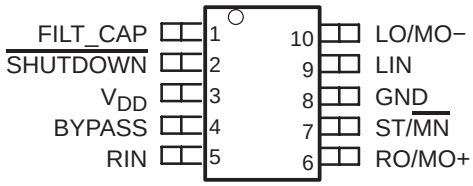
- **Ideal for Notebook Computers, PDAs, and Other Small Portable Audio Devices**
- **2 W Into 4 Ω From 5-V Supply**
- **0.6 W Into 4 Ω From 3-V Supply**
- **Stereo Head Phone Drive**
- **Mono (BTL) Signal Created by Summing Left and Right Signals**
- **Wide Power Supply Compatibility 3 V to 5 V**
- **Meets PC99 Portable Specs (target)**
- **Low Supply Current**
  - **4 mA Typical at 5 V**
  - **3.3 mA Typical at 3 V**
- **Shutdown Control . . . 1 μA Typical**
- **Shutdown Pin is TTL Compatible**
- **−40°C to 85°C Operating Temperature Range**
- **Space-Saving, Thermally-Enhanced MSOP Packaging**

DGQ PACKAGE
(TOP VIEW)



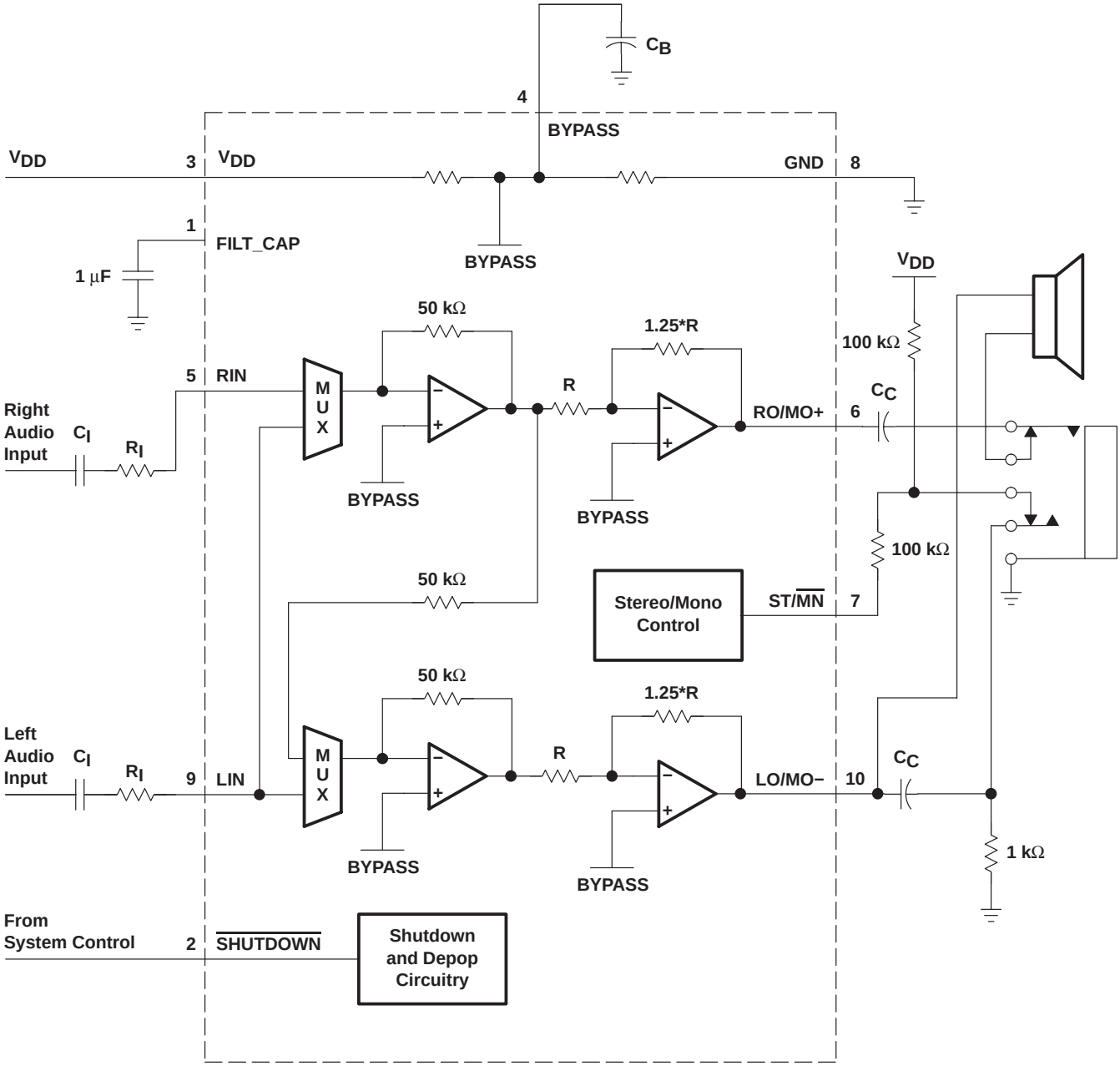
description

The TPA0233 is a 2-W mono bridge-tied-load (BTL) amplifier designed to drive speakers with as low as 4-Ω impedance. The mono signal is created by summing left and right inputs. The amplifier can be reconfigured on the fly to drive two stereo single-ended (SE) signals into head phones. This makes the device ideal for use in small notebook computers, PDAs, digital personal audio players, anyplace a mono speaker and stereo headphones are required. From a 5-V supply, the TPA0233 deliver 2 W of power into a 4-Ω speaker.

The gain of the input stage is set by the user-selected input resistor and a 50-kΩ internal feedback resistor ($A_V = - R_F / R_I$). The power stage is internally configured with a gain of −1.25 V/V in SE mode, and −2.5 V/V in BTL mode. Thus, the overall gain of the amplifier is 62.5 kΩ/ R_I in SE mode and 125 kΩ/ R_I in BTL mode. The input terminals are high-impedance CMOS inputs, and can be used as summing nodes.

The TPA0233 is available in the 10-pin thermally-enhanced MSOP package (DGQ) and operates over an ambient temperature range of −40°C to 85°C.

functional block diagram



AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	MSOP SYMBOLIZATION
	MSOP† (DGQ)	
−40°C to 85°C	TPA0233DGQ	AEJ

† The DGQ package are available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0233DGQR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	4	I	BYPASS is the tap to the voltage divider for internal mid-supply bias. This terminal should be connected to a 0.1-μF to 1-μF capacitor.
FILT_CAP	1	I	Terminal is used to filter supply.
GND	8		Ground terminal
LIN	9	I	Left-channel input terminal
LO/MO−	10	O	Left-output in SE mode and mono negative output in BTL mode.
RIN	5	I	Right-channel input terminal
RO/MO+	6	O	Right-output in SE mode and mono positive output in BTL mode
$\overline{\text{SHUTDOWN}}$	2	I	$\overline{\text{SHUTDOWN}}$ places the entire device in shutdown mode when held low. TTL compatible input.
ST/$\overline{\text{MN}}$	7	I	Selects between stereo and mono mode. When held high, the amplifier is in SE stereo mode, while held low, the amplifier is in BTL mono mode.
V_{DD}	3	I	V_{DD} is the supply voltage terminal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} . . . . . 6 V
Input voltage range, V_I . . . . . −0.3 V to V_{DD} +0.3 V
Continuous total power dissipation . . . . . internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A (see Table 3) . . . . . −40°C to 85°C
Operating junction temperature range, T_J . . . . . −40°C to 150°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
DGQ	2.14 W‡	17.1 mW/°C	1.37 W	1.11 W

‡ See the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (SLMA002), for more information on the PowerPAD™ package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of that document.

recommended operating conditions

			MIN	MAX	UNIT
Supply voltage, V_{DD}			2.5	5.5	V
High-level input voltage, V_{IH}	ST/$\overline{\text{MN}}$	V_{DD} = 3 V	2.7		V
		V_{DD} = 5 V	4.5		
	$\overline{\text{SHUTDOWN}}$		2		
Low-level input voltage, V_{IL}	ST/$\overline{\text{MN}}$	V_{DD} = 3 V		1.65	V
		V_{DD} = 5 V		2.75	
	$\overline{\text{SHUTDOWN}}$			0.8	
Operating free-air temperature, T_A			−40	85	°C

PowerPAD is a trademark of Texas Instruments.

electrical characteristics at specified free-air temperature, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)	$\overline{SHUTDOWN}$ = 2 V, ST/$\overline{MN}$ = 0, R_L = 4 Ω			30	mV
I_{DD}	Supply current	V_{DD} 2.5 V, $\overline{SHUTDOWN}$ = 2 V		3.3	5	mA
$I_{DD(SD)}$	Supply current, shutdown mode	$\overline{SHUTDOWN}$ = 0 V		1	10	µA
$\|I_{IH}\|$	High-level input current	$\overline{SHUTDOWN}$, V_{DD} = 3.3 V, V_I = 3.3 V			1	µA
		ST/$\overline{MN}$, V_{DD} = 3.3 V, V_I = 3.3 V			1	
$\|I_{IL}\|$	Low-level input current	$\overline{SHUTDOWN}$, V_{DD} = 3.3 V, V_I = 0 V			1	µA
		ST/$\overline{MN}$, V_{DD} = 3.3 V, V_I = 0 V			1	
R_F	Feedback resistor	V_{DD} = 2.5 V, R_L = 4 Ω, $\overline{SHUTDOWN}$ = 2 V, ST/$\overline{MN}$ = 1.375 V	47	50	57	kΩ

operating characteristics, V_{DD} = 3 V, T_A = 25°C, R_L = 4 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power, See Note 1	THD = 1%, BTL mode		660		mW
		THD = 0.1%, SE mode, R_L = 32 Ω		33		
THD + N	Total harmonic distortion plus noise	P_O = 500 mW, f = 20 Hz to 20 kHz		0.3%		
B_{OM}	Maximum output power bandwidth	Gain = 2, THD = 2%		20		kHz

NOTE 1: Output power is measured at the output terminals of the device at f = 1 kHz.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)	$\overline{SHUTDOWN}$ = 2 V, ST/$\overline{MN}$ = 0, R_L = 4 Ω			30	mV
I_{DD}	Supply current	$\overline{SHUTDOWN}$ = 2 V		4	7	mA
$I_{DD(SD)}$	Supply current, shutdown mode	$\overline{SHUTDOWN}$ = 0 V		1	10	µA
$\|I_{IH}\|$	High-level input current	$\overline{SHUTDOWN}$, V_{DD} = 5.5 V, V_I = 5.5 V			1	µA
		ST/$\overline{MN}$, V_{DD} = 5.5 V, V_I = 5.5 V			1	
$\|I_{IL}\|$	Low-level input current	$\overline{SHUTDOWN}$, V_{DD} = 5.5 V, V_I = 0 V			1	µA
		ST/$\overline{MN}$, V_{DD} = 5.5 V, V_I = 0 V			1	

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 4 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power, see Note 1	THD = 1%, BTL mode		2		W
		THD = 0.1%, SE mode, R_L = 32 Ω		92		mW
THD + N	Total harmonic distortion plus noise	P_O = 1 W, f = 20 Hz to 20 kHz		0.2%		
B_{OM}	Maximum output power bandwidth	Gain = 2.5, THD = 2%		20		kHz

NOTE 1: Output power is measured at the output terminals of the device at f = 1 kHz.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Supply ripple rejection ratio	vs Frequency	1, 2
I_{DD}	Supply current	vs Supply voltage	3
P_O	Output power	vs Supply voltage	4, 5
		vs Load resistance	6, 7
THD+N	Total harmonic distortion plus noise	vs Frequency	8, 9, 10, 11
		vs Output power	12, 13, 14, 15, 16, 17
V_n	Output noise voltage	vs Frequency	18, 19
	Closed loop response		20, 21
	Crosstalk	vs Frequency	22, 23

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

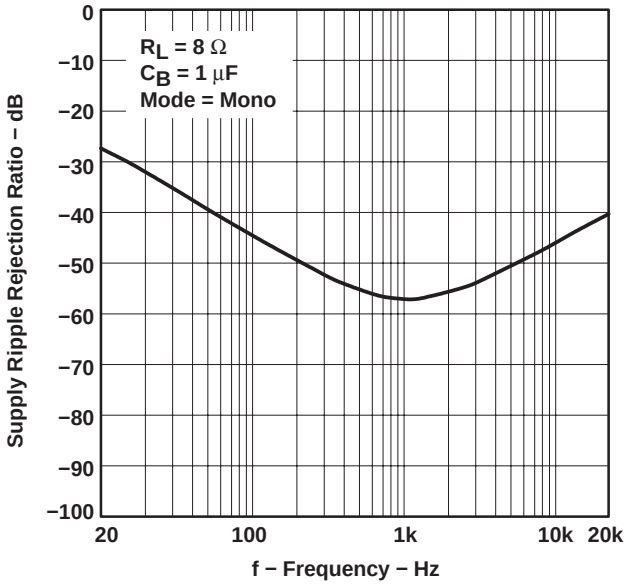


Figure 1

SUPPLY RIPPLE REJECTION RATIO
vs
FREQUENCY

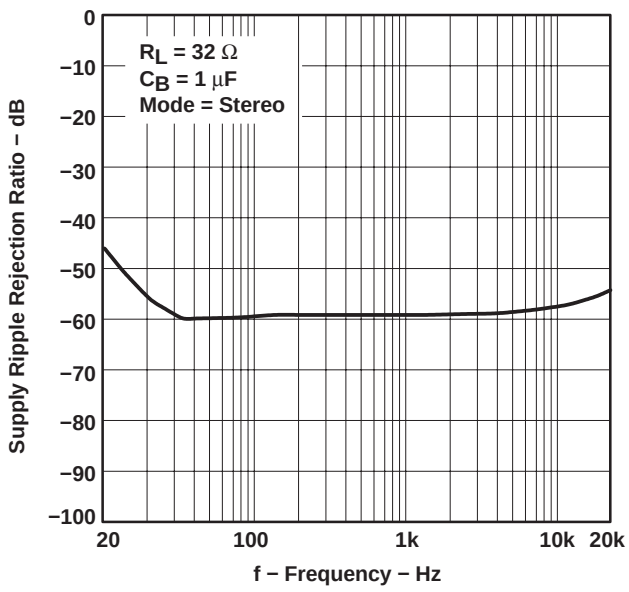


Figure 2

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

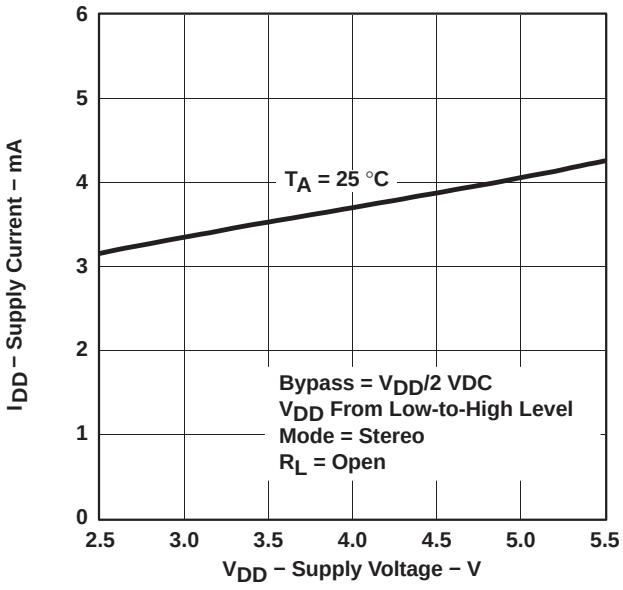


Figure 3

OUTPUT POWER vs SUPPLY VOLTAGE

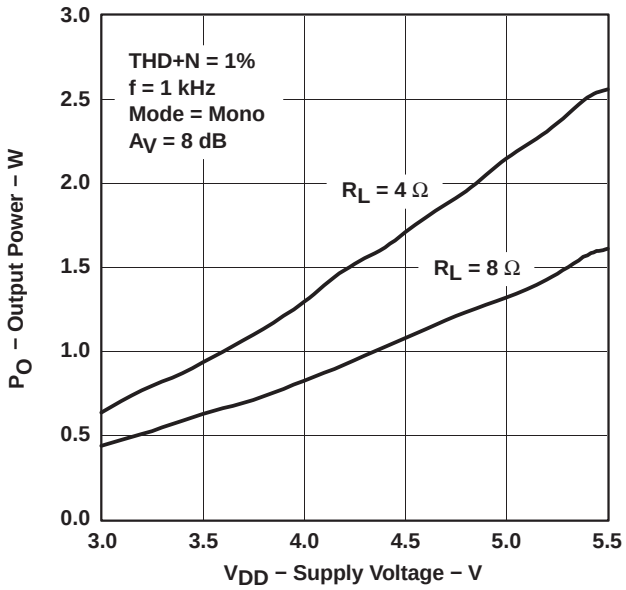


Figure 4

OUTPUT POWER vs SUPPLY VOLTAGE

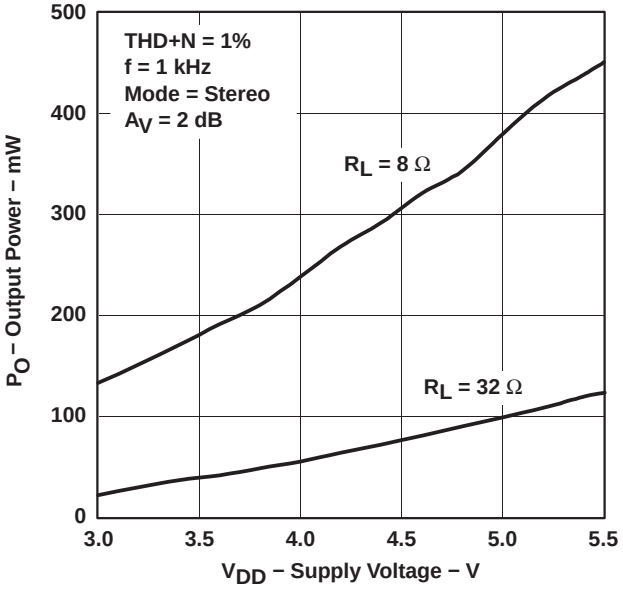


Figure 5

OUTPUT POWER vs LOAD RESISTANCE

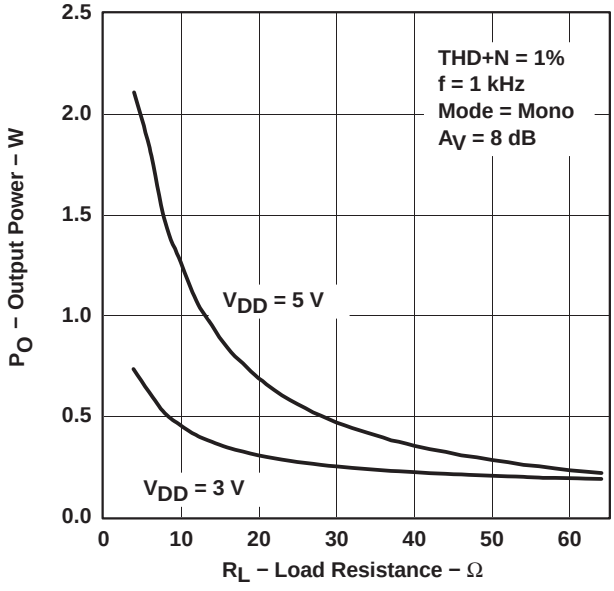


Figure 6

TYPICAL CHARACTERISTICS

**OUTPUT POWER
vs
LOAD RESISTANCE**

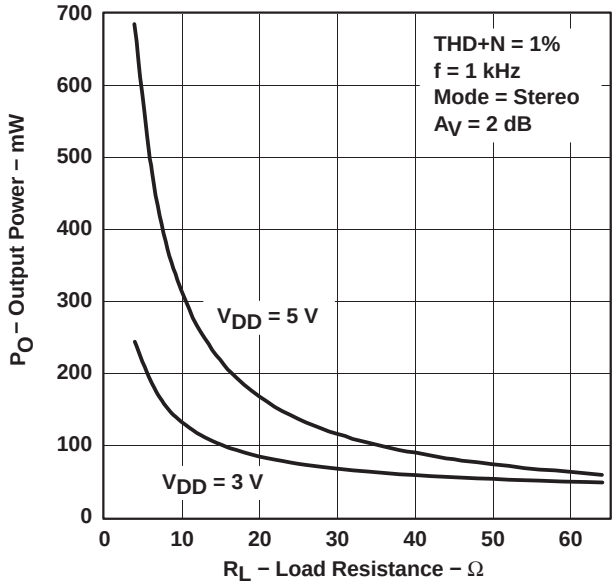


Figure 7

**TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY**

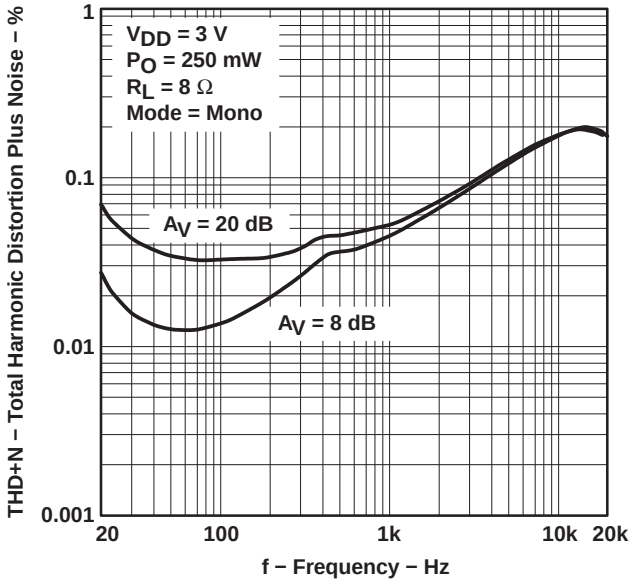


Figure 8

**TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY**

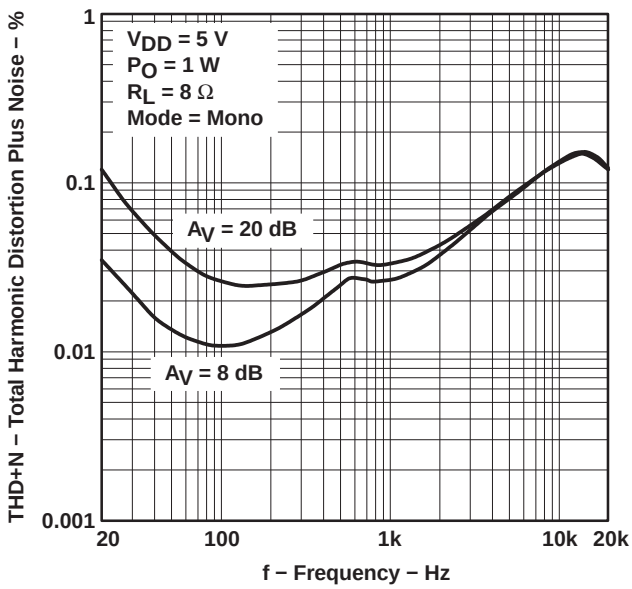


Figure 9

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

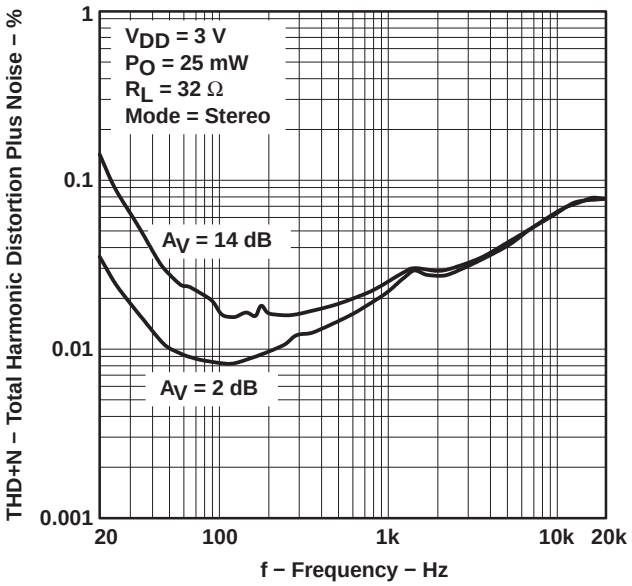


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

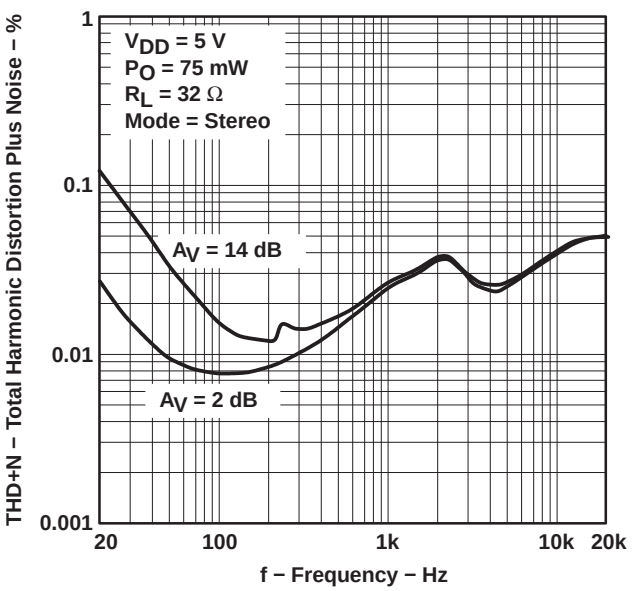


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

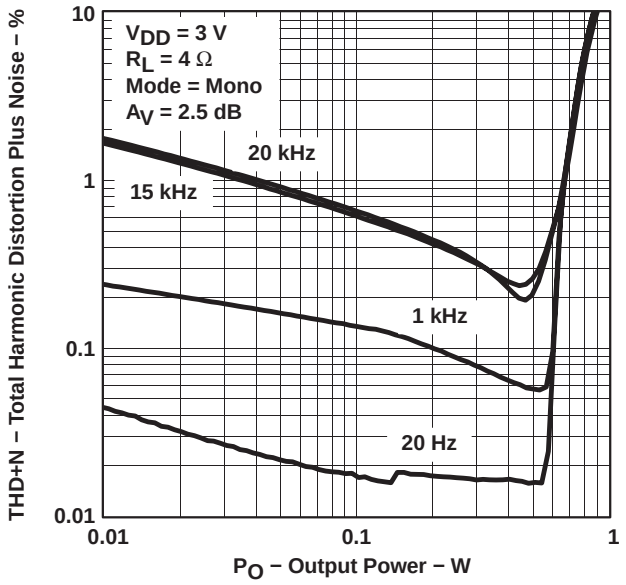


Figure 12

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

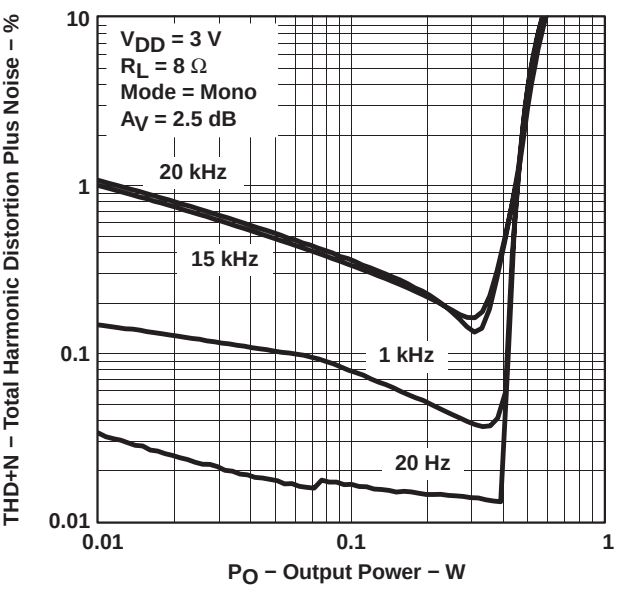


Figure 13

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

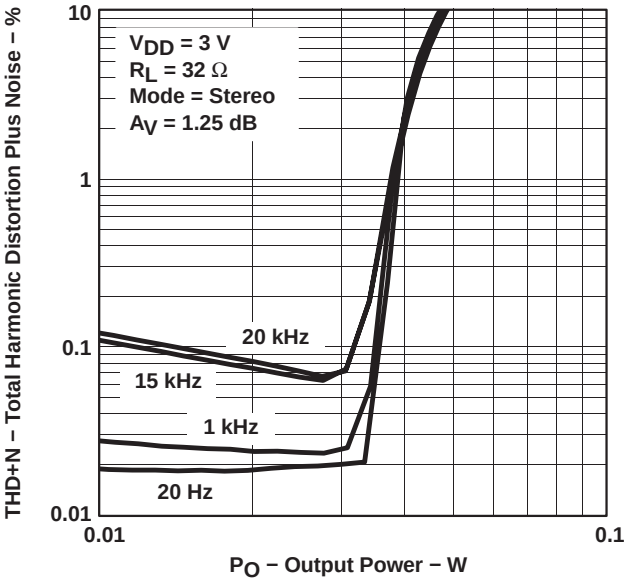


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

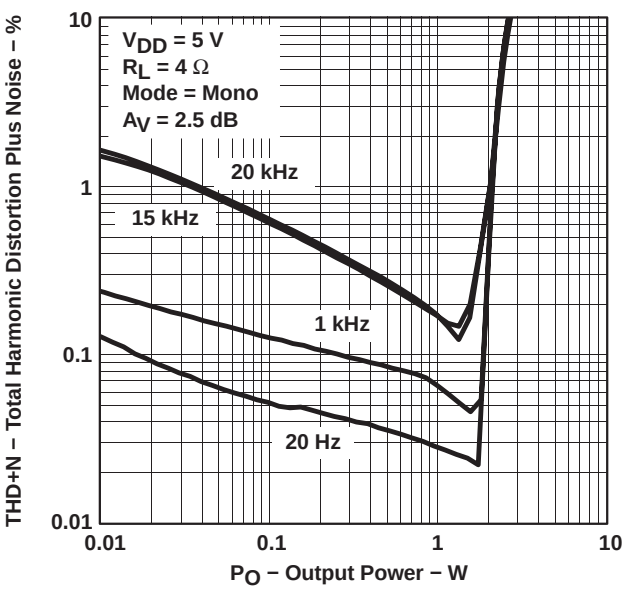


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

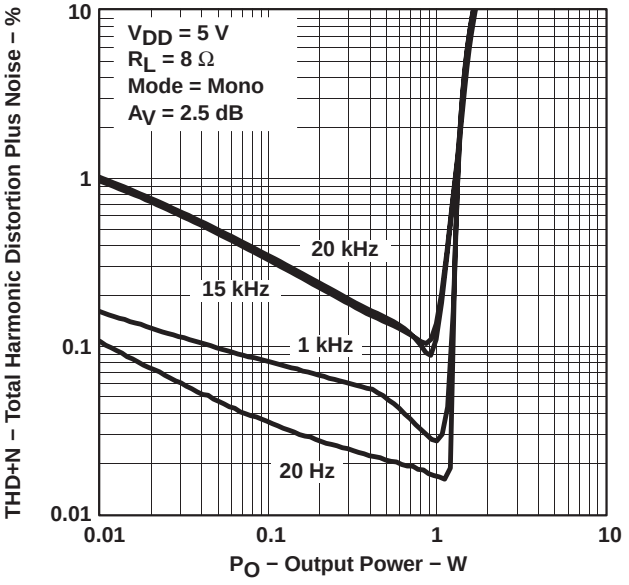


Figure 16

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

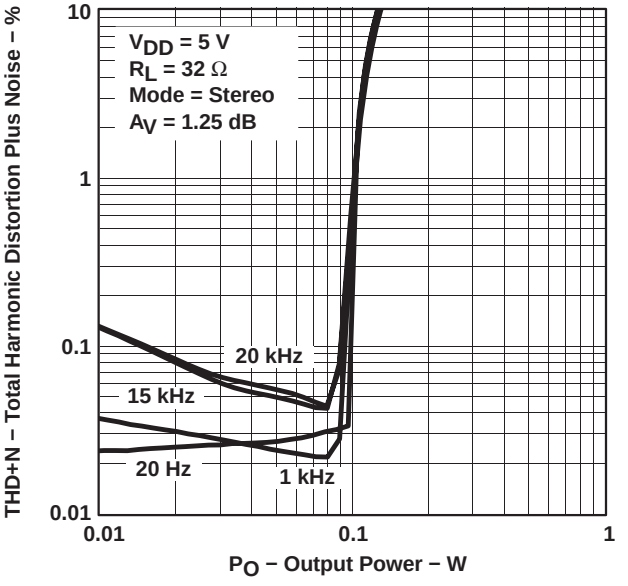


Figure 17

TYPICAL CHARACTERISTICS

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

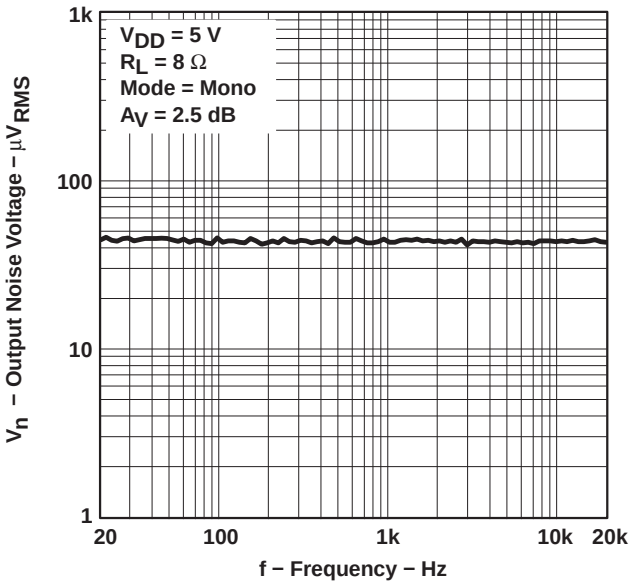


Figure 18

OUTPUT NOISE VOLTAGE
vs
FREQUENCY

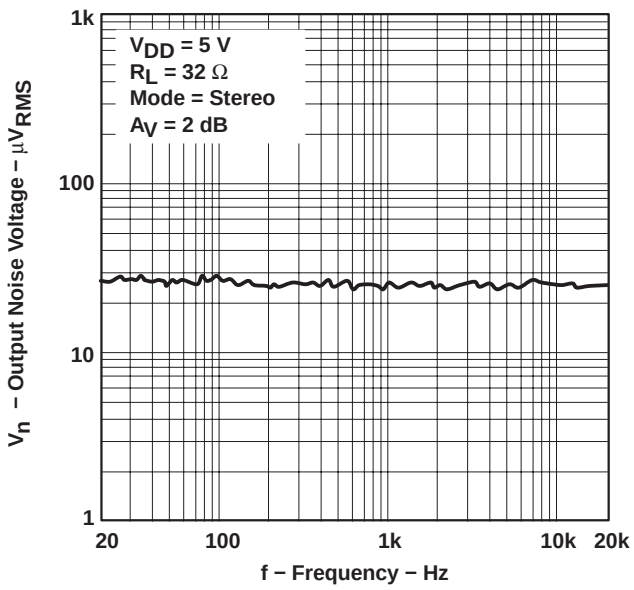


Figure 19

CLOSED LOOP RESPONSE

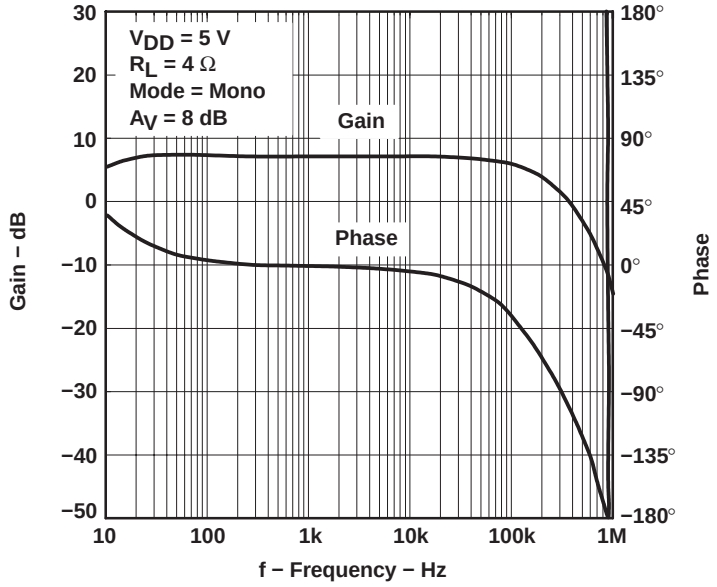


Figure 20

TYPICAL CHARACTERISTICS

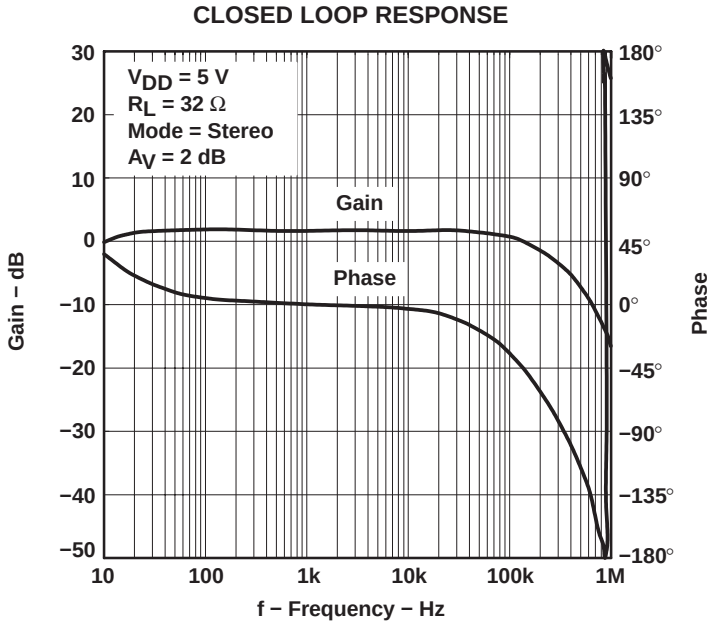


Figure 21

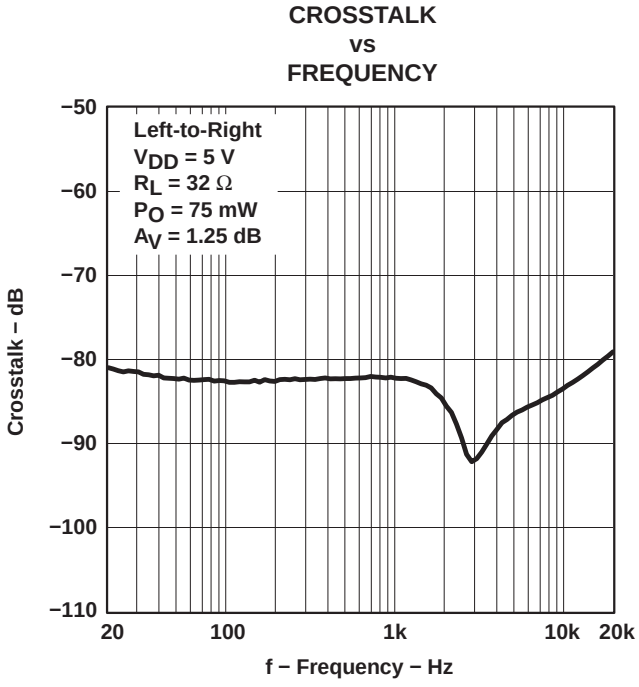


Figure 22

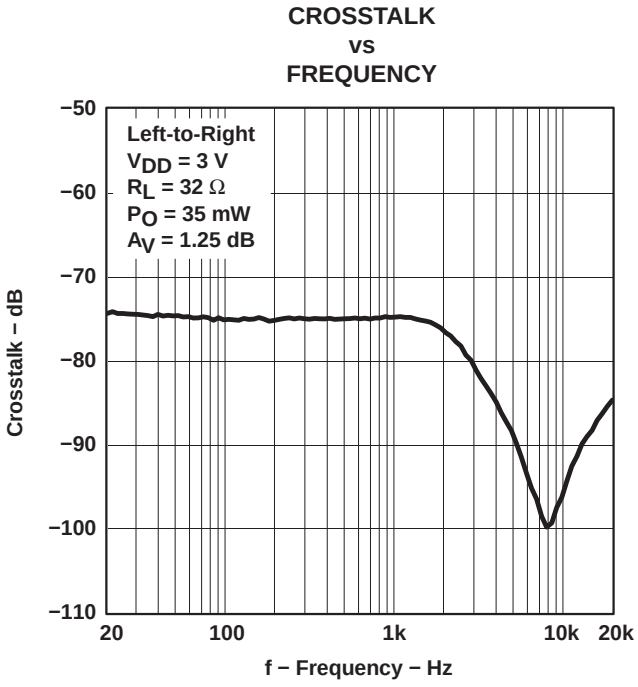


Figure 23

APPLICATION INFORMATION

gain setting via input resistance

The gain of the input stage is set by the user-selected input resistor and a 50-kΩ internal feedback resistor.

However, the power stage is internally configured with a gain of −1.25 V/V in stereo mode, and −2.5 V/V in mono mode. Thus, the feedback resistor (R_F) is effectively 62.5 kΩ in stereo mode and 125 kΩ in mono mode. Therefore, the overall gain can be calculated using equations (1) and (2) stereo.

$$A_V = \frac{-125\ k\Omega}{R_I} \quad \text{(Mono)} \tag{1}$$

$$A_V = \frac{-62.5\ k\Omega}{R_I} \quad \text{(Stereo)} \tag{2}$$

The −3 dB frequency can be calculated using equation 3.

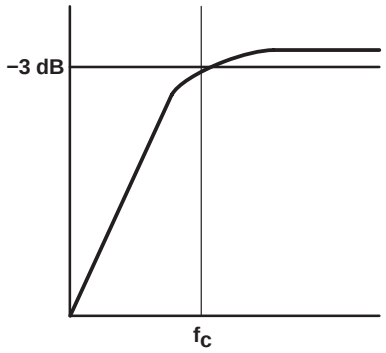
$$f_{-3\ dB} = \frac{1}{2\pi R_I C_i} \tag{3}$$

If the filter must be more accurate, the value of the capacitor should be increased while the value of the resistor to ground should be decreased. In addition, the order of the filter could be increased.

input capacitor, C_i

In the typical application an input capacitor (C_i), is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input resistance of the amplifier, R_I, form a high-pass filter with the corner frequency determined in equation 4.

$$f_{c(highpass)} = \frac{1}{2\pi R_I C_i} \tag{4}$$



The value of C_i is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 2 is reconfigured as equation 5.

$$C_i = \frac{1}{2\pi R_I f_c} \tag{5}$$

In this example, C_I is 0.4 μF so one would likely choose a value in the range of 0.47 μF to 1 μF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

APPLICATION INFORMATION

power supply decoupling, $C_{(S)}$

The TPA0233 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, $C_{(BYP)}$

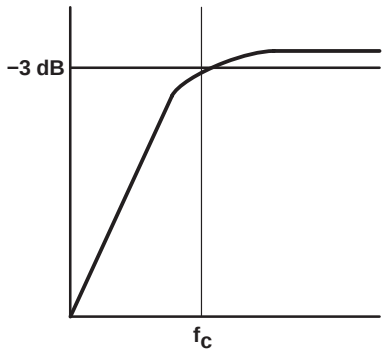
The midrail bypass capacitor ($C_{(BYP)}$), is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, $C_{(BYP)}$ determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor ($C_{(BYP)}$), values of 0.47-μF to 1-μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

output coupling capacitor, $C_{(C)}$

In the typical single-supply stereo configuration, an output coupling capacitor ($C_{(C)}$) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 6.

$$f_{c(high)} = \frac{1}{2\pi R_L C_{(C)}} \quad (6)$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher, degrading the bass response. Large values of $C_{(C)}$ are required to pass low frequencies into the load. Consider the example where a $C_{(C)}$ of 330 μF is chosen and loads vary from 3 Ω, 4 Ω, 8 Ω, 32 Ω, 10 kΩ, to 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

Table 1. Common Load Impedances vs Low Frequency Output Characteristics in Stereo (SE) Mode

R_L	$C_{(C)}$	Lowest Frequency
3 Ω	330 μF	161 Hz
4 Ω	330 μF	120 Hz
8 Ω	330 μF	60 Hz
32 Ω	330 μF	15 Hz
10,000 Ω	330 μF	0.05 Hz
47,000 Ω	330 μF	0.01 Hz

APPLICATION INFORMATION

output coupling capacitor, $C_{(C)}$ (continued)

As Table 1 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

Furthermore, the total amount of ripple current that must flow through the capacitor must be considered when choosing the component. As shown in the application circuit, one coupling capacitor must be in series with the mono loudspeaker for proper operation of the stereo-mono switching circuit. For a 4-Ω load, this capacitor must be able to handle about 700 mA of ripple current for a continuous output power of 2 W.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

bridged-tied load versus single-ended mode

Figure 24 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The TPA0233 BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This, in effect, doubles the voltage swing on the load as compared to a ground referenced load. Plugging $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance. See equation 7.

$$V_{(RMS)} = \frac{V_{O(PP)}}{2\sqrt{2}} \qquad (7)$$

$$\text{Power} = \frac{V_{(RMS)}^2}{R_L}$$

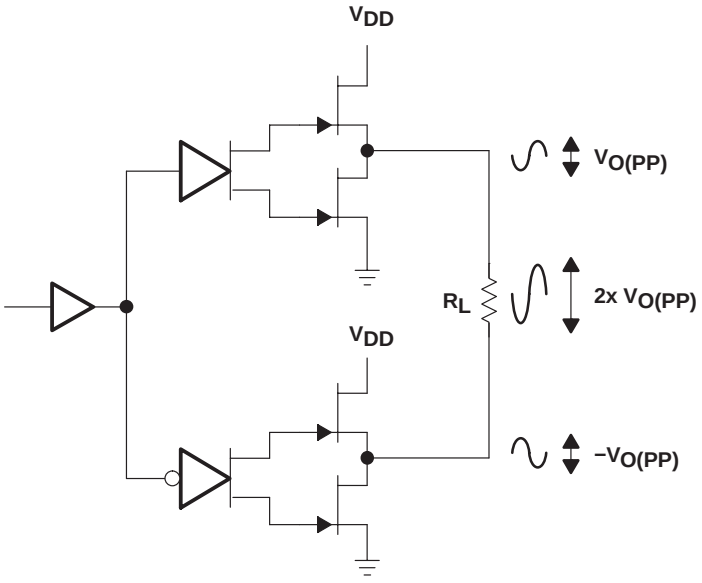


Figure 24. Bridge-Tied Load Configuration

APPLICATION INFORMATION

bridged-tied load versus single-ended mode (continued)

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power, that is a 6-dB improvement—which is loudness that can be heard. In addition to increased power, there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 25. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 μF to 1000 μF) so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high-pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 8.

$$f_c = \frac{1}{2\pi R_L C_{(C)}} \quad (8)$$

For example, a 68-μF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

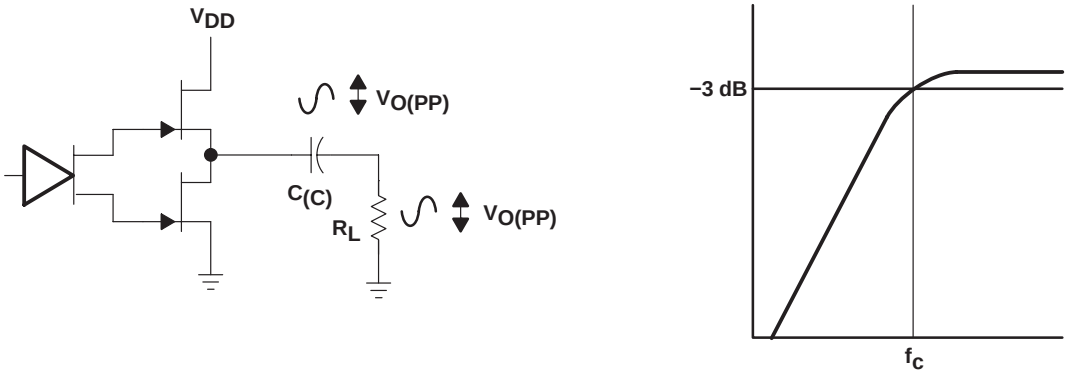


Figure 25. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *crest factor and thermal considerations* section.

single-ended (stereo) operation

In SE (stereo) mode (see Figure 24 and Figure 25), the load is driven from the primary amplifier output for each channel (LO and RO, terminals 6 and 10).

The amplifier switches to single-ended operation when the ST/$\overline{\text{MN}}$ terminal is held high.

input operation

The input allows stereo inputs to be applied to the amplifier. When the ST/$\overline{\text{MN}}$ terminal is held high, the inputs (LIN and RIN) drive the outputs as LO and RO in stereo mode. When the ST/$\overline{\text{MN}}$ terminal is held low, the inputs are surrounded internally to create the mono BTL signal, driving the outputs as MO+ and MO−.

APPLICATION INFORMATION

BTL amplifier efficiency

Class-AB amplifiers are inefficient. The primary cause of inefficiencies is the voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood. See Figure 26.

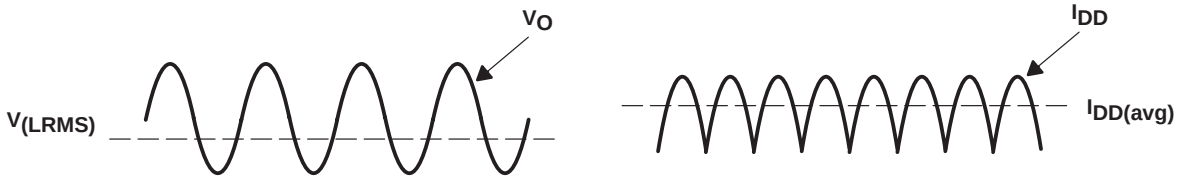


Figure 26. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}} \tag{9}$$

where

$$P_L = \frac{V_{LRMS}^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P^2}{2R_L}$$

and $P_{SUP} = V_{DD}\, I_{DD}avg$ and $I_{DD}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L} \sin(t)\, dt = \frac{1}{\pi} \times \frac{V_P}{R_L} [\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$

therefore,

$$P_{SUP} = \frac{2\, V_{DD}\, V_P}{\pi\, R_L}$$

substituting P_L and P_{SUP} into equation 9,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P^2}{2\, R_L}}{\frac{2\, V_{DD}\, V_P}{\pi\, R_L}} = \frac{\pi\, V_P}{4\, V_{DD}}$$

where

$$V_P = \sqrt{2\, P_L\, R_L}$$

APPLICATION INFORMATION

BTL amplifier efficiency (continued)

therefore,

$$\eta_{BTL} = \frac{\pi \sqrt{2 P_L R_L}}{4 V_{DD}} \quad (10)$$

P_L = Power devilered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

Table 2 employs equation 10 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased, resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 2. Efficiency vs Output Power in 5-V, 8-Ω BTL Systems

Output Power (W)	Efficiency (%)	Peak Voltage (V)	Internal Dissipation (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47†	0.53

† High peak voltages cause the THD to increase.

A final point to remember about Class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 10, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

crest factor and thermal considerations

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature, the internal dissipated power at the average output power level must be used. The TPA0233 data sheet shows that when the TPA0233 is operating from a 5-V supply into a 4-Ω speaker, 4-W peaks are available. Converting watts to dB:

$$P_{dB} = 10 \text{Log} \frac{P_W}{P_{ref}} = 10 \text{Log} \frac{4\ W}{1\ W} = 6\ dB \quad (11)$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields

6 dB − 15 dB = −9 dB (15-dB crest factor)
6 dB − 12 dB = −6 dB (12-dB crest factor)
6 dB − 9 dB = −3 dB (9-dB crest factor)
6 dB − 6 dB = 0 dB (6-dB crest factor)
6 dB − 3 dB = 3 dB (3-dB crest factor)

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \quad (12)$$

$$= 63 \text{ mW (18-dB crest factor)}$$
$$= 125 \text{ mW (15-dB crest factor)}$$
$$= 250 \text{ mW (9-dB crest factor)}$$
$$= 500 \text{ mW (6-dB crest factor)}$$
$$= 1000 \text{ mW (3-dB crest factor)}$$
$$= 2000 \text{ mW (15-dB crest factor)}$$

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 2 W of continuous power output with a 3-dB crest factor, against 12-dB and 15-dB applications drastically affects maximum ambient temperature ratings for the system. Table 3 shows maximum ambient temperatures and TPA0233 internal power dissipation for various output-power levels.

Table 3. TPA0233 Power Rating, 5-V, 3-Ω, Mono

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3-dB crest factor)	1.7	−3°C
4	1000 mW (6-dB crest factor)	1.6	6°C
4	500 mW (9-dB crest factor)	1.4	24°C
4	250 mW (12-dB crest factor)	1.1	51°C
4	125 mW (15-dB crest factor)	0.8	78°C
4	63 mW (18-dB crest factor)	0.6	96°C

Table 4. TPA0233 Power Rating, 5-V, 8-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W)	MAXIMUM AMBIENT TEMPERATURE
2.5	1250 mW (3-dB crest factor)	0.55	100°C
2.5	1000 mW (4-dB crest factor)	0.62	94°C
2.5	500 mW (7-dB crest factor)	0.59	97°C
2.5	250 mW (10-dB crest factor)	0.53	102°C

The maximum dissipated power (P_{Dmax}), is reached at a much lower output power level for an 8-Ω load than for a 4-Ω load. As a result, this simple formula for calculating P_{Dmax} may be used for a 4-Ω application.

$$P_{Dmax} = \frac{2V_{DD}^2}{\pi^2 R_L} \quad (13)$$

However, in the case of a 4-Ω load, the P_{Dmax} occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the P_{Dmax} formula for a 4-Ω load.

The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the DGQ package is shown in the dissipation rating table. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.0171} = 58.48°C/W \quad (14)$$

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated power needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA0233 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$T_A \text{ Max} = T_J \text{ Max} - \Theta_{JA} P_D = 150 - 58.48(0.8 \times 2) = 56°\text{C (15-dB crest factor)} \quad (15)$$

NOTE:
Internal dissipation of 0.8 W is estimated for a 2-W system with 15-dB crest factor per channel.

Tables 3 and 4 show that for some applications no airflow is required to keep junction temperatures in the specified range. The TPA0233 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Tables 3 and 4 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

ST/$\overline{\text{MN}}$ (stereo/mono) operation

The ability of the TPA0233 to easily switch between mono BTL and stereo SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where an internal speaker is driven in BTL mode but external stereo headphone or speakers must be accommodated. When ST/$\overline{\text{MN}}$ is held high, the RIN and LIN inputs drive the output as Lo and Ro in stereo SE mode. When ST/$\overline{\text{MN}}$ is held low, the inputs are summed internally and the output is driven as Mo+ and Mo− in mono BTL mode. Control of the ST/$\overline{\text{MN}}$ input can be from a logic-level CMOS source or, more typically, from a switch-controlled resistor divider network as shown in the functional block diagram.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA0233DGQ	Active	Production	HVSSOP (DGQ) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AEJ
TPA0233DGQ.A	Active	Production	HVSSOP (DGQ) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AEJ
TPA0233DGQR	Active	Production	HVSSOP (DGQ) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AEJ
TPA0233DGQR.A	Active	Production	HVSSOP (DGQ) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AEJ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

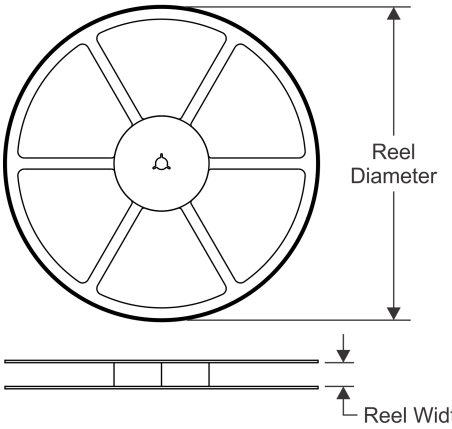
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

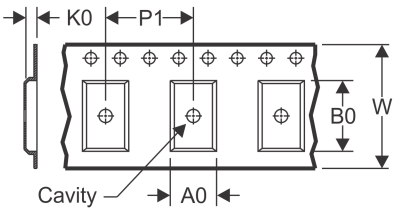
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

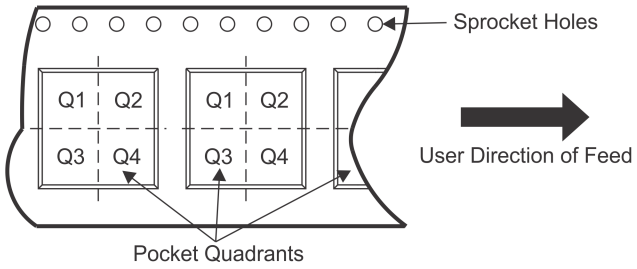


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

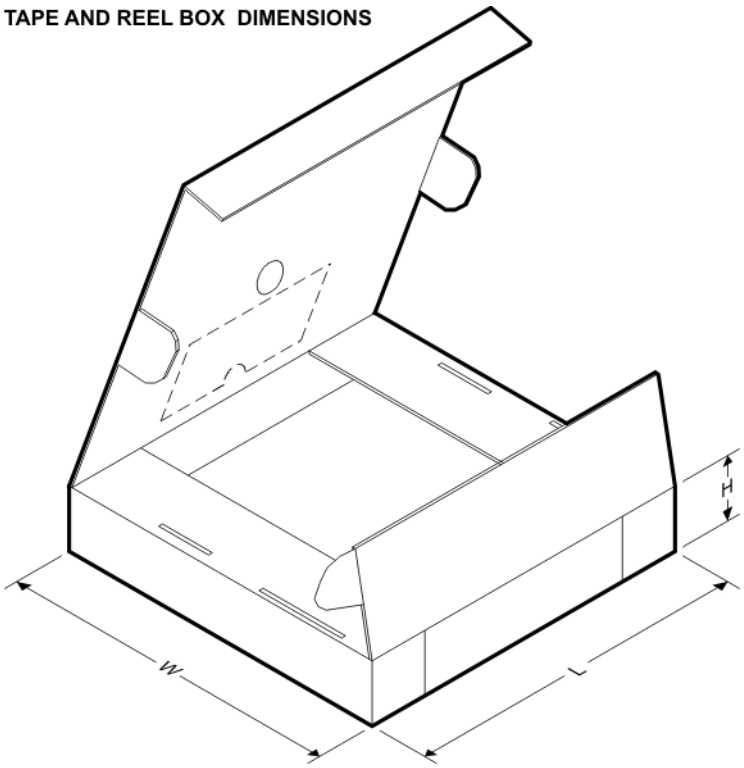
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA0233DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA0233DGQR	HVSSOP	DGQ	10	2500	358.0	335.0	35.0

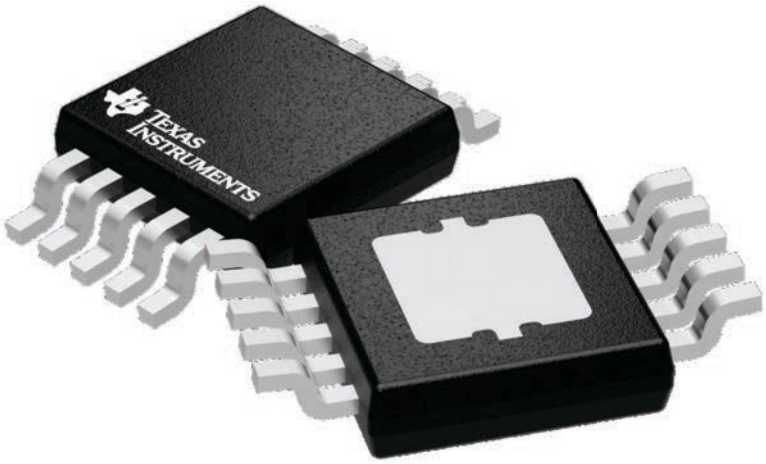
GENERIC PACKAGE VIEW

DGQ 10

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

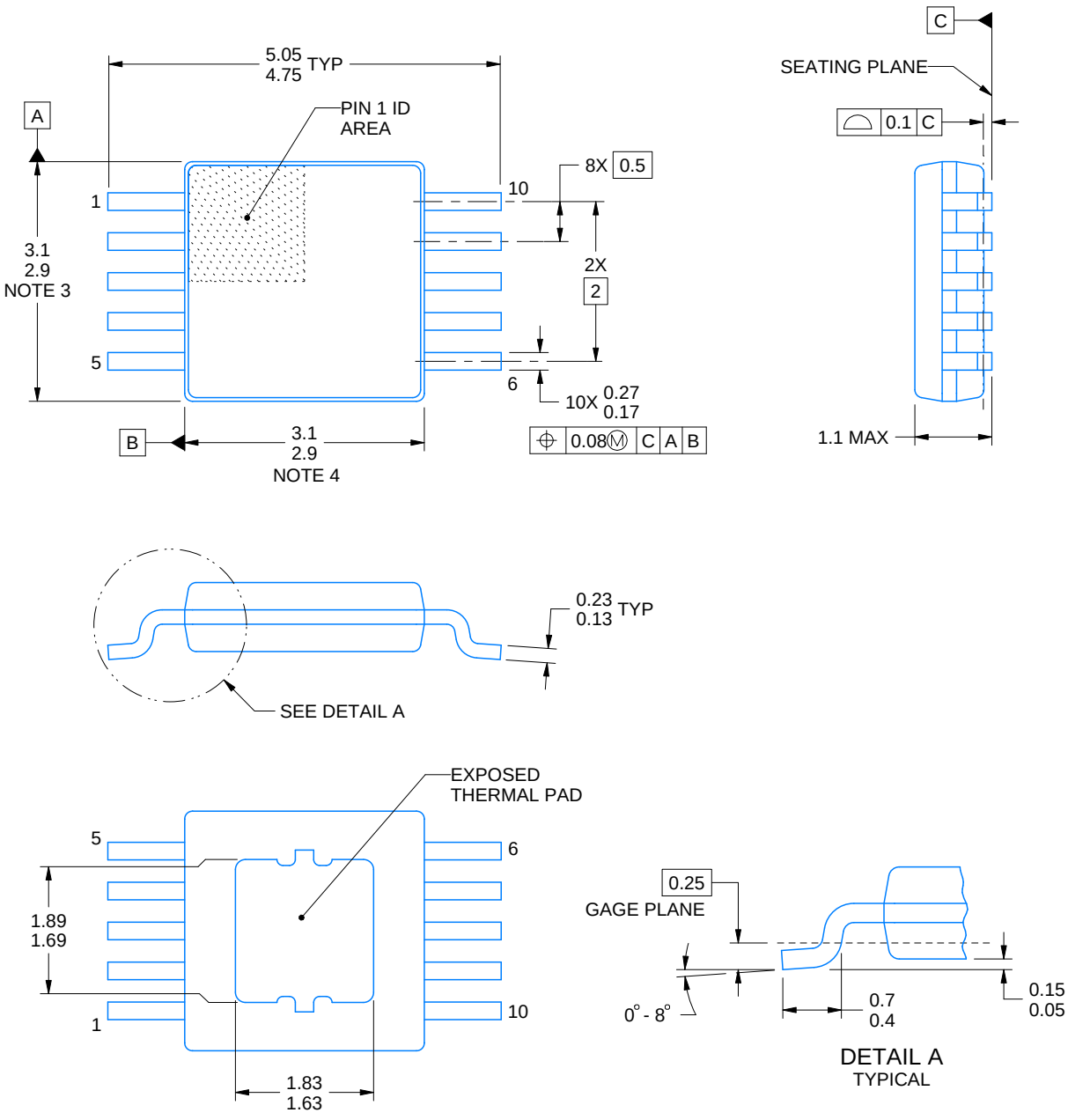
4224775/A

PACKAGE OUTLINE

DGQ0010D

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



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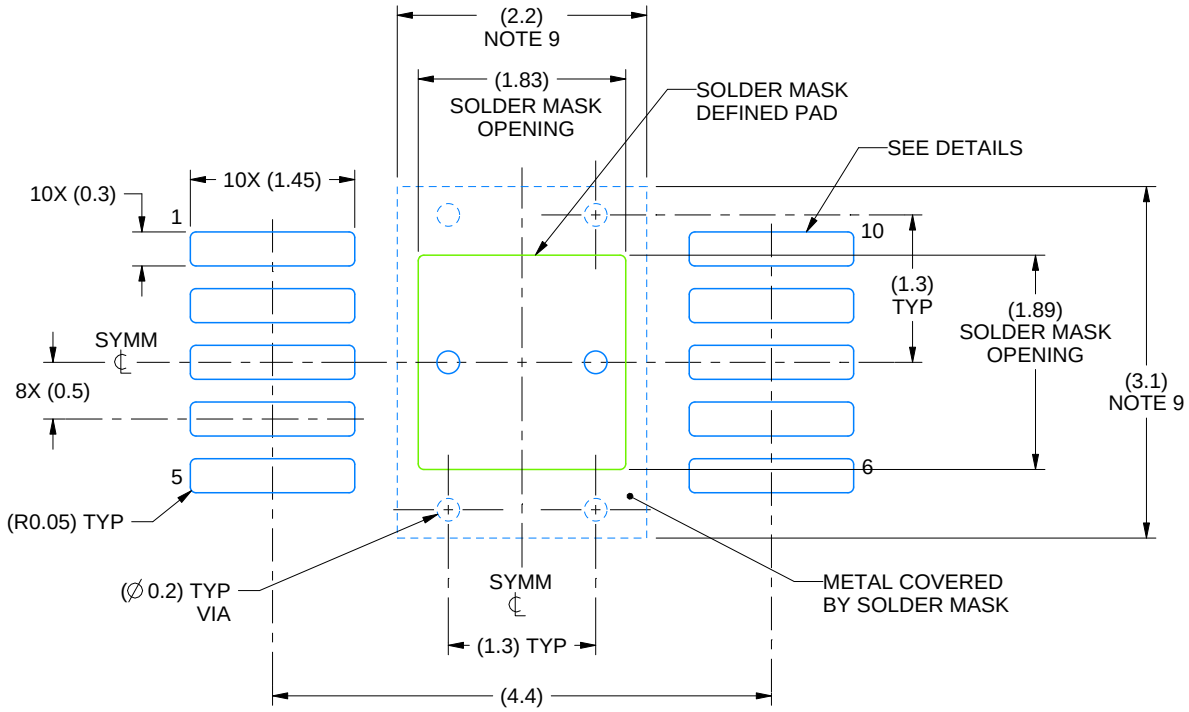
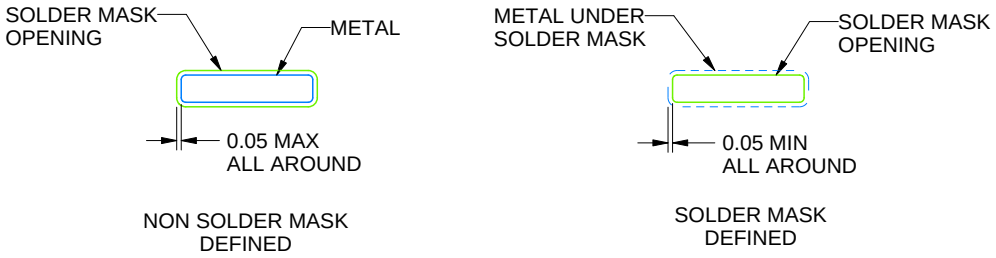
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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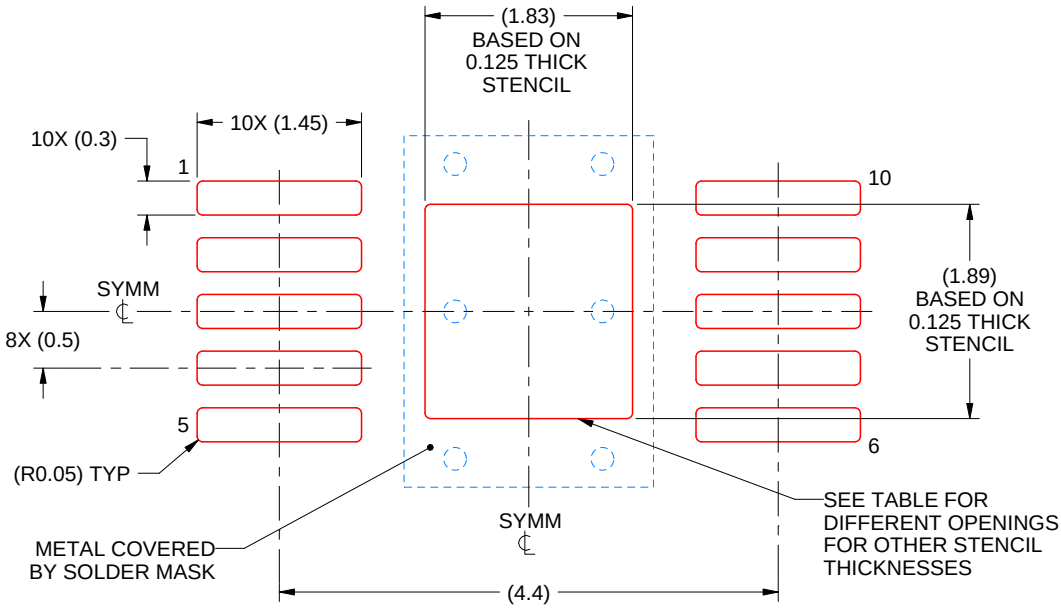
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.05 X 2.11
0.125	1.83 X 1.89 (SHOWN)
0.150	1.67 X 1.73
0.175	1.55 X 1.60

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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