20-W STEREO CLASS-D AUDIO POWER AMPLIFIER

FEATURES

- **Qualified for Automotive Applications**
- **20 W/Channel Into an 8-Ω Load From an 18-V Supply**
- **10 W/Channel Into an 8-Ω Load From a 12-V Supply**
- **15 W/Channel Into an 4-Ω Load From a 12-V Supply**
- **Operates From 10 V to 26 V**
- **92% Efficient Class-D Operation Eliminates Need for Heat Sinks**
- **Four Selectable Fixed-Gain Settings**
- **Differential Inputs**
- **Thermal and Short-Circuit Protection With Auto-Recovery Feature**
- **Clock Output for Synchronization With Multiple Class-D Devices**
- **Surface Mount 7-mm × 7-mm 48-pin QFN (RGZ) Package**

APPLICATIONS

- **Televisions**

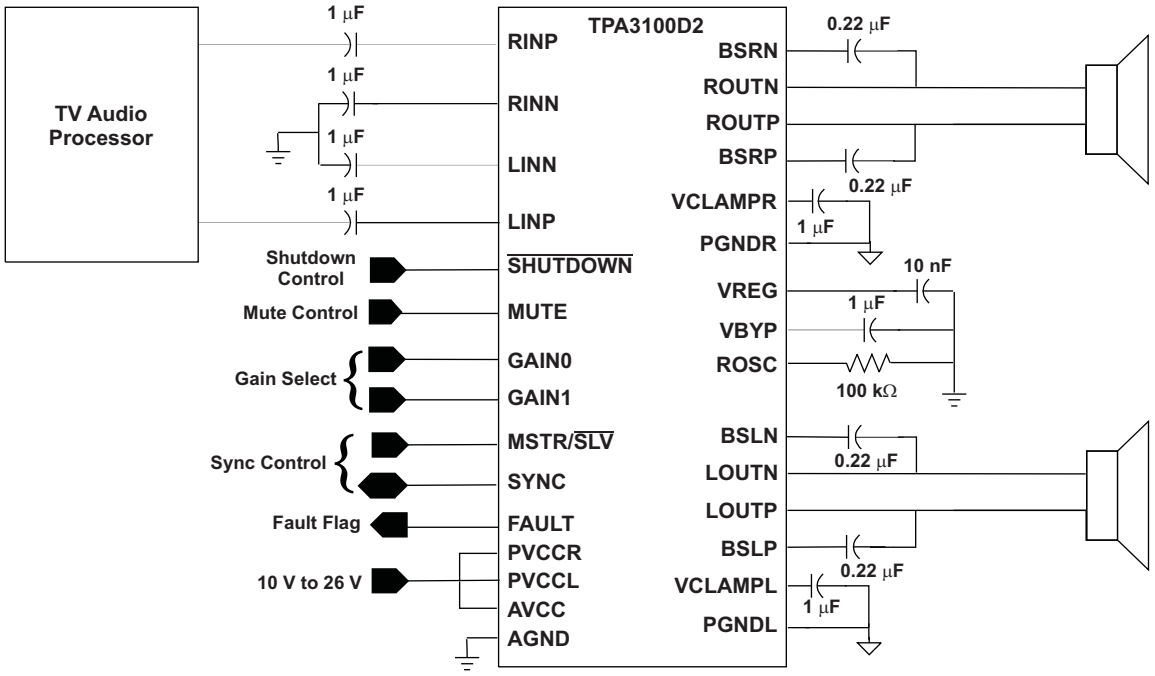
DESCRIPTION

The TPA3100D2 is a 20-W per channel, efficient, class-D audio power amplifier for driving bridged-tied stereo speakers. The TPA3100D2 can drive stereo speakers as low as 4 Ω. The high efficiency of the TPA3100D2, 92%, eliminates the need for an external heat sink when playing music.

The gain of the amplifier is controlled by two gain select pins. The gain selections are 20 dB, 26 dB, 32 dB, or 36 dB.

The outputs are fully protected against shorts to GND, V_{CC}, and output-to-output shorts with an auto-recovery feature and monitor output.

Simplified Application Circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGZ	Reel of 2500	TPA3100D2IRGZRQ1	TPA3100D2I

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

V_{CC}	Supply voltage range	AVCC, PVCC	–0.3 V to 30 V
V_I	Input voltage range	$\overline{\text{SHUTDOWN}}$, MUTE	–0.3 V to V_{CC} + 0.3 V
		GAIN0, GAIN1, RINN, RINP, LINN, LINP, MSTR/$\overline{\text{SLV}}$, SYNC	–0.3 V to VREG + 0.5 V
	Continuous total power dissipation		See Dissipation Ratings Table
T_A	Operating free-air temperature range		–40°C to 85°C
T_J	Operating junction temperature range(2)		–40°C to 150°C
T_{stg}	Storage temperature range		–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C
R_{Load}	Load resistance		3.2 Ω Minimum
	Electrostatic discharge	Human-Body Model (3) (all pins)	2 kV
		Machine Model (4) (all pins)	150 V
		Charged-Device Model (5) (all pins)	750 V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The TPA3100D2 incorporates an exposed thermal pad on the underside of the chip. This acts as a heatsink, and it must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in the device going into thermal protection shutdown. See TI Technical Brief SLMA002 for more information about using the thermal pad.
(3) In accordance with AEC Q100, Test method Q100-002
(4) In accordance with AEC Q100, Test method Q100-003
(5) In accordance with AEC Q100, Test method Q100-011

TYPICAL DISSIPATION RATINGS

PACKAGE	POWER RATING $T_A \le 25°C$	DERATING FACTOR $T_A > 25°C$	POWER RATING $T_A = 70°C$	POWER RATING $T_A = 85°C$
48-pin RGZ (QFN)	4.63 W	37 mW/°C(1)	2.96 W	2.41 W

(1) This data was taken using 1-oz trace and copper pad that is soldered directly to a JEDEC standard high-K PCB. The thermal pad must be soldered to a thermal land on the printed-circuit board. See TI Technical Brief SLMA002 for more information about using the thermal pad.

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RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CC}	Supply voltage	PVCC, AVCC	10	26	V
V_{IH}	High-level input voltage	$\overline{SHUTDOWN}$, MUTE, GAIN0, GAIN1, MSTR/$\overline{SLV}$, SYNC	2		V
V_{IL}	Low-level input voltage	$\overline{SHUTDOWN}$, MUTE, GAIN0, GAIN1, MSTR/$\overline{SLV}$, SYNC		0.8	V
I_{IH}	High-level input current	$\overline{SHUTDOWN}$, $V_I = V_{CC}$, V_{CC} = 24 V		125	µA
		MUTE, $V_I = V_{CC}$, V_{CC} = 24 V		75	
		GAIN0, GAIN1, MSTR/$\overline{SLV}$, SYNC, V_I = VREG, V_{CC} = 24 V		2	
I_{IL}	Low-level input current	$\overline{SHUTDOWN}$, V_I = 0, V_{CC} = 24 V		2	µA
		SYNC, MUTE, GAIN0, GAIN1, MSTR/$\overline{SLV}$, V_I = 0 V, V_{CC} = 24 V		1	
V_{OH}	High-level output voltage	FAULT, I_{OH} = 1 mA	VREG – 0.6		V
V_{OL}	Low-level output voltage	FAULT, I_{OL} = –1 mA		AGND + 0.4	V
f_{OSC}	Oscillator frequency	R_{osc} resistor = 100 kΩ, MSTR/$\overline{SLV}$ = 2 V	200	300	kHz
T_A	Operating free-air temperature		–40	85	°C

DC CHARACTERISTICS

T_A = 25°C, V_{CC} = 24 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
| V_{OS} |	Class-D output offset voltage (measured differentially)	V_I = 0 V, Gain = 36 dB			5	50	mV
	Bypass reference for input amplifier	VBYP, no load		1.1	1.25	1.45	V
	4-V internal supply voltage	VREG, no load, V_{CC} = 10 V to 26 V		3.75	4	4.25	V
PSRR	DC power-supply rejection ratio	V_{CC} = 12 V to 24 V, inputs ac coupled to AGND, Gain = 36 dB			–70		dB
I_{CC}	Quiescent supply current	$\overline{SHUTDOWN}$ = 2 V, MUTE = 0 V, No load, filter, or snubber			22	26.5	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SHUTDOWN}$ = 0.8 V, No load, filter, or snubber			180	250	µA
$I_{CC(MUTE)}$	Quiescent supply current in mute mode	MUTE = 2 V, No load, filter, or snubber			8	10	mA
$r_{DS(on)}$	Drain-source on-state resistance	V_{CC} = 12 V, I_O = 500 mA, T_J = 25°C	High side		200		mΩ
			Low side		200		
			Total		400	500	
G	Gain	GAIN1 = 0.8 V	GAIN0 = 0.8 V	19	20	21	dB
			GAIN0 = 2 V	25	26	27	
		GAIN1 = 2 V	GAIN0 = 0.8 V	31	32	33	
			GAIN0 = 2 V	35	36	37	
	Gain matching	Between channels			2		%
t_{ON}	Turn-on time	$C_{(VBYP)}$ = 1 µF, $\overline{SHUTDOWN}$ = 2 V			25		ms
t_{OFF}	Turn-off time	$C_{(VBYP)}$ = 1 µF, $\overline{SHUTDOWN}$ = 0.8 V			0.1		ms

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DC CHARACTERISTICS

T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured differentially)	V_I = 0 V, Gain = 36 dB			5	50	mV
	Bypass reference for input amplifier	VBYP, No load		1.1	1.25	1.45	V
	4-V internal supply voltage	VREG, No load		3.75	4	4.25	V
PSRR	DC power-supply rejection ratio	V_{CC} = 12 V to 24 V, Inputs ac-coupled to AGND, Gain = 36 dB			-70		dB
I_{CC}	Quiescent supply current	$\overline{SHUTDOWN}$ = 2 V, MUTE = 0 V, No load, filter, or snubber			18	22.5	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SHUTDOWN}$ = 0.8 V, No load, filter, or snubber			80	200	µA
$I_{CC(MUTE)}$	Quiescent supply current in mute mode	MUTE = 2 V, no load, filter, or snubber			7	9	mA
$r_{DS(on)}$	Drain-source on-state resistance	V_{CC} = 12 V, I_O = 500 mA, T_J = 25°C	High side		200		mΩ
			Low side		200		
			Total		400	500	
G	Gain	GAIN1 = 0.8 V	GAIN0 = 0.8 V	19	20	21	dB
			GAIN0 = 2 V	25	26	27	
		GAIN1 = 2 V	GAIN0 = 0.8 V	31	32	33	
			GAIN0 = 2 V	35	36	37	
t_{ON}	Turn-on time	$C_{(VBYP)}$ = 1 µF, $\overline{SHUTDOWN}$ = 2 V			25		ms
t_{OFF}	Turn-off time	$C_{(VBYP)}$ = 1 µF, $\overline{SHUTDOWN}$ = 0.8 V			0.1		ms

AC CHARACTERISTICS

T_A = 25°C, V_{CC} = 24 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Supply ripple rejection	200-mV_{PP} ripple from 20 Hz to 1 kHz, Gain = 20 dB, Inputs ac-coupled to AGND		–70		dB
P_O	Continuous output power	THD+N = 7%, f = 1 kHz, V_{CC} = 18 V		20.6		W
		THD+N = 10%, f = 1 kHz, V_{CC} = 18 V		21.8		
THD+N	Total harmonic distortion + noise	V_{CC} = 18 V, f = 1 kHz, P_O = 10 W (half power)		0.11		%
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		100		µV
				–80		dBV
	Crosstalk	V_O = 1 Vrms, Gain = 20 dB, f = 1 kHz		–92		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		102		dB
	Thermal trip point			150		°C
	Thermal hysteresis			30		°C

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AC CHARACTERISTICS

T_A = 25°C, V_{CC} = 12 V, R_L = 8 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{SVR}	Supply ripple rejection	200-mV_{PP} ripple from 20 Hz to 1 kHz, Gain = 20 dB, Inputs ac-coupled to AGND		–70		dB
P_O	Continuous output power	THD+N = 7%, f = 1 kHz		9.4		W
		THD+N = 10%, f = 1 kHz		10		
		THD+N = 7%, f = 1 kHz, R_L = 4 Ω		15.6		
		THD+N = 10%, f = 1 kHz, R_L = 4 Ω		16.4		
THD+N	Total harmonic distortion + noise	R_L = 8 Ω, f = 1 kHz, P_O = 5 W (half power)		0.11		%
		R_L = 4 Ω, f = 1 kHz, P_O = 8 W (half power)		0.15		
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 20 dB		100		µV
				–80		dBV
	Crosstalk	P_o = 1 W, Gain = 20 dB, f = 1 kHz		–94		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 20 dB, A-weighted		98		dB
	Thermal trip point			150		°C
	Thermal hysteresis			30		°C

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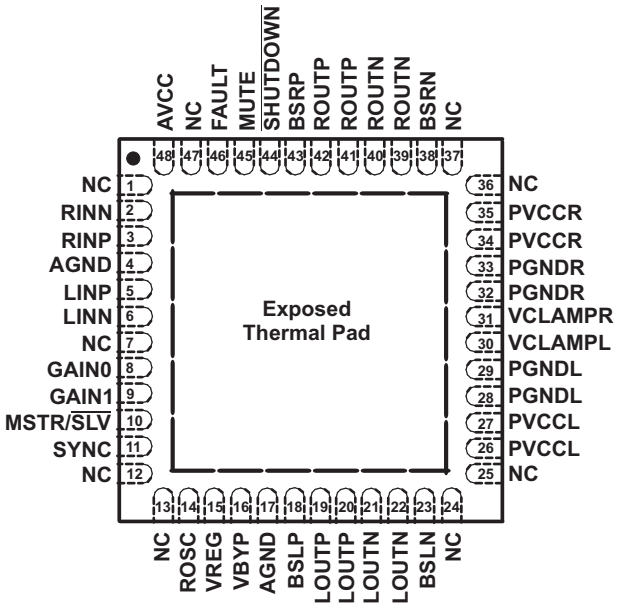
48 PIN, QFN PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	4, 17		Analog ground for digital/analog cells in core.
AVCC	48		High-voltage analog power supply. Not internally connected to PVCCR or PVCCL.
BSLN	23	I/O	Bootstrap I/O for left channel, negative high-side FET
BSLP	18	I/O	Bootstrap I/O for left channel, positive high-side FET
BSRN	38	I/O	Bootstrap I/O for right channel, negative high-side FET
BSRP	43	I/O	Bootstrap I/O for right channel, positive high-side FET
FAULT	46	O	TTL-compatible output. HIGH = short-circuit fault. LOW = no fault. Only reports short-circuit faults. Thermal faults are not reported on this terminal.
GAIN0	8	I	Gain select least significant bit. TTL logic levels with compliance to VREG.
GAIN1	9	I	Gain select most significant bit. TTL logic levels with compliance to VREG.
GND			Ground. Connect to the thermal pad.
LINN	6	I	Negative audio input for left channel. Biased at VREG/2
LINP	5	I	Positive audio input for left channel. Biased at VREG/2
LOUTN	21, 22	O	Class-D 1/2-H-bridge negative output for left channel
LOUTP	19, 20	O	Class-D 1/2-H-bridge positive output for left channel
MSTR/$\overline{\text{SLV}}$	10	I	Master/slave select for determining direction of SYNC terminal. High = master mode, SYNC terminal is an output; low = slave mode, SYNC terminal accepts a clock input. TTL logic levels with compliance to VREG.
MUTE	45	I	Mute signal for quick disable/enable of outputs (high = outputs high-Z, low = outputs enabled). TTL logic levels with compliance to AVCC.
NC	1, 7, 12, 13, 24, 25, 36, 37, 47		No internal connection
PGNDL	28, 29		Power ground for left channel H-bridge
PGNDR	32, 33		Power ground for right channel H-bridge
PVCCL	26, 27		Power supply for left channel H-bridge, not internally connected to PVCCR or AVCC.
PVCCR	34, 35		Power supply for right channel H-bridge, not connected to PVCCL or AVCC
RINN	2	I	Negative audio input for right channel. Biased at VREG/2.

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TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
RINP	3	I	Positive audio input for right channel. Biased at VREG/2.
ROSC	14	I/O	I/O for current setting resistor of ramp generator
ROUTN	39, 40	O	Class-D 1/2-H-bridge negative output for right channel
ROUTP	41, 42	O	Class-D 1/2-H-bridge positive output for right channel
$\overline{\text{SHUTDOWN}}$	44	I	Shutdown signal for IC (LOW = disabled, HIGH = operational). TTL logic levels with compliance to AVCC.
SYNC	11	I/O	Clock input/output for synchronizing multiple class-D devices. Direction determined by MSTR/$\overline{\text{SLV}}$ terminal. Input signal not to exceed VREG.
VBYP	16	O	Reference for preamplifier. Nominally equal to 1.25 V. Also controls start-up time via external capacitor sizing.
VCLAMPL	30		Internally generated voltage supply for left channel bootstrap capacitor
VCLAMPR	31		Internally generated voltage supply for right channel bootstrap capacitor
VREG	15	O	4-V regulated output for use by internal cells, GAINx, MUTE, and MSTR/$\overline{\text{SLV}}$ pins only. Not specified for driving other external circuitry.
Thermal Pad			Connect to AGND and PGND. Should be star point for both grounds. Internal resistive connection to AGND and PGND. Thermal vias on the PCB should connect this pad to a large copper area on an internal or bottom layer for the best thermal performance. *The Thermal Pad must be soldered to the PCB for mechanical reliability.*

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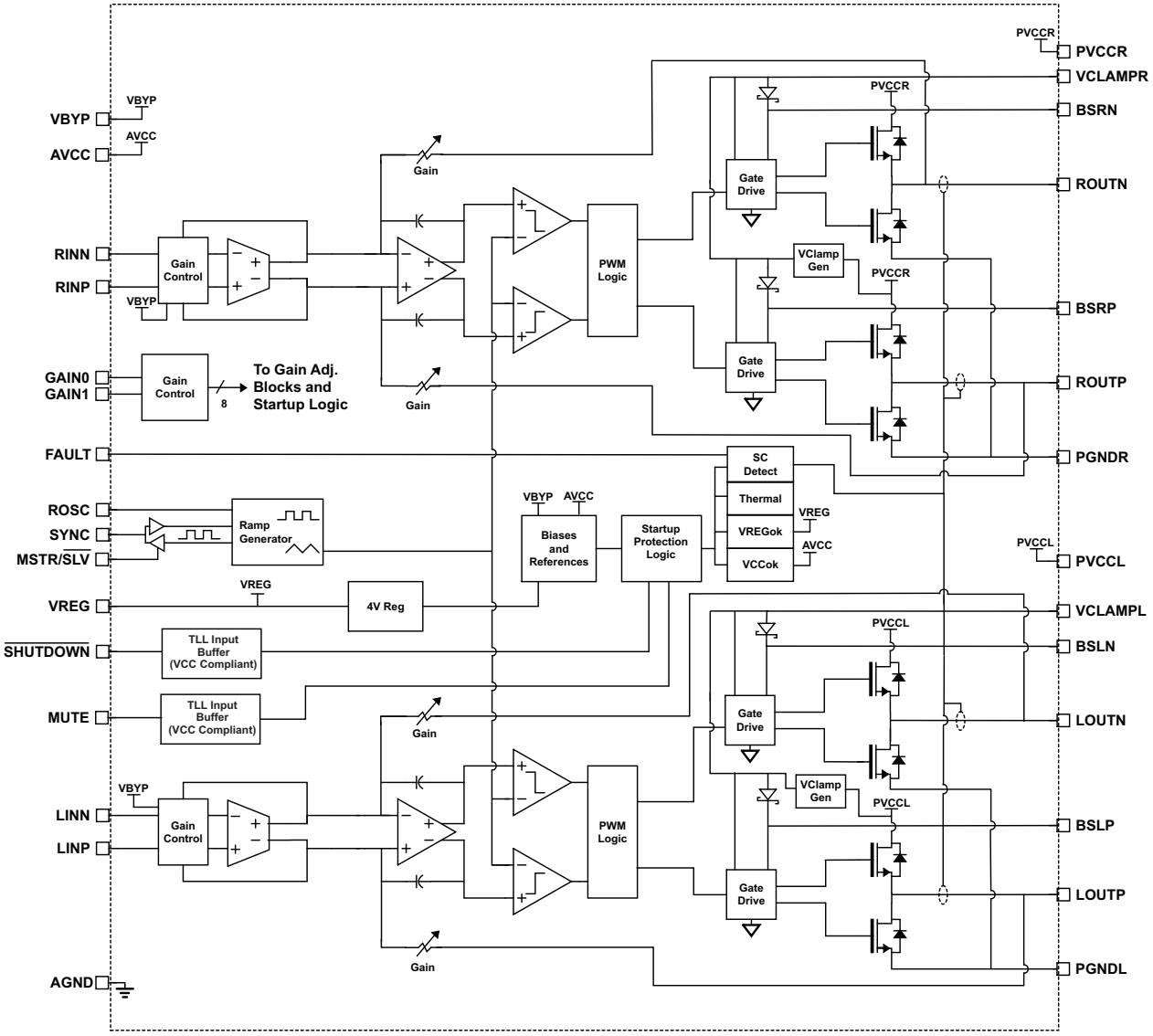
FUNCTIONAL BLOCK DIAGRAM



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TYPICAL CHARACTERISTICS

TABLE OF GRAPHS(1)

			FIGURE
THD+N	Total harmonic distortion + noise	vs Frequency	1, 2, 3, 4
		vs Output power	5, 6, 7, 8
	Closed-loop response	vs Frequency	9, 10
	Output power	vs Supply voltage	11. 12
	Efficiency	vs Output power	13, 14
V_{CC}	Supply current	vs Total output power	15, 16
	Crosstalk	vs Frequency	17, 18
k_{SVR}	Supply ripple rejection ratio	vs Frequency	19, 20

(1) All graphs were measured using the TPA3100D2 EVM.

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TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

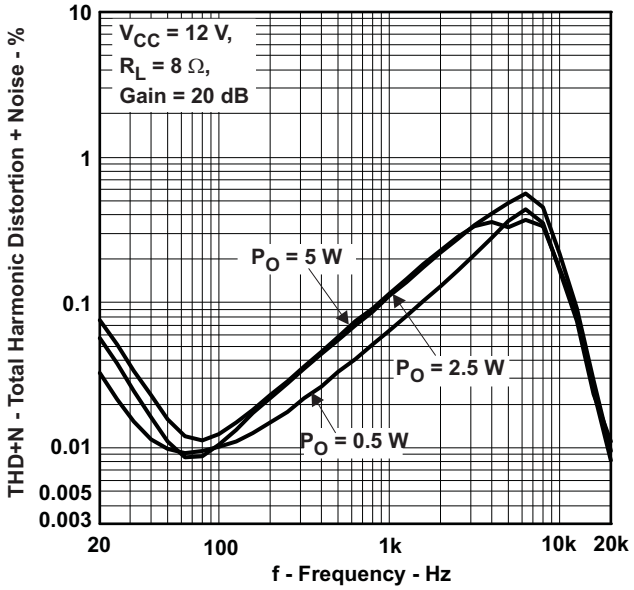

Figure 1.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

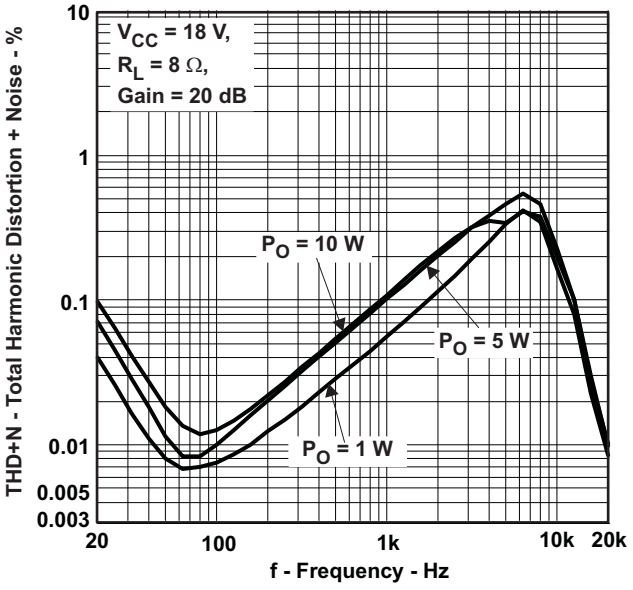

Figure 2.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

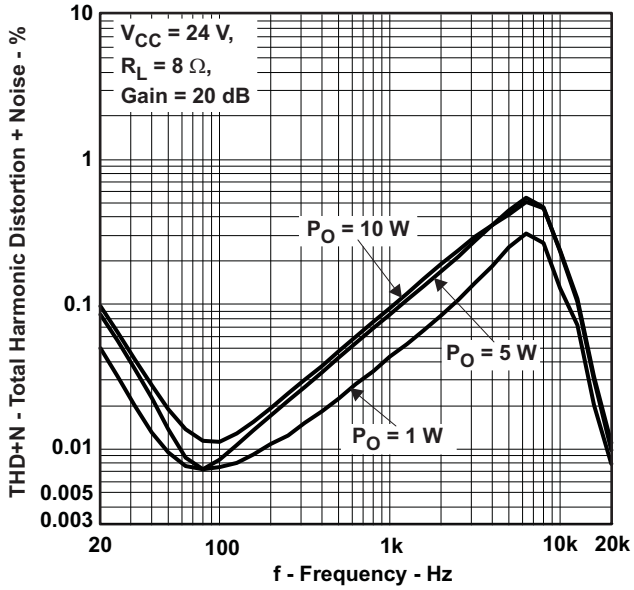

Figure 3.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

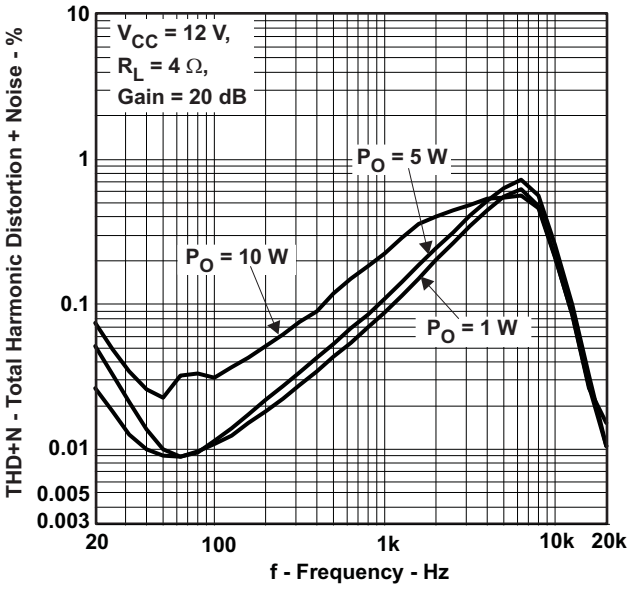

Figure 4.

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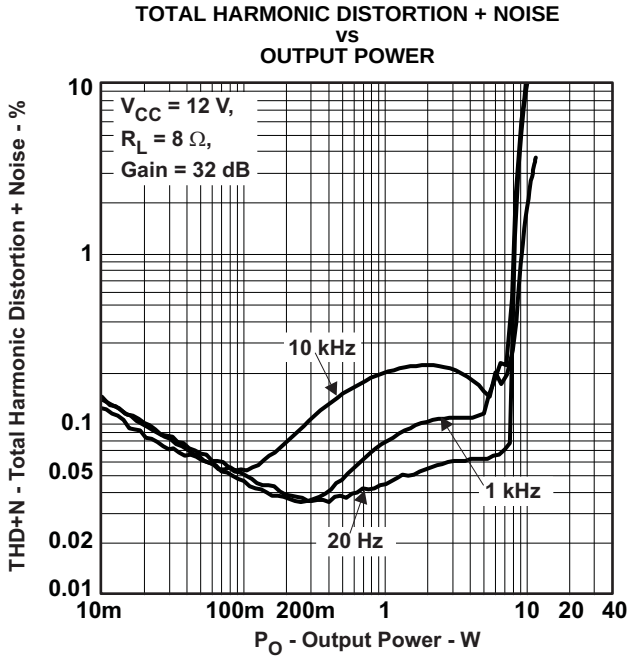

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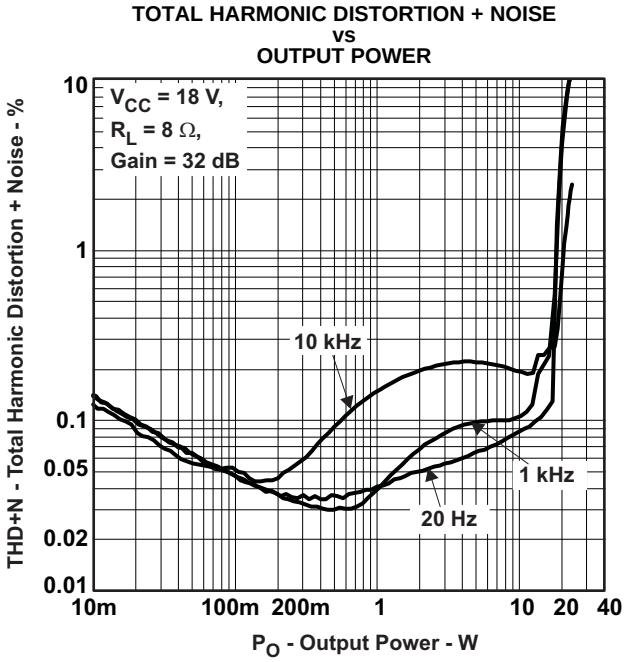

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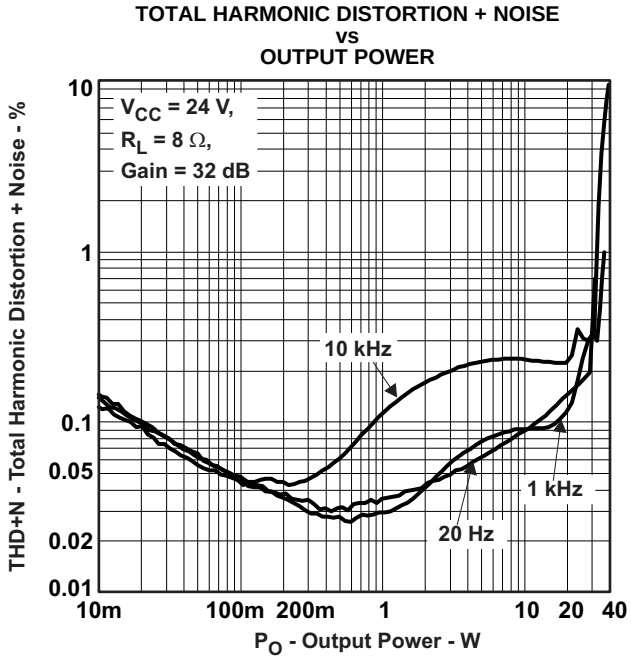

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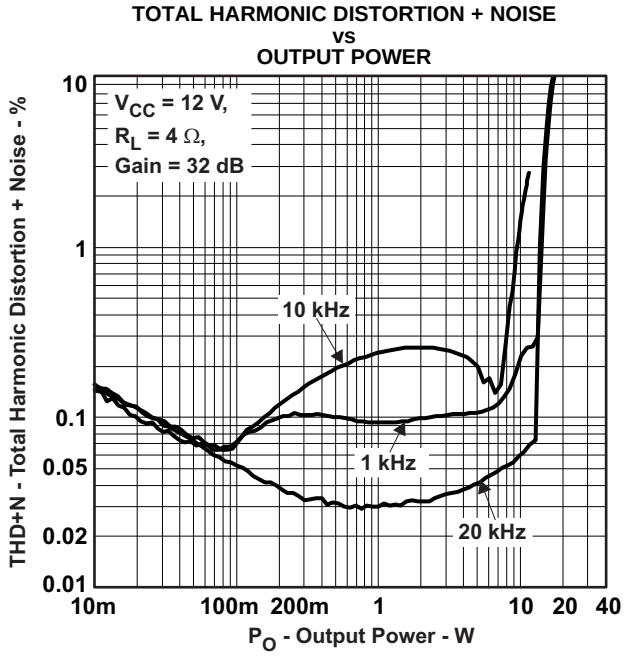

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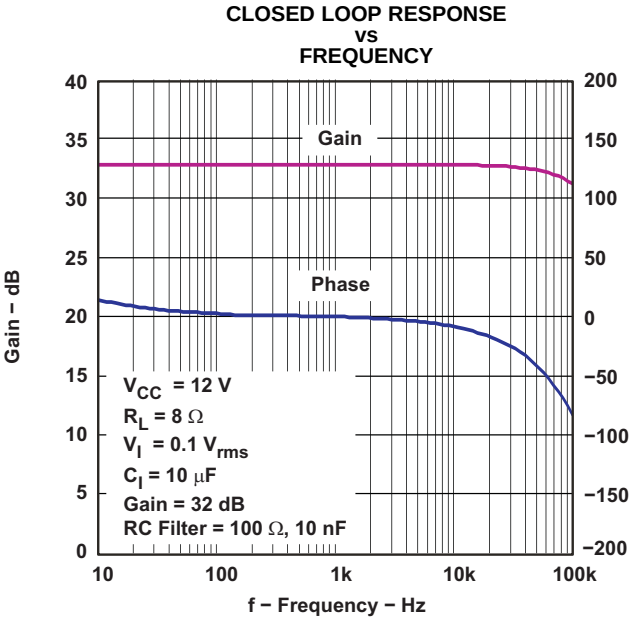

Figure 9.

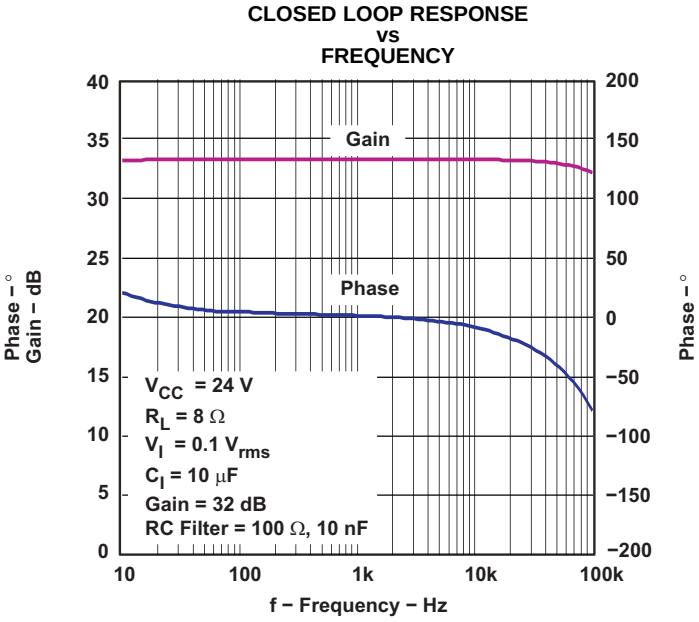

Figure 10.

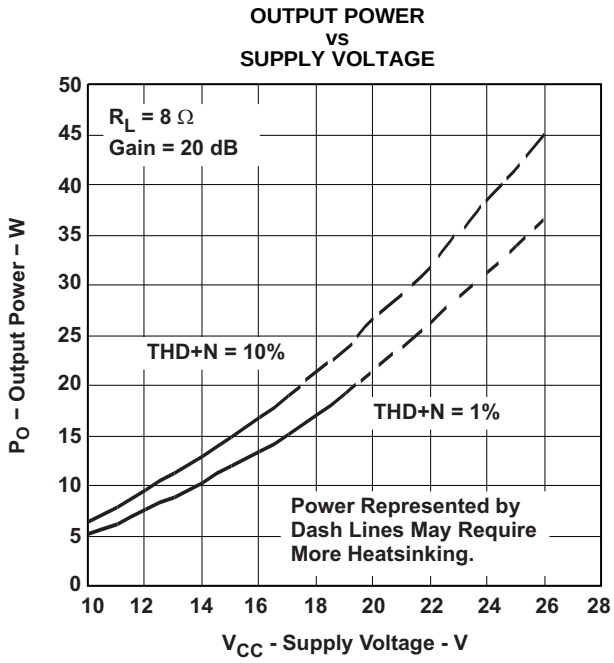

Figure 11.

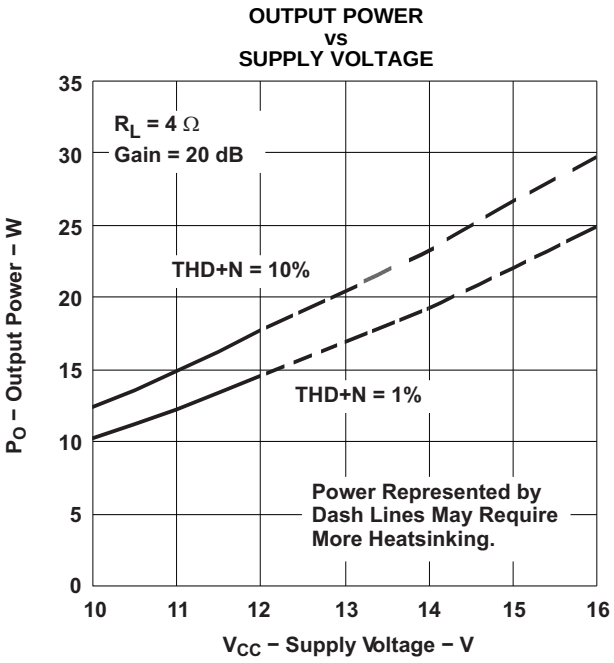

Figure 12.

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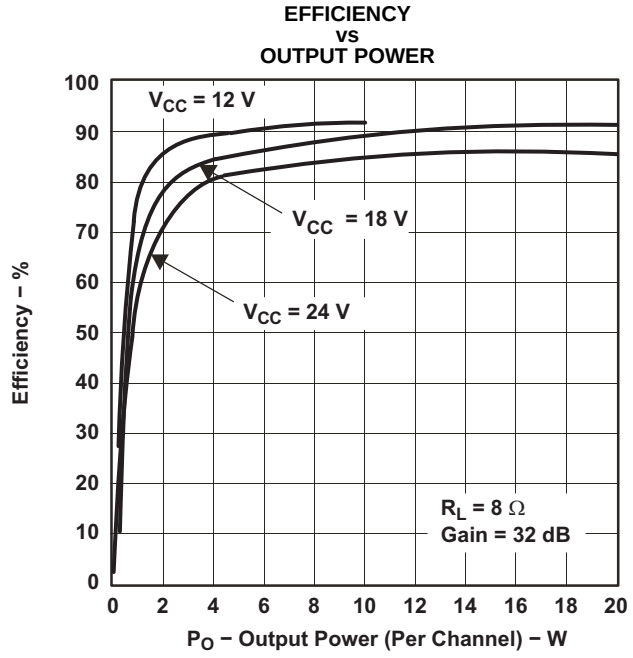

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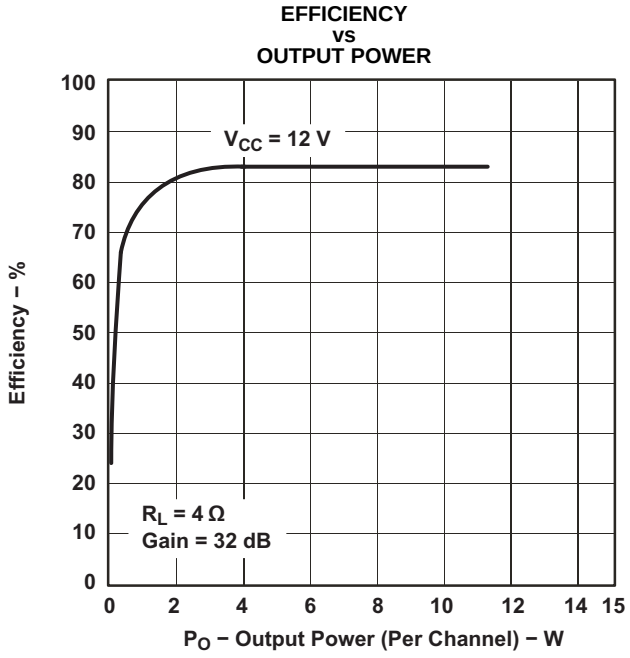

Figure 14.

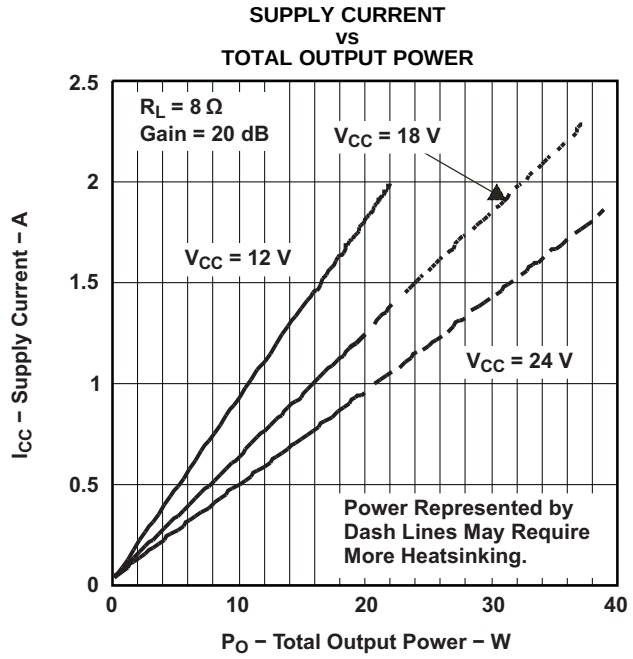

Figure 15.

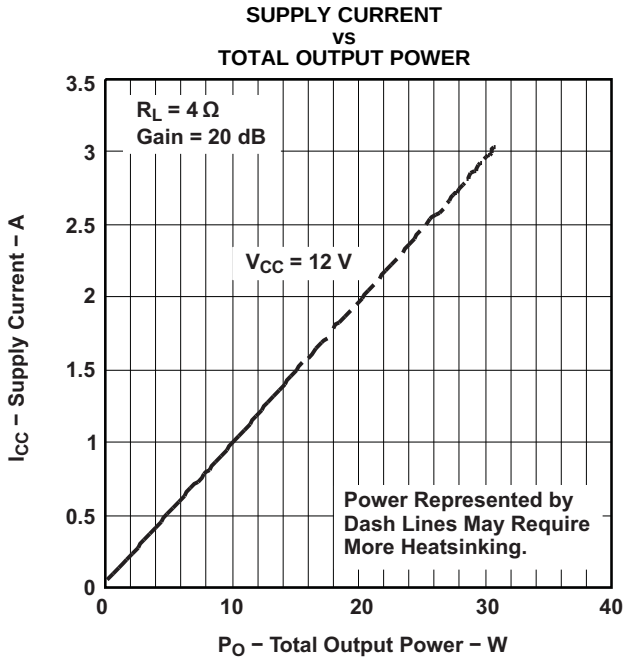

Figure 16.

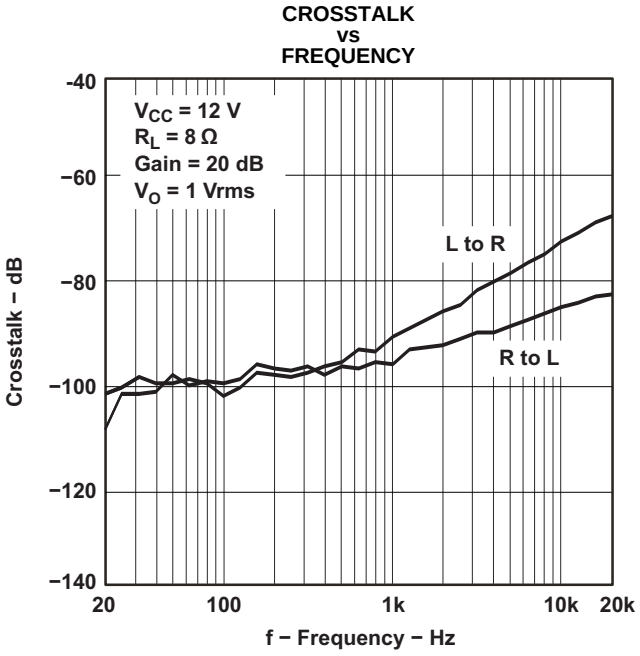

Figure 17.

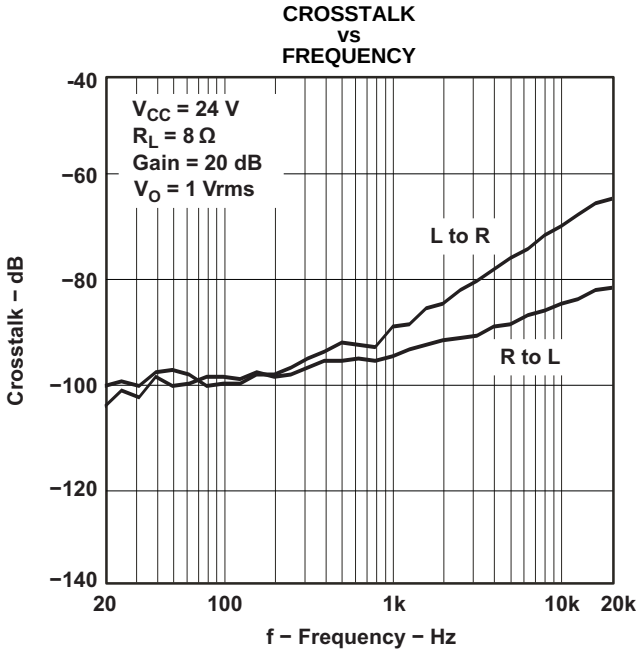

Figure 18.

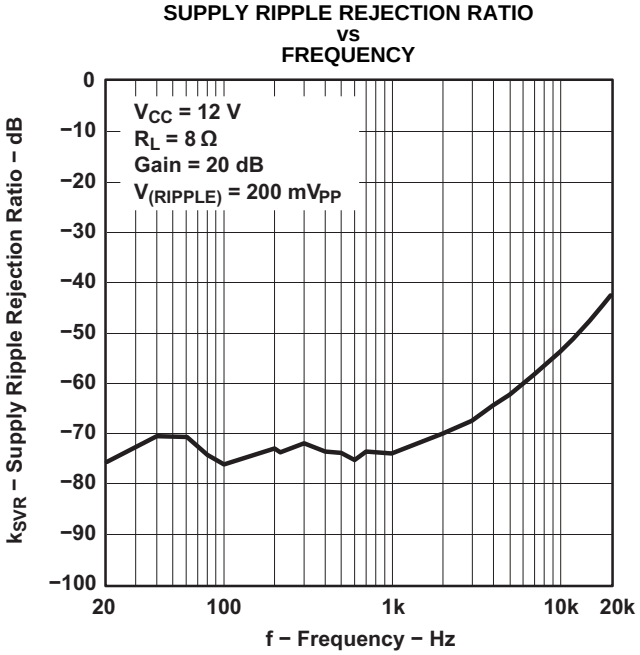

Figure 19.

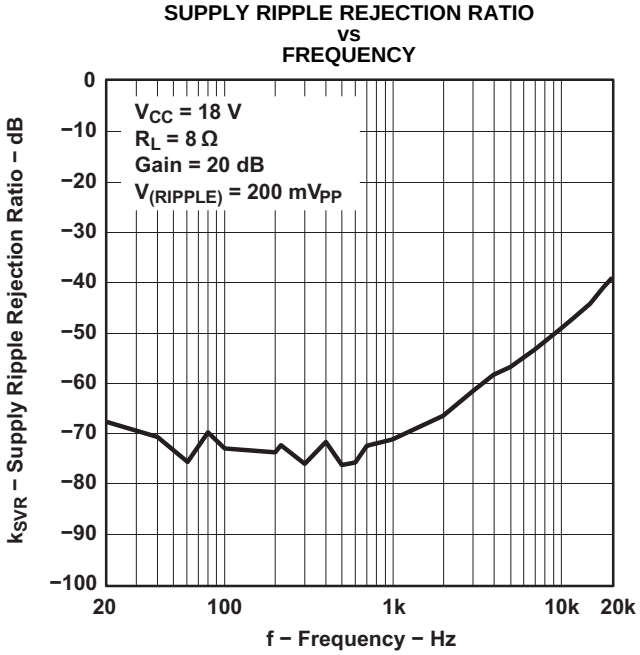

Figure 20.

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APPLICATION INFORMATION

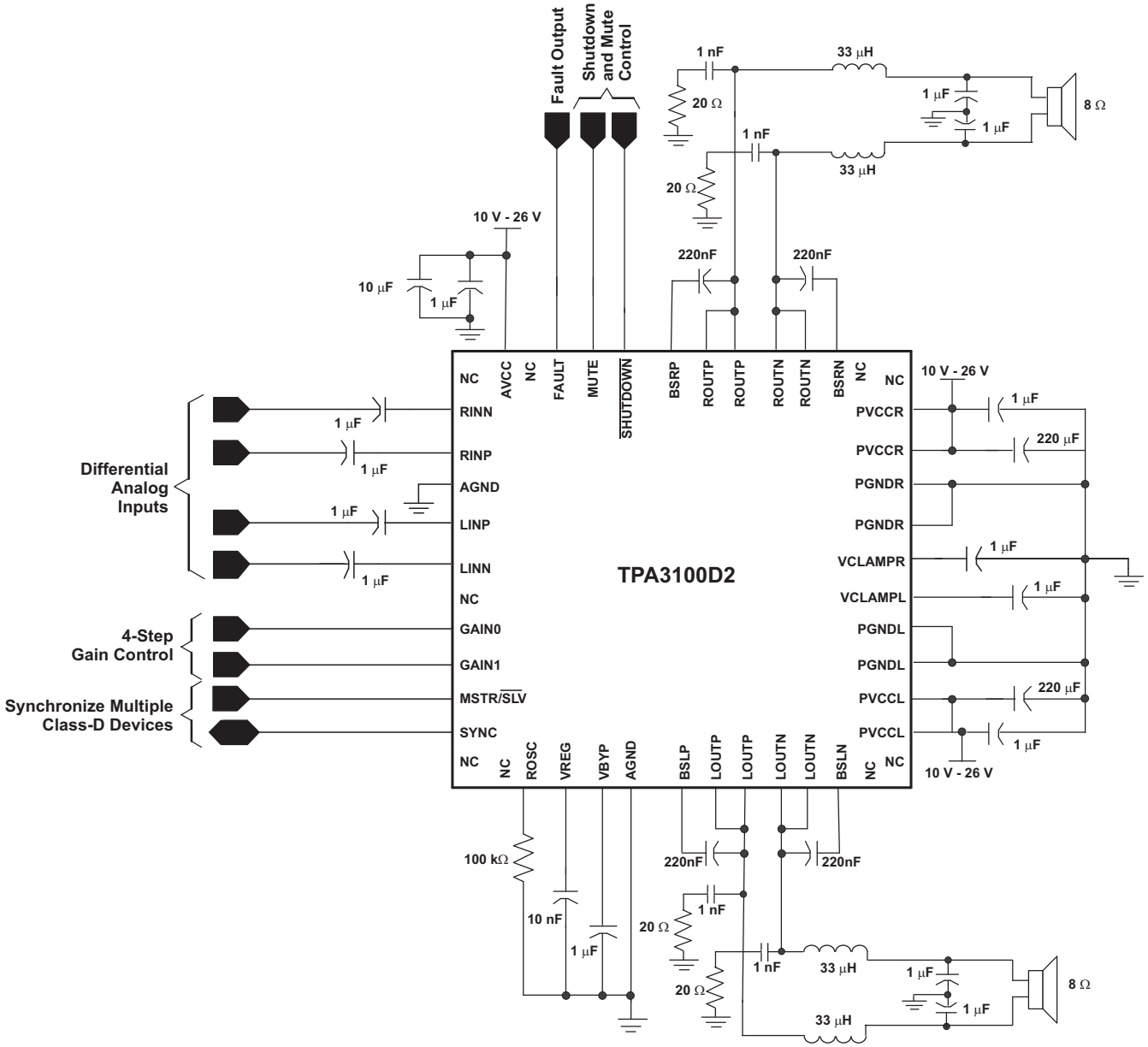

Figure 21. Stereo Class-D With Differential Inputs (QFN)

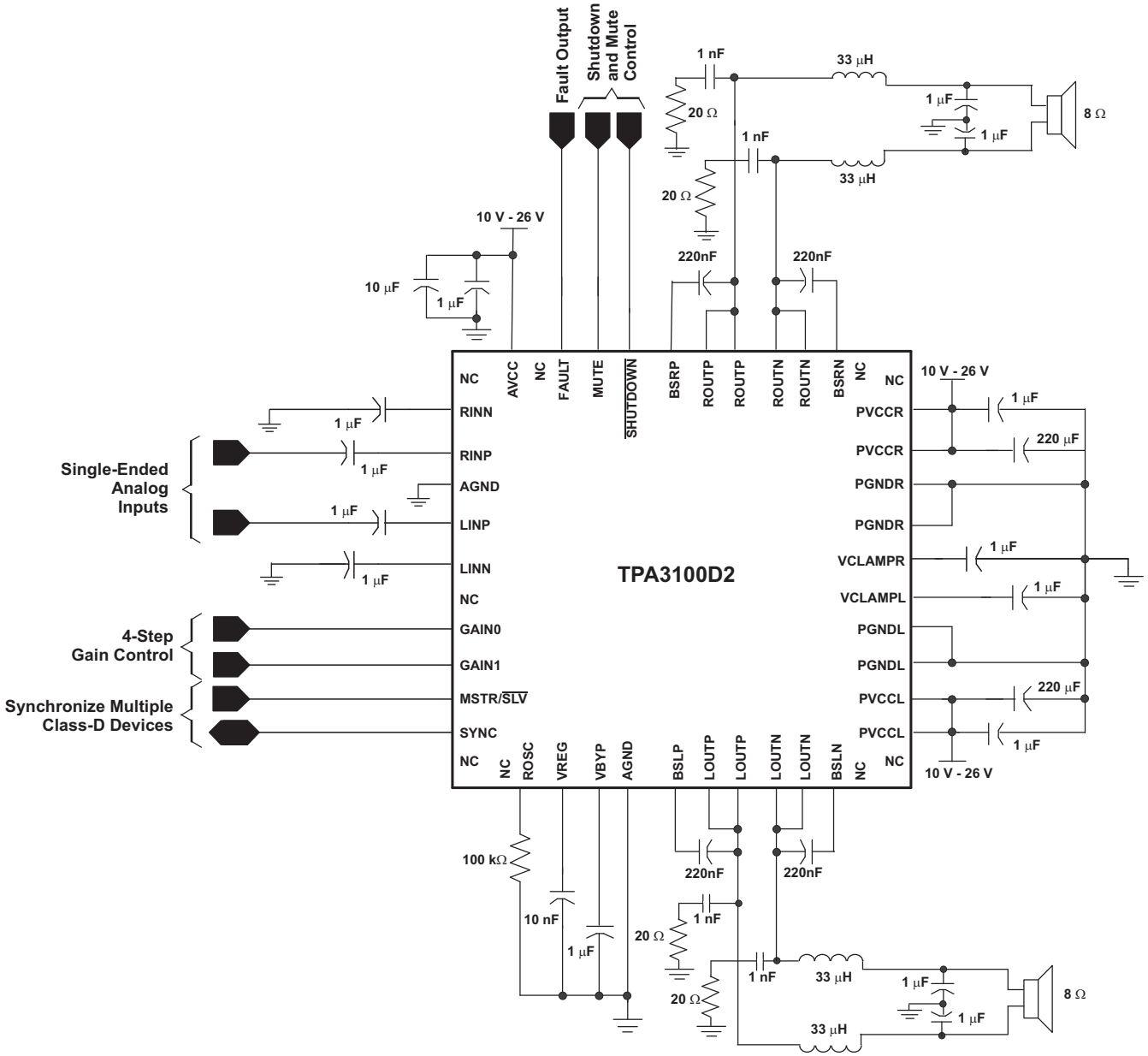

Figure 22. Stereo Class-D With Single-Ended Inputs (QFN)

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Class-D Operation

This section focuses on the class-D operation of the TPA3100D2.

Traditional Class-D Modulation Scheme

The traditional class-D modulation scheme, which is used in the TPA032D0x family, has a differential output in which each output is 180° out of phase and changes from ground to the supply voltage, V_{CC}. Therefore, the differential prefiltered output varies between positive and negative V_{CC}, where filtered 50% duty cycle yields 0 V across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 23. Note that even at an average of 0 V across the load (50% duty cycle), the current to the load is high, causing high loss and, thus, causing a high supply current.

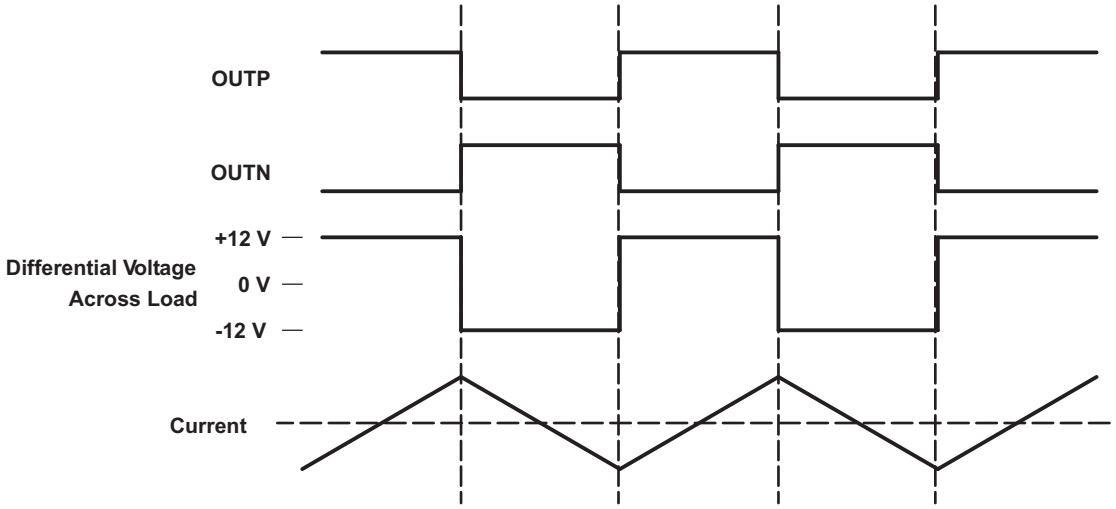

Figure 23. Traditional Class-D Modulation Scheme Output Voltage and Current Waveforms Into an Inductive Load With No Input

TPA3100D2 Modulation Scheme

The TPA3100D2 uses a modulation scheme that still has each output switching from 0 V to the supply voltage. However, OUTP and OUTN are in phase with each other with no input. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load stays at 0 V throughout most of the switching period, greatly reducing the switching current, which reduces I^2R losses in the load.

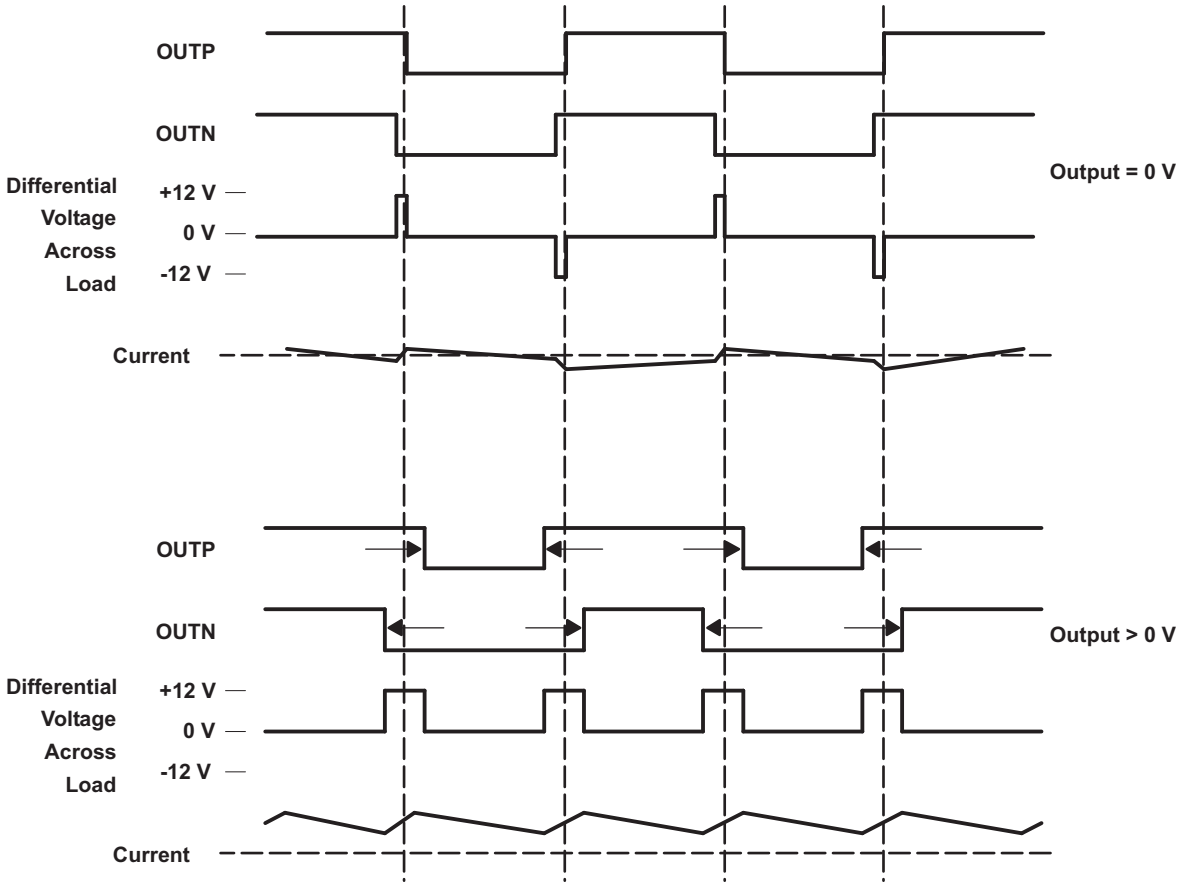

Figure 24. The TPA3100D2 Output Voltage and Current Waveforms Into an Inductive Load

Efficiency: LC Filter Required With Traditional Class-D Modulation Scheme

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is $2 \times V_{CC}$, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA3100D2 modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is V_{CC} instead of $2 \times V_{CC}$. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

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When to Use an Output Filter for EMI Suppression

Design the TPA3100D2 without the filter if the traces from amplifier to speaker are short (<10 cm). Powered speakers, in which the speaker is in the same enclosure as the amplifier, are a typical application for class-D without a filter.

Most applications require a ferrite bead filter. The ferrite filter reduces EMI around 1 MHz and higher (FCC and CE only test radiated emissions greater than 30 MHz). When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

Use an LC output filter if there are low-frequency (<1 MHz) EMI-sensitive circuits and/or there are long wires from the amplifier to the speaker.

When both an LC filter and a ferrite bead filter are used, the LC filter should be placed as close as possible to the IC followed by the ferrite bead filter.

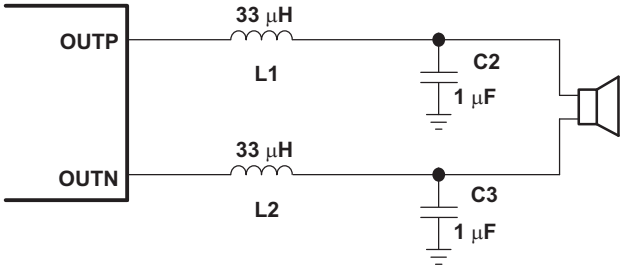

Figure 25. Typical LC Output Filter, Cutoff Frequency of 28 kHz, Speaker Impedance = 8 Ω

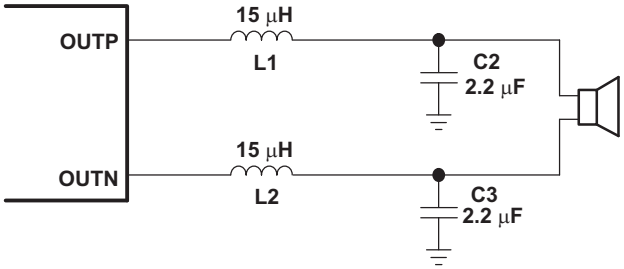

Figure 26. Typical LC Output Filter, Cutoff Frequency of 28 kHz, Speaker Impedance = 4 Ω

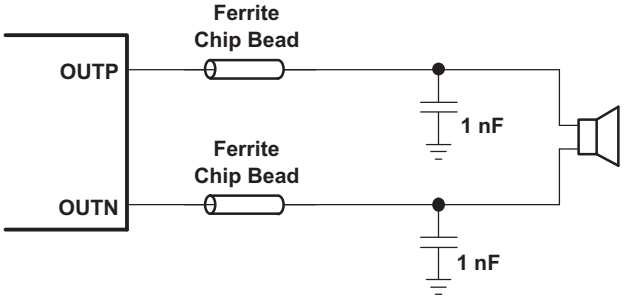

Figure 27. Typical Ferrite Chip Bead Filter (Chip Bead Example: Fair-Rite 2512067007Y3)

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Using the LC filter in Figure 25, the TPA3100D2 EMI EVM passed the FCC Part 15 Class B radiated emissions with 21-inch speaker wires. Quasi-peak measurements were taken for the four standard test configurations, and the TPA3100D2 EVM passed with at least 17-dB margin. A plot of the peak measurement for the horizontal rear configuration is shown in Figure 28.

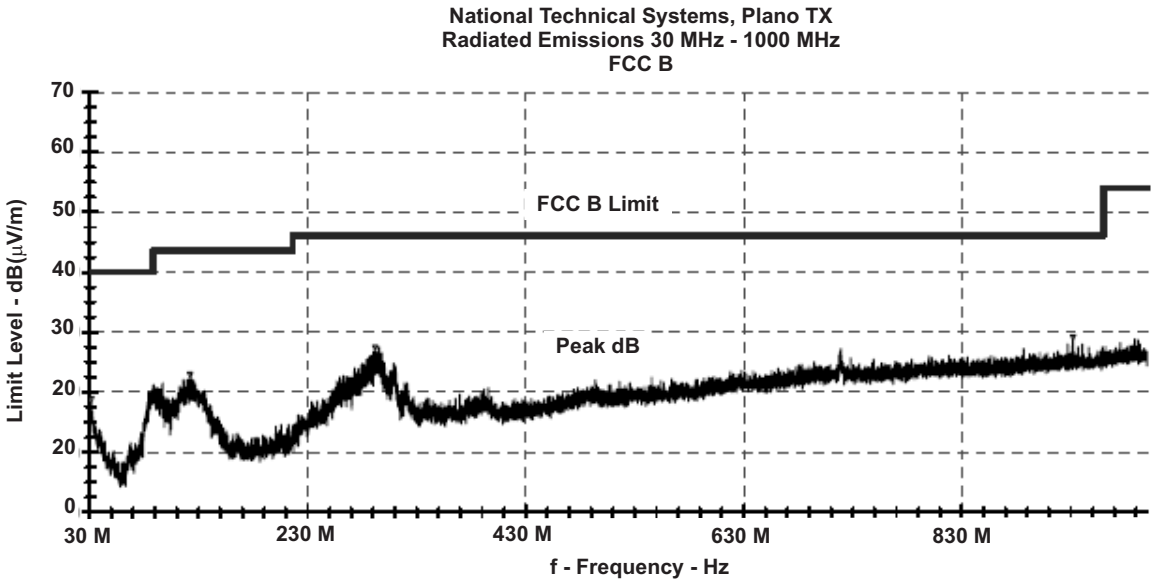

Figure 28. Radiated Emissions Prescan 30 MHz to 1000 MHz

Inductors used in LC filters must be chosen carefully. A significant change in inductance at the peak output current of the TPA3100D2 causes increased distortion. The change of inductance at currents up to the peak output current must be less than 0.1 µH per amp to avoid this distortion. Also note that smaller inductors than 33 µH may cause an increase in distortion above what is shown in Figure 1 through Figure 8.

Capacitors used in LC filters must also be chosen carefully. A significant change in capacitance at the peak output voltage of the TPA3100D2 causes increased distortion. LC filter capacitors should have dc voltage ratings at least twice the peak application voltage (the power-supply voltage) and should be made of X5R or better material. In all cases avoid using capacitors with loose temperature ratings, such as Y5V.

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Adaptive Dynamic Range Control

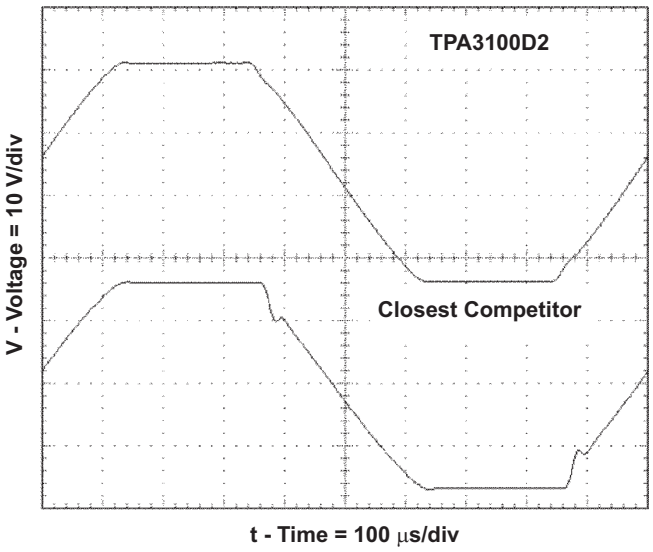

Figure 29. 1-kHz Sine Output at 10% THD+N

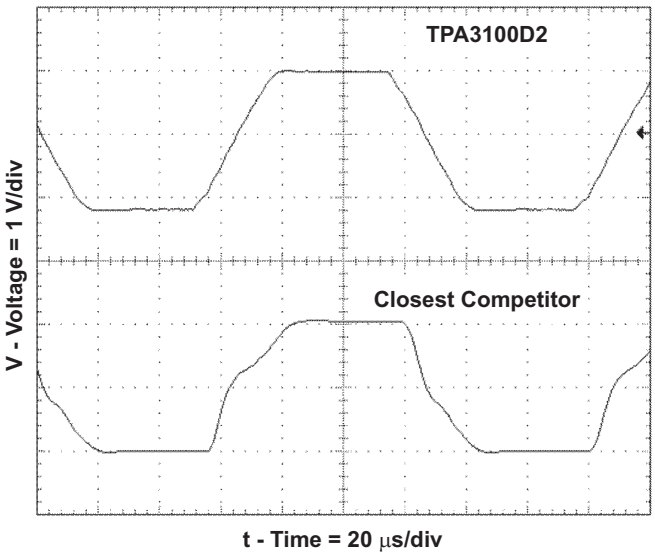

Figure 30. 8-kHz Sine Output at 10% THD+N

The Texas Instruments patent-pending adaptive dynamic range control (ADRC) technology removes the notch inherent in class-D audio power amplifiers when they come out of clipping. This effect is more severe at higher frequencies as shown in Figure 30.

Gain Setting Via GAIN0 and GAIN1 Inputs

The gain of the TPA3100D2 is set by two input terminals, GAIN0 and GAIN1.

The gains listed in Table 1 are realized by changing the taps on the input resistors and feedback resistors inside the amplifier. This causes the input impedance (Z_I) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part to part is small. However, the input impedance from part to part at the same gain may shift by ±20% due to shifts in the actual resistance of the input resistors.

For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 12.8 kΩ, which is the absolute minimum input impedance of the TPA3100D2. At the lower gain settings, the input impedance could increase as high as 38.4 kΩ

Table 1. Gain Setting

GAIN1	GAIN0	AMPLIFIER GAIN (dB)	INPUT IMPEDANCE (kΩ)
		TYP	TYP
0	0	20	32
0	1	26	16
1	0	32	16
1	1	36	16

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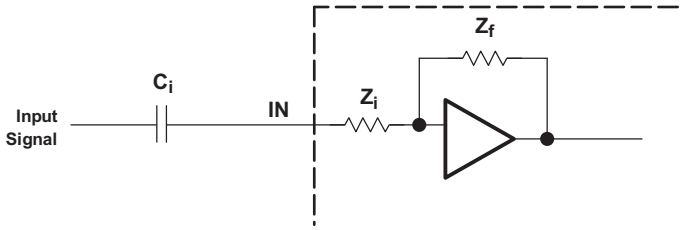
Input Resistance

Changing the gain setting can vary the input resistance of the amplifier from its smallest value, 16 kΩ ± 20%, to the largest value, 32 kΩ ± 20%. As a result, if a single capacitor is used in the input high-pass filter, the –3-dB or cutoff frequency may change when changing gain steps.



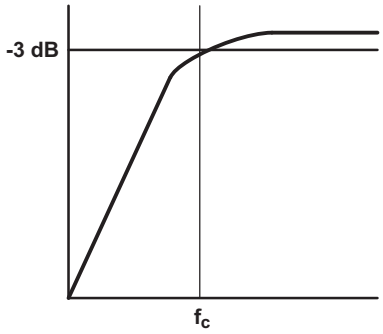
The –3-dB frequency can be calculated using Equation 1. Use the Z_I values given in Table 1.

$$f = \frac{1}{2\pi Z_i C_i} \quad (1)$$

Input Capacitor, C_I

In the typical application, an input capacitor (C_I) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier (Z_I) form a high-pass filter with the corner frequency determined in Equation 2.

$$f_c = \frac{1}{2\pi Z_i C_i} \quad (2)$$



The value of C_I is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Z_I is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 2 is reconfigured as Equation 3.

$$C_i = \frac{1}{2\pi Z_i f_c} \quad (3)$$

In this example, C_I is 0.4 µF; so, one would likely choose a value of 0.47 µF as this value is commonly used. If the gain is known and is constant, use Z_I from Table 1 to calculate C_I. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 2 V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create dc offset voltages and it is important to ensure that boards are cleaned properly.

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Power-Supply Decoupling, C_S

The TPA3100D2 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF to 1 µF placed as close as possible to the device V_{CC} lead works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 220 µF or greater placed near the audio power amplifier is recommended. The 220 µF capacitor also serves as local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC terminals provide the power to the output transistors, so a 220 µF or larger capacitor should be placed on each PVCC terminal. A 10 µF capacitor on the AVCC terminal is adequate.

IC Output Snubbers

The 1-nF capacitors in series with 20-Ω resistors from the outputs of the TPA3100D2 IC to ground are switching snubbers (see Figure 31). They linearize switching transitions and reduce overshoot and ringing. By doing so they improve THD+N, reducing it by a factor near 3 at 1 kHz and 1 W. They also improve EMC by 2 dB to 6 dB at middle frequencies. They increase quiescent current by 5 mA to 15 mA, depending on power-supply voltage.

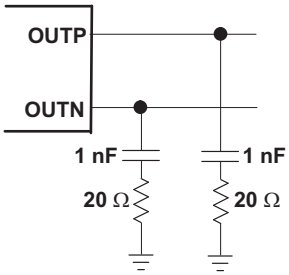

Figure 31. IC Output Snubbers

BSN and BSP Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220-nF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 220-nF capacitor must be connected from xOUTP to BSxx, and one 220-nF capacitor must be connected from xOUTN to BSxx (see the application circuit diagram in Figure 21).

The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

VCLAMP Capacitors

To ensure that the maximum gate-to-source voltage for the NMOS output transistors is not exceeded, two internal regulators clamp the gate voltage. Two 1-µF capacitors must be connected from VCLAMPL (pin 30) and VCLAMPR (pin 31) to ground and must be rated for at least 16 V. The voltages at the VCLAMP terminals may vary with V_{CC} and may not be used for powering any other circuitry.

Internal Regulated 4-V Supply (VREG)

The VREG terminal (pin 15) is the output of an internally generated 4-V supply, used for the oscillator, preamplifier, and gain control circuitry. It requires a 10-nF capacitor placed close to the pin to keep the regulator stable.

This regulated voltage can be used to control GAIN0, GAIN1, MSTR/$\overline{\text{SLV}}$, and MUTE terminals, but should not be used to drive external circuitry.

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VBYP Capacitor Selection

The internal bias generator (VBYP) nominally provides a 1.25-V internal bias for the preamplifier stages. The external input capacitors and this internal reference allow the inputs to be biased within the optimal common-mode range of the input preamplifiers.

The selection of the capacitor value on the VBYP terminal is critical for achieving the best device performance. During power up or recovery from the shutdown state, the VBYP capacitor determines the rate at which the amplifier starts up. When the voltage on the VBYP capacitor equals VBYP, the device starts a 16.4-ms timer. When this timer completes, the outputs start switching. The charge rate of the capacitor is calculated using the standard charging formula for a capacitor, I = C × dV/dT. The charge current is nominally equal to 250 µA and dV is equal to VBYP. For example, a 1-µF capacitor on VBYP would take 5 ms to reach the value of VBYP and begin a 16.4-ms count before the outputs turn on. This equates to a turn-on time of <30 ms for a 1-µF capacitor on the VBYP terminal.

A secondary function of the VBYP capacitor is to filter high-frequency noise on the internal 1.25-V bias generator. A value of at least 0.47 µF is recommended for the VBYP capacitor. For the best power-up and shutdown pop performance, the VBYP capacitor should be greater than or equal to the input capacitors.

ROSC Resistor Selection

The resistor connected to the ROSC terminal controls the class-D output switching frequency using Equation 4:

$$F_{OSC} = \frac{1}{2 \times ROSC \times COSC} \quad (4)$$

COSC is an internal capacitor that is nominally equal to 20 pF. Variation over process and temperature can result in a ±15% change in this capacitor value.

For example, if ROSC is fixed at 100 kΩ, the frequency from device to device with this fixed resistance could vary from 217 kHz to 294 kHz with a 15% variation in the internal COSC capacitor. The tolerance of the ROSC resistor should also be considered to determine the range of expected switching frequencies from device to device. It is recommended that 1% tolerance resistors be used.

Differential Input

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3100D2 with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA3100D2 with a single-ended source, ac ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance.

$\overline{\text{SHUTDOWN}}$ Operation

The TPA3100D2 employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of nonuse for power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state. Never leave $\overline{\text{SHUTDOWN}}$ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown or mute mode prior to removing the power supply voltage.

MUTE Operation

The MUTE pin is an input for controlling the output state of the TPA3100D2. A logic high on this terminal disables the outputs. A logic low on MUTE enables the outputs. This terminal may be used as a quick disable/enable of outputs when changing channels on a television or transitioning between different audio sources.

The MUTE terminal should never be left floating. For power conservation, the $\overline{\text{SHUTDOWN}}$ terminal should be used to reduce the quiescent current to the absolute minimum level.

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The MUTE terminal can also be used with the FAULT output to automatically recover from a short-circuit event. When a short-circuit event occurs, the FAULT terminal transitions high indicating a short-circuit has been detected. When directly connected to MUTE, the MUTE terminal transitions high, and clears the internal fault flag. This causes the FAULT terminal to cycle low, and normal device operation resumes if the short-circuit is removed from the output. If a short remains at the output, the cycle continues until the short is removed.

If external MUTE control is desired, and automatic recovery from a short-circuit event is also desired, an OR gate can be used to combine the functionality of the FAULT output and external MUTE control (see Figure 32).

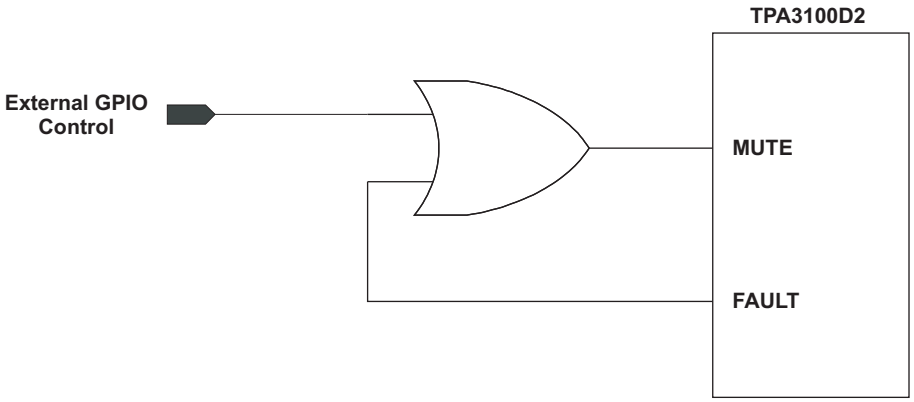

Figure 32. External MUTE Control

MSTR/$\overline{\text{SLV}}$ and SYNC Operation

The MSTR/$\overline{\text{SLV}}$ and SYNC terminals can be used to synchronize the frequency of the class-D output switching. When the MSTR/$\overline{\text{SLV}}$ terminal is high, the output switching frequency is determined by the selection of the resistor connected to the ROSC terminal (see ROSC Resistor Selection). The SYNC terminal becomes an output in this mode, and the frequency of this output is also determined by the selection of the ROSC resistor. This TTL compatible, push-pull output can be connected to another TPA3100D2, configured in the slave mode. The output switching is synchronized to avoid any beat frequencies that could occur in the audio band when two class-D amplifiers in the same system are switching at slightly different frequencies.

When the MSTR/$\overline{\text{SLV}}$ terminal is low, the output switching frequency is determined by the incoming square wave on the SYNC input. The SYNC terminal becomes an input in this mode and accepts a TTL compatible square wave from another TPA3100D2 configured in the master mode or from an external GPIO. If connecting to an external GPIO, recommended frequencies are 200 kHz to 300 kHz for proper device operation, and the maximum amplitude is 4 V.

Using Low-ESR Capacitors

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

Short-Circuit Protection and Automatic-Recovery Feature

The TPA3100D2 has short-circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts, output-to-GND shorts, and output-to-V_{CC} shorts. When a short circuit is detected on the outputs, the part immediately disables the output drive. This is a latched fault and must be reset by cycling the voltage on the $\overline{\text{SHUTDOWN}}$ pin or MUTE pin. This clears the short-circuit flag and allows for normal operation if the short was removed. If the short was not removed, the protection circuitry again activates.

The FAULT terminal can be used for automatic recovery from a short-circuit event, or used to monitor the status with an external GPIO. For automatic recovery from a short-circuit event, connect the FAULT terminal directly to the MUTE terminal. When a short-circuit event occurs, the FAULT terminal transitions high indicating a

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short-circuit has been detected. When directly connected to MUTE, the MUTE terminal transitions high, and clears the internal fault flag. This causes the FAULT terminal to cycle low, and normal device operation resumes if the short-circuit is removed from the output. If a short remains at the output, the cycle continues until the short is removed. If external MUTE control and automatic recovery from a short-circuit event are desired, an OR gate can be used to combine the functionality of the FAULT output and external MUTE control (see Figure 32).

Thermal Protection

Thermal protection on the TPA3100D2 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 30°C. The device begins normal operation at this point with no external system interaction.

Printed Circuit Board (PCB) Layout

Because the TPA3100D2 is a class-D amplifier that switches at a high frequency, the layout of the PCB should be optimized according to the following guidelines for the best possible performance.

- Decoupling capacitors—The high-frequency 1-µF decoupling capacitors should be placed as close to the PVCC (pins 26, 27, 34, and 35) and AVCC (pin 48) terminals as possible. The VBYP (pin 16) capacitor, VREG (pin 15) capacitor, and VCLAMP (pins 30 and 31) capacitor should also be placed as close to the device as possible. Large (220-µF or greater) bulk power-supply decoupling capacitors should be placed near the TPA3100D2 on the PVCCL, PVCCR, and AVCC terminals.
- Grounding—The AVCC (pin 48) decoupling capacitor, VREG (pin 15) capacitor, VBYP (pin 16) capacitor, and ROSC (pin 14) resistor should each be grounded to analog ground (AGND, pin 17). The PVCC decoupling capacitors and VCLAMP capacitors should each be grounded to power ground (PGND, pins 28, 29, 32, and 33). Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the TPA3100D2.
- Output filter—The ferrite EMI filter (Figure 27) should be placed as close to the output terminals as possible for the best EMI performance. The LC filter (Figure 25 and Figure 26) should be placed close to the outputs. The capacitors used in both the ferrite and LC filters should be grounded to power ground. If both filters are used, the LC filter should be placed first, following the outputs.
- Thermal Pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land should be 5,1 mm by 5,1 mm. Five rows of solid vias (five vias per row, 0,3302 mm or 13 mils diameter) should be equally spaced underneath the thermal land. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB. The vias must be solid vias, not thermal relief or webbed vias. See TI Technical Briefs SCBA017 and SLUA271 for more information about using the QFN thermal pad. See TI Technical Briefs SLMA002 for more information about using the thermal pad. For recommended PCB footprints, see the mechanical information at the end of this data sheet.

For an example layout, see the TPA3100D2 Evaluation Module (TPA3100D2EVM) User Manual (SLOU179). Both the EVM user manual and the thermal pad application report are available on the TI Web site at http://www.ti.com.

Basic Measurement System

This application report focuses on methods that use the following equipment:

- Audio analyzer or spectrum analyzer
- Digital multimeter (DMM)
- Oscilloscope
- Twisted-pair wires
- Signal generator
- Power resistor(s)
- Linear regulated power supply
- Filter components
- EVM or other complete audio circuit

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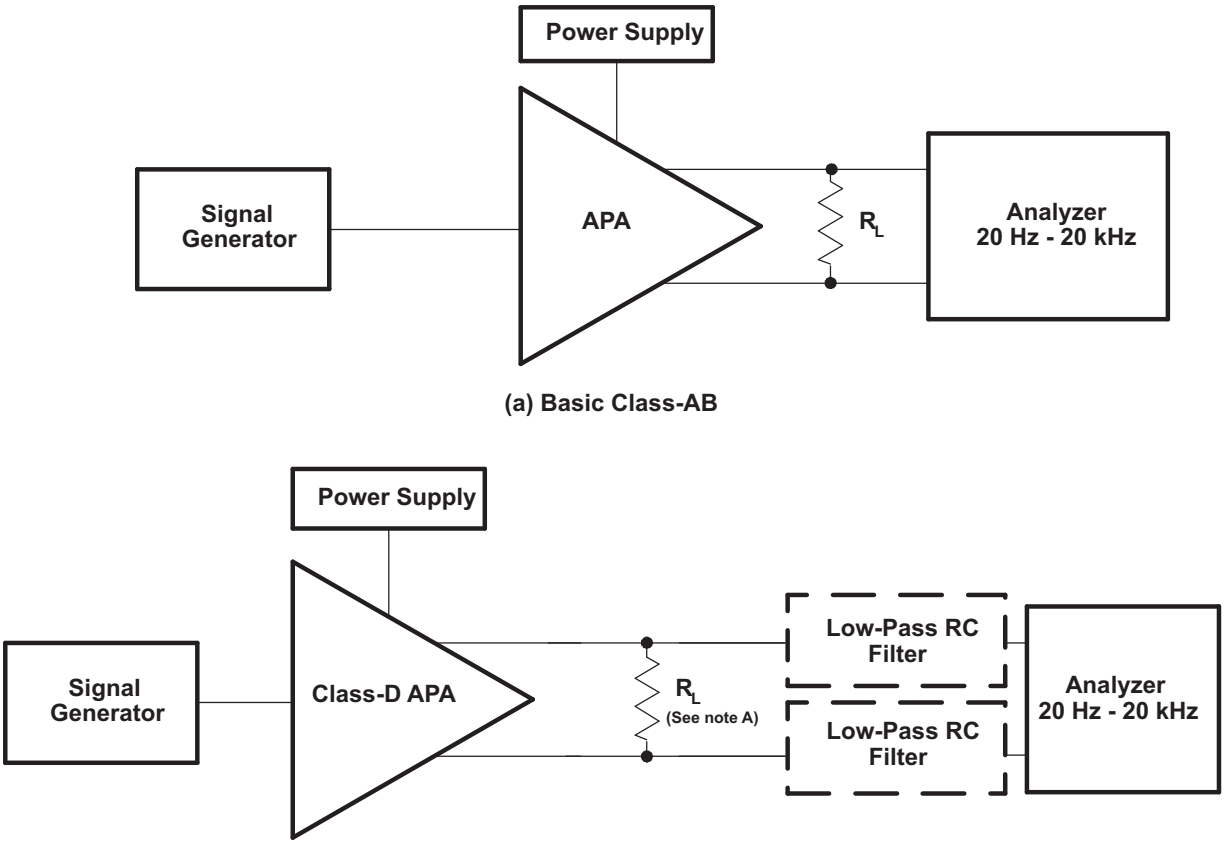
Figure 33 shows the block diagrams of basic measurement systems for class-AB and class-D amplifiers. A sine wave is normally used as the input signal because it consists of the fundamental frequency only (no other harmonics are present). An analyzer is then connected to the APA output to measure the voltage output. The analyzer must be capable of measuring the entire audio bandwidth. A regulated dc power supply is used to reduce the noise and distortion injected into the APA through the power pins. A System Two audio measurement system (AP-II) (Reference 1) by Audio Precision includes the signal generator and analyzer in one package.

The generator output and amplifier input must be ac-coupled. However, the EVMs already have the ac-coupling capacitors, (C_{IN}), so no additional coupling is required. The generator output impedance should be low to avoid attenuating the test signal, and is important because the input resistance of APAs is not high. Conversely, the analyzer-input impedance should be high. The output resistance, R_{OUT}, of the APA is normally in the hundreds of milliohms and can be ignored for all but the power-related calculations.

Figure 33(a) shows a class-AB amplifier system. It takes an analog signal input and produces an analog signal output. This amplifier circuit can be directly connected to the AP-II or other analyzer input.

This is not true of the class-D amplifier system shown in Figure 33(b), which requires low-pass filters in most cases in order to measure the audio output waveforms. This is because it takes an analog input signal and converts it into a pulse-width modulated (PWM) output signal that is not accurately processed by some analyzers.



A. For efficiency measurements with filter-free class-D, R_L should be an inductive load like a speaker.

Figure 33. Audio Measurement Systems

The TPA3100D2 uses a modulation scheme that does not require an output filter for operation, but they do sometimes require an RC low-pass filter when making measurements. This is because some analyzer inputs cannot accurately process the rapidly changing square-wave output and therefore record an extremely high level of distortion. The RC low-pass measurement filter is used to remove the modulated waveforms so the analyzer can measure the output sine wave.

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Differential Input and Bridge-Tied Load (BTL) Output

All of the class-D APAs and many class-AB APAs have differential inputs and BTL outputs. Differential inputs have two input pins per channel and amplify the difference in voltage between the pins. Differential inputs reduce the common-mode noise and distortion of the input circuit. BTL is a term commonly used in audio to describe differential outputs. BTL outputs have two output pins providing voltages that are 180 degrees out of phase. The load is connected between these pins. This has the added benefits of quadrupling the output power to the load and eliminating a dc blocking capacitor.

A block diagram of the measurement circuit is shown in Figure 34. The differential input is a balanced input, meaning the positive (+) and negative (–) pins have the same impedance to ground. Similarly, the BTL output equates to a balanced output.

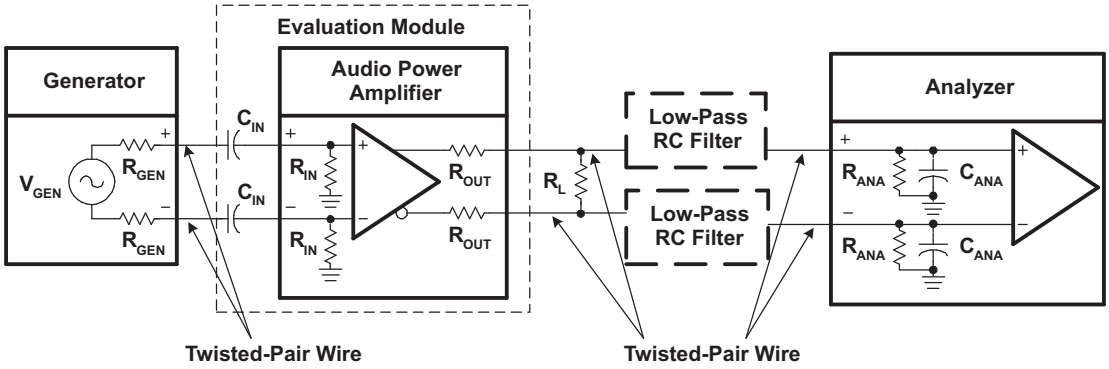

Figure 34. Differential Input, BTL Output Measurement Circuit

The generator should have balanced outputs, and the signal should be balanced for best results. An unbalanced output can be used, but it may create a ground loop that affects the measurement accuracy. The analyzer must also have balanced inputs for the system to be fully balanced, thereby cancelling out any common-mode noise in the circuit and providing the most accurate measurement.

The following general rules should be followed when connecting to APAs with differential inputs and BTL outputs:

- Use a balanced source to supply the input signal.
- Use an analyzer with balanced inputs.
- Use twisted-pair wire for all connections.
- Use shielding when the system environment is noisy.
- Ensure that the cables from the power supply to the APA, and from the APA to the load, can handle the large currents (see Table 2).

Table 2 shows the recommended wire size for the power supply and load cables of the APA system. The real concern is the dc or ac power loss that occurs as the current flows through the cable. These recommendations are based on 12-inch long wire with a 20-kHz sine-wave signal at 25°C.

Table 2. Recommended Minimum Wire Size for Power Cables

P_{OUT} (W)	R_L (Ω)	AWG Size		DC POWER LOSS (mW)		AC POWER LOSS (mW)	
10	4	18	22	16	40	18	42
2	4	18	22	3.2	8	3.7	8.5
1	8	22	28	2	8	2.1	8.1
< 0.75	8	22	28	1.5	6.1	1.6	6.2

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Class-D RC Low-Pass Filter

An RC filter is used to reduce the square-wave output when the analyzer inputs cannot process the pulse-width modulated class-D output waveform. This filter has little effect on the measurement accuracy because the cutoff frequency is set above the audio band. The high frequency of the square wave has negligible impact on measurement accuracy because it is well above the audible frequency range, and the speaker cone cannot respond at such a fast rate. The RC filter is not required when an LC low-pass filter is used, such as with the class-D APAs that employ the traditional modulation scheme (TPA032D0x, TPA005Dxx).

The component values of the RC filter are selected using the equivalent output circuit as shown in Figure 35. R_L is the load impedance that the APA is driving for the test. The analyzer input impedance specifications should be available and substituted for R_{ANA} and C_{ANA}. The filter components, R_{FILT} and C_{FILT}, can then be derived for the system. The filter should be grounded to the APA near the output ground pins or at the power supply ground pin to minimize ground loops.

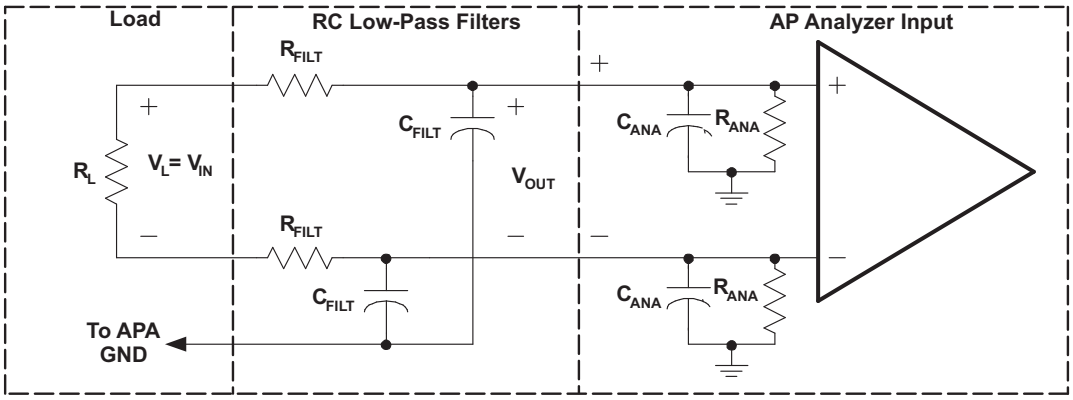

Figure 35. Measurement Low-Pass Filter Derivation Circuit-Class-D APAs

The transfer function for this circuit is shown in Equation 5 where $\omega_O = R_{EQ}C_{EQ}$, $R_{EQ} = R_{FILT} \parallel R_{ANA}$ and $C_{EQ} = (C_{FILT} + C_{ANA})$. The filter frequency should be set above f_{MAX}, the highest frequency of the measurement bandwidth, to avoid attenuating the audio signal. Equation 6 provides this cutoff frequency, f_C. The value of R_{FILT} must be chosen large enough to minimize current that is shunted from the load, yet small enough to minimize the attenuation of the analyzer-input voltage through the voltage divider formed by R_{FILT} and R_{ANA}. A general rule is that R_{FILT} should be small (~100 Ω) for most measurements. This reduces the measurement error to less than 1% for $R_{ANA} \geq 10$ kΩ.

$$\left(\frac{V_{OUT}}{V_{IN}}\right) = \frac{\left(\frac{R_{ANA}}{R_{ANA} + R_{FILT}}\right)}{1 + j\left(\frac{\omega}{\omega_O}\right)} \quad (5)$$

$$f_c = \sqrt{2} \times f_{max} \quad (6)$$

An exception occurs with the efficiency measurements, where R_{FILT} must be increased by a factor of ten to reduce the current shunted through the filter. C_{FILT} must be decreased by a factor of ten to maintain the same cutoff frequency. See Table 3 for the recommended filter component values.

Once f_C is determined and R_{FILT} is selected, the filter capacitance is calculated using Equation 7. When the calculated value is not available, it is better to choose a smaller capacitance value to keep f_C above the minimum desired value calculated in Equation 7.

$$C_{FILT} = \frac{1}{2\pi \times f_c \times R_{FILT}} \quad (7)$$

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Table 3 shows recommended values of R_{FILT} and C_{FILT} based on common component values. The value of f_C was originally calculated to be 28 kHz for an f_{MAX} of 20 kHz. C_{FILT}, however, was calculated to be 57,000 pF, but the nearest values of 56,000 pF and 51,000 pF were not available. A 47,000-pF capacitor was used instead, and f_C is 34 kHz, which is above the desired value of 28 kHz.

Table 3. Typical RC Measurement Filter Values

MEASUREMENT	R_{FILT} (Ω)	C_{FILT} (pF)
Efficiency	1000	5,600
All other measurements	100	56,000

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA3100D2IRGZRQ1	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA 3100D2I
TPA3100D2IRGZRQ1.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA 3100D2I

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPA3100D2-Q1 :

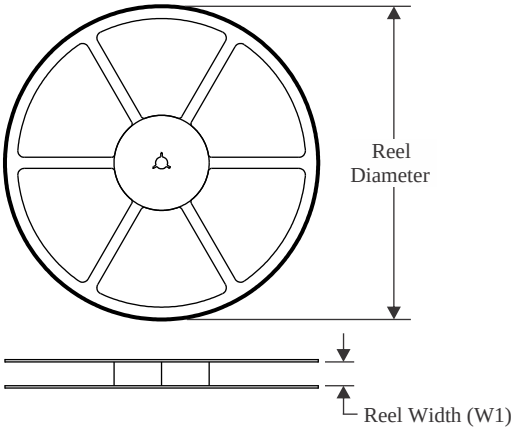
- Catalog : TPA3100D2

NOTE: Qualified Version Definitions:

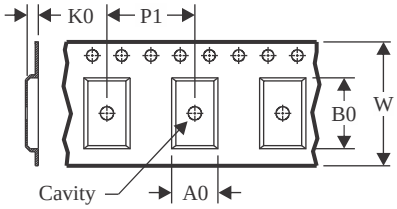
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

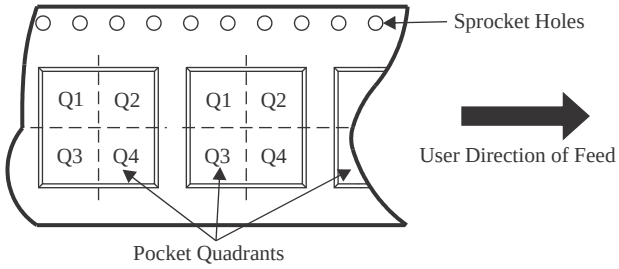


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

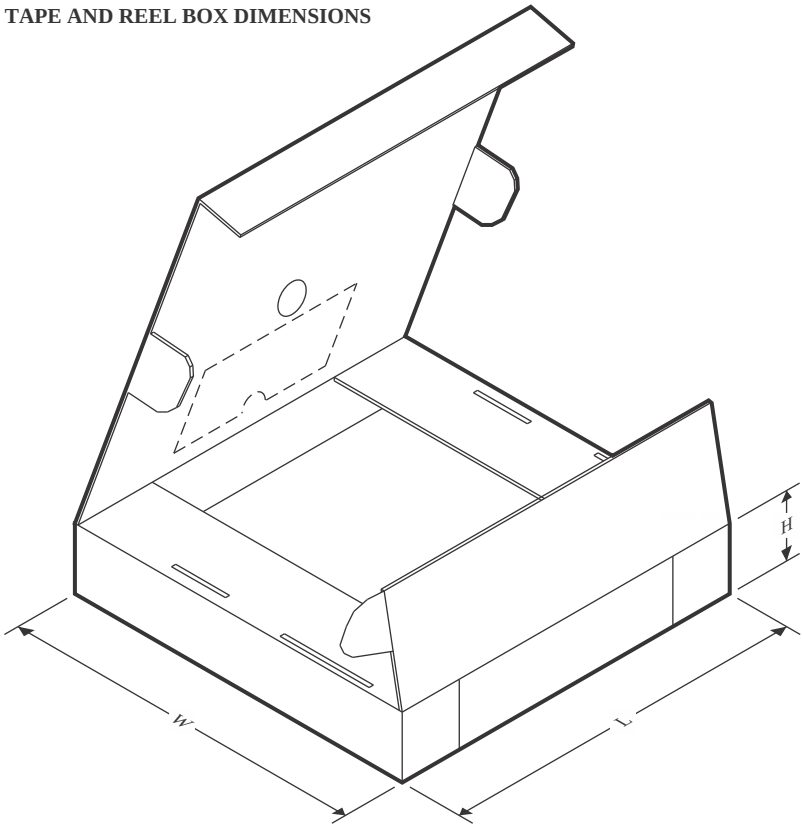
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3100D2IRGZRQ1	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3100D2IRGZRQ1	VQFN	RGZ	48	2500	353.0	353.0	32.0

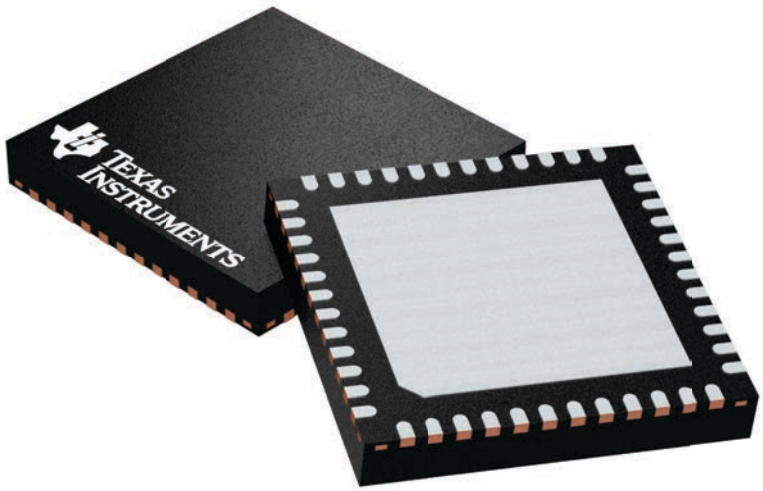
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

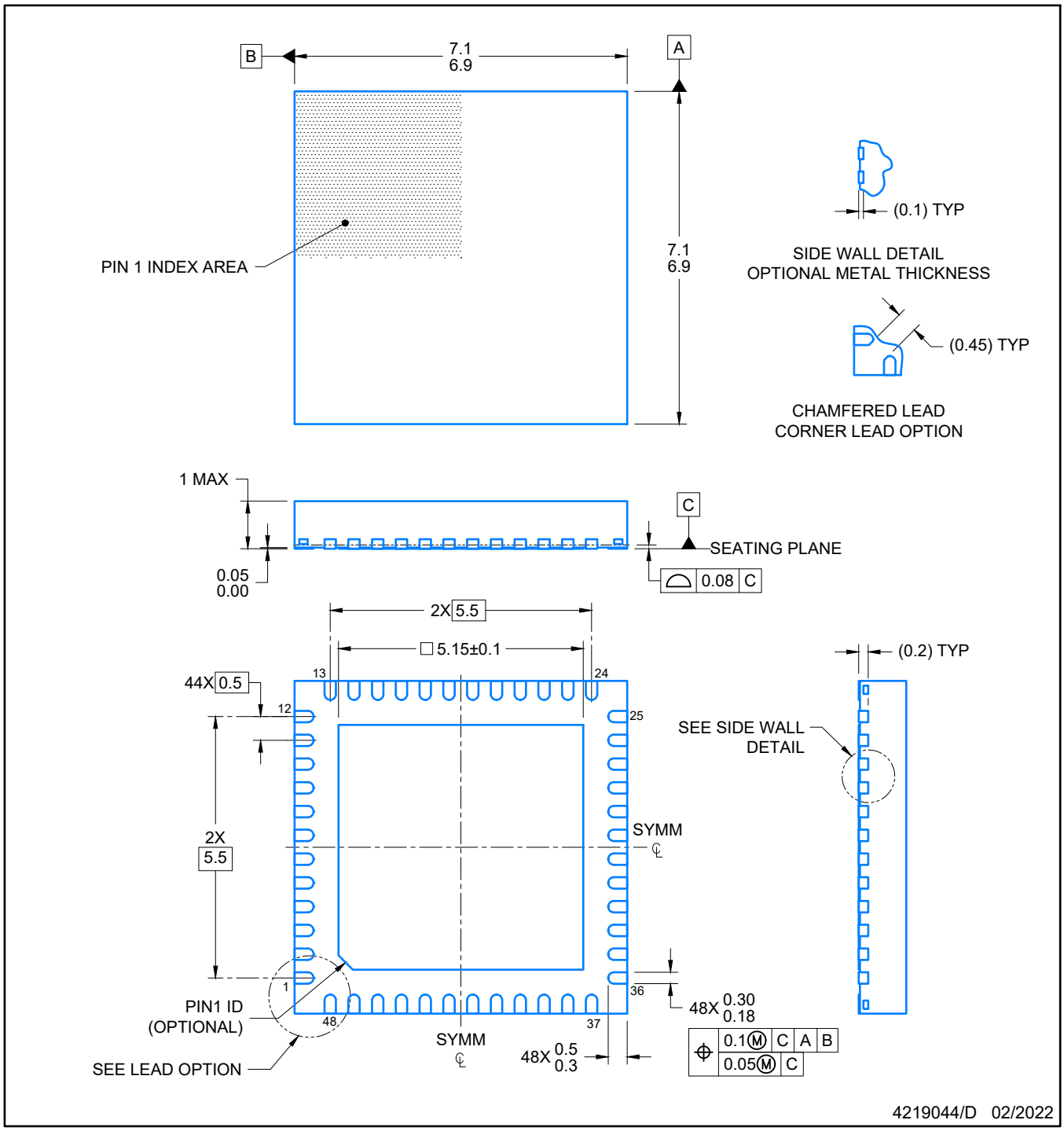
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



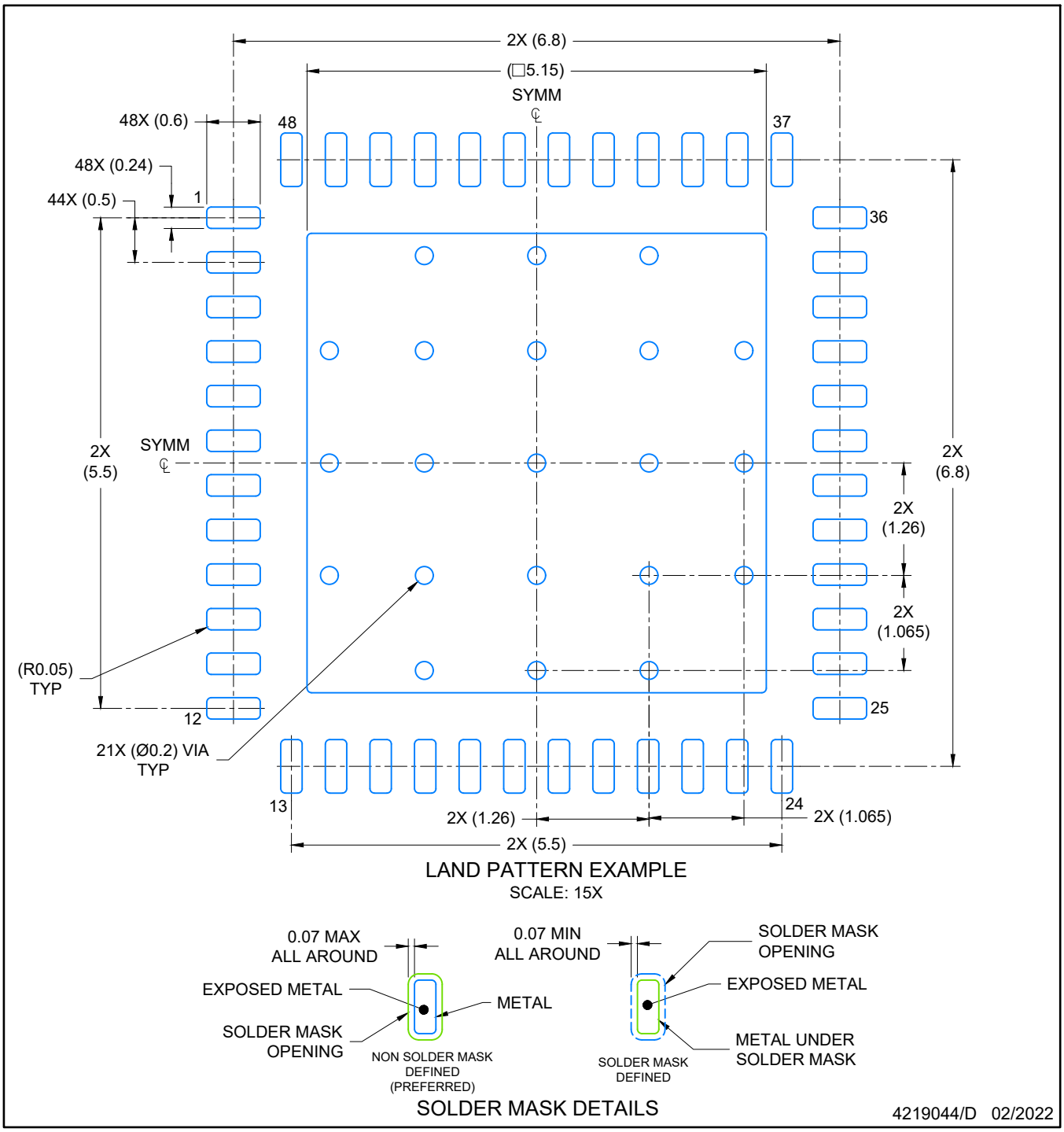
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A



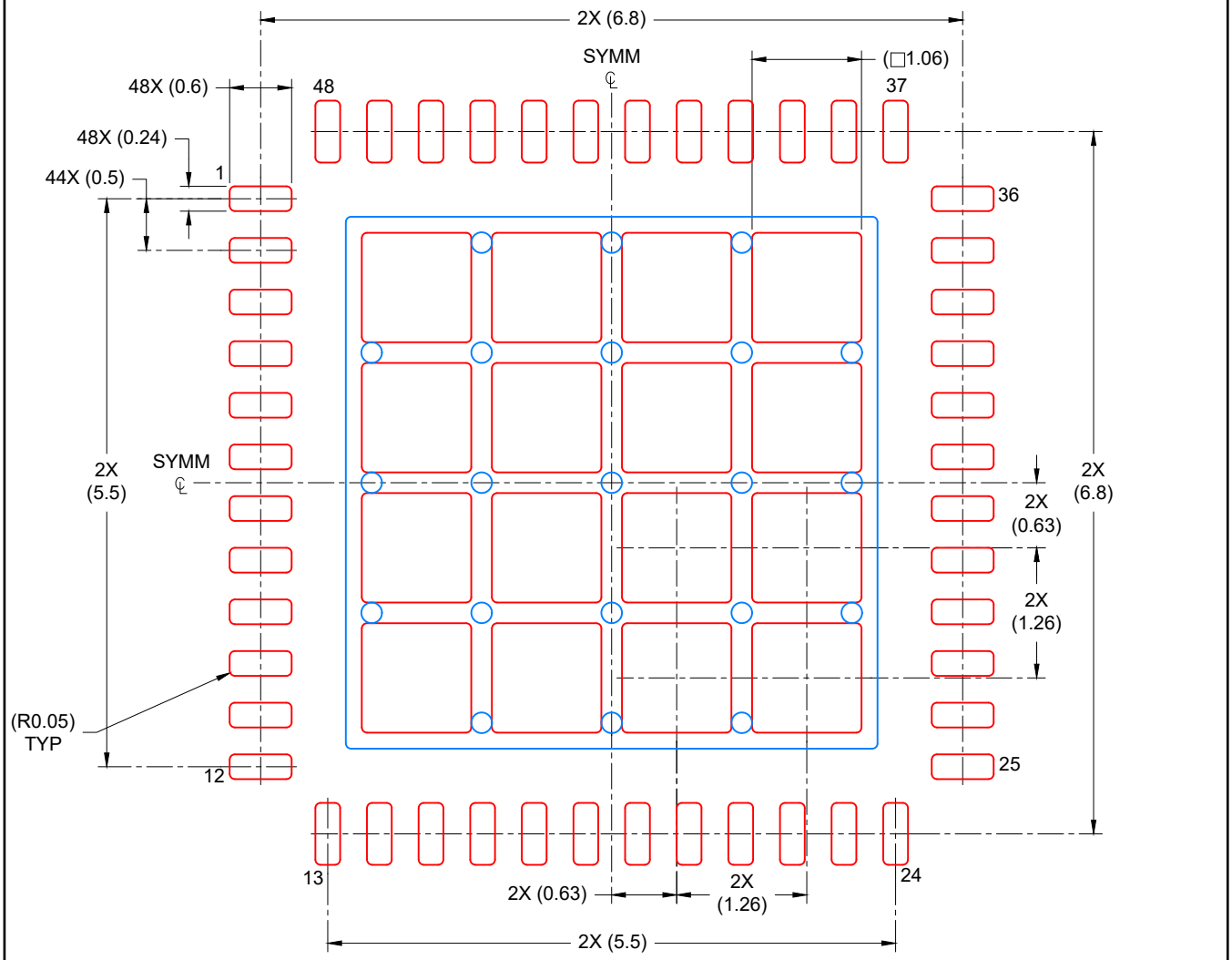
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

4219044/D 02/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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